# RL78/L1C

RENESAS MCU

R01DS0192EJ0230
Rev.2.30
Mar 20, 2023

Integrated LCD controller/driver, 12-bit resolution A/D Converter, USB 2.0 controller (function), True Low Power Platform (as low as 112.5 µA/MHz, and 0.68 µA for RTC2 + LVD), 1.6 V to 3.6 V operation, 64 to 256 Kbyte Flash, 33 DMIPS at 24 MHz, for All LCD Based Applications

# 1. OUTLINE

## 1.1 Features

**Ultra-low power consumption technology**
- $V_{DD}$ = single power supply voltage of 1.6 to 3.6 V
- HALT mode
- STOP mode
- SNOOZE mode

**RL78 CPU core**
- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.04167 µs: @ 24 MHz operation with high-speed on-chip oscillator clock or PLL clock) to ultra-low speed (30.5 µs: @ 32.768 kHz operation with subsystem clock)
- Multiply/divide and multiply/accumulate instructions are supported.
- Address space: 1 Mbyte
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 8 to 16 KB

**Code flash memory**
- Code flash memory: 64 to 256 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

**Data flash memory**
- Data flash memory: 8 KB
- Background operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: $V_{DD}$ = 1.8 to 3.6 V

**High-speed on-chip oscillator**
- Select from 48 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: ±1.0% ($V_{DD}$ = 1.8 to 3.6 V, $T_A$ = -20 to +85°C)

**Operating ambient temperature**
- $T_A$ = -40 to +85°C (A: Consumer applications)
- $T_A$ = -40 to +105°C (G: Industrial applications)

**Power management and reset function**
- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 12 levels)

**Data transfer controller (DTC)**
- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources (30 to 33 sources).
- Chain transfer function

**Event link controller (ELC)**
- Event signals of 30 or 31 types can be linked to the specified peripheral function.

**Serial interfaces**
- Simplified SPI (CSI Note 1): 4 channels
- UART/UART (LIN-bus supported): 4 channels
- $I^2C$/simplified $I^2C$: 5 channels

**Timers**
- 16-bit timer: 11 channels
- 12-bit interval timer: 1 channel
- Real-time clock 2: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

**LCD controller/driver**
- Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.
- Segment signal output: 44 (40) Note 2 to 56 (52) Note 2
- Common signal output: 4 (8) Note 2

**USB Note 3**
- USB version 2.0 (function controller)
- Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported
- Compliant to Battery Charging Specification Revision 1.2

**A/D converter**
- 8/10-bit resolution A/D converter ($V_{DD}$ = 1.6 to 3.6 V)
- 12-bit resolution A/D converter ($V_{DD}$ = 2.4 to 3.6 V)
- Analog input: 9 to 13 channels
- Internal reference voltage (TYP. 1.45 V) and temperature sensor Note 3

**D/A converter**
- 8-bit resolution D/A converter ($V_{DD}$ = 1.6 to 3.6 V)
- Analog output: 2 channels
- Output voltage: 0 V to $V_{DD}$
- Real-time output function

**Comparator**
- 2 channels
- Operating modes: Comparator high-speed mode, comparator low-speed mode, window mode
- The external reference voltage or internal reference voltage can be selected as the reference voltage.

**I/O ports**
- I/O ports: 59 to 77 (N-ch open drain I/O [withstand voltage of 6 V]: 2)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

**Others**
- On-chip BCD (binary-coded decimal) correction circuit

**Note 1.** Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

**Note 2.** The number in parentheses indicates the number of signal outputs when 8 coms are used.

**Note 3.** Selectable only in HS (high-speed main) mode.

**Remark** The functions mounted depend on the product. See **1.6 Outline of Functions**.

○ ROM, RAM capacities

**Products with USB**

| Flash ROM | Data Flash | RAM | RL78/L1C | | |
|---|---|---|---|---|---|
| | | | 80 pins | 85 pins | 100 pins |
| 256 KB | 8 KB | 16 KB Note | R5F110MJ | R5F110NJ | R5F110PJ |
| 192 KB | 8 KB | 16 KB Note | R5F110MH | R5F110NH | R5F110PH |
| 128 KB | 8 KB | 12 KB | R5F110MG | R5F110NG | R5F110PG |
| 96 KB | 8 KB | 10 KB | R5F110MF | R5F110NF | R5F110PF |
| 64 KB | 8 KB | 8 KB | R5F110ME | R5F110NE | R5F110PE |

**Products without USB**

| Flash ROM | Data Flash | RAM | RL78/L1C | | |
|---|---|---|---|---|---|
| | | | 80 pins | 85 pins | 100 pins |
| 256 KB | 8 KB | 16 KB Note | R5F111MJ | R5F111NJ | R5F111PJ |
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| 96 KB | 8 KB | 10 KB | R5F111MF | R5F111NF | R5F111PF |
| 64 KB | 8 KB | 8 KB | R5F111ME | R5F111NE | R5F111PE |

**Note** This is about 15 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/L1C User's Manual).

## 1.2 Ordering Information

**Products with USB**

| Pin Count | Package | Fields of Application | Orderable Part Number | | RENESAS Code |
|---|---|---|---|---|---|
| | | | Product Name | Packaging Specifications | |
| 80 pins | 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch) | A | R5F110MEAFB, R5F110MFAFB, R5F110MGAFB, R5F110MHAFB, R5F110MJAFB | #10,#50 | PLQP0080KB-B PLQP0080KJ-A |
| | | | | #30 | PLQP0080KB-B |
| | | G | R5F110MEGFB, R5F110MFGFB, R5F110MGGFB, R5F110MHGFB, R5F110MJGFB | #10,#50 | PLQP0080KB-B PLQP0080KJ-A |
| | | | | #30 | PLQP0080KB-B |
| 85 pins | 85-pin plastic VFLGA (7 × 7 mm, 0.65 mm pitch) | A | R5F110NEALA, R5F110NFALA, R5F110NGALA, R5F110NHALA, R5F110NJALA | #U0,#W0 | PVLG0085JA-A |
| | | G | R5F110NEGLA, R5F110NFGLA, R5F110NGGLA, R5F110NHGLA, R5F110NJGLA | | |
| 100 pins | 100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch) | A | R5F110PEAFB, R5F110PFAFB, R5F110PGAFB, R5F110PHAFB, R5F110PJAFB | #10,#50 | PLQP0100KB-B PLQP0100KP-A |
| | | | | #30 | PLQP0100KB-B |
| | | G | R5F110PEGFB, R5F110PFGFB, R5F110PGGFB, R5F110PHGFB, R5F110PJGFB | #10,#50 | PLQP0100KB-B PLQP0100KP-A |
| | | | | #30 | PLQP0100KB-B |

**Products without USB**

| Pin Count | Package | Fields of Application | Orderable Part Number | | RENESAS Code |
|---|---|---|---|---|---|
| | | | Product Name | Packaging Specifications | |
| 80 pins | 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch) | A | R5F111MEAFB, R5F111MFAFB, R5F111MGAFB, R5F111MHAFB, R5F111MJAFB | #10,#50 | PLQP0080KB-B PLQP0080KJ-A |
| | | | | #30 | PLQP0080KB-B |
| | | G | R5F111MEGFB, R5F111MFGFB, R5F111MGGFB, R5F111MHGFB, R5F111MJGFB | #10,#50 | PLQP0080KB-B PLQP0080KJ-A |
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| | | G | R5F111NEGLA, R5F111NFGLA, R5F111NGGLA, R5F111NHGLA, R5F111NJGLA | | |
| 100 pins | 100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch) | A | R5F111PEAFB, R5F111PFAFB, R5F111PGAFB, R5F111PHAFB, R5F111PJAFB | #10,#50 | PLQP0100KB-B PLQP0100KP-A |
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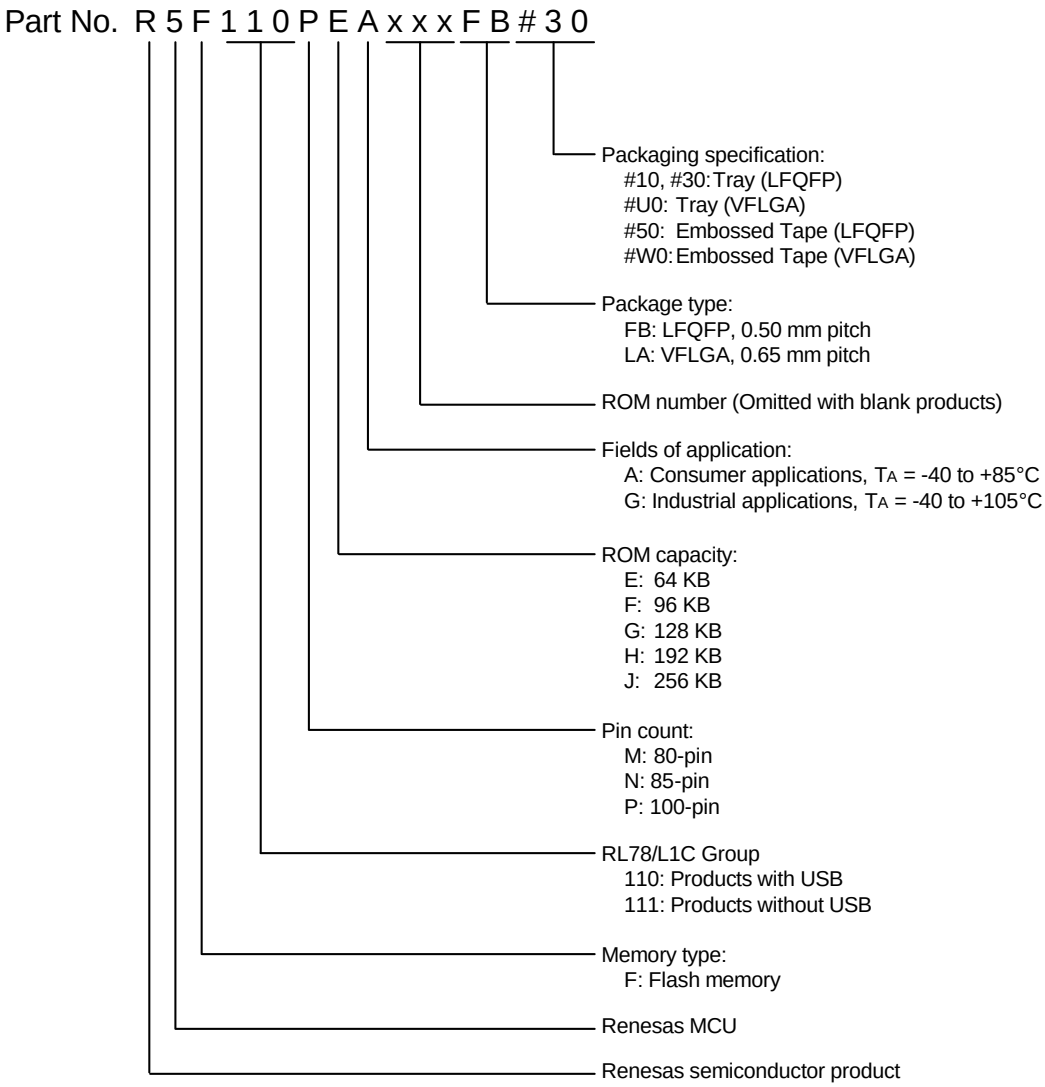
| | | | | #30 | PLQP0100KB-B |

**Figure 1 - 1 Part Number, Memory Size, and Package of RL78/L1C**

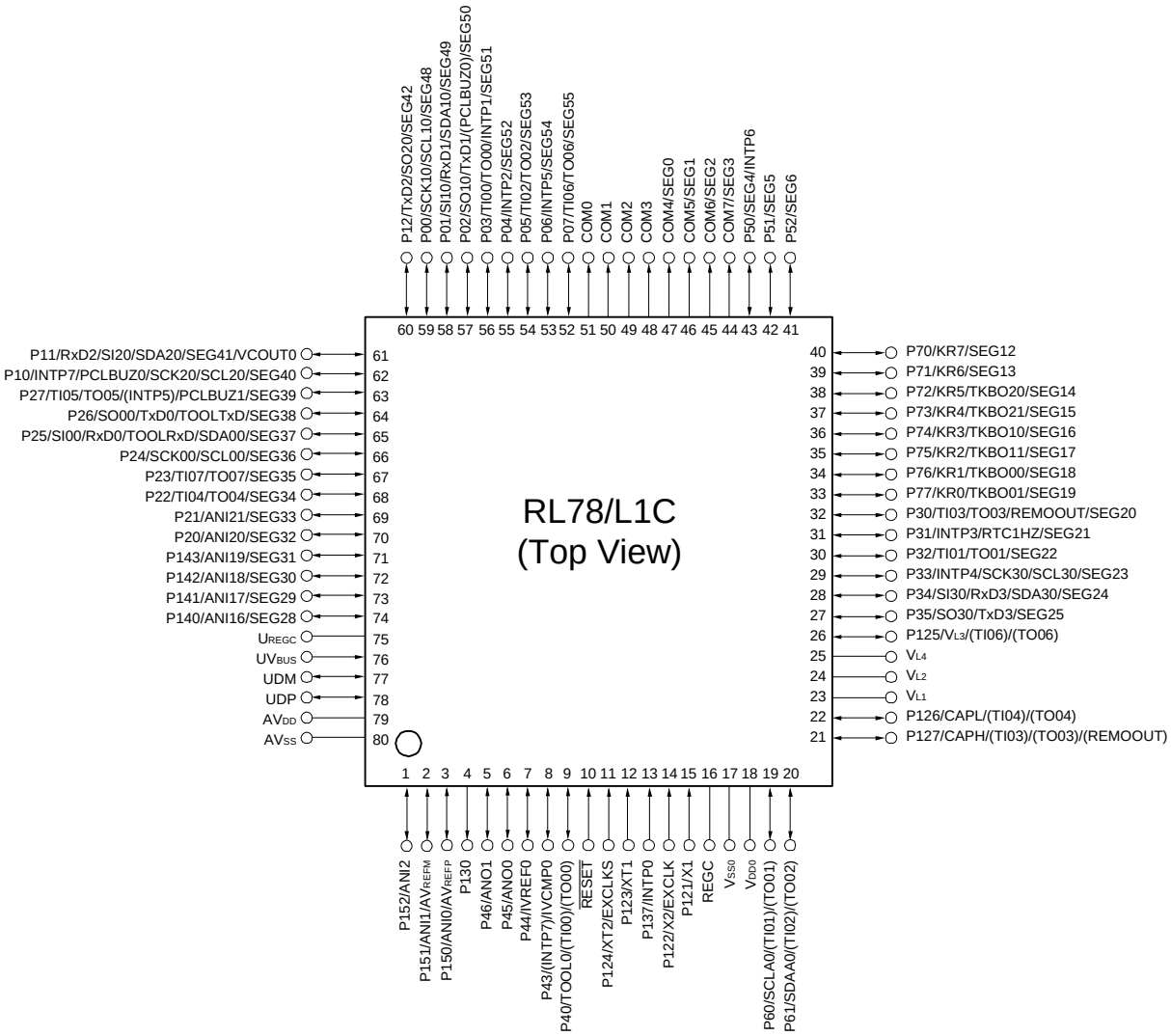



**Caution Orderable part numbers are current as of when this manual was published.**
**Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.**

## 1.3 Pin Configuration (Top View)

### 1.3.1 80-pin products (with USB)

• 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)




**Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 µF).**

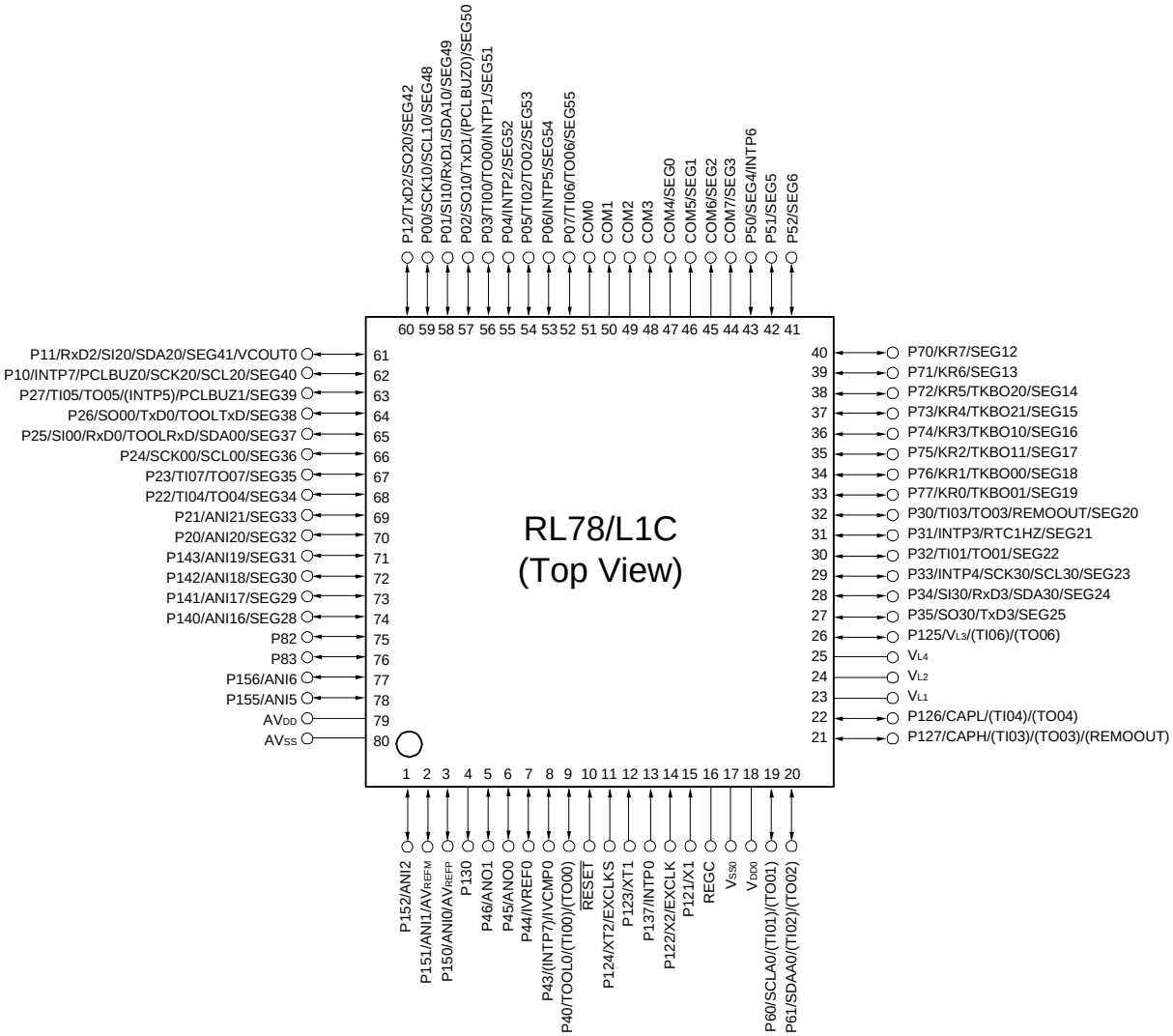
**Caution 2. Connect the UREGC pin to Vss pin via a capacitor (0.33 µF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

### 1.3.2 80-pin products (without USB)

• 80-pin plastic LFQFP (fine pitch) (12 × 12 mm, 0.5 mm pitch)

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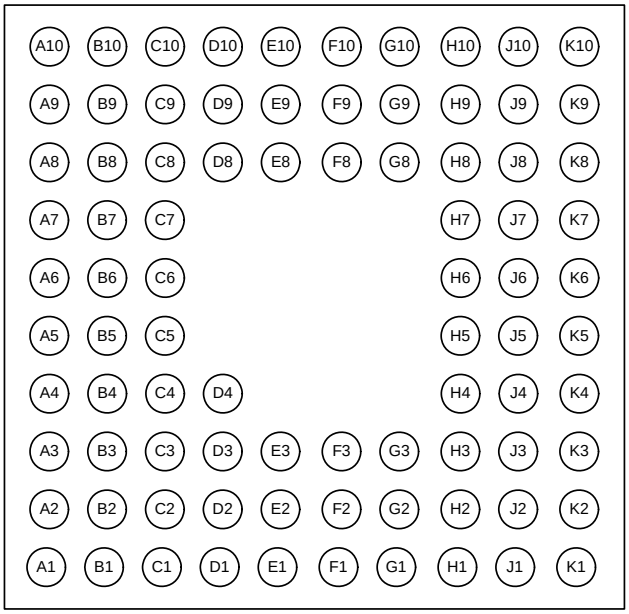
**Remark 1.** For pin identification, see **1.4 Pin Identification**.

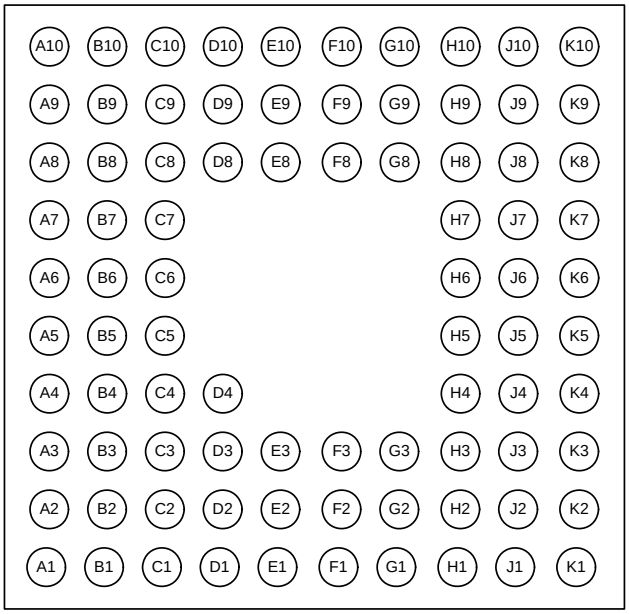
**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

### 1.3.3 85-pin products (with USB)




| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|---|---|---|---|---|---|---|---|---|---|
| A1 | COM7/SEG3 | C1 | COM2 | E1 | P04/INTP2/SEG52 | G1 | P00/SCK10/SCL10/ SEG48 | J1 | $V_{SS0}$ |
| A2 | P51/SEG5 | C2 | COM5/SEG1 | E2 | P05/TI02/TO02/SEG53 | G2 | $V_{SS0}$ | J2 | P11/RxD2/SI20/SDA20/ SEG41/VCOUT0 |
| A3 | P70/KR7/SEG12 | C3 | COM6/SEG2 | E3 | P06/INTP5/SEG54 | G3 | P12/TxD2/SO20/SEG42/ VCOUT1 | J3 | P26/SO00/TxD0/ TOOLTxD/SEG38 |
| A4 | P73/KR4/TKBO21/SEG15 | C4 | P71/KR6/SEG13 | E4 | — | G4 | — | J4 | P23/TI07/TO07/SEG35 |
| A5 | P74/KR3/TKBO10/SEG16 | C5 | P76/KR1/TKBO00/SEG18 | E5 | — | G5 | — | J5 | P20/ANI20/SEG32 |
| A6 | P31/INTP3/RTC1HZ/ SEG21 | C6 | P77/KR0/TKBO01/SEG19 | E6 | — | G6 | — | J6 | P141/ANI17/SEG29 |
| A7 | P33/INTP4/SCK30/SCL30/ SEG23 | C7 | P34/SI30/RxD3/SDA30/ SEG24 | E7 | — | G7 | — | J7 | $U_{REGC}$ |
| A8 | P35/SO30/TxD3/SEG25 | C8 | $V_{L1}$ | E8 | P40/TOOL0/(TI00)/(TO00) | G8 | P44/(SCK10)/(SCL10)/ IVREF0 | J8 | $UV_{BUS}$ |
| A9 | $V_{L4}$ | C9 | P61/SDAA0/(TI02)/(TO02) | E9 | P137/INTP0 | G9 | P45/ANO0 | J9 | $AV_{DD}$ |
| A10 | P126/CAPL/(TI04)/(TO04) | C10 | $V_{DD0}$ | E10 | P122/X2/EXCLK | G10 | P123/XT1 | J10 | P150/ANI0/$AV_{REFP}$ |
| B1 | COM4/SEG0 | D1 | COM0 | F1 | P03/TI00/TO00/INTP1/ SEG51 | H1 | $V_{SS0}$ | K1 | $V_{SS0}$ |
| B2 | P50/SEG4/INTP6 | D2 | COM1 | F2 | P02/SO10/TxD1/ (PCLBUZ0)/SEG50 | H2 | $V_{SS0}$ | K2 | P27/TI05/TO05/(INTP5)/ PCLBUZ1/SEG39 |
| B3 | P52/SEG6 | D3 | P07/TI06/TO06/SEG55 | F3 | P01/SI10/RxD1/SDA10/ SEG49 | H3 | P10/INTP7/PCLBUZ0/ SCK20/SCL20/SEG40 | K3 | P25/SI00/RxD0/ TOOLRxD/SDA00/SEG37 |
| B4 | P72/KR5/TKBO20/SEG14 | D4 | COM3 | F4 | — | H4 | P24/SCK00/SCL00/ SEG36 | K4 | P22/TI04/TO04/SEG34 |
| B5 | P75/KR2/TKBO11/SEG17 | D5 | — | F5 | — | H5 | P21/ANI21/SEG33 | K5 | P143/ANI19/SEG31 |
| B6 | P30/TI03/TO03/ REMOOUT/SEG20 | D6 | — | F6 | — | H6 | P140/ANI16/SEG28 | K6 | P142/ANI18/SEG30 |
| B7 | P32/TI01/TO01/SEG22 | D7 | — | F7 | — | H7 | P152/ANI2 | K7 | UDM |
| B8 | P125/$V_{L3}$/(TI06)/(TO06) | D8 | P60/SCLA0/(TI01)/(TO01) | F8 | P43/(INTP7)/(SI10)/ (RxD1)/(SDA10)/IVCMP0 | H8 | P46/ANO1 | K8 | UDP |
| B9 | $V_{L2}$ | D9 | REGC | F9 | $\overline{\text{RESET}}$ | H9 | P130 | K9 | $AV_{SS}$ |
| B10 | P127/CAPH/(TI03)/ (TO03)/(REMOOUT) | D10 | P121/X1 | F10 | $V_{SS0}$ | H10 | P124/XT2/EXCLKS | K10 | P151/ANI1/$AV_{REFM}$ |

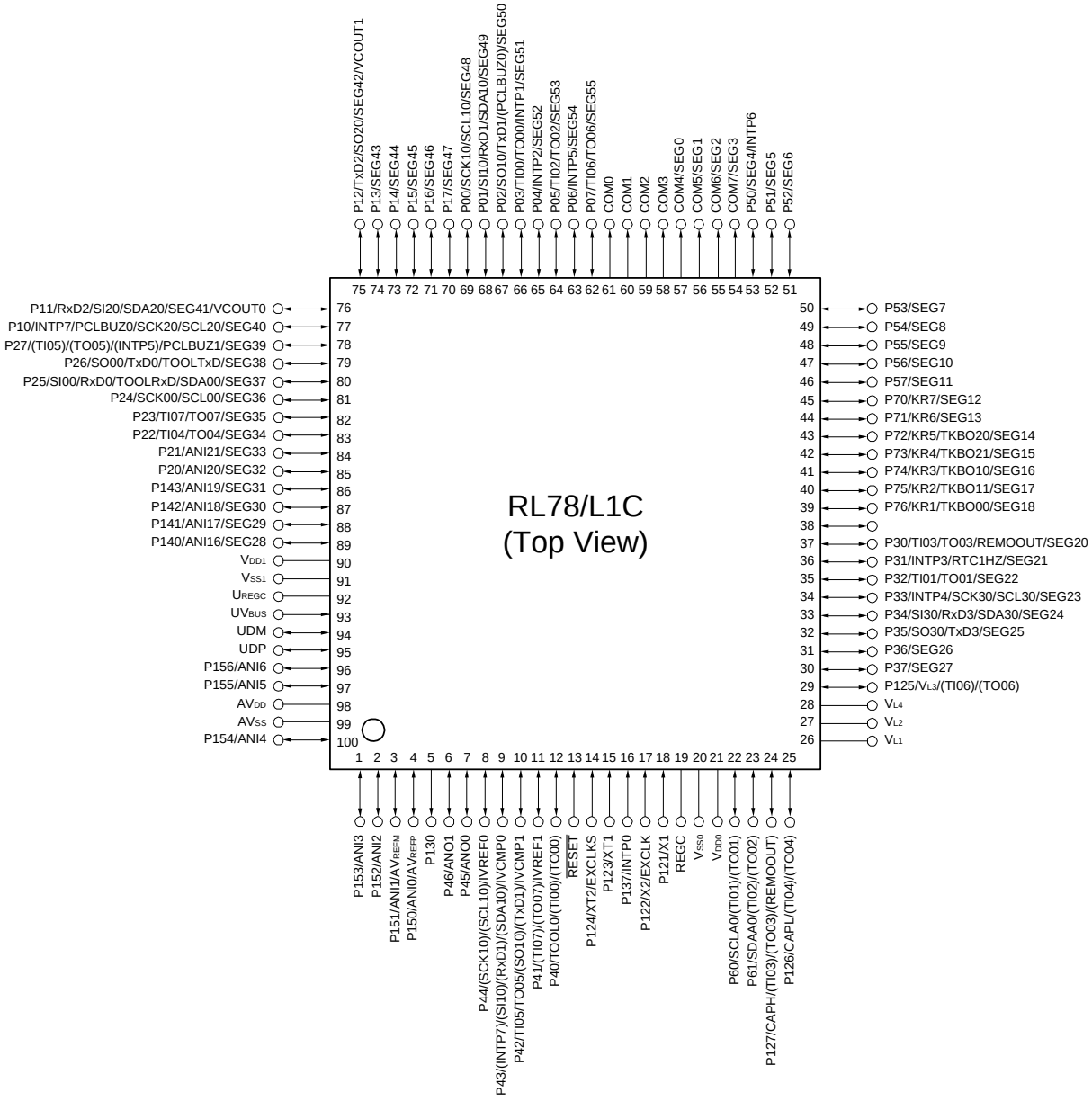
### 1.3.4 85-pin products (without USB)




| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|---|---|---|---|---|---|---|---|---|---|
| A1 | COM7/SEG3 | C1 | COM2 | E1 | P04/INTP2/SEG52 | G1 | P00/SCK10/SCL10/ SEG48 | J1 | $V_{SS0}$ |
| A2 | P51/SEG5 | C2 | COM5/SEG1 | E2 | P05/TI02/TO02/SEG53 | G2 | $V_{SS0}$ | J2 | P11/RxD2/SI20/SDA20/ SEG41/VCOUT0 |
| A3 | P70/KR7/SEG12 | C3 | COM6/SEG2 | E3 | P06/INTP5/SEG54 | G3 | P12/TxD2/SO20/SEG42/ VCOUT1 | J3 | P26/SO00/TxD0/ TOOLTxD/SEG38 |
| A4 | P73/KR4/TKBO21/SEG15 | C4 | P71/KR6/SEG13 | E4 | — | G4 | — | J4 | P23/TI07/TO07/SEG35 |
| A5 | P74/KR3/TKBO10/SEG16 | C5 | P76/KR1/TKBO00/SEG18 | E5 | — | G5 | — | J5 | P20/ANI20/SEG32 |
| A6 | P31/INTP3/RTC1HZ/ SEG21 | C6 | P77/KR0/TKBO01/ SEG19 | E6 | — | G6 | — | J6 | P141/ANI17/SEG29 |
| A7 | P33/INTP4/SCK30/ SCL30/SEG23 | C7 | P34/SI30/RxD3/SDA30/ SEG24 | E7 | — | G7 | — | J7 | P82 |
| A8 | P35/SO30/TxD3/SEG25 | C8 | $V_{L1}$ | E8 | P40/TOOL0/(TI00)/(TO00) | G8 | P44/(SCK10)/(SCL10)/ IVREF0 | J8 | P83 |
| A9 | $V_{L4}$ | C9 | P61/SDAA0/(TI02)/(TO02) | E9 | P137/INTP0 | G9 | P45/ANO0 | J9 | $AV_{DD}$ |
| A10 | P126/CAPL/(TI04)/(TO04) | C10 | $V_{DD0}$ | E10 | P122/X2/EXCLK | G10 | P123/XT1 | J10 | P150/ANI0/$AV_{REFP}$ |
| B1 | COM4/SEG0 | D1 | COM0 | F1 | P03/TI00/TO00/INTP1/ SEG51 | H1 | $V_{SS0}$ | K1 | $V_{SS0}$ |
| B2 | P50/SEG4/INTP6 | D2 | COM1 | F2 | P02/SO10/TxD1/ (PCLBUZ0)/SEG50 | H2 | $V_{SS0}$ | K2 | P27/TI05/TO05/(INTP5)/ PCLBUZ1/SEG39 |
| B3 | P52/SEG6 | D3 | P07/TI06/TO06/SEG55 | F3 | P01/SI10/RxD1/SDA10/ SEG49 | H3 | P10/INTP7/PCLBUZ0/ SCK20/SCL20/SEG40 | K3 | P25/SI00/RxD0/ TOOLRxD/SDA00/SEG37 |
| B4 | P72/KR5/TKBO20/SEG14 | D4 | COM3 | F4 | — | H4 | P24/SCK00/SCL00/ SEG36 | K4 | P22/TI04/TO04/SEG34 |
| B5 | P75/KR2/TKBO11/SEG17 | D5 | — | F5 | — | H5 | P21/ANI21/SEG33 | K5 | P143/ANI19/SEG31 |
| B6 | P30/TI03/TO03/ REMOOUT/SEG20 | D6 | — | F6 | — | H6 | P140/ANI16/SEG28 | K6 | P142/ANI18/SEG30 |
| B7 | P32/TI01/TO01/SEG22 | D7 | — | F7 | — | H7 | P152/ANI2 | K7 | P156/ANI6 |
| B8 | P125/$V_{L3}$/(TI06)/(TO06) | D8 | P60/SCLA0/(TI01)/(TO01) | F8 | P43/(INTP7)/(SI10)/ (RxD1)/(SDA10)/IVCMP0 | H8 | P46/ANO1 | K8 | P155/ANI5 |
| B9 | $V_{L2}$ | D9 | REGC | F9 | $\overline{\text{RESET}}$ | H9 | P130 | K9 | $AV_{SS}$ |
| B10 | P127/CAPH/(TI03)/ (TO03)/(REMOOUT) | D10 | P121/X1 | F10 | $V_{SS0}$ | H10 | P124/XT2/EXCLKS | K10 | P151/ANI1/$AV_{REFM}$ |

### 1.3.5 100-pin products (with USB)

• 100-pin plastic LFQFP (fine pitch) (14 × 14 mm, 0.5 mm pitch)




**Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 µF).**

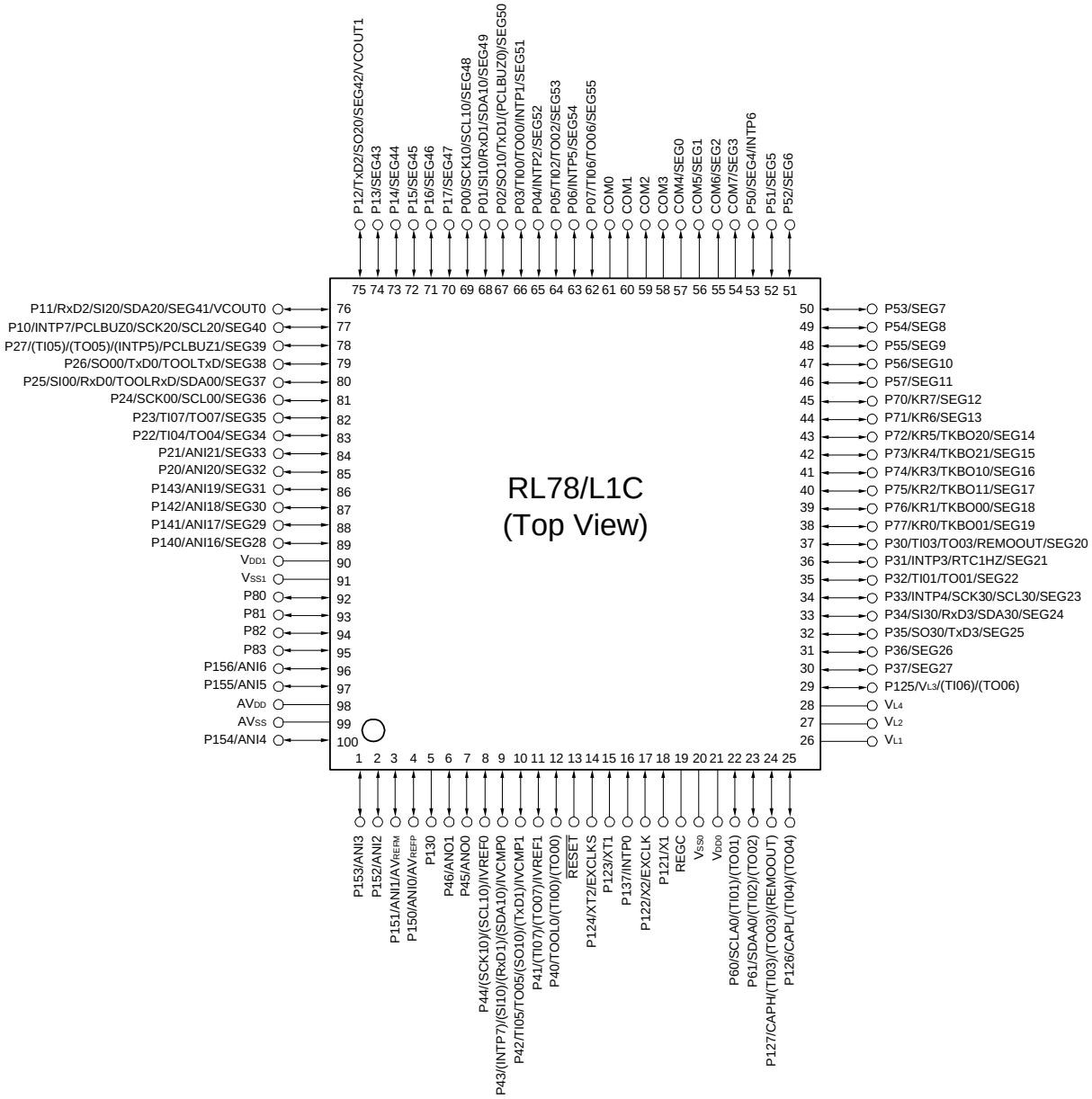
**Caution 2. Connect the UREGC pin to Vss pin via a capacitor (0.33 µF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

### 1.3.6 100-pin products (without USB)

• 100-pin plastic LFQFP (fine pitch) (14 × 14 mm, 0.5 mm pitch)




**Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 µF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

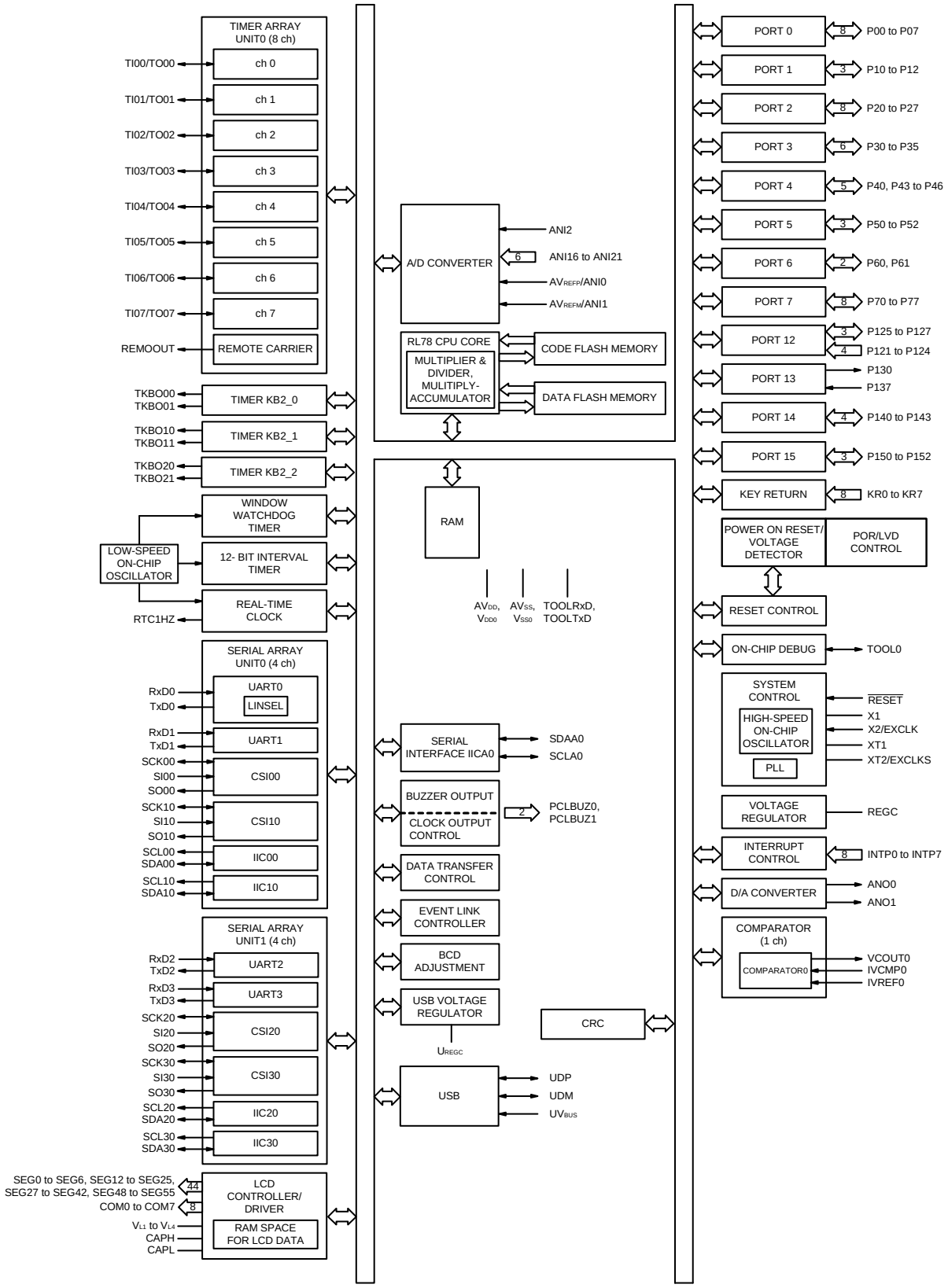
**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

## 1.4 Pin Identification

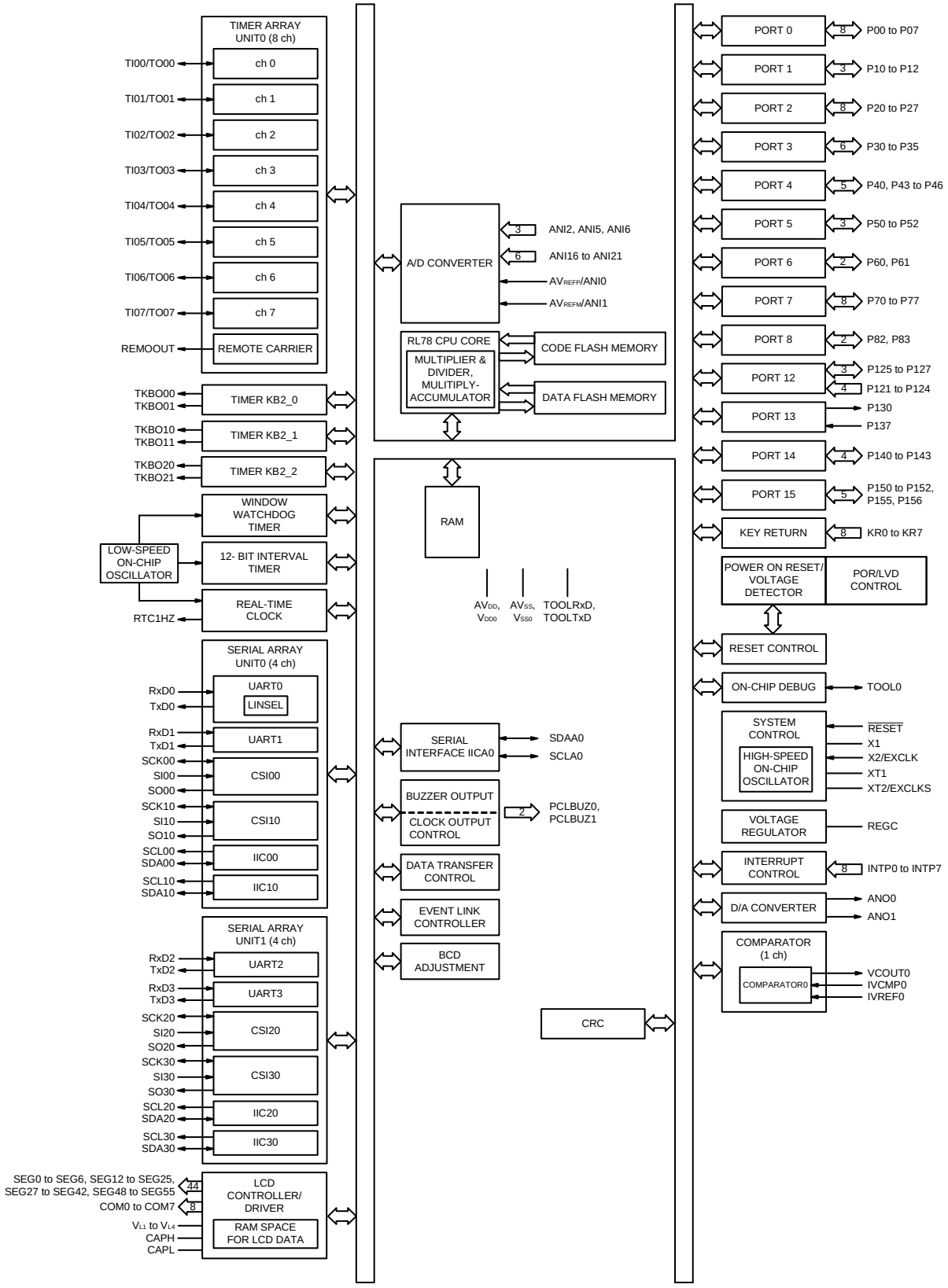
ANI0 to ANI6, ANI16 to ANI21 : Analog Input
ANO0, ANO1 : Analog Output
$AV_{DD}$ : Analog Power Supply
$AV_{REFM}$ : Analog Reference Voltage Minus
$AV_{REFP}$ : Analog Reference Voltage Plus
$AV_{SS}$ : Analog Ground
CAPH, CAPL : Capacitor for LCD
COM0 to COM7 : LCD Common Output
EXCLK : External Clock Input (Main System Clock)
EXCLKS : External Clock Input (Subsystem Clock)
INTP0 to INTP7 : External Interrupt Input
IVCMP0, IVCMP1 : Comparator Input
IVREF0, IVREF1 : Comparator Reference Input
KR0 to KR7 : Key Return
P00 to P07 : Port 0
P10 to P17 : Port 1
P20 to P27 : Port 2
P30 to P37 : Port 3
P40 to P46 : Port 4
P50 to P57 : Port 5
P60 to P62 : Port 6
P70 to P77 : Port 7
P80 to P83 : Port 8
P121 to P127 : Port 12
P130, P137 : Port 13
P140 to P143 : Port 14
P150 to P156 : Port 15
PCLBUZ0, PCLBUZ1 : Programmable Clock Output/ Buzzer Output
REGC : Regulator Capacitance
REMOOUT : Remote Control Output
$\overline{\text{RESET}}$ : Reset
RTC1HZ : Real-time Clock Correction Clock (1 Hz) Output
RxD0 to RxD3 : Receive Data
SCK00, SCK10, SCK20, SCK30 : Serial Clock Input/Output
SCLA0 : Serial Clock Input/Output
SCL00, SCL10, SCL20, SCL30 : Serial Clock Output
SDAA0, SDA00, SDA10, SDA20, SDA30 : Serial Data Input/Output
SEG0 to SEG55 : LCD Segment Output
SI00, SI10, SI20, SI30 : Serial Data Input
SO00, SO10, SO20, SO30 : Serial Data Output
TI00 to TI07 : Timer Input
TO00 to TO07 : Timer Output
TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21
TOOL0 : Data Input/Output for Tool
TOOLRxD, TOOLTxD : Data Input/Output for External Device
UDM, UDP : USB Input/Output
$U_{REGC}$ : USB Regulator Capacitance
$UV_{BUS}$ : USB Input/USB Power Supply
TxD0 to TxD3 : Transmit Data
VCOUT0, VCOUT1 : Comparator Output
$V_{DD0}$, $V_{DD1}$ : Power Supply
$V_{L1}$ to $V_{L4}$ : LCD Power Supply
$V_{SS0}$, $V_{SS1}$ : Ground
X1, X2 : Crystal Oscillator (Main System Clock)
XT1, XT2 : Crystal Oscillator (Subsystem Clock)

## 1.5 Block Diagram

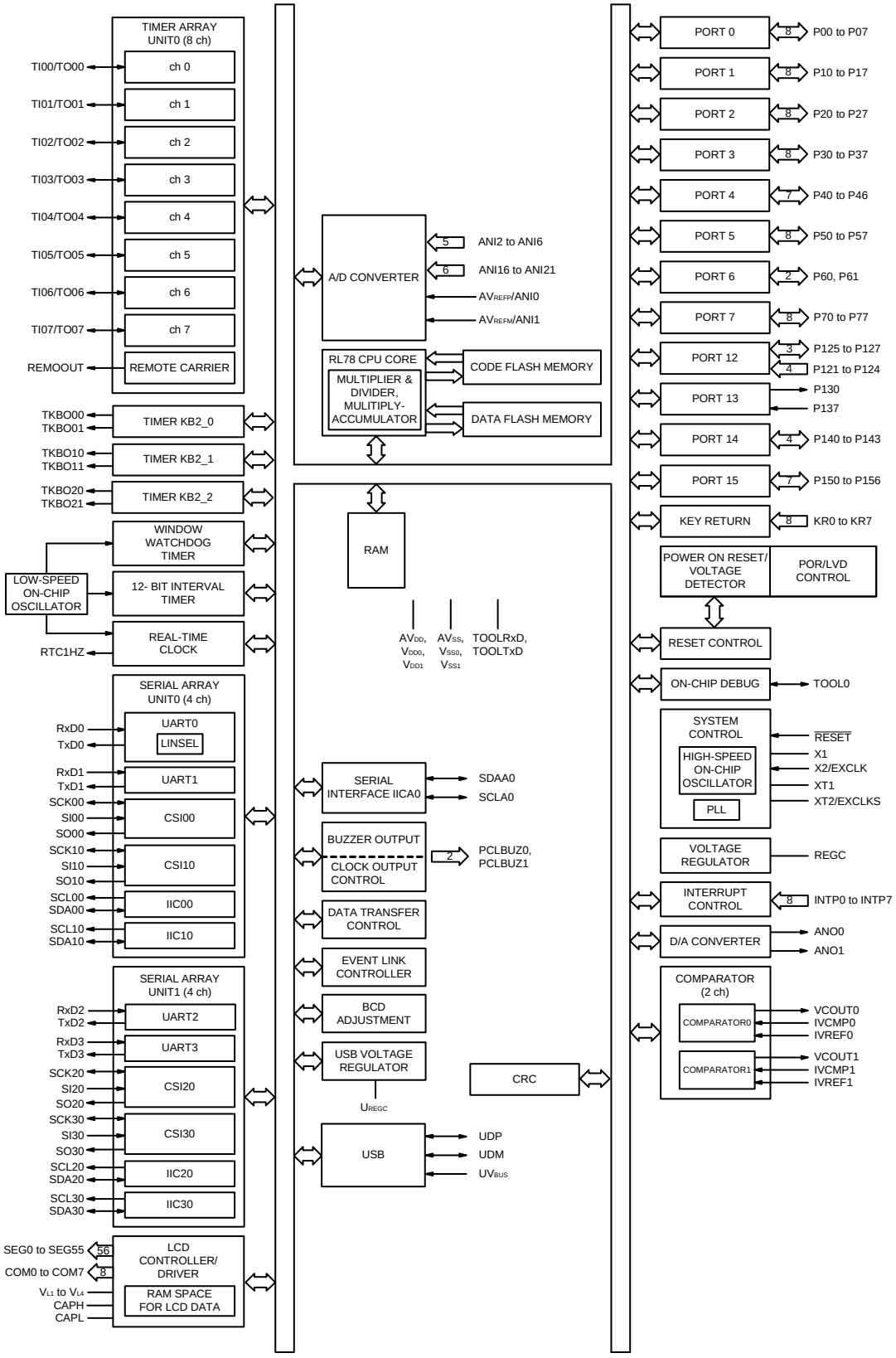
### 1.5.1 80/85-pin products (with USB)



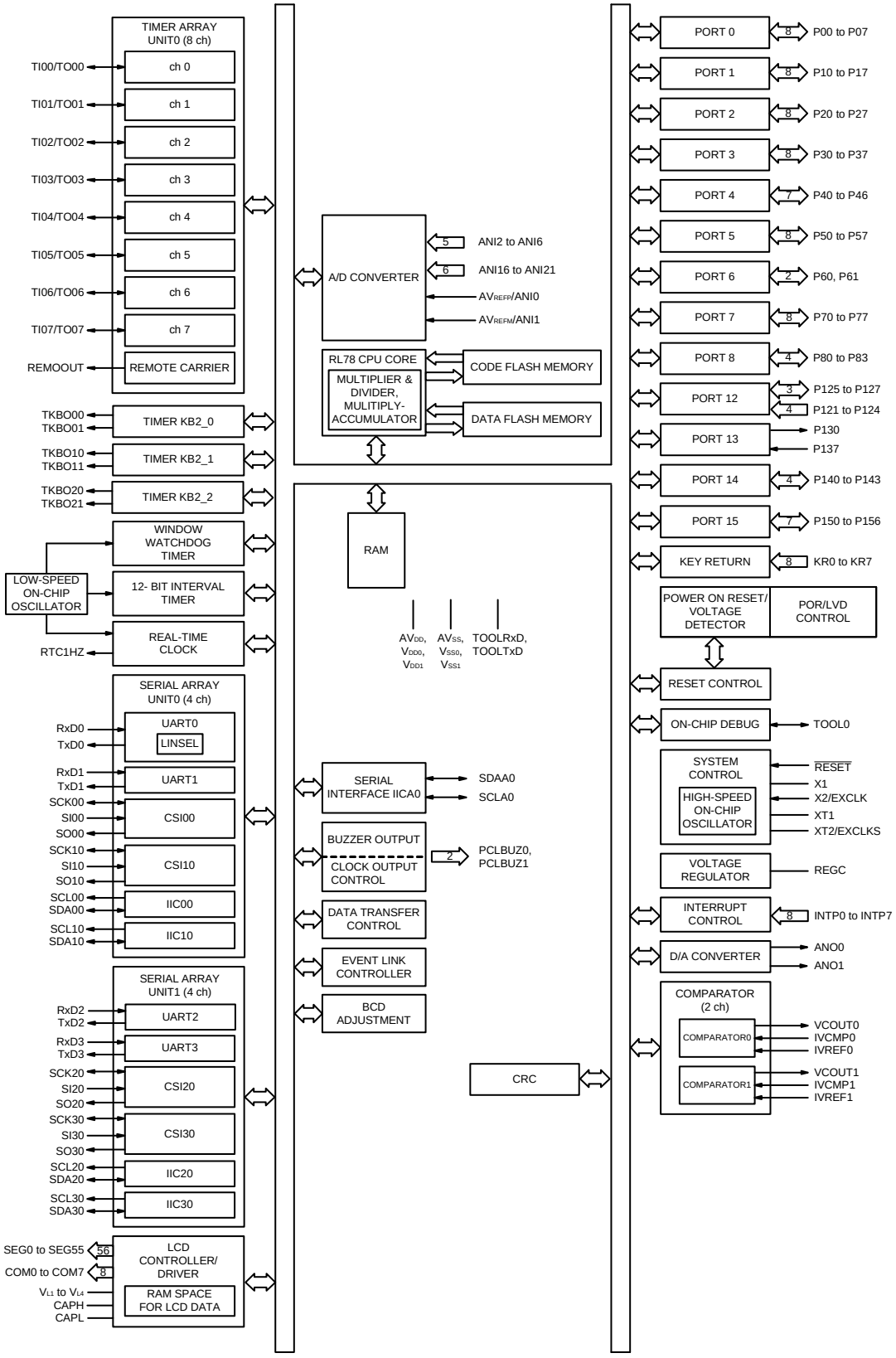
## 1.5.2 80/85-pin products (without USB)



### 1.5.3 100-pin products (with USB)



### 1.5.4 100-pin products (without USB)



## 1.6 Outline of Functions

**[80/85-pin, 100-pin products (with USB)]** **(1/2)**

| Item | | 80/85-pin | 100-pin |
|---|---|---|---|
| | | R5F110Mx/R5F110Nx (x = E to H, J) | R5F110Px (x = E to H, J) |
| Code flash memory (KB) | | 64 to 256 | 64 to 256 |
| Data flash memory (KB) | | 8 | 8 |
| RAM (KB) | | 8 to 16 Note 1 | 8 to 16 Note 1 |
| Memory space | | 1 MB | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>1 to 20 MHz: VDD = 2.7 to 3.6 V, 1 to 8 MHz: VDD = 1.8 to 2.7 V, 1 to 4 MHz: VDD = 1.6 to 1.8 V | |
| | High-speed on-chip oscillator clock | HS (high-speed main) operation mode: 1 to 24 MHz (VDD = 2.7 to 3.6 V),<br>HS (high-speed main) operation mode: 1 to 16 MHz (VDD = 2.4 to 3.6 V),<br>LS (low-speed main) operation mode: 1 to 8 MHz (VDD = 1.8 to 3.6 V),<br>LV (low-voltage main) operation mode: 1 to 4 MHz (VDD = 1.6 to 3.6 V) | |
| | PLL clock | 6, 12, 24 MHz Note 2: VDD = 2.4 to 3.6 V | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS)<br>32.768 kHz (TYP.): VDD = 1.6 to 3.6 V | |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): VDD = 1.6 to 3.6 V | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | |
| Minimum instruction execution time | | 0.04167 μs (High-speed on-chip oscillator clock: fHOCO = fIH = 24 MHz operation) | |
| | | 0.04167 μs (PLL clock: fPLL = 48 MHz/fIH = 24 MHz Note 2 operation) | |
| | | 0.05 μs (High-speed system clock: fMX = 20 MHz operation) | |
| | | 30.5 μs (Subsystem clock: fSUB = 32.768 kHz operation) | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | |
| I/O port | Total | 59 | 77 |
| | CMOS I/O | 51 | 69 |
| | CMOS input | 5 | 5 |
| | CMOS output | 1 | 1 |
| | N-ch open-drain I/O (6 V tolerance) | 2 | 2 |
| Timer | 16-bit timer TAU | 8 channels (with 1 channel remote control output function) (Timer outputs: 8, PWM outputs: 7 Note 3) | |
| | 16-bit timer KB2 | 3 channels (PWM outputs: 6) | |
| | Watchdog timer | 1 channel | |
| | 12-bit interval timer | 1 channel | |
| | Real-time clock 2 | 1 channel | |
| | RTC output | 1<br>1 Hz (subsystem clock: fSUB = 32.768 kHz) | |

**Note 1.** In the case of the 16 KB, this is about 15 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/L1C User's Manual).

**Note 2.** In the PLL clock 48 MHz operation, the system clock is 2/4/8 dividing ratio.

**Note 3.** The number of outputs varies, depending on the setting of channels in use and the number of the master.

**(2/2)**

| Item | | | 80/85-pin | 100-pin |
|---|---|---|---|---|
| | | | R5F110Mx/R5F110Nx (x = E to H, J) | R5F110Px (x = E to H, J) |
| Clock output/buzzer output | | | 2 | 2 |
| | | | • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | |
| 8/12-bit resolution A/D converter | | | 9 channels | 13 channels |
| D/A converter | | | 2 channels | 2 channels |
| Comparator | | | 1 channel | 2 channels |
| Serial interface | | | • Simplified SPI (CSI): 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 1 channel<br>• Simplified SPI (CSI): 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• Simplified SPI (CSI): 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• Simplified SPI (CSI): 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel | |
| | $I^2C$ bus | | 1 channel | 1 channel |
| USB | Function | | 1 channel | |
| LCD controller/driver | | | Internal voltage boosting method, capacitor split method, and external resistance division method are switchable. | |
| | Segment signal output | | 44 (40) Note 1 | 56 (52) Note 1 |
| | Common signal output | | 4 (8) Note 1 | |
| Data transfer controller (DTC) | | | 32 sources | 33 sources |
| Event link controller (ELC) | | | Event input: 30, Event trigger output: 22 | Event input: 31, Event trigger output: 22 |
| Vectored interrupt sources | Internal | | 36 | 37 |
| | External | | 9 | 9 |
| Key interrupt | | | 8 | 8 |
| Reset | | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note 2<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | |
| Power-on-reset circuit | | | • Power-on-reset: 1.51 ± 0.03 V<br>• Power-down-reset: 1.50 ± 0.03 V | |
| Voltage detector | | | • Rising edge: 1.67 V to 3.13 V (12 stages)<br>• Falling edge: 1.63 V to 3.06 V (12 stages) | |
| On-chip debug function | | | Provided | |
| Power supply voltage | | | $V_{DD}$ = 1.6 to 3.6 V ($T_A$ = -40 to +85°C)<br>$V_{DD}$ = 2.4 to 3.6 V ($T_A$ = -40 to +105°C) | |
| Operating ambient temperature | | | $T_A$ = -40 to +85°C (A: Consumer applications), $T_A$ = -40 to +105°C (G: Industrial applications) | |

**Note 1.** The number in parentheses indicates the number of signal outputs when 8 coms are used.

**Note 2.** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

**[80/85-pin, 100-pin products (without USB)]** **(1/2)**

| Item | | 80/85-pin | 100-pin |
|---|---|---|---|
| | | R5F111Mx/R5F111Nx (x = E to H, J) | R5F111Px (x = E to H, J) |
| Code flash memory (KB) | | 64 to 256 | 64 to 256 |
| Data flash memory (KB) | | 8 | 8 |
| RAM (KB) | | 8 to 16 Note 1 | 8 to 16 Note 1 |
| Memory space | | 1 MB | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>1 to 20 MHz: VDD = 2.7 to 3.6 V, 1 to 8 MHz: VDD = 1.8 to 2.7 V, 1 to 4 MHz: VDD = 1.6 to 1.8 V | |
| | High-speed on-chip oscillator clock | HS (high-speed main) operation mode: 1 to 24 MHz (VDD = 2.7 to 3.6 V),<br>HS (high-speed main) operation mode: 1 to 16 MHz (VDD = 2.4 to 3.6 V,<br>LS (low-speed main) operation mode: 1 to 8 MHz (VDD = 1.8 to 3.6 V),<br>LV (low-voltage main) operation mode: 1 to 4 MHz (VDD = 1.6 to 3.6 V) | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS)<br>32.768 kHz (TYP.): VDD = 1.6 to 3.6 V | |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): VDD = 1.6 to 3.6 V | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | |
| Minimum instruction execution time | | 0.04167 μs (High-speed on-chip oscillator clock: fHOCO = fIH = 24 MHz operation) | |
| | | 0.05 μs (High-speed system clock: fMX = 20 MHz operation) | |
| | | 30.5 μs (Subsystem clock: fSUB = 32.768 kHz operation) | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | |
| I/O port | Total | 63 | 81 |
| | CMOS I/O | 55 | 73 |
| | CMOS input | 5 | 5 |
| | CMOS output | 1 | 1 |
| | N-ch open-drain I/O (6 V tolerance) | 2 | 2 |
| Timer | 16-bit timer TAU | 8 channels (with 1 channel remote control output function) (Timer outputs: 8, PWM outputs: 7 Note 2) | |
| | 16-bit timer KB2 | 3 channels (PWM outputs: 6) | |
| | Watchdog timer | 1 channel | |
| | 12-bit interval timer | 1 channel | |
| | Real-time clock 2 | 1 channel | |
| | RTC output | 1<br>1 Hz (subsystem clock: fSUB = 32.768 kHz) | |

**Note 1.** In the case of the 16 KB, this is about 15 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/L1C User's Manual).

**Note 2.** The number of outputs varies, depending on the setting of channels in use and the number of the master.

**(2/2)**

| Item | | | 80/85-pin | 100-pin |
|---|---|---|---|---|
| | | | R5F111Mx/R5F111Nx (x = E to H, J) | R5F111Px (x = E to H, J) |
| Clock output/buzzer output | | | 2 | 2 |
| | | | • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | |
| 8/12-bit resolution A/D converter | | | 11 channels | 13 channels |
| D/A converter | | | 2 channels | 2 channels |
| Comparator | | | 1 channel | 2 channels |
| Serial interface | | | • Simplified SPI (CSI): 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 1 channel<br>• Simplified SPI (CSI): 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• Simplified SPI (CSI): 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• Simplified SPI (CSI): 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel | |
| | $I^2C$ bus | | 1 channel | 1 channel |
| LCD controller/driver | | | Internal voltage boosting method, capacitor split method, and external resistance division method are switchable. | |
| | Segment signal output | | 44 (40) Note 1 | 56 (52) Note 1 |
| | Common signal output | | 4 (8) Note 1 | |
| Data transfer controller (DTC) | | | 30 sources | 31 sources |
| Event link controller (ELC) | | | Event input: 30, Event trigger output: 22 | Event input: 31, Event trigger output: 22 |
| Vectored interrupt sources | | Internal | 32 | 33 |
| | | External | 9 | 9 |
| Key interrupt | | | 8 | 8 |
| Reset | | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note 2<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | |
| Power-on-reset circuit | | | • Power-on-reset: 1.51 ± 0.03 V<br>• Power-down-reset: 1.50 ± 0.03 V | |
| Voltage detector | | | • Rising edge: 1.67 V to 3.13 V (12 stages)<br>• Falling edge: 1.63 V to 3.06 V (12 stages) | |
| On-chip debug function | | | Provided | |
| Power supply voltage | | | $V_{DD}$ = 1.6 to 3.6 V ($T_A$ = -40 to +85°C)<br>$V_{DD}$ = 2.4 to 3.6 V ($T_A$ = -40 to +105°C) | |
| Operating ambient temperature | | | $T_A$ = -40 to +85°C (A: Consumer applications), $T_A$ = -40 to +105°C (G: Industrial applications) | |

**Note 1.** The number in parentheses indicates the number of signal outputs when 8 coms are used.

**Note 2.** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

# 2. ELECTRICAL SPECIFICATIONS ($T_A$ = -40 to +85°C)

This chapter describes the electrical specifications for the products A: Consumer applications ($T_A$ = -40 to +85°C) and G: Industrial applications (when used in the range of $T_A$ = -40 to +85°C).

**Caution 1. The RL78 microcontroller has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 With functions for each product in the RL78/L1C User's Manual.**

## 2.1 Absolute Maximum Ratings

**Absolute Maximum Ratings ($T_A$ = 25°C) (1/3)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | -0.5 to + 6.5 | V |
| | $UV_{BUS}$ | | -0.5 to + 6.5 | V |
| | $AV_{DD}$ | $AV_{DD} \leq V_{DD}$ | -0.5 to + 4.6 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | -0.3 to + 2.8 and -0.3 to $V_{DD}$ + 0.3 Note 1 | V |
| $U_{REGC}$ pin input voltage | $V_{IUREGC}$ | $U_{REGC}$ | -0.3 to $UV_{BUS}$ + 0.3 Note 2 | V |
| Input voltage | $V_{I1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P137, P140 to P143, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | -0.3 to $V_{DD}$ + 0.3 Note 3 | V |
| | $V_{I2}$ | P60, P61 (N-ch open-drain) | -0.3 to + 6.5 | V |
| | $V_{I3}$ | UDP, UDM | -0.3 to + 6.5 | V |
| | $V_{I4}$ | P150 to P156 | -0.3 to $AV_{DD}$ + 0.3 Note 4 | V |
| Output voltage | $V_{O1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | -0.3 to $V_{DD}$ + 0.3 Note 3 | V |
| | $V_{O2}$ | P150 to P156 | -0.3 to $AV_{DD}$ + 0.3 Note 3 | V |
| | $V_{O3}$ | UDP, UDM | -0.3 to + 3.8 | V |
| Analog input voltage | $V_{AI1}$ | ANI16 to ANI21 | -0.3 to $V_{DD}$ + 0.3 and $AV_{REF(+)}$ + 0.3 Notes 3, 5 | V |
| | $V_{AI2}$ | ANI0 to ANI6 | -0.3 to $AV_{DD}$ + 0.3 and $AV_{REF(+)}$ + 0.3 Notes 3, 5 | V |

**Note 1.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**Note 2.** Connect the $U_{REGC}$ pin to Vss via a capacitor (0.33 μF). This value regulates the absolute maximum rating of the $U_{REGC}$ pin. Do not use this pin with voltage applied to it.

**Note 3.** Must be 6.5 V or lower.

**Note 4.** Must be 4.6 V or lower.

**Note 5.** Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** $AV_{REF(+)}$: + side reference voltage of the A/D converter.

**Remark 3.** $V_{SS}$: Reference voltage

**Absolute Maximum Ratings ($T_A$ = 25°C) (2/3)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| LCD voltage | $V_{LI1}$ | $V_{L1}$ input voltage Note 1 | | -0.3 to +2.8 | V |
| | $V_{LI2}$ | $V_{L2}$ input voltage Note 1 | | -0.3 to +6.5 | V |
| | $V_{LI3}$ | $V_{L3}$ input voltage Note 1 | | -0.3 to +6.5 | V |
| | $V_{LI4}$ | $V_{L4}$ input voltage Note 1 | | -0.3 to +6.5 | V |
| | $V_{LI5}$ | CAPL, CAPH input voltage Note 1 | | -0.3 to +6.5 | V |
| | $V_{LO1}$ | $V_{L1}$ output voltage | | -0.3 to +2.8 | V |
| | $V_{LO2}$ | $V_{L2}$ output voltage | | -0.3 to +6.5 | V |
| | $V_{LO3}$ | $V_{L3}$ output voltage | | -0.3 to +6.5 | V |
| | $V_{LO4}$ | $V_{L4}$ output voltage | | -0.3 to +6.5 | V |
| | $V_{LO5}$ | CAPL, CAPH output voltage | | -0.3 to +6.5 | V |
| | $V_{LO6}$ | COM0 to COM7<br>SEG0 to SEG55<br>output voltage | External resistance division method | -0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| | | | Capacitor split method | -0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| | | | Internal voltage boosting method | -0.3 to $V_{LI4}$ + 0.3 Note 2 | V |

**Note 1.** This value only indicates the absolute maximum ratings when applying voltage to the $V_{L1}$, $V_{L2}$, $V_{L3}$, and $V_{L4}$ pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to $V_{SS}$ via a capacitor (0.47 ± 30%) and connect a capacitor (0.47 ± 30%) between the CAPL and CAPH pins.

**Note 2.** Must be 6.5 V or lower.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Absolute Maximum Ratings ($T_A$ = 25°C) (3/3)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | -40 | mA |
| | | Total of all pins -170 mA | P40 to P46 | -70 | mA |
| | | | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | -100 | mA |
| | $I_{OH2}$ | Per pin | P150 to P156 | -0.1 | mA |
| | | Total of all pins | | -0.7 | mA |
| | $I_{OH3}$ | Per pin | UDP, UDM | -3 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | 40 | mA |
| | | Total of all pins 170 mA | P40 to P46 | 70 | mA |
| | | | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | 100 | mA |
| | $I_{OL2}$ | Per pin | P150 to P156 | 0.4 | mA |
| | | Total of all pins | | 2.8 | mA |
| | $I_{OL3}$ | Per pin | UDP, UDM | 3 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | -40 to +85 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | -65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.2 Oscillator Characteristics

### 2.2.1 X1 and XT1 oscillator characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$) Note | Ceramic resonator/crystal resonator | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 16.0 | |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | 1.0 | | 8.0 | |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | 1.0 | | 4.0 | |
| XT1 clock oscillation frequency ($f_{XT}$) Note | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/L1C User's Manual.

## 2.2.2 On-chip oscillator characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{HOCO}$ | | | 1 | | 48 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | -20 to +85°C | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | -1.0 | | +1.0 | % |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 1.8 V | -5.0 | | +5.0 | % |
| | | -40 to -20°C | 1.8 V ≤ $V_{DD}$ < 3.6 V | -1.5 | | +1.5 | % |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 1.8 V | -5.5 | | +5.5 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | -15 | | +15 | % |

**Note 1.** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

**Note 2.** This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

## 2.2.3 PLL oscillator characteristics

**($T_A$ = -40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| PLL input frequency Note | $f_{PLLIN}$ | High-speed system clock | 6.00 | | 16.00 | MHz |
| PLL output frequency Note | $f_{PLL}$ | | | 48.00 | | MHz |

**Note** Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high Note 1 | $I_{OH1}$ | Per pin for P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | | | | -10.0 Note 2 | mA |
| | | Total of P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 (When duty ≤ 70% Note 3) | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | -15.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | -7.0 | mA |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | -3.0 | mA |
| | $I_{OH2}$ | Per pin for P150 to P156 | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | -0.1 Note 2 | mA |
| | | Total of all pins | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | -0.7 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ pin to an output pin.

**Note 2.** However, do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = -10.0 mA
Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Caution P00 to P02, P10 to P12, P24 to P26, P33 to P35, and P42 to P44 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low Note 1 | $I_{OL1}$ | Per pin for P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | | | | 20.0 Note 2 | mA |
| | | Per pin for P60 and P61 | | | | 15.0 Note 2 | mA |
| | | Total of P40 to P46, P130 (When duty ≤ 70% Note 3) | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 15.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 9.0 | mA |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 4.5 | mA |
| | | Total of P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P140 to P143 (When duty ≤ 70% Note 3) | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 35.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 20.0 | mA |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 10.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | 50.0 | mA |
| | $I_{OL2}$ | Per pin for P150 to P156 | | | | 0.4 Note 2 | mA |
| | | Total of all pins | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | 2.8 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $V_{SS}$ pin.

**Note 2.** However, do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression
(when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P140 to P143 | Normal input buffer | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | P00, P01, P10, P11, P24, P25, P33, P34, P43, P44 | TTL input buffer 3.3 V ≤ $V_{DD}$ ≤ 3.6 V | 2.0 | | $V_{DD}$ | V |
| | | | TTL input buffer 1.6 V ≤ $V_{DD}$ < 3.3 V | 1.50 | | $V_{DD}$ | V |
| | $V_{IH3}$ | P150 to P156 | | 0.7 $AV_{DD}$ | | $AV_{DD}$ | V |
| | $V_{IH4}$ | P60, P61 | | 0.7 $V_{DD}$ | | 6.0 | V |
| | $V_{IH5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P140 to P143 | Normal input buffer | 0 | | 0.2 $V_{DD}$ | V |
| | $V_{IL2}$ | P00, P01, P10, P11, P24, P25, P33, P34, P43, P44 | TTL input buffer 3.3 V ≤ $V_{DD}$ ≤ 3.6 V | 0 | | 0.5 | V |
| | | | TTL input buffer 1.6 V ≤ $V_{DD}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P150 to P156 | | 0 | | 0.3 $AV_{DD}$ | V |
| | $V_{IL4}$ | P60, P61 | | 0 | | 0.3 $V_{DD}$ | V |
| | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0 | | 0.2 $V_{DD}$ | V |

**Caution The maximum value of $V_{IH}$ of pins P00 to P02, P10 to P12, P24 to P26, P33 to P35, and P42 to P44 is $V_{DD}$, even in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH1}$ = -2.0 mA | $V_{DD}$ - 0.6 | | | V |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH1}$ = -1.5 mA | $V_{DD}$ - 0.5 | | | V |
| | | | 1.6 V ≤ $V_{DD}$ < 3.6 V, $I_{OH1}$ = -1.0 mA | $V_{DD}$ - 0.5 | | | V |
| | $V_{OH2}$ | P150 to P156 | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH2}$ = -100 µA | $AV_{DD}$ - 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V, $I_{OL1}$ = 0.3 mA | | | 0.4 | V |
| | $V_{OL2}$ | P150 to P156 | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL2}$ = 400 µA | | | 0.4 | V |
| | $V_{OL3}$ | P60, P61 | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL3}$ = 3.0 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL3}$ = 2.0 mA | | | 0.4 | V |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 1.8 V, $I_{OL3}$ = 1.0 mA | | | 0.4 | V |

**Caution P00 to P02, P10 to P12, P24 to P26, P33 to P35, and P42 to P44 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P137, P140 to P143, $\overline{RESET}$ | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P20, P21, P140 to P143 | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS) | $V_I$ = $V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| | $I_{LIH4}$ | P150 to P156 | $V_I$ = $AV_{DD}$ | | | | 1 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P137, P140 to P143, $\overline{RESET}$ | $V_I$ = $V_{SS}$ | | | | -1 | μA |
| | $I_{LIL2}$ | P20, P21, P140 to P143 | $V_I$ = $V_{SS}$ | | | | -1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS) | $V_I$ = $V_{SS}$ | In input port or external clock input | | | -1 | μA |
| | | | | In resonator connection | | | -10 | μA |
| | $I_{LIL4}$ | P150 to P156 | $V_I$ = $AV_{SS}$ | | | | -1 | μA |
| On-chip pull-up resistance | $R_{U1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P140 to P143, P125 to P127 | $V_I$ = $V_{SS}$ | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | 10 | 20 | 100 | kΩ |
| | | | | 1.6 V ≤ $V_{DD}$ ≤ 2.4 V | 10 | 30 | 100 | |
| | $R_{U2}$ | P40 to P46, P80 to P83 | $V_I$ = $V_{SS}$ | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.3.2 Supply current characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 48 MHz Note 3, $f_{IH}$ = 24 MHz Note 3 | Basic operation | $V_{DD}$ = 3.6 V | | 2.2 | 2.8 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.2 | 2.8 | |
| | | | | | Normal operation | $V_{DD}$ = 3.6 V | | 4.4 | 8.5 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.4 | 8.5 | |
| | | | | $f_{HOCO}$ = 24 MHz Note 3, $f_{IH}$ = 24 MHz Note 3 | Basic operation | $V_{DD}$ = 3.6 V | | 2.0 | 2.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.0 | 2.6 | |
| | | | | | Normal operation | $V_{DD}$ = 3.6 V | | 4.2 | 6.8 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.2 | 6.8 | |
| | | | | $f_{HOCO}$ = 16 MHz Note 3, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 3.6 V | | 3.1 | 4.9 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.1 | 4.9 | |
| | | | LS (low-speed main) mode Note 5 | $f_{HOCO}$ = 8 MHz Note 3, $f_{IH}$ = 8 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.4 | 2.2 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.4 | 2.2 | |
| | | | LV (low-voltage main) mode Note 5 | $f_{HOCO}$ = 4 MHz Note 3, $f_{IH}$ = 4 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.3 | 1.8 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.3 | 1.8 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.6 V | Normal operation | Square wave input | | 3.5 | 5.5 | mA |
| | | | | | | Resonator connection | | 3.6 | 5.7 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.5 | 5.5 | |
| | | | | | | Resonator connection | | 3.6 | 5.7 | |
| | | | | $f_{MX}$ = 16 MHz Note 2, $V_{DD}$ = 3.6 V | Normal operation | Square wave input | | 2.9 | 4.5 | |
| | | | | | | Resonator connection | | 3.1 | 4.6 | |
| | | | | $f_{MX}$ = 16 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.9 | 4.5 | |
| | | | | | | Resonator connection | | 3.1 | 4.6 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.6 V | Normal operation | Square wave input | | 2.1 | 3.2 | |
| | | | | | | Resonator connection | | 2.2 | 3.2 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.1 | 3.2 | |
| | | | | | | Resonator connection | | 2.2 | 3.2 | |
| | | | LS (low-speed main) mode Note 5 | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.6 V | Normal operation | Square wave input | | 1.2 | 2.0 | mA |
| | | | | | | Resonator connection | | 1.3 | 2.0 | |
| | | | | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.2 | 2.1 | |
| | | | | | | Resonator connection | | 1.3 | 2.2 | |
| | | | HS (High-speed main) mode (PLL operation) | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 24 MHz Note 2 | Normal operation | $V_{DD}$ = 3.6 V | | 4.7 | 7.5 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.7 | 7.5 | |
| | | | | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 12 MHz Note 2 | Normal operation | $V_{DD}$ = 3.6 V | | 3.1 | 5.1 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.1 | 5.1 | |
| | | | | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 6 MHz Note 2 | Normal operation | $V_{DD}$ = 3.6 V | | 2.3 | 3.9 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.3 | 3.9 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.6 | 6.9 | μA |
| | | | | | | Resonator connection | | 4.7 | 6.9 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.9 | 7.0 | |
| | | | | | | Resonator connection | | 5.0 | 7.2 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 5.2 | 7.6 | |
| | | | | | | Resonator connection | | 5.2 | 7.7 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 5.5 | 9.3 | |
| | | | | | | Resonator connection | | 5.6 | 9.4 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.2 | 13.3 | |
| | | | | | | Resonator connection | | 6.2 | 13.4 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, or $V_{SS}$. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.
<R>
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into LCD controller/driver, A/D converter, D/A converter, comparator, LVD circuit, USB 2.0 function module, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the real-time clock 2.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

<R> **Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

| | |
|---|---|
| HS (high-speed main) mode: | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 24 MHz |
| | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 4 MHz |

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (48 MHz max.)

**Remark 3.** $f_{IH}$: Main system clock source frequency when the high-speed on-chip oscillator clock divided 1, 2, 4, or 8, or the PLL clock divided by 2, 4, or 8 is selected (24 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 6 | $f_{HOCO}$ = 48 MHz Note 4, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 3.6 V | | 0.77 | 2.70 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.77 | 2.70 | |
| | | | | $f_{HOCO}$ = 24 MHz Note 4, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 3.6 V | | 0.55 | 1.91 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.55 | 1.90 | |
| | | | | $f_{HOCO}$ = 16 MHz Note 4, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 3.6 V | | 0.48 | 1.41 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.47 | 1.41 | |
| | | | LS (low-speed main) mode Note 6 | $f_{HOCO}$ = 8 MHz Note 4, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 300 | 770 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 300 | 770 | |
| | | | LV (low-voltage main) mode Note 6 | $f_{HOCO}$ = 4 MHz Note 4, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 440 | 770 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 440 | 770 | |
| | | | HS (high-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.6 V | Square wave input | | 0.35 | 1.63 | mA |
| | | | | | Resonator connection | | 0.51 | 1.68 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.34 | 1.63 | |
| | | | | | Resonator connection | | 0.51 | 1.68 | |
| | | | | $f_{MX}$ = 16 MHz Note 3, $V_{DD}$ = 3.6 V | Square wave input | | 0.30 | 1.22 | |
| | | | | | Resonator connection | | 0.45 | 1.39 | |
| | | | | $f_{MX}$ = 16 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.29 | 1.20 | |
| | | | | | Resonator connection | | 0.45 | 1.38 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.6 V | Square wave input | | 0.23 | 0.82 | |
| | | | | | Resonator connection | | 0.30 | 0.90 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.22 | 0.81 | |
| | | | | | Resonator connection | | 0.30 | 0.89 | |
| | | | LS (low-speed main) mode Note 6 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 120 | 510 | μA |
| | | | | | Resonator connection | | 170 | 560 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 130 | 520 | |
| | | | | | Resonator connection | | 170 | 570 | |
| | | | HS (High-speed main) mode (PLL operation) | $f_{MX}$ = 48 MHz, $f_{CLK}$ = 24 MHz Note 3 | $V_{DD}$ = 3.6 V | | 0.99 | 2.89 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.99 | 2.88 | |
| | | | | $f_{MX}$ = 48 MHz, $f_{CLK}$ = 12 MHz Note 3 | $V_{DD}$ = 3.6 V | | 0.89 | 2.48 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.89 | 2.47 | |
| | | | | $f_{MX}$ = 48 MHz, $f_{CLK}$ = 6 MHz Note 3 | $V_{DD}$ = 3.6 V | | 0.84 | 2.27 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.84 | 2.27 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = -40°C | Square wave input | | 0.32 | 0.61 | μA |
| | | | | | Resonator connection | | 0.51 | 0.80 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +25°C | Square wave input | | 0.41 | 0.74 | |
| | | | | | Resonator connection | | 0.62 | 0.91 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +50°C | Square wave input | | 0.52 | 2.30 | |
| | | | | | Resonator connection | | 0.75 | 2.49 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +70°C | Square wave input | | 0.82 | 4.03 | |
| | | | | | Resonator connection | | 1.08 | 4.22 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +85°C | Square wave input | | 1.38 | 8.04 | |
| | | | | | Resonator connection | | 1.62 | 8.23 | |
| | $I_{DD3}$ | STOP mode Note 7 | $T_A$ = -40°C | | | | 0.18 | 0.52 | μA |
| | | | $T_A$ = +25°C | | | | 0.25 | 0.52 | |
| | | | $T_A$ = +50°C | | | | 0.34 | 2.21 | |
| | | | $T_A$ = +70°C | | | | 0.64 | 3.94 | |
| | | | $T_A$ = +85°C | | | | 1.18 | 7.95 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.
<R>
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into LCD controller/driver, A/D converter, D/A converter, comparator, LVD circuit, USB 2.0 function module, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the real-time clock 2.
In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).
<R>

**Note 6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

| | |
|---|---|
| HS (high-speed main) mode: | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 24 MHz |
| | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 4 MHz |

**Note 7.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (48 MHz max.)

**Remark 3.** $f_{IH}$: Main system clock source frequency when the high-speed on-chip oscillator clock divided 1, 2, 4, or 8, or the PLL clock divided by 2, 4, or 8 is selected (24 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

<R> **Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | | | 0.20 | | μA |
| RTC2 operating current | $I_{RTC}$ Notes 1, 3 | | | | | | 0.02 | | μA |
| 12-bit interval timer operating current | $I_{TMKA}$ Notes 1, 2, 4 | | | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 5 | $f_{IL}$ = 15 kHz | | | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 6, 7 | $AV_{DD}$ = 3.0 V, when conversion at maximum speed | | | | | 422 | 720 | μA |
| $AV_{REF(+)}$ current | $I_{AVREF}$ Note 8 | $AV_{DD}$ = 3.0 V, ADREFP1 = 0, ADREFP0 = 0 Note 7 | | | | | 14.0 | 25.0 | μA |
| | | $AV_{REFP}$ = 3.0 V, ADREFP1 = 0, ADREFP0 = 1 Note 10 | | | | | 14.0 | 25.0 | |
| | | ADREFP1 = 1, ADREFP0 = 0 Note 1 | | | | | 14.0 | 25.0 | |
| A/D converter reference voltage current | $I_{ADREF}$ Notes 1, 9 | $V_{DD}$ = 3.0 V | | | | | 75.0 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | | | 78 | | μA |
| D/A converter operating current | $I_{DAC}$ Notes 1, 11 | Per D/A converter channel | | | | | 0.53 | 1.5 | mA |
| Comparator operating current | $I_{CMP}$ Notes 1, 12 | $V_{DD}$ = 3.6 V, Regulator output voltage = 2.1 V | Window mode | | | | 12.5 | | μA |
| | | | Comparator high-speed mode | | | | 4.5 | | μA |
| | | | Comparator low-speed mode | | | | 1.2 | | μA |
| | | $V_{DD}$ = 3.6 V, Regulator output voltage = 1.8 V | Window mode | | | | 7.05 | | μA |
| | | | Comparator high-speed mode | | | | 2.2 | | μA |
| | | | Comparator low-speed mode | | | | 0.9 | | μA |
| LVD operating current | $I_{LVI}$ Notes 1, 13 | | | | | | 0.06 | | μA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 14 | | | | | | 2.50 | 12.20 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 15 | | | | | | 1.68 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 16 | | | | 0.34 | 1.10 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | | | 0.53 | 2.04 | |
| | | Simplified SPI (CSI)/UART operation | | | | | 0.70 | 1.54 | mA |
| LCD operating current | $I_{LCD1}$ Notes 17, 18 | External resistance division method | $f_{LCD}$ = $f_{SUB}$ LCD clock = 128 Hz | 1/3 bias 4-time slice | $V_{DD}$ = 3.6 V, $L_{V4}$ = 3.6 V | | 0.14 | | μA |
| | $I_{LCD2}$ Note 17 | Internal voltage boosting method | $f_{LCD}$ = $f_{SUB}$ LCD clock = 128 Hz | 1/3 bias 4-time slice | $V_{DD}$ = 3.0 V, $L_{V4}$ = 3.0 V (VLCD = 04H) | | 0.61 | | μA |
| | $I_{LCD3}$ Note 17 | Capacitor split method | $f_{LCD}$ = $f_{SUB}$ LCD clock = 128 Hz | 1/3 bias 4-time slice | $V_{DD}$ = 3.0 V, $L_{V4}$ = 3.0 V | | 0.12 | | μA |
| USB current Note 19 | $I_{USB}$ Note 20 | Operating current during USB communication | | | | | 4.88 | | mA |
| | $I_{USB}$ Note 21 | Operating current in the USB suspended state | | | | | 0.04 | | mA |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Current flowing to $V_{DD}$.

**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**Note 3.** Current flowing only to the real-time clock 2 (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock 2 operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock 2.

**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{TMKA}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the 12-bit interval timer.

**Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer operates in STOP mode.

**Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$, $I_{AVREF}$, $I_{ADREF}$ when the A/D converter operates in an operation mode or the HALT mode.

**Note 7.** Current flowing to the $AV_{DD}$.

**Note 8.** Current flowing from the reference voltage source of A/D converter.

**Note 9.** Operation current flowing to the internal reference voltage.

**Note 10.** Current flowing to the $AV_{REFP}$.

**Note 11.** Current flowing only to the D/A converter. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{DA}$ when the D/A converter operates in an operation mode or the HALT mode.

**Note 12.** Current flowing only to the comparator circuit. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{CMP}$ when the comparator circuit operates in the Operating, HALT or STOP mode.

**Note 13.** Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVI}$ when the LVD circuit operates in the Operating, HALT or STOP mode.

**Note 14.** Current flowing only during self-programming.

**Note 15.** Current flowing only during data flash rewrite.

**Note 16.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/L1C User's Manual.

**Note 17.** Current flowing only to the LCD controller/driver ($V_{DD}$ pin). The current value of the RL78 microcontrollers is the sum of the LCD operating current ($I_{LCD1}$, $I_{LCD2}$ or $I_{LCD3}$) to the supply current ($I_{DD1}$, or $I_{DD2}$) when the LCD controller/driver operates in an operation mode or HALT mode. Not including the current that flows through the LCD panel.

**Note 18.** Not including the current that flows through the external divider resistor divider resistor.

**Note 19.** Current flowing to the $UV_{BUS}$.

**Note 20.** Including the operating current when $f_{PLL}$ = 48 MHz.

**Note 21.** Including the current supplied from the pull-up resistor of the UDP pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.

**Remark 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**Remark 2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 3.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**Remark 4.** Temperature condition of the TYP. value is $T_A$ = 25°C

## 2.4 AC Characteristics

### 2.4.1 Basic operation

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)** **(1/2)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 0.0417 | | 1 | μs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | μs |
| | | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | 0.125 | | 1 | μs |
| | | | LV (low-voltage main) mode | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | 0.25 | | 1 | μs |
| | | Subsystem clock ($f_{SUB}$) operation | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | 28.5 | 30.5 | 31.3 | μs |
| | | In the self-programming mode | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 0.0417 | | 1 | μs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | μs |
| | | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | 0.125 | | 1 | μs |
| | | | LV (low-voltage main) mode | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | 0.25 | | 1 | μs |
| External main system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 1.0 | | 8.0 | MHz |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 1.0 | | 4.0 | MHz |
| | $f_{EXT}$ | | | | 32 | | 35 | kHz |
| External main system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 30 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 60 | | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 120 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | μs |
| TI00 to TI07 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 | | | ns |

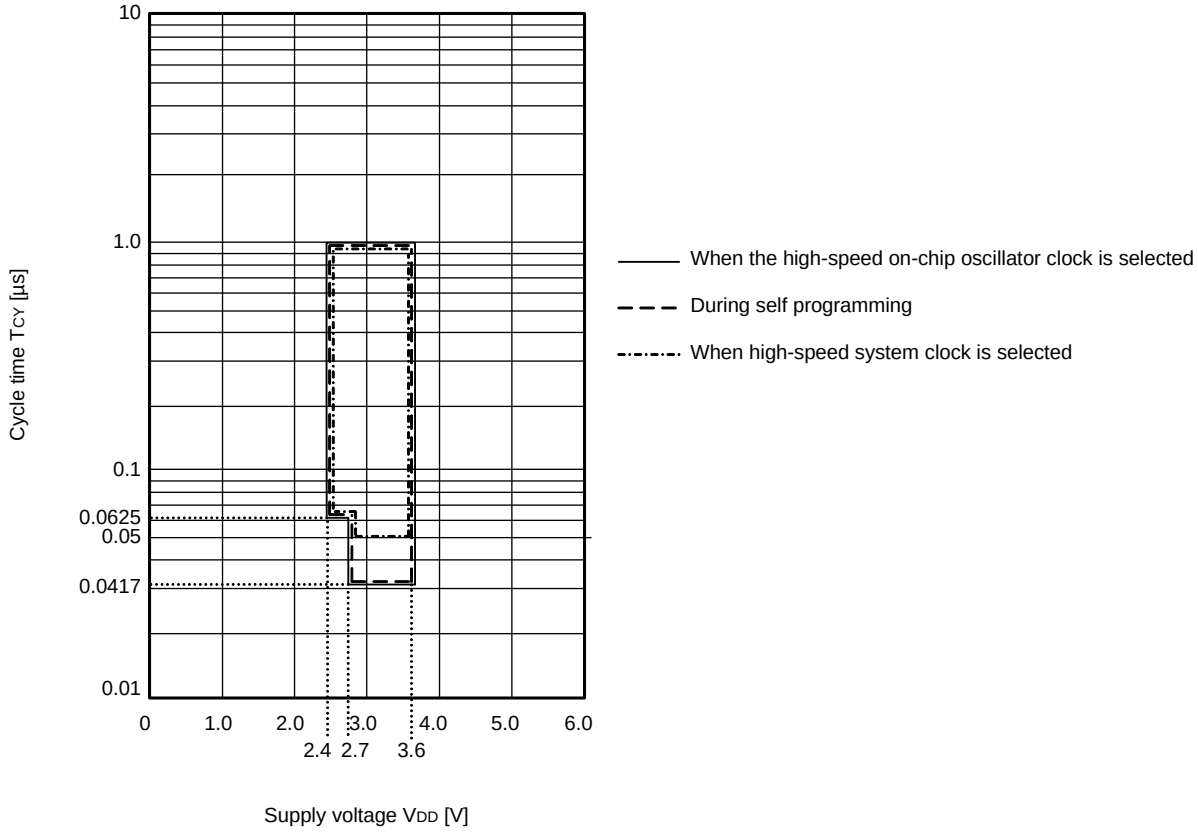
**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 7))

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)** **(2/2)**

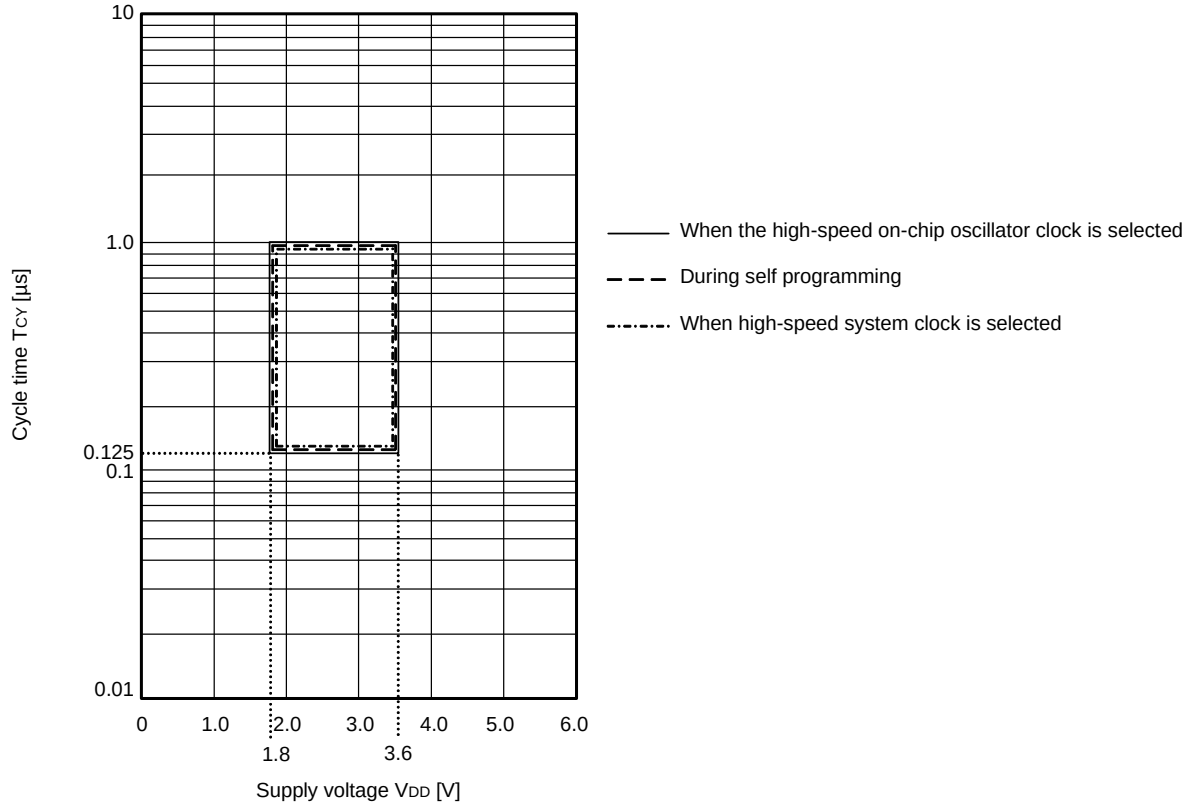
| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| TO00 to TO07, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21 output frequency | $f_{TO}$ | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 8 | MHz |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 8 | MHz |
| | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | | 4 | MHz |
| | | LV (low-voltage main) mode | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | 2 | MHz |
| PCLBUZ0, PCLBUZ1 output frequency | $f_{PCL}$ | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 8 | MHz |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 8 | MHz |
| | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | | 4 | MHz |
| | | LV (low-voltage main) mode | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | | 2 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 to INTP7 | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | 1 | | | µs |
| Key interrupt input low-level width | $t_{KR}$ | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | 250 | | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | 1 | | | µs |
| TMKB2 forced output stop input high-level width | $t_{IHR}$ | INTP0 to INTP7 | $f_{CLK}$ > 16 MHz | 125 | | | ns |
| | | | $f_{CLK}$ ≤ 16 MHz | 2 | | | $f_{CLK}$ |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | 10 | | | µs |

Minimum Instruction Execution Time during Main System Clock Operation

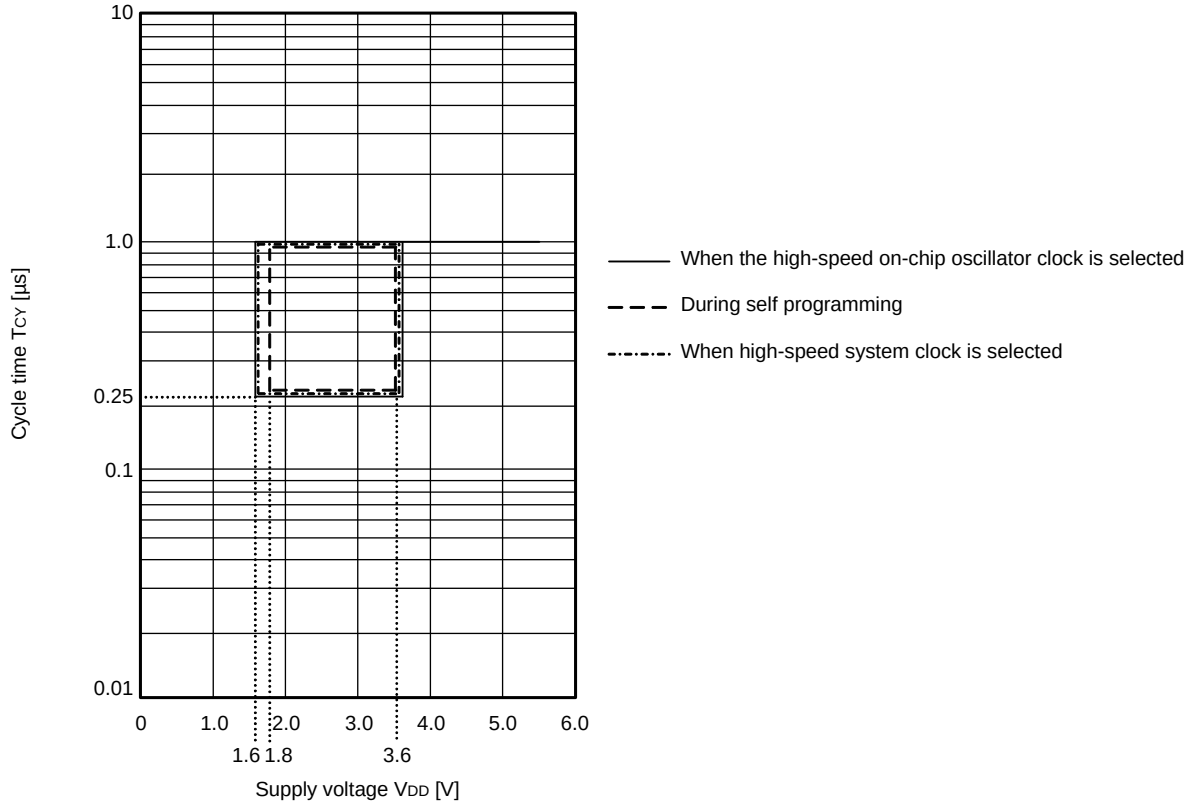
$T_{CY}$ vs $V_{DD}$ (HS (high-speed main) mode)



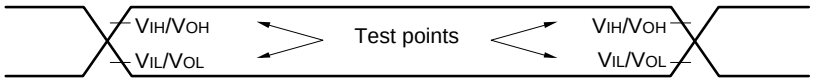
$T_{CY}$ vs $V_{DD}$ (LS (low-speed main) mode)



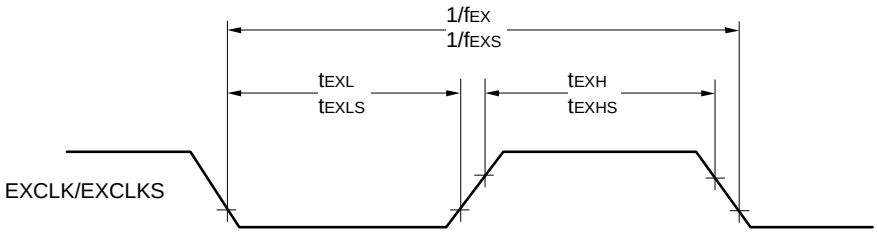

$T_{CY}$ vs $V_{DD}$ (LV (low-voltage main) mode)



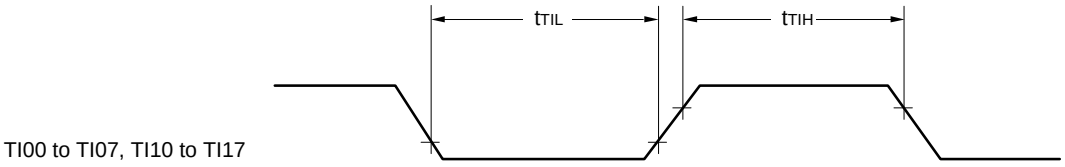
AC Timing Test Points

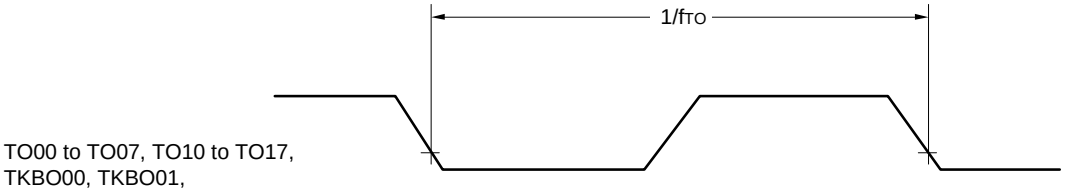



External System Clock Timing

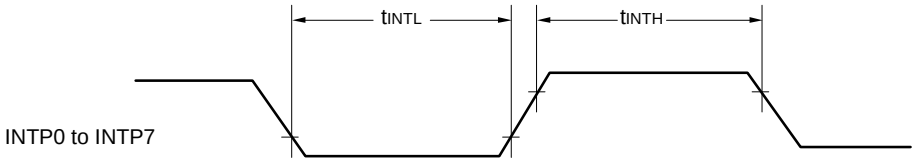



TI/TO Timing

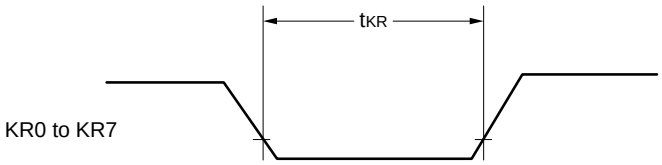


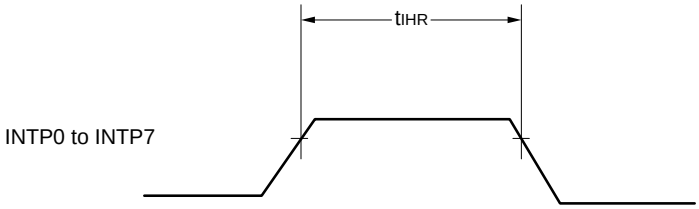

Interrupt Request Input Timing



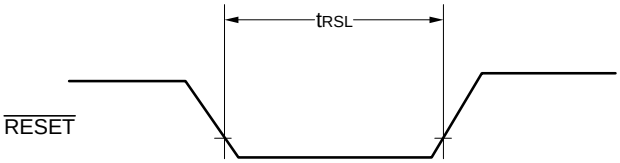
Key Interrupt Input Timing




Timer KB2 Input Timing

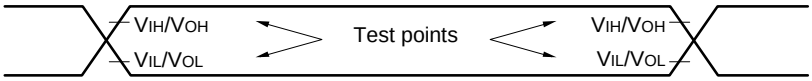



$\overline{\text{RESET}}$ Input Timing



## 2.5 Peripheral Functions Characteristics

AC Timing Test Points




### 2.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 1 | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 4.0 | | 1.3 | | 0.6 | Mbps |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | | 1.3 | | 0.6 | Mbps |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | — | | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | — | | | 1.3 | | 0.6 | Mbps |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | — | | — | | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | — | | — | | | 0.6 | Mbps |

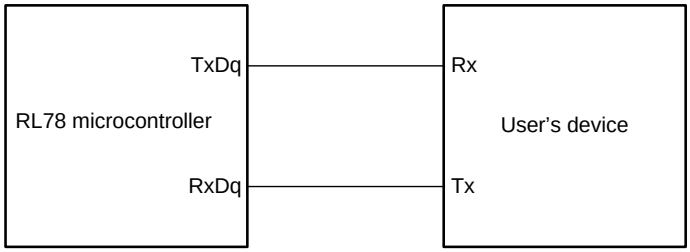
**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**Note 2.** The following conditions are required for low voltage interface.
2.4 V ≤ $V_{DD}$ < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ $V_{DD}$ < 2.4 V: MAX. 1.3 Mbps
1.6 V ≤ $V_{DD}$ < 1.8 V: MAX. 0.6 Mbps

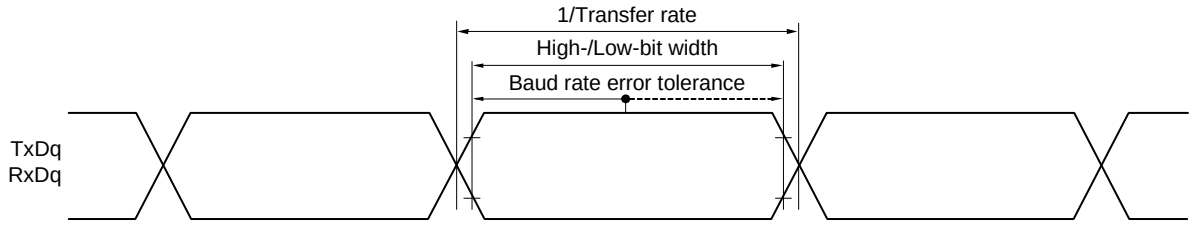
**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 3.6 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 3.6 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 3.6 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ $V_{DD}$ ≤ 3.6 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remark 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 3)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (2) During communication at same potential (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq f_{CLK}/2$ 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 167 | | 250 | | 500 | | ns |
| SCKp high-/low-level width | $t_{KL1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $t_{KCY1}/2$ - 10 | | $t_{KCY1}/2$ - 50 | | $t_{KCY1}/2$ - 50 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 33 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 20 pF Note 4 | | 10 | | 10 | | 10 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 2)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

### (3) During communication at same potential (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq f_{CLK}/4$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 167 | | 500 | | 1000 | | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | 250 | | 500 | | 1000 | | ns |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | — | | 500 | | 1000 | | ns |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | — | | — | | 1000 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | $t_{KCY1}$/2 - 18 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | $t_{KCY1}$/2 - 38 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | $t_{KCY1}$/2 - 100 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 44 | | 110 | | 110 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 75 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | 110 | | 110 | | ns |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | 220 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | 19 | | 19 | | ns |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 30 pF Note 4 | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 25 | | 50 | | 50 | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 25 | | 50 | | 50 | ns |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | 50 | | 50 | ns |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | 50 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0 to 3)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (4) During communication at same potential (Simplified SPI (CSI) mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 2.7 V ≤ $V_{DD}$ < 3.6 V | $f_{MCK}$ > 16 MHz | 8/$f_{MCK}$ | | — | | — | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.6 V | | 6/$f_{MCK}$ and 500 | | 6/$f_{MCK}$ and 500 | | 6/$f_{MCK}$ and 500 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.6 V | | — | | 6/$f_{MCK}$ and 750 | | 6/$f_{MCK}$ and 750 | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 3.6 V | | — | | — | | 6/$f_{MCK}$ and 1500 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | $t_{KCY2}$/2 - 8 | | $t_{KCY2}$/2 - 8 | | $t_{KCY2}$/2 - 8 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | $t_{KCY2}$/2 - 18 | | $t_{KCY2}$/2 - 18 | | ns |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | $t_{KCY1}$/2 - 66 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.6 V | | — | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 3.6 V | | — | | — | | 1/$f_{MCK}$ + 40 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | 2.4 V ≤ $V_{DD}$ < 3.6 V | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.6 V | | — | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 3.6 V | | — | | — | | 1/$f_{MCK}$ + 250 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 2/$f_{MCK}$ + 44 | | 2/$f_{MCK}$ + 110 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 2.4 V ≤ $V_{DD}$ < 3.6 V | | 2/$f_{MCK}$ + 75 | | 2/$f_{MCK}$ + 110 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 1.8 V ≤ $V_{DD}$ < 3.6 V | | — | | 2/$f_{MCK}$ + 110 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 1.6 V ≤ $V_{DD}$ < 3.6 V | | — | | — | | 2/$f_{MCK}$ + 220 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SOp output lines.

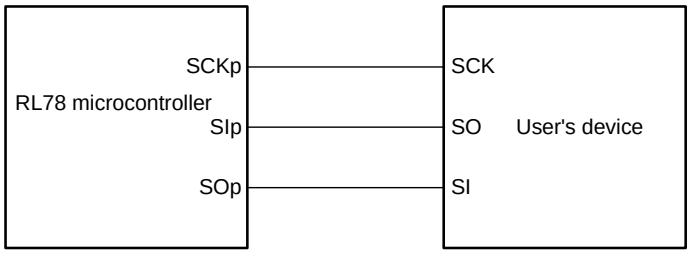
**Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0 to 3)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

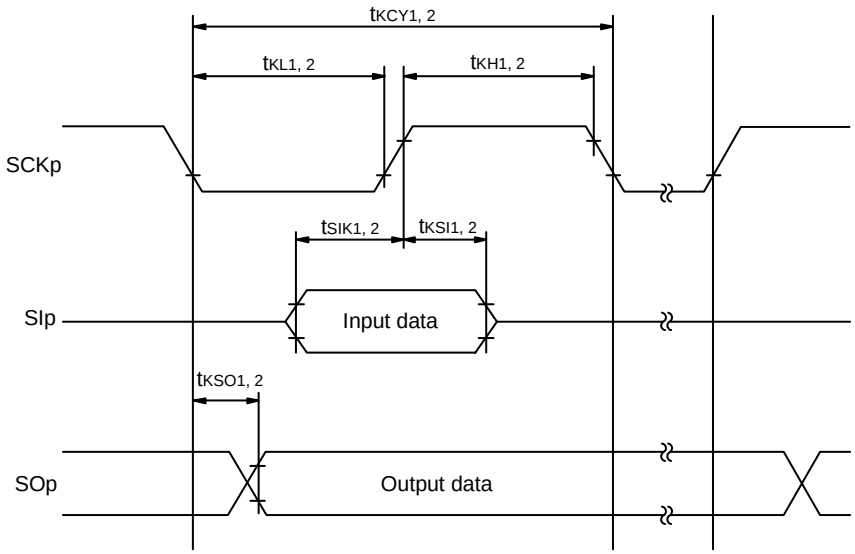
**Simplified SPI (CSI) mode connection diagram (during communication at same potential)**



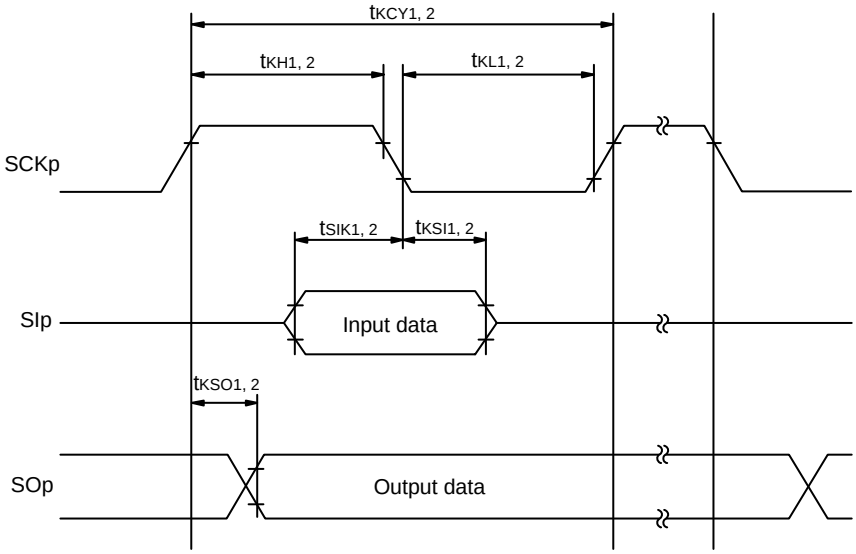

**Remark 1.** p: CSI number (p = 00, 10, 20, 30)

**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 10, 20, 30)
**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

### (5) During communication at same potential (simplified I²C mode)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

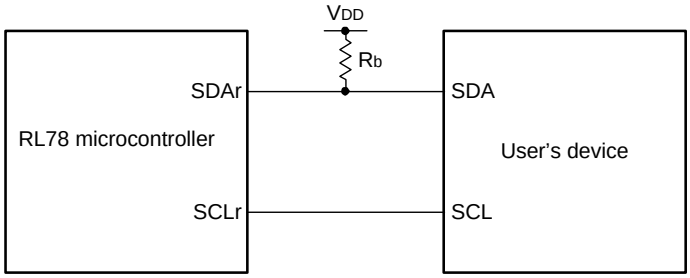
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 400 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 400 Note 1 | | 400 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | 300 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | — | | — | | 250 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | — | | 1850 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | — | | 1850 | | ns |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 85 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1/$f_{MCK}$ + 230 Note 2 | | 1/$f_{MCK}$ + 230 Note 2 | | 1/$f_{MCK}$ + 230 Note 2 | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | — | | 1/$f_{MCK}$ + 290 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD: DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | — | | 0 | 405 | ns |

**Note 1.** The value must be equal to or less than $f_{MCK}$/4.

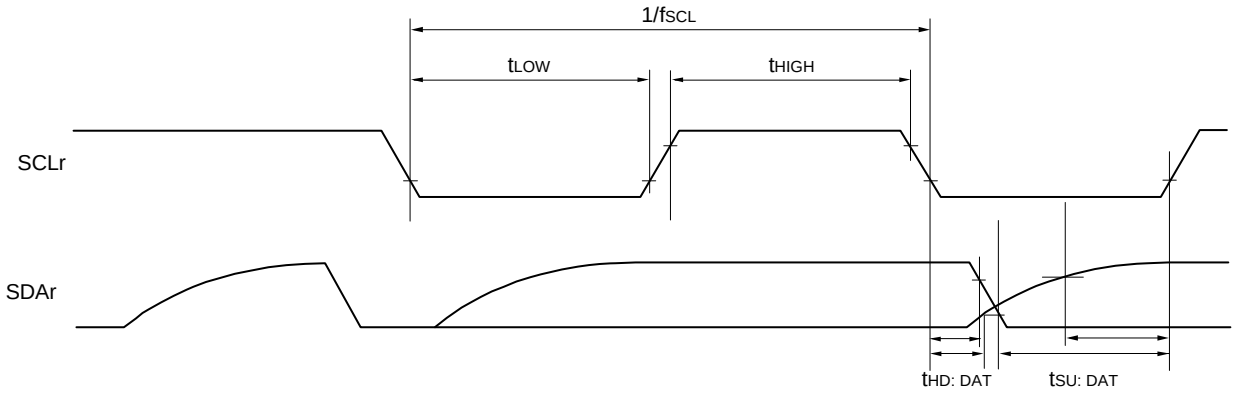
**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

**Simplified I²C mode connection diagram (during communication at same potential)**




**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

**Remark 2.** r: IIC number (r = 00, 10, 20, 30), g: PIM number (g = 0 to 3),
h: POM number (h = 0 to 3)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

### (6) Communication at different potential (1.8 V, 2.5 V) (UART mode)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Notes 1, 2 | | reception | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 4.0 | | 1.3 | | 0.6 | Mbps |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/6 Notes 1, 2, 3 | | $f_{MCK}$/6 Notes 1, 2, 3 | | $f_{MCK}$/6 Notes 1, 2, 3 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 4.0 | | 1.3 | | 0.6 | Mbps |

**Note 1.** Transfer rate in the SNOOZE mode is 4,800 bps only.

**Note 2.** Use it with $V_{DD} \geq V_b$.

**Note 3.** The following conditions are required for low voltage interface.
2.4 V ≤ $V_{DD}$ < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ $V_{DD}$ < 2.4 V: MAX. 1.3 Mbps
1.6 V ≤ $V_{DD}$ < 1.8 V: MAX. 0.6 Mbps

**Note 4.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 3.6 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 3.6 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 3.6 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ $V_{DD}$ ≤ 3.6 V)

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $V_b$[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 3)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (6) Communication at different potential (1.8 V, 2.5V) (UART mode)

**($T_A$ = -40 to +85°C, 1.8 ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 2 | | transmission | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | Note 1 | | Note 1 | | Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 2 | | 1.2 Note 2 | | 1.2 Note 2 | Mbps |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | Notes 3, 4 | | Notes 3, 4 | | Notes 3, 4 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 5 | | 0.43 Note 5 | | 0.43 Note 5 | Mbps |

**Note 1.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ $V_{DD}$ < 3.6 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 2.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

**Note 3.** Use it with $V_{DD} \geq V_b$.

**Note 4.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ $V_{DD}$ < 3.3 V and 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

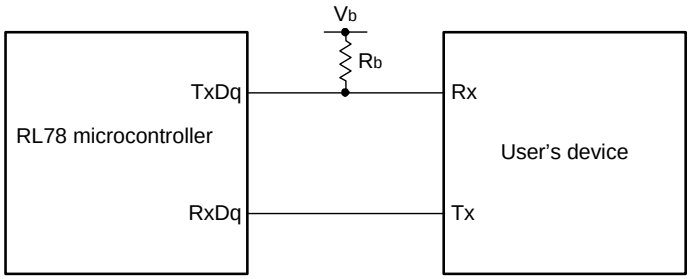
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

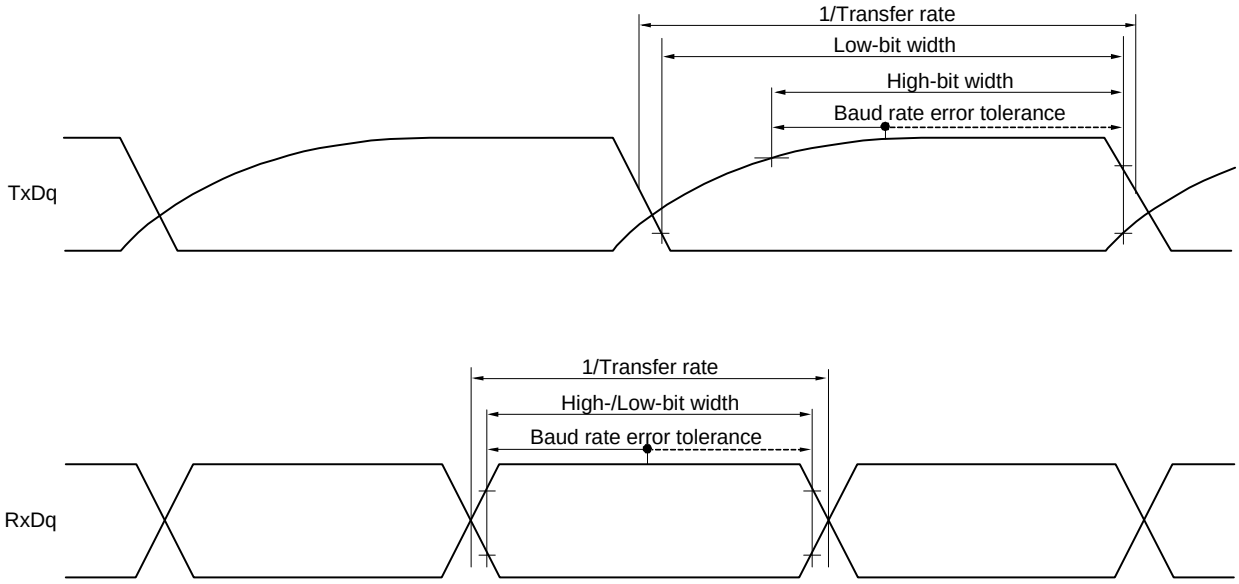
**Note 5.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**UART mode connection diagram (during communication at different potential)**




**UART mode bit width (during communication at different potential) (reference)**




**Remark 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance, $C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 3)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (7) Communication at different potential (2.5 V) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq f_{CLK}/2$ | 2.7V ≤ $V_{DD}$ < 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 300 | | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 2.7 V ≤ $V_{DD}$ < 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 120 | | $t_{KCY1}$/2 - 120 | | $t_{KCY1}$/2 - 120 | | ns |
| SCKp low-level width | $t_{KL1}$ | 2.7 V ≤ $V_{DD}$ < 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 10 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ < 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 121 | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 2.7 V ≤ $V_{DD}$ < 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 2.7 V ≤ $V_{DD}$ < 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 130 | | 130 | | 130 | ns |
| SIp setup time (to SCKp↓) Note 2 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ < 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 33 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) Note 2 | $t_{KSI1}$ | 2.7 V ≤ $V_{DD}$ < 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↑ to SOp output Note 2 | $t_{KSO1}$ | 2.7 V ≤ $V_{DD}$ < 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 10 | | 10 | | 10 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0),
n: Channel number (n = 0), g: PIM and POM number (g = 2)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

### (8) Communication at different potential (1.8 V, 2.5 V) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ $f_{CLK}$/4 | 2.7V ≤ $V_{DD}$ < 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 500 Note | | 1150 | | 1150 | | ns |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 1.8 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 1150 Note | | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 170 | | $t_{KCY1}$/2 - 170 | | $t_{KCY1}$/2 - 170 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 458 | | $t_{KCY1}$/2 - 458 | | $t_{KCY1}$/2 - 458 | | ns |
| SCKp low-level width | $t_{KL1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 18 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |

**Note** Use it with $V_{DD}$ ≥ $V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

### (8) Communication at different potential (1.8 V, 2.5 V) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 177 | | 479 | | 479 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 479 | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 195 | | 195 | | 195 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 483 | | 483 | | 483 | ns |
| SIp setup time (to SCKp↓) Note 2 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 44 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 110 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) Note 2 | $t_{KSI1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↑ to SOp output Note 2 | $t_{KSO1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 25 | | 25 | | 25 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 25 | | 25 | | 25 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

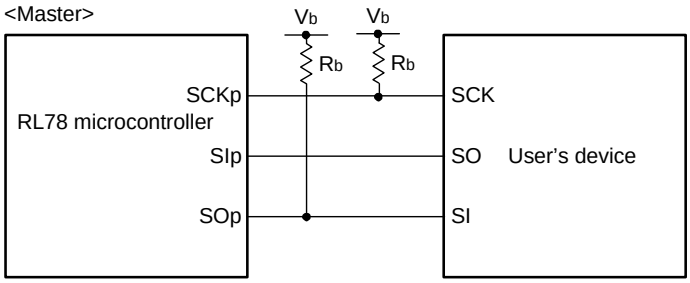
**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** Use it with $V_{DD}$ ≥ $V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Simplified SPI (CSI) mode connection diagram (during communication at different potential)**

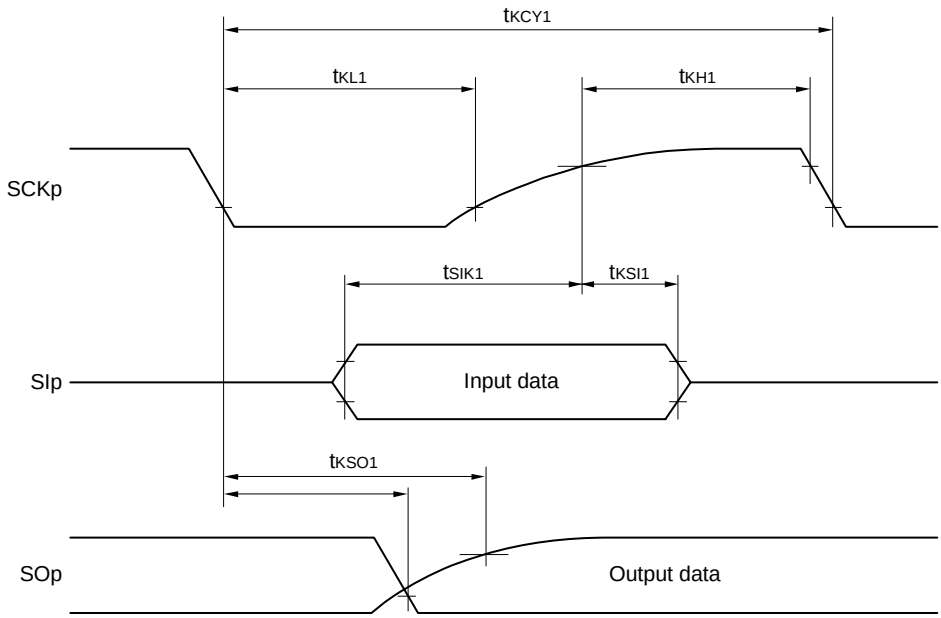



**Remark 1.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

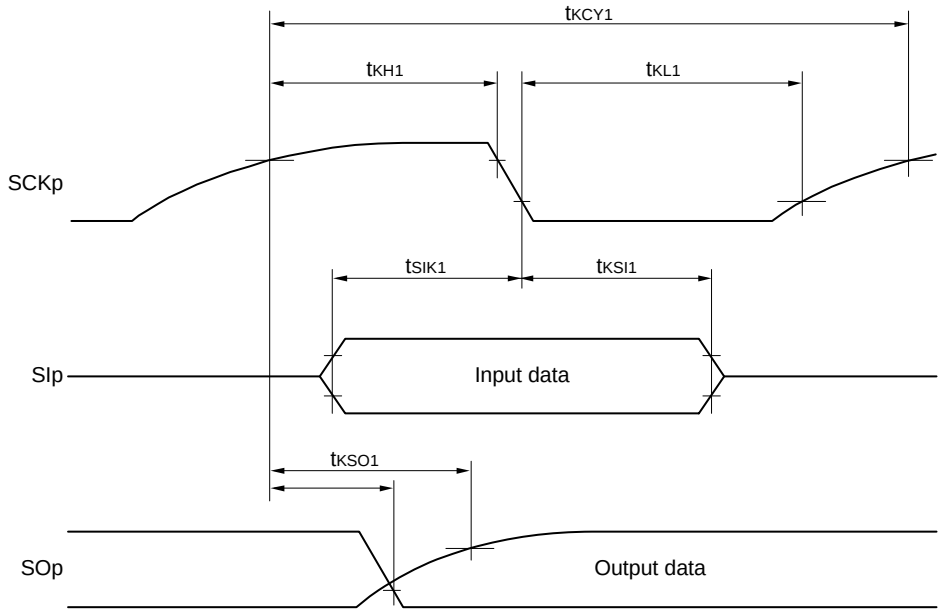
**Remark 2.** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0 to 3)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0 to 3)

### (9) Communication at different potential (1.8 V, 2.5 V) (Simplified SPI (CSI) mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | — | | — | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | — | | — | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | — | | — | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | — | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | — | | — | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | — | | — | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | — | | — | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | — | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 - 18 | | $t_{KCY2}$/2 - 50 | | $t_{KCY2}$/2 - 50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | $t_{KCY2}$/2 - 50 | | $t_{KCY2}$/2 - 50 | | $t_{KCY2}$/2 - 50 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 5 | $t_{KSO2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

**Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Note 2.** Use it with $V_{DD}$ ≥ $V_b$.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

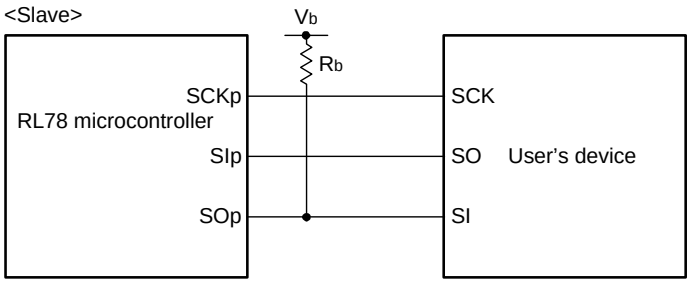
**Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Simplified SPI (CSI) mode connection diagram (during communication at different potential)**

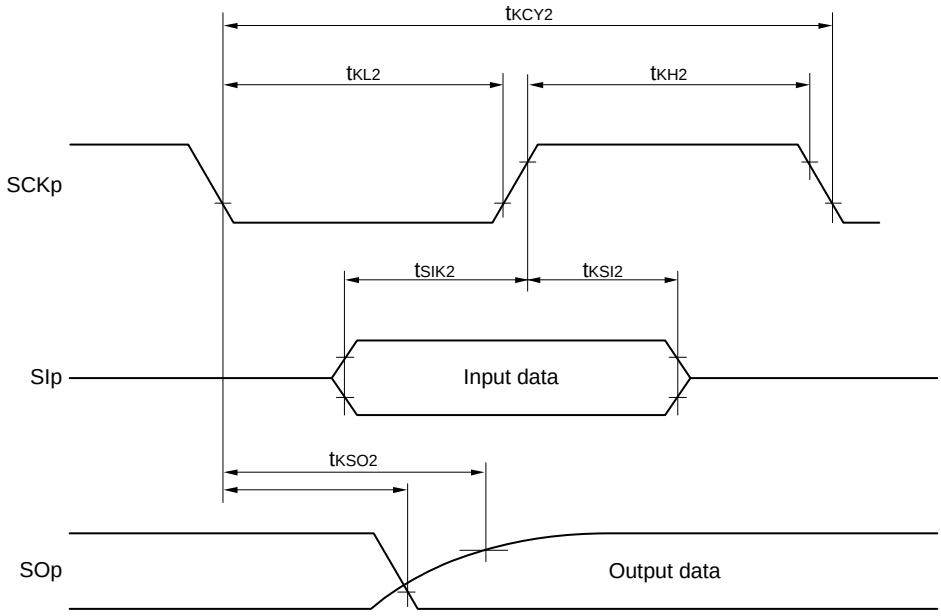



**Remark 1.** $R_b$[Ω]: Communication line (SOp) pull-up resistance, $C_b$[F]: Communication line (SOp) load capacitance, $V_b$[V]: Communication line voltage

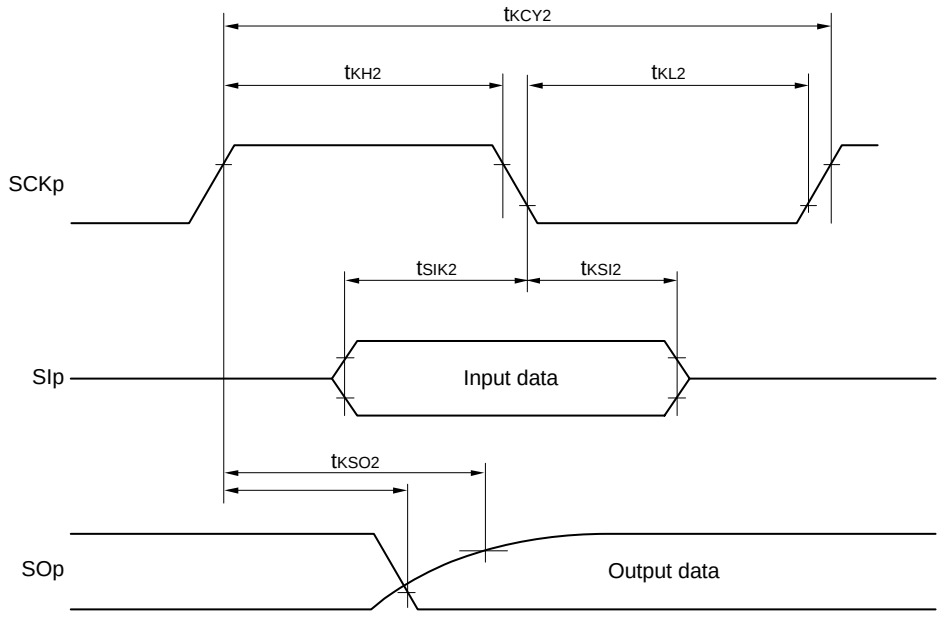
**Remark 2.** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0 to 3)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10, 12))

**Simplified SPI (CSI) mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**Simplified SPI (CSI) mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0 to 3)

### (10) Communication at different potential (1.8 V, 2.5 V) (simplified $I^2C$ mode)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 400 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| Hold time when SCLr = "L" | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ <2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| Hold time when SCLr = "H" | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 200 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 600 | | 610 | | 610 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 610 | | 610 | | 610 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 135 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |

**Note 1.** The value must be equal to or less than $f_{MCK}$/4.

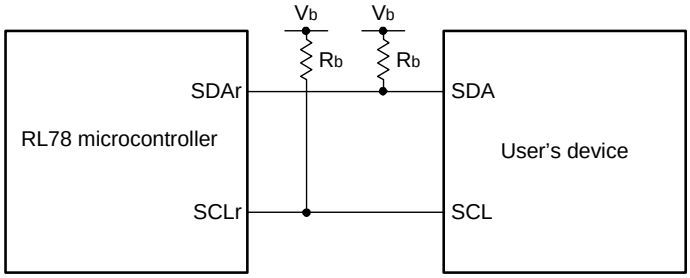
**Note 2.** Use it with $V_{DD}$ ≥ $V_b$.

**Note 3.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

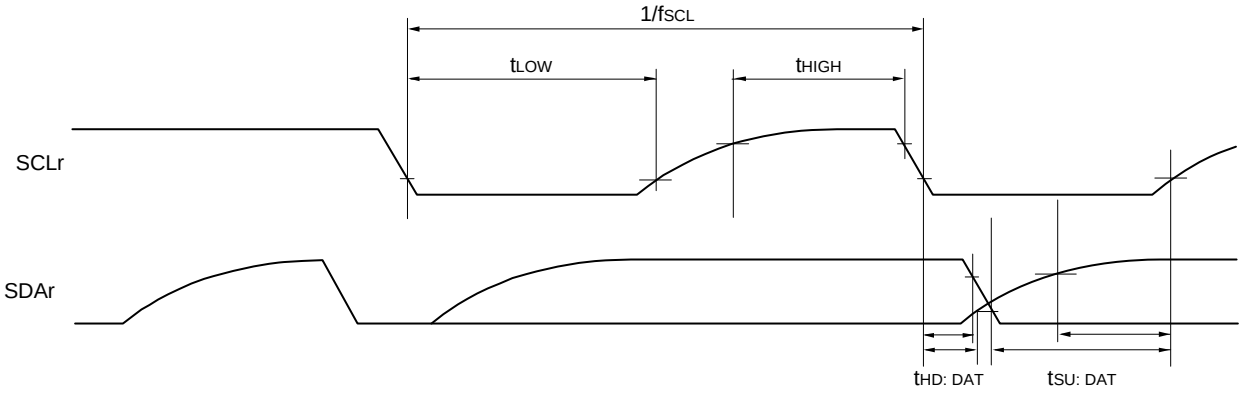
**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** r: IIC number (r = 00, 10, 20, 30), g: PIM, POM number (g = 0 to 3)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10, 12)

## 2.5.2 Serial interface IICA

### (1) $I^2C$ standard mode

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Standard mode: $f_{CLK}$ ≥ 1 MHz | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | — | — | 0 | 100 | 0 | 100 | kHz |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | — | — | — | — | 0 | 100 | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | 4.7 | | µs |
| Hold time Note 1 | $t_{HD: STA}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | 4.0 | | µs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | 4.7 | | µs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | 4.0 | | µs |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 250 | | 250 | | 250 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | 250 | | 250 | | ns |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | 250 | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | — | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | — | — | — | 0 | 3.45 | µs |
| Setup time of stop condition | $t_{SU: STO}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | 4.0 | | µs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | 4.7 | | µs |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: $C_b$ = 400 pF, $R_b$ = 2.7 kΩ

### (2) $I^2C$ fast mode

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| Hold time Note 1 | $t_{HD: STA}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.3 | | 1.3 | | 1.3 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.3 | | 1.3 | | 1.3 | | μs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 100 | | 100 | | 100 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | 100 | | 100 | | 100 | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | μs |
| Setup time of stop condition | $t_{SU: STO}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.3 | | 1.3 | | 1.3 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.3 | | 1.3 | | 1.3 | | μs |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

### (3) $I^2C$ fast mode plus

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

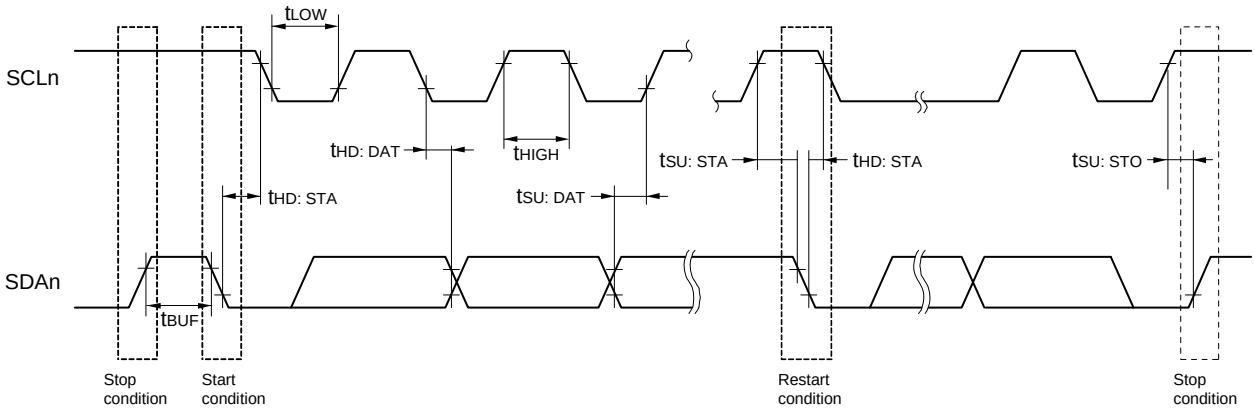
| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode plus: $f_{CLK}$ ≥ 10 MHz | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 0 | 1000 | — | | — | | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.26 | | — | | — | | μs |
| Hold time Note 1 | $t_{HD: STA}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.26 | | — | | — | | μs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.5 | | — | | — | | μs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.26 | | — | | — | | μs |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 50 | | — | | — | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0 | 0.45 | — | | — | | μs |
| Setup time of stop condition | $t_{SU: STO}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.26 | | — | | — | | μs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.5 | | — | | — | | μs |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: $C_b$ = 120 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**



## 2.5.3 USB

### (1) Electrical specifications

**($T_A$ = -40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, HS (High-speed main) mode only)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $U_{REGC}$ | $U_{REGC}$ output voltage characteristic | $U_{REGC}$ | $UV_{BUS}$ = 4.0 to 5.5 V, PXXCON = VDDUSBE = 1 | 3.0 | 3.3 | 3.6 | V |
| $UV_{BUS}$ | $UV_{BUS}$ input voltage characteristic | $UV_{BUS}$ | Function | 4.35 (4.02 Note) | 5.00 | 5.25 | V |

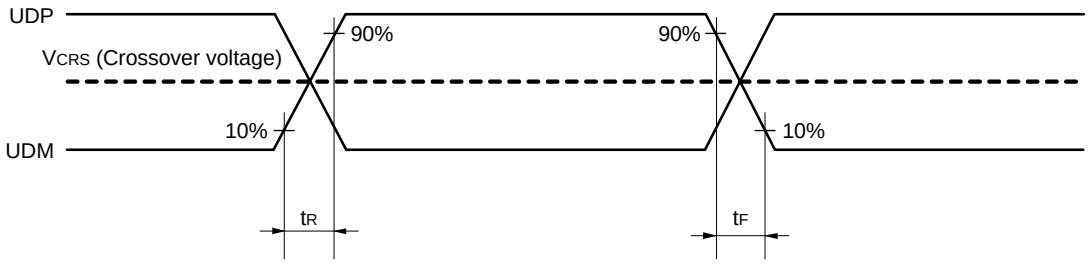
**Note** Value of instantaneous voltage

**($T_A$ = -40 to +85°C, 4.35 V ≤ $UV_{BUS}$ ≤ 5.25 V, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, HS (High-speed main) mode only)**

| Parameter | | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input characteristic (FS/LS receiver) | Input voltage | | $V_{IH}$ | | 2.0 | | | V |
| | | | $V_{IL}$ | | | | 0.8 | V |
| | Difference input sensitivity | | $V_{DI}$ | \| UDP voltage - UDM voltage \| | 0.2 | | | V |
| | Difference common mode range | | $V_{CM}$ | | 0.8 | | 2.5 | V |
| Output characteristic (FS driver) | Output voltage | | $V_{OH}$ | $I_{OH}$ = -200 µA | 2.8 | | 3.6 | V |
| | | | $V_{OL}$ | $I_{OL}$ = 2 mA | 0 | | 0.3 | V |
| | Transition time | Rising | $t_{FR}$ | Rising: From 10% to 90% of amplitude, Falling: From 90% to 10% of amplitude, CL = 50 pF | 4 | | 20 | ns |
| | | Falling | $t_{FF}$ | | 4 | | 20 | ns |
| | Matching (TFR/TFF) | | $V_{FRFM}$ | | 90 | | 111.1 | % |
| | Crossover voltage | | $V_{FCRS}$ | | 1.3 | | 2.0 | V |
| | Output Impedance | | $Z_{DRV}$ | | 28 | | 44 | Ω |
| Output characteristic (LS driver) | Output voltage | | $V_{OH}$ | | 2.8 | | 3.6 | V |
| | | | $V_{OL}$ | | 0 | | 0.3 | V |
| | Transition time | Rising | $t_{LR}$ | Rising: From 10% to 90% of amplitude, Falling: From 90% to 10% of amplitude, CL = 250 pF to 750 pF<br><br>The UDP and UDM pins are individually pulled down via 15 kΩ | 75 | | 300 | ns |
| | | Falling | $t_{LF}$ | | 75 | | 300 | ns |
| | Matching (TFR/TFF) Note | | $V_{LTFM}$ | | 80 | | 125 | % |
| | Crossover voltage Note | | $V_{LCRS}$ | | 1.3 | | 2.0 | V |
| Pull-up, Pull-down | Pull-down resistor | | $R_{PD}$ | | 14.25 | | 24.80 | kΩ |
| | Pull-up resistor | Idle | $R_{PUI}$ | | 0.9 | | 1.575 | kΩ |
| | | Reception | $R_{PUA}$ | | 1.425 | | 3.09 | kΩ |
| $UV_{BUS}$ | $UV_{BUS}$ pull-down resistor | | $R_{VBUS}$ | $UV_{BUS}$ voltage = 5.5 V | | 1000 | | kΩ |
| | $UV_{BUS}$ input voltage | | $V_{IH}$ | | 3.20 | | | V |
| | | | $V_{IL}$ | | | | 0.8 | V |

**Note** Excludes the first signal transition from the idle state.

**Timing of UDP and UDM**




**(2) BC standard**

**($T_A$ = -40 to +85°C, 4.35 V ≤ $UV_{BUS}$ ≤ 5.25 V, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, HS (High-speed main) mode only)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| USB standard BC1.2 | UDP sink current | $I_{DP\_SINK}$ | | 25 | 100 | 175 | μA |
| | UDM sink current | $I_{DM\_SINK}$ | | 25 | 100 | 175 | μA |
| | DCD source current | $I_{DP\_SRC}$ | | 7 | 10 | 13 | μA |
| | Data detection voltage | $V_{DAT\_REF}$ | | 0.25 | 0.325 | 0.4 | V |
| | UDP source voltage | $V_{DP\_SRC}$ | Output current 250 μA | 0.5 | 0.6 | 0.7 | V |
| | UDM source voltage | $V_{DM\_SRC}$ | Output current 250 μA | 0.5 | 0.6 | 0.7 | V |

### (3) BC option standard

**($T_A$ = -40 to +85°C, 4.35 V ≤ $UV_{BUS}$ ≤ 5.25 V, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, HS (High-speed main) mode only)**

| Parameter | | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| UDP/UDM input reference voltage ($UV_{BUS}$ divider ratio) (Function) | VDSELi [3: 0] (i = 0, 1) | 0000 | $V_{DDET0}$ | | 27 | 32 | 37 | %UVBUS |
| | | 0001 | $V_{DDET1}$ | | 29 | 34 | 39 | %UVBUS |
| | | 0010 | $V_{DDET2}$ | | 32 | 37 | 42 | %UVBUS |
| | | 0011 | $V_{DDET3}$ | | 35 | 40 | 45 | %UVBUS |
| | | 0100 | $V_{DDET4}$ | | 38 | 43 | 48 | %UVBUS |
| | | 0101 | $V_{DDET5}$ | | 41 | 46 | 51 | %UVBUS |
| | | 0110 | $V_{DDET6}$ | | 44 | 49 | 54 | %UVBUS |
| | | 0111 | $V_{DDET7}$ | | 47 | 52 | 57 | %UVBUS |
| | | 1000 | $V_{DDET8}$ | | 51 | 56 | 61 | %UVBUS |
| | | 1001 | $V_{DDET9}$ | | 55 | 60 | 65 | %UVBUS |
| | | 1010 | $V_{DDET10}$ | | 59 | 64 | 69 | %UVBUS |
| | | 1011 | $V_{DDET11}$ | | 63 | 68 | 73 | %UVBUS |
| | | 1100 | $V_{DDET12}$ | | 67 | 72 | 73 | %UVBUS |
| | | 1101 | $V_{DDET13}$ | | 71 | 76 | 81 | %UVBUS |
| | | 1110 | $V_{DDET14}$ | | 75 | 80 | 85 | %UVBUS |
| | | 1111 | $V_{DDET15}$ | | 79 | 84 | 89 | %UVBUS |

## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

**Classification of A/D converter characteristics**

| Reference Voltage / Input Channel | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (-) = $AV_{REFM}$ | Reference voltage (+) = $AV_{DD}$<br>Reference voltage (-) = $AV_{SS}$ | Reference voltage (+) = Internal reference voltage<br>Reference voltage (-) = $AV_{SS}$ |
|---|---|---|---|
| High-accuracy channel; ANI0 to ANI6 (input buffer power supply: $AV_{DD}$) | Refer to **2.6.1 (1)**.<br>Refer to **2.6.1 (2)**. | Refer to **2.6.1 (3)**. | Refer to **2.6.1 (6)**. |
| Standard channel; ANI16 to ANI21 (input buffer power supply: $V_{DD}$) | Refer to **2.6.1 (4)**. | Refer to **2.6.1 (5)**. | |
| Internal reference voltage, Temperature sensor output voltage | Refer to **2.6.1 (4)**. | Refer to **2.6.1 (5)**. | — |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI6**

**($T_A$ = -40 to +85°C, 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, reference voltage (+) = $AV_{REFP}$, reference voltage (-) = $AV_{REFM}$ = 0 V, HALT mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | | 12 | bit |
| Overall error Notes 1, 2, 3 | AINL | 12-bit resolution | | ±1.7 | ±3.3 | LSB |
| Conversion time | $t_{CONV}$ | ADTYP = 0, 12-bit resolution | 3.375 | | | μs |
| Zero-scale error Notes 1, 2, 3 | $E_{ZS}$ | 12-bit resolution | | ±1.3 | ±3.2 | LSB |
| Full-scale error Notes 1, 2, 3 | $E_{FS}$ | 12-bit resolution | | ±0.7 | ±2.9 | LSB |
| Integral linearity error Notes 1, 2, 3 | ILE | 12-bit resolution | | ±1.0 | ±1.4 | LSB |
| Differential linearity error Notes 1, 2, 3 | DLE | 12-bit resolution | | ±0.9 | ±1.2 | LSB |
| Analog input voltage | $V_{AIN}$ | | 0 | | $AV_{REFP}$ | V |

**Note 1.** TYP. Value is the average value at $AV_{DD}$ = $AV_{REFP}$ = 3 V and $T_A$ = 25°C. MAX. value is the average value ±3σ at normalized distribution.

**Note 2.** These values are the results of characteristic evaluation and are not checked for shipment.

**Note 3.** Excludes quantization error (±1/2 LSB).

**Caution 1. Route the wiring so that noise will not be superimposed on each power line and ground line, and insert a capacitor to suppress noise.**
**In addition, separate the reference voltage line of $AV_{REFP}$ from the other power lines to keep it free from the influences of noise.**

**Caution 2. During A/D conversion, keep a pulse, such as a digital signal, that abruptly changes its level from being input to or output from the pins adjacent to the converter pins and P150 to P156.**

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), conversion target: ANI2 to ANI6**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| | | | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 10 Note 1 | |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 Note 2 | | | |
| Overall error Note 3 | AINL | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±6.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.5 | |
| Conversion time | $t_{CONV}$ | ADTYP = 0, 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 3.375 | | | µs |
| | | ADTYP = 0, 10-bit resolution Note 1 | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 6.75 | | | |
| | | ADTYP = 0, 8-bit resolution Note 2 | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 13.5 | | | |
| | | ADTYP = 1, 8-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 2.5625 | | | |
| | | | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 5.125 | | | |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 10.25 | | | |
| Zero-scale error Note 3 | $E_{ZS}$ | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±4.5 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±4.5 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | |
| Full-scale error Note 3 | $E_{FS}$ | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±4.5 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±4.5 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | |
| Integral linearity error Note 3 | ILE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.5 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.0 | |
| Differential linearity error Note 3 | DLE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.5 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.5 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.0 | |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $AV_{REFP}$ | V |

**Note 1.** Cannot be used for lower 2 bit of ADCR register

**Note 2.** Cannot be used for lower 4 bit of ADCR register

**Note 3.** Excludes quantization error (±1/2 LSB).

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

**(3) When reference voltage (+) = $AV_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = $AV_{SS}$ (ADREFM = 0), conversion target: ANI0 to ANI6**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{DD}$, Reference voltage (-) = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| | | | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 10 Note 1 | |
| | | | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | 8 Note 2 | | | |
| Overall error Note 3 | AINL | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±7.5 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.5 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | |
| Conversion time | $t_{CONV}$ | ADTYP = 0, 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | 3.375 | | | µs |
| | | ADTYP = 0, 10-bit resolution Note 1 | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | 6.75 | | | |
| | | ADTYP = 0, 8-bit resolution Note 2 | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | 13.5 | | | |
| | | ADTYP = 1, 8-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | 2.5625 | | | |
| | | | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | 5.125 | | | |
| | | | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | 10.25 | | | |
| Zero-scale error Note 3 | $E_{ZS}$ | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±6.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.5 | |
| Full-scale error Note 3 | $E_{FS}$ | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±6.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.5 | |
| Integral linearity error Note 3 | ILE | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.5 | |
| Differential linearity error Note 3 | DLE | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.5 | |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI6 | | 0 | | $AV_{DD}$ | V |

**Note 1.** Cannot be used for lower 2 bit of ADCR register

**Note 2.** Cannot be used for lower 4 bit of ADCR register

**Note 3.** Excludes quantization error (±1/2 LSB).

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

**(4) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), conversion target: ANI16 to ANI21, internal reference voltage, temperature sensor output voltage**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| | | | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 10 Note 1 | |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 Note 2 | | | |
| Overall error Note 3 | AINL | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±7.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.5 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | |
| Conversion time | tCONV | ADTYP = 0, 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 4.125 | | | µs |
| | | ADTYP = 0, 10-bit resolution Note 1 | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 9.5 | | | |
| | | ADTYP = 0, 8-bit resolution Note 2 | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 57.5 | | | |
| | | ADTYP = 1, 8-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 3.3125 | | | |
| | | | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 7.875 | | | |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 54.25 | | | |
| Zero-scale error Note 3 | EZS | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.5 | |
| Full-scale error Note 3 | EFS | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.5 | |
| Integral linearity error Note 3 | ILE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.5 | |
| Differential linearity error Note 3 | DLE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.5 | |
| Analog input voltage | VAIN | | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage (2.4 V ≤ $V_{DD}$ ≤ 3.6 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 4 | | | |
| | | Temperature sensor output voltage (2.4 V ≤ $V_{DD}$ ≤ 3.6 V, HS (high-speed main) mode) | | $V_{TMP25}$ Note 4 | | | |

**Note 1.** Cannot be used for lower 2 bits of ADCR register

**Note 2.** Cannot be used for lower 4 bits of ADCR register

**Note 3.** Excludes quantization error (±1/2 LSB).

**Note 4.** Refer to **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

**(5) When reference voltage (+) = $AV_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = $AV_{SS}$ (ADREFM = 0), conversion target: ANI16 to ANI21, internal reference voltage, temperature sensor output voltage**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{DD}$, Reference voltage (-) = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| | | | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 10 Note 1 | |
| | | | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | 8 Note 2 | | | |
| Overall error Note 3 | AINL | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±8.5 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±6.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.5 | |
| Conversion time | $t_{CONV}$ | ADTYP = 0, 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | 4.125 | | | µs |
| | | ADTYP = 0, 10-bit resolution Note 1 | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | 9.5 | | | |
| | | ADTYP = 0, 8-bit resolution Note 2 | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | 57.5 | | | |
| | | ADTYP = 1, 8-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | 3.3125 | | | |
| | | | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | 7.875 | | | |
| | | | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | 54.25 | | | |
| Zero-scale error Note 3 | $E_{ZS}$ | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±8.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.5 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | |
| Full-scale error Note 3 | $E_{FS}$ | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±8.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.5 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | |
| Integral linearity error Note 3 | ILE | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.5 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.5 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.5 | |
| Differential linearity error Note 3 | DLE | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.5 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.5 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $AV_{DD}$ | V |
| | | Internal reference voltage (2.4 V ≤ $V_{DD}$ ≤ 3.6 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 4 | | | |
| | | Temperature sensor output voltage (2.4 V ≤ $V_{DD}$ ≤ 3.6 V, HS (high-speed main) mode) | | $V_{TMP25}$ Note 4 | | | |

**Note 1.** Cannot be used for lower 2 bits of ADCR register

**Note 2.** Cannot be used for lower 4 bits of ADCR register

**Note 3.** Excludes quantization error (±1/2 LSB).

**Note 4.** Refer to **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

**(6) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVSS (ADREFM = 0), conversion target: ANI0 to ANI6, ANI16 to ANI21**

**($T_A$ = -40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, 1.6 V ≤ $V_{DD}$, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = internal reference voltage, Reference voltage (-) = $AV_{SS}$ = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | bit |
| Conversion time | tCONV | 8-bit resolution | 16 | | | µs |
| Zero-scale error Note | EZS | 8-bit resolution | | | ±4.0 | LSB |
| Integral linearity error Note | ILE | 8-bit resolution | | | ±2.0 | LSB |
| Differential linearity error Note | DLE | 8-bit resolution | | | ±2.5 | LSB |
| Reference voltage (+) | $AV_{REF(+)}$ | = Internal reference voltage ($V_{BGR}$) | 1.38 | 1.45 | 1.5 | V |
| Analog input voltage | VAIN | | 0 | | $V_{BGR}$ | V |

**Note** Excludes quantization error (±1/2 LSB).

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

## 2.6.2 Temperature sensor, internal reference voltage output characteristics

**($T_A$ = -40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V (HS (high-speed main) mode))**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | FVTMPS | Temperature sensor output voltage that depends on the temperature | | -3.6 | | mV/°C |
| Operation stabilization wait time | tAMP | | 10 | | | µs |

## 2.6.3 D/A converter characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | | 8 | bit |
| Overall error | AINL | Rload = 4 MΩ | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | | ±2.5 | LSB |
| | | Rload = 8 MΩ | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | | ±2.5 | LSB |
| Settling time | tSET | Cload = 20 pF | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 3 | µs |
| | | | 1.6 V ≤ $V_{DD}$ < 2.7 V | | | 6 | µs |

## 2.6.4 Comparator

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage range | Ivref | | | 0 | | $V_{DD}$ - 1.4 | V |
| | Ivcmp | | | -0.3 | | $V_{DD}$ + 0.3 | V |
| Output delay | td | $V_{DD}$ = 3.0 V<br>Input slew rate > 50 mV/μs | High-speed comparator mode, standard mode | | | 1.2 | μs |
| | | | High-speed comparator mode, window mode | | | 2.0 | μs |
| | | | Low-speed comparator mode, standard mode | | 3 | 5.0 | μs |
| High-electric-potential judgment voltage | VTW+ | High-speed comparator mode, window mode | | | 0.76 $V_{DD}$ | | V |
| Low-electric-potential judgment voltage | VTW- | High-speed comparator mode, window mode | | | 0.24 $V_{DD}$ | | V |
| Operation stabilization wait time | $t_{CMP}$ | | | 100 | | | μs |
| Internal reference voltage Note | $V_{BGR}$ | | | 1.38 | 1.45 | 1.50 | V |

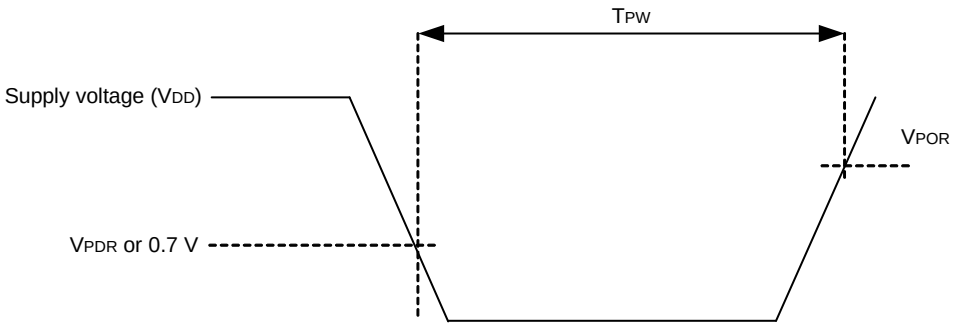
**Note** Not usable in LS (low-speed main) mode, LV (low-voltage main) mode, sub-clock operation, or STOP mode.

## 2.6.5 POR circuit characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Power supply rise time | 1.47 | 1.51 | 1.55 | V |
| | $V_{PDR}$ | Power supply fall time Note | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width | $T_{PW}$ | | 300 | | | μs |

**Note** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 2.6.6 LVD circuit characteristics

**($T_A$ = -40 to +85°C, $V_{PDR} \leq V_{DD} \leq 3.6$ V $\leq V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | Supply voltage level | $V_{LVD2}$ | Power supply rise time | 3.07 | 3.13 | 3.19 | V |
| | | | Power supply fall time | 3.00 | 3.06 | 3.12 | V |
| | | $V_{LVD3}$ | Power supply rise time | 2.96 | 3.02 | 3.08 | V |
| | | | Power supply fall time | 2.90 | 2.96 | 3.02 | V |
| | | $V_{LVD4}$ | Power supply rise time | 2.86 | 2.92 | 2.97 | V |
| | | | Power supply fall time | 2.80 | 2.86 | 2.91 | V |
| | | $V_{LVD5}$ | Power supply rise time | 2.76 | 2.81 | 2.87 | V |
| | | | Power supply fall time | 2.70 | 2.75 | 2.81 | V |
| | | $V_{LVD6}$ | Power supply rise time | 2.66 | 2.71 | 2.76 | V |
| | | | Power supply fall time | 2.60 | 2.65 | 2.70 | V |
| | | $V_{LVD7}$ | Power supply rise time | 2.56 | 2.61 | 2.66 | V |
| | | | Power supply fall time | 2.50 | 2.55 | 2.60 | V |
| | | $V_{LVD8}$ | Power supply rise time | 2.45 | 2.50 | 2.55 | V |
| | | | Power supply fall time | 2.40 | 2.45 | 2.50 | V |
| | | $V_{LVD9}$ | Power supply rise time | 2.05 | 2.09 | 2.13 | V |
| | | | Power supply fall time | 2.00 | 2.04 | 2.08 | V |
| | | $V_{LVD10}$ | Power supply rise time | 1.94 | 1.98 | 2.02 | V |
| | | | Power supply fall time | 1.90 | 1.94 | 1.98 | V |
| | | $V_{LVD11}$ | Power supply rise time | 1.84 | 1.88 | 1.91 | V |
| | | | Power supply fall time | 1.80 | 1.84 | 1.87 | V |
| | | $V_{LVD12}$ | Power supply rise time | 1.74 | 1.77 | 1.81 | V |
| | | | Power supply fall time | 1.70 | 1.73 | 1.77 | V |
| | | $V_{LVD13}$ | Power supply rise time | 1.64 | 1.67 | 1.70 | V |
| | | | Power supply fall time | 1.60 | 1.63 | 1.66 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | μs |
| Detection delay time | | | | | | 300 | μs |

**Caution Set the detection voltage ($V_{LVD}$) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.**

**HS (high-speed main) mode: $V_{DD}$ = 2.7 to 3.6 V at 1 MHz to 24 MHz**
**$V_{DD}$ = 2.4 to 3.6 V at 1 MHz to 16 MHz**
**LS (low-speed main) mode: $V_{DD}$ = 1.8 to 3.6 V at 1 MHz to 8 MHz**
**LV (low-voltage main) mode: $V_{DD}$ = 1.6 to 3.6 V at 1 MHz to 4 MHz**

**LVD Detection Voltage of Interrupt & Reset Mode**

**($T_A$ = -40 to +85°C, $V_{PDR} \leq V_{DD} \leq 3.6$ V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDA0}$ | $V_{POC0}$, $V_{POC1}$, $V_{POC2}$ = 0, 0, 0, falling reset voltage: 1.6 V | | | 1.60 | 1.63 | 1.66 | V |
| | $V_{LVDA1}$ | LVIS0, LVIS1 = 1, 0 | | Rising release reset voltage | 1.74 | 1.77 | 1.81 | V |
| | | | | Falling interrupt voltage | 1.70 | 1.73 | 1.77 | V |
| | $V_{LVDA2}$ | LVIS0, LVIS1 = 0, 1 | | Rising release reset voltage | 1.84 | 1.88 | 1.91 | V |
| | | | | Falling interrupt voltage | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDA3}$ | LVIS0, LVIS1 = 0, 0 | | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDB0}$ | $V_{POC0}$, $V_{POC1}$, $V_{POC2}$ = 0, 0, 1, falling reset voltage: 1.8 V | | | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDB1}$ | LVIS0, LVIS1 = 1, 0 | | Rising release reset voltage | 1.94 | 1.98 | 2.02 | V |
| | | | | Falling interrupt voltage | 1.90 | 1.94 | 1.98 | V |
| | $V_{LVDB2}$ | LVIS0, LVIS1 = 0, 1 | | Rising release reset voltage | 2.05 | 2.09 | 2.13 | V |
| | | | | Falling interrupt voltage | 2.00 | 2.04 | 2.08 | V |
| | $V_{LVDB3}$ | LVIS0, LVIS1 = 0, 0 | | Rising release reset voltage | 3.07 | 3.13 | 3.19 | V |
| | | | | Falling interrupt voltage | 3.00 | 3.06 | 3.12 | V |
| | $V_{LVDC0}$ | $V_{POC0}$, $V_{POC1}$, $V_{POC2}$ = 0, 1, 0, falling reset voltage: 2.4 V | | | 2.40 | 2.45 | 2.50 | V |
| | $V_{LVDC1}$ | LVIS0, LVIS1 = 1, 0 | | Rising release reset voltage | 2.56 | 2.61 | 2.66 | V |
| | | | | Falling interrupt voltage | 2.50 | 2.55 | 2.60 | V |
| | $V_{LVDC2}$ | LVIS0, LVIS1 = 0, 1 | | Rising release reset voltage | 2.66 | 2.71 | 2.76 | V |
| | | | | Falling interrupt voltage | 2.60 | 2.65 | 2.70 | V |
| | $V_{LVDD0}$ | $V_{POC0}$, $V_{POC1}$, $V_{POC2}$ = 0, 1, 1, falling reset voltage: 2.7 V | | | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVDD1}$ | LVIS0, LVIS1 = 1, 0 | | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDD2}$ | LVIS0, LVIS1 = 0, 1 | | Rising release reset voltage | 2.96 | 3.02 | 3.08 | V |
| | | | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V |

## 2.7 Power supply voltage rising slope characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Power supply voltage rising slope | $SV_{DD}$ | | | 54 | V/ms |

**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 2.4 AC Characteristics.**

## 2.8 LCD Characteristics

### 2.8.1 Resistance division method

**(1) Static display mode**

**($T_A$ = -40 to +85°C, $V_{L4}$ (MIN.) ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| LCD drive voltage | $V_{L4}$ | | 2.0 | | $V_{DD}$ | V |

**(2) 1/2 bias method, 1/4 bias method**

**($T_A$ = -40 to +85°C, $V_{L4}$ (MIN.) ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| LCD drive voltage | $V_{L4}$ | | 2.7 | | $V_{DD}$ | V |

**(3) 1/3 bias method**

**($T_A$ = -40 to +85°C, $V_{L4}$ (MIN.) ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| LCD drive voltage | $V_{L4}$ | | 2.5 | | $V_{DD}$ | V |

## 2.8.2 Internal voltage boosting method

**(1) 1/3 bias method**

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| LCD output voltage variation range | $V_{L1}$ | C1 to C4 Note 1 = 0.47 μF Note 2 | VLCD = 04H | 0.90 | 1.00 | 1.08 | V |
| | | | VLCD = 05H | 0.95 | 1.05 | 1.13 | V |
| | | | VLCD = 06H | 1.00 | 1.10 | 1.18 | V |
| | | | VLCD = 07H | 1.05 | 1.15 | 1.23 | V |
| | | | VLCD = 08H | 1.10 | 1.20 | 1.28 | V |
| | | | VLCD = 09H | 1.15 | 1.25 | 1.33 | V |
| | | | VLCD = 0AH | 1.20 | 1.30 | 1.38 | V |
| | | | VLCD = 0BH | 1.25 | 1.35 | 1.43 | V |
| | | | VLCD = 0CH | 1.30 | 1.40 | 1.48 | V |
| | | | VLCD = 0DH | 1.35 | 1.45 | 1.53 | V |
| | | | VLCD = 0EH | 1.40 | 1.50 | 1.58 | V |
| | | | VLCD = 0FH | 1.45 | 1.55 | 1.63 | V |
| | | | VLCD = 10H | 1.50 | 1.60 | 1.68 | V |
| | | | VLCD = 11H | 1.55 | 1.65 | 1.73 | V |
| | | | VLCD = 12H | 1.60 | 1.70 | 1.78 | V |
| | | | VLCD = 13H | 1.65 | 1.75 | 1.83 | V |
| Doubler output voltage | $V_{L2}$ | C1 to C4 Note 1 = 0.47 μF | | 2 $V_{L1}$ - 0.1 | 2 $V_{L1}$ | 2 $V_{L1}$ | V |
| Tripler output voltage | $V_{L3}$ | C1 to C4 Note 1 = 0.47 μF | | 3 $V_{L1}$ - 0.15 | 3 $V_{L1}$ | 3 $V_{L1}$ | V |
| Reference voltage setup time Note 2 | $t_{VWAIT1}$ | | | 5 | | | ms |
| Voltage boost wait time Note 3 | $t_{VWAIT2}$ | C1 to C4 Note 1 = 0.47μF | | 500 | | | ms |

**Note 1.** This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between $V_{L1}$ and GND
C3: A capacitor connected between $V_{L2}$ and GND
C4: A capacitor connected between $V_{L4}$ and GND
C1 = C2 = C3 = C4 = 0.47 μF±30%

**Note 2.** This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

**Note 3.** This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

**(2) 1/4 bias method**

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| LCD output voltage variation range | $V_{L1}$ | C1 to C4 Note 1 = 0.47 μF Note 2 | VLCD = 04H | 0.90 | 1.00 | 1.08 | V |
| | | | VLCD = 05H | 0.95 | 1.05 | 1.13 | V |
| | | | VLCD = 06H | 1.00 | 1.10 | 1.18 | V |
| | | | VLCD = 07H | 1.05 | 1.15 | 1.23 | V |
| | | | VLCD = 08H | 1.10 | 1.20 | 1.28 | V |
| | | | VLCD = 09H | 1.15 | 1.25 | 1.33 | V |
| | | | VLCD = 0AH | 1.20 | 1.30 | 1.38 | V |
| Doubler output voltage | $V_{L2}$ | C1 to C4 Note 1 = 0.47 μF | | 2 $V_{L1}$ - 0.08 | 2 $V_{L1}$ | 2 $V_{L1}$ | V |
| Tripler output voltage | $V_{L3}$ | C1 to C4 Note 1 = 0.47 μF | | 3 $V_{L1}$ - 0.12 | 3 $V_{L1}$ | 3 $V_{L1}$ | V |
| Quadruply output voltage | $V_{L4}$ | C1 to C5 Note 1 = 0.47 μF | | 4 $V_{L1}$ - 0.16 | 4 $V_{L1}$ | 4 $V_{L1}$ | V |
| Reference voltage setup time Note 2 | $t_{VWAIT1}$ | | | 5 | | | ms |
| Voltage boost wait time Note 3 | $t_{VWAIT2}$ | C1 to C5 Note 1 = 0.47μF | | 500 | | | ms |

**Note 1.** This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between $V_{L1}$ and GND
C3: A capacitor connected between $V_{L2}$ and GND
C4: A capacitor connected between $V_{L3}$ and GND
C5: A capacitor connected between $V_{L4}$ and GND
C1 = C2 = C3 = C4 = 0.47 μF±30%

**Note 2.** This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

**Note 3.** This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

## 2.8.3 Capacitor split method

**(1) 1/3 bias method**

**($T_A$ = -40 to +85°C, 2.2 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $V_{L4}$ voltage | $V_{L4}$ | C1 to C4 = 0.47 µF Note 2 | | $V_{DD}$ | | V |
| $V_{L2}$ voltage | $V_{L2}$ | C1 to C4 = 0.47 µF Note 2 | 2/3 $V_{L4}$ - 0.1 | 2/3 $V_{L4}$ | 2/3 $V_{L4}$ + 0.1 | V |
| $V_{L1}$ voltage | $V_{L1}$ | C1 to C4 = 0.47 µF Note 2 | 1/3 $V_{L4}$ - 0.1 | 1/3 $V_{L4}$ | 1/3 $V_{L4}$ + 0.1 | V |
| Capacitor split wait time Note 1 | tVWAIT | | 100 | | | ms |

**Note 1.** This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

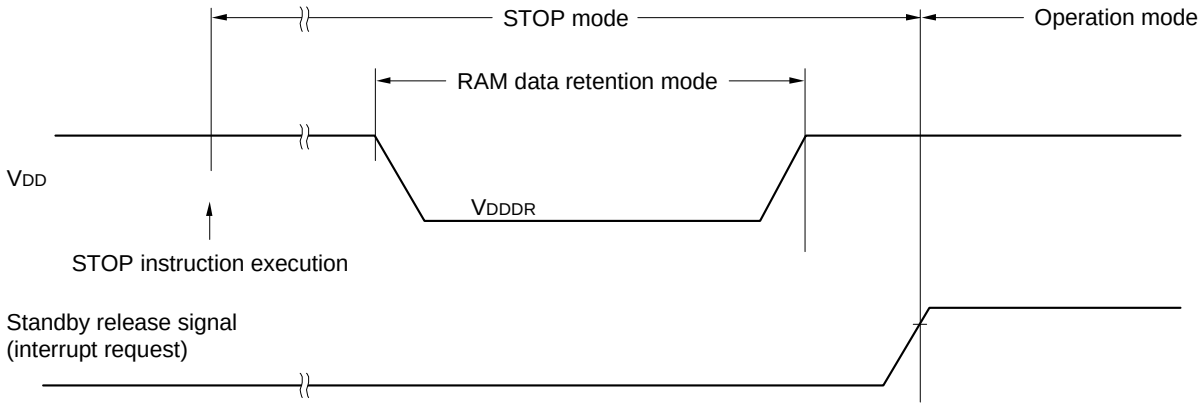
**Note 2.** This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between $V_{L1}$ and GND
C3: A capacitor connected between $V_{L2}$ and GND
C4: A capacitor connected between $V_{L4}$ and GND
C1 = C2 = C3 = C4 = 0.47 µF±30%

## 2.9 RAM Data Retention Characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.46 Note | | 3.6 | V |

**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.




## 2.10 Flash Memory Programming Characteristics

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CPU/peripheral hardware clock frequency | $f_{CLK}$ | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | 1 | | 24 | MHz |
| Number of code flash rewrites Notes 1, 2, 3 | Cerwr | Retained for 20 years $T_A$ = 85°C | 1,000 | | | Times |
| Number of data flash rewrites Notes 1, 2, 3 | | Retained for 1 year $T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years $T_A$ = 85°C | 100,000 | | | |
| | | Retained for 20 years $T_A$ = 85°C | 10,000 | | | |

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**Note 2.** When using flash memory programmer and Renesas Electronics self programming library

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.11 Dedicated Flash Memory Programmer Communication (UART)

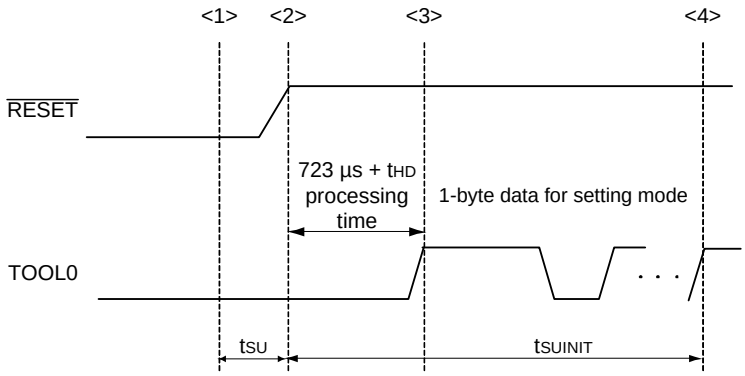
**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 2.12 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| How long from when an external reset ends until the initial communication settings are specified | $t_{SUINIT}$ | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until an external reset ends | $t_{SU}$ | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| Time to hold the TOOL0 pin at the low level after an external reset is released (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must end before the external reset ends. | 1 | | | ms |




<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.
$t_{SU}$: How long from when the TOOL0 pin is placed at the low level until a external reset ends
$t_{HD}$: How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)

# 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A$ = -40 to +105°C)

This chapter describes the following electrical specifications.
Target products G: Industrial applications $T_A$ = -40 to +105°C
R5F110xxGxx, R5F111xxGxx

**Caution 1. The RL78 microcontroller has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 With functions for each product in the RL78/L1C User's Manual.**

**Caution 3. Please contact Renesas Electronics sales office for derating of operation under $T_A$ = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.**

**Remark** When the RL78 microcontroller is used in the range of $T_A$ = -40 to +85°C, see **2. ELECTRICAL SPECIFICATIONS ($T_A$ = -40 to +85°C)**.

The following functions differ between the products "G: Industrial applications ($T_A$ = -40 to +105°C)" and the products "A: Consumer applications and G: Industrial applications (when used in the range of $T_A$ = -40 to +85°C)".

| Parameter | A: Consumer applications | G: Industrial applications |
|---|---|---|
| Operating ambient temperature | $T_A$ = -40 to +85°C | $T_A$ = -40 to +105°C |
| Operating mode<br>Operating voltage range | HS (high-speed main) mode:<br>2.7 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 24 MHz<br>2.4 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 16 MHz<br>LS (low-speed main) mode:<br>1.8 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 8 MHz<br>LV (low-voltage main) mode:<br>1.6 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 4 MHz | HS (high-speed main) mode only:<br>2.7 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 24 MHz<br>2.4 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 16 MHz |
| High-speed on-chip oscillator clock accuracy | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V:<br>±1.0% @ $T_A$ = -20 to +85°C<br>±1.5% @ $T_A$ = -40 to -20°C<br>1.6 V ≤ $V_{DD}$ ≤ 1.8 V:<br>±5.0% @ $T_A$ = -20 to +85°C<br>±5.5% @ $T_A$ = -40 to -20°C | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V:<br>±2.0% @ $T_A$ = +85 to +105°C<br>±1.0% @ $T_A$ = -20 to +85°C<br>±1.5% @ $T_A$ = -40 to -20°C |
| Serial array unit | UART<br>Simplified SPI (CSI): $f_{CLK}$/4<br>Simplified $I^2C$ communication | UART<br>Simplified SPI (CSI): $f_{CLK}$/4<br>Simplified $I^2C$ communication |
| IICA | Normal mode<br>Fast mode<br>Fast mode plus | Normal mode<br>Fast mode |
| Voltage detector | • Rise detection: 1.67 V to 3.13 V (12 levels)<br>• Fall detection: 1.63 V to 3.06 V (12 levels) | • Rise detection: 2.61 V to 3.13 V (6 levels)<br>• Fall detection: 2.55 V to 3.06 V (6 levels) |

**Remark** The electrical characteristics of the products G: Industrial applications ($T_A$ = -40 to +105°C) are different from those of the products "A: Consumer applications". For details, refer to **3.1** to **3.12**.

## 3.1 Absolute Maximum Ratings

**Absolute Maximum Ratings ($T_A$ = 25°C) (1/3)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | -0.5 to + 6.5 | V |
| | $UV_{BUS}$ | | -0.5 to + 6.5 | V |
| | $AV_{DD}$ | $AV_{DD} \leq V_{DD}$ | -0.5 to + 4.6 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | -0.3 to + 2.8 and -0.3 to $V_{DD}$ + 0.3 Note 1 | V |
| $U_{REGC}$ pin input voltage | $V_{IUREGC}$ | $U_{REGC}$ | -0.3 to $UV_{BUS}$ + 0.3 Note 2 | V |
| Input voltage | $V_{I1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P137, P140 to P143, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | -0.3 to $V_{DD}$ + 0.3 Note 3 | V |
| | $V_{I2}$ | P60, P61 (N-ch open-drain) | -0.3 to + 6.5 | V |
| | $V_{I3}$ | UDP, UDM | -0.3 to + 6.5 | V |
| | $V_{I4}$ | P150 to P156 | -0.3 to $AV_{DD}$ + 0.3 Note 4 | V |
| Output voltage | $V_{O1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | -0.3 to $V_{DD}$ + 0.3 Note 3 | V |
| | $V_{O2}$ | P150 to P156 | -0.3 to $AV_{DD}$ + 0.3 Note 3 | V |
| | $V_{O3}$ | UDP, UDM | -0.3 to + 3.8 | V |
| Analog input voltage | $V_{AI1}$ | ANI16 to ANI21 | -0.3 to $V_{DD}$ + 0.3 and $AV_{REF(+)}$ + 0.3 Notes 3, 5 | V |
| | $V_{AI2}$ | ANI0 to ANI6 | -0.3 to $AV_{DD}$ + 0.3 and $AV_{REF(+)}$ + 0.3 Notes 3, 5 | V |

**Note 1.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**Note 2.** Connect the $U_{REGC}$ pin to Vss via a capacitor (0.33 μF). This value regulates the absolute maximum rating of the $U_{REGC}$ pin. Do not use this pin with voltage applied to it.

**Note 3.** Must be 6.5 V or lower.

**Note 4.** Must be 4.6 V or lower.

**Note 5.** Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** $AV_{REF(+)}$: + side reference voltage of the A/D converter.

**Remark 3.** $V_{SS}$: Reference voltage

**Absolute Maximum Ratings ($T_A$ = 25°C)** **(2/3)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| LCD voltage | $V_{LI1}$ | $V_{L1}$ input voltage Note 1 | | -0.3 to +2.8 | V |
| | $V_{LI2}$ | $V_{L2}$ input voltage Note 1 | | -0.3 to +6.5 | V |
| | $V_{LI3}$ | $V_{L3}$ input voltage Note 1 | | -0.3 to +6.5 | V |
| | $V_{LI4}$ | $V_{L4}$ input voltage Note 1 | | -0.3 to +6.5 | V |
| | $V_{LI5}$ | CAPL, CAPH input voltage Note 1 | | -0.3 to +6.5 | V |
| | $V_{LO1}$ | $V_{L1}$ output voltage | | -0.3 to +2.8 | V |
| | $V_{LO2}$ | $V_{L2}$ output voltage | | -0.3 to +6.5 | V |
| | $V_{LO3}$ | $V_{L3}$ output voltage | | -0.3 to +6.5 | V |
| | $V_{LO4}$ | $V_{L4}$ output voltage | | -0.3 to +6.5 | V |
| | $V_{LO5}$ | CAPL, CAPH output voltage | | -0.3 to +6.5 | V |
| | $V_{LO6}$ | COM0 to COM7<br>SEG0 to SEG55<br>output voltage | External resistance division method | -0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| | | | Capacitor split method | -0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| | | | Internal voltage boosting method | -0.3 to $V_{LI4}$ + 0.3 Note 2 | V |

**Note 1.** This value only indicates the absolute maximum ratings when applying voltage to the $V_{L1}$, $V_{L2}$, $V_{L3}$, and $V_{L4}$ pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to $V_{SS}$ via a capacitor (0.47 ± 30%) and connect a capacitor (0.47 ± 30%) between the CAPL and CAPH pins.

**Note 2.** Must be 6.5 V or lower.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Absolute Maximum Ratings ($T_A$ = 25°C) (3/3)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | -40 | mA |
| | | Total of all pins -170 mA | P40 to P46 | -70 | mA |
| | | | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | -100 | mA |
| | $I_{OH2}$ | Per pin | P150 to P156 | -0.1 | mA |
| | | Total of all pins | | -0.7 | mA |
| | $I_{OH3}$ | Per pin | UDP, UDM | -3 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | 40 | mA |
| | | Total of all pins 170 mA | P40 to P46 | 70 | mA |
| | | | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | 100 | mA |
| | $I_{OL2}$ | Per pin | P150 to P156 | 0.4 | mA |
| | | Total of all pins | | 2.8 | mA |
| | $I_{OL3}$ | Per pin | UDP, UDM | 3 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | -40 to +105 | °C |
| | | In flash memory programming mode | | -40 to +105 | |
| Storage temperature | $T_{stg}$ | | | -65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 3.2 Oscillator Characteristics

### 3.2.1 X1 and XT1 oscillator characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$) Note | Ceramic resonator/crystal resonator | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 16.0 | |
| XT1 clock oscillation frequency ($f_{XT}$) Note | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/L1C User's Manual.

## 3.2.2 On-chip oscillator characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{HOCO}$ | | 1 | | 24 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | -20 to +85°C | -1.0 | | +1.0 | % |
| | | -40 to -20°C | -1.5 | | +1.5 | % |
| | | +85 to +105°C | -2.0 | | +2.0 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | -15 | | +15 | % |

**Note 1.** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

**Note 2.** This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

## 3.2.3 PLL oscillator characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ VDD ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| PLL input frequency Note | $f_{PLLIN}$ | High-speed system clock | 6.00 | | 16.00 | MHz |
| PLL output frequency Note | $f_{PLL}$ | | | 48.00 | | MHz |

**Note** Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

## 3.3 DC Characteristics

### 3.3.1 Pin characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high Note 1 | IOH1 | Per pin for P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | | | | -3.0 Note 2 | mA |
| | | Total of P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 (When duty ≤ 70% Note 3) | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | -15.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | -7.0 | mA |
| | $I_{OH2}$ | Per pin for P150 to P156 | | | | -0.1 Note 2 | mA |
| | | Total of all pins | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | | -0.7 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ pin to an output pin.

**Note 2.** However, do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = -10.0 mA
Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Caution P00 to P02, P10 to P12, P24 to P26, P33 to P35, and P42 to P44 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low Note 1 | $I_{OL1}$ | Per pin for P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | | | | 8.5 Note 2 | mA |
| | | Per pin for P60 and P61 | | | | 15.0 Note 2 | mA |
| | | Total of P40 to P46, P130 (When duty ≤ 70% Note 3) | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 15.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 9.0 | mA |
| | | Total of P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P140 to P143 (When duty ≤ 70% Note 3) | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 35.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 20.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | 50.0 | mA |
| | $I_{OL2}$ | Per pin for P150 to P156 | | | | 0.4 Note 2 | mA |
| | | Total of all pins | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | | 2.8 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $V_{SS}$ pin.

**Note 2.** However, do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression
(when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | VIH1 | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P140 to P143 | Normal input buffer | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | P00, P01, P10, P11, P24, P25, P33, P34, P43, P44 | TTL input buffer 3.3 V ≤ $V_{DD}$ ≤ 3.6 V | 2.0 | | $V_{DD}$ | V |
| | | | TTL input buffer 2.4 V ≤ $V_{DD}$ < 3.3 V | 1.50 | | $V_{DD}$ | V |
| | $V_{IH3}$ | P150 to P156 | | 0.7 $AV_{DD}$ | | $AV_{DD}$ | V |
| | $V_{IH4}$ | P60, P61 | | 0.7 $V_{DD}$ | | 6.0 | V |
| | $V_{IH5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P140 to P143 | Normal input buffer | 0 | | 0.2 $V_{DD}$ | V |
| | $V_{IL2}$ | P00, P01, P10, P11, P24, P25, P33, P34, P43, P44 | TTL input buffer 3.3 V ≤ $V_{DD}$ ≤ 3.6 V | 0 | | 0.5 | V |
| | | | TTL input buffer 2.4 V ≤ $V_{DD}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P150 to P156 | | 0 | | 0.3 $AV_{DD}$ | V |
| | $V_{IL4}$ | P60, P61 | | 0 | | 0.3 $V_{DD}$ | V |
| | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0 | | 0.2 $V_{DD}$ | V |

**Caution The maximum value of $V_{IH}$ of pins P00 to P02, P10 to P12, P24 to P26, P33 to P35, and P42 to P44 is $V_{DD}$, even in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH1}$ = -2.0 mA | $V_{DD}$ - 0.6 | | | V |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH1}$ = -1.5 mA | $V_{DD}$ - 0.5 | | | V |
| | $V_{OH2}$ | P150 to P156 | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH2}$ = -100 µA | $AV_{DD}$ - 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143 | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | P150 to P156 | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL2}$ = 400 µA | | | 0.4 | V |
| | $V_{OL3}$ | P60, P61 | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL3}$ = 3.0 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL3}$ = 2.0 mA | | | 0.4 | V |

**Caution P00 to P02, P10 to P12, P24 to P26, P33 to P35, and P42 to P44 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P137, P140 to P143, $\overline{RESET}$ | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P20, P21, P140 to P143 | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS) | $V_I$ = $V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| | $I_{LIH4}$ | P150 to P156 | $V_I$ = $AV_{DD}$ | | | | 1 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P137, P140 to P143, $\overline{RESET}$ | $V_I$ = $V_{SS}$ | | | | -1 | μA |
| | $I_{LIL2}$ | P20, P21, P140 to P143 | $V_I$ = $V_{SS}$ | | | | -1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS) | $V_I$ = $V_{SS}$ | In input port or external clock input | | | -1 | μA |
| | | | | In resonator connection | | | -10 | μA |
| | $I_{LIL4}$ | P150 to P156 | $V_I$ = $AV_{SS}$ | | | | -1 | μA |
| On-chip pull-up resistance | $R_{U1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P140 to P143, P125 to P127 | $V_I$ = $V_{SS}$ | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | 10 | 20 | 100 | kΩ |
| | $R_{U2}$ | P40 to P46, P80 to P83 | $V_I$ = $V_{SS}$ | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 3.3.2 Supply current characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 48 MHz Note 3, $f_{IH}$ = 24 MHz Note 3 | Basic operation | $V_{DD}$ = 3.6 V | | 2.2 | 2.9 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.2 | 2.9 | |
| | | | | | Normal operation | $V_{DD}$ = 3.6 V | | 4.4 | 9.2 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.4 | 9.2 | |
| | | | | $f_{HOCO}$ = 24 MHz Note 3, $f_{IH}$ = 24 MHz Note 3 | Basic operation | $V_{DD}$ = 3.6 V | | 2.0 | 2.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.0 | 2.6 | |
| | | | | | Normal operation | $V_{DD}$ = 3.6 V | | 4.2 | 7.0 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.2 | 7.0 | |
| | | | | $f_{HOCO}$ = 16 MHz Note 3, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 3.6 V | | 3.1 | 5.0 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.1 | 5.0 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.6 V | Normal operation | Square wave input | | 3.5 | 5.9 | mA |
| | | | | | | Resonator connection | | 3.6 | 6.0 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.5 | 5.9 | |
| | | | | | | Resonator connection | | 3.6 | 6.0 | |
| | | | | $f_{MX}$ = 16 MHz Note 2, $V_{DD}$ = 3.6 V | Normal operation | Square wave input | | 2.9 | 4.5 | |
| | | | | | | Resonator connection | | 3.1 | 4.6 | |
| | | | | $f_{MX}$ = 16 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.9 | 4.5 | |
| | | | | | | Resonator connection | | 3.1 | 4.6 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.6 V | Normal operation | Square wave input | | 2.1 | 3.5 | |
| | | | | | | Resonator connection | | 2.2 | 3.5 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.1 | 3.5 | |
| | | | | | | Resonator connection | | 2.2 | 3.5 | |
| | | | HS (High-speed main) mode (PLL operation) | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 24 MHz Note 2 | Normal operation | $V_{DD}$ = 3.6 V | | 4.7 | 7.6 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.7 | 7.6 | |
| | | | | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 12 MHz Note 2 | Normal operation | $V_{DD}$ = 3.6 V | | 3.1 | 5.2 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.1 | 5.1 | |
| | | | | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 6 MHz Note 2 | Normal operation | $V_{DD}$ = 3.6 V | | 2.3 | 3.9 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.3 | 3.9 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.6 | 6.9 | µA |
| | | | | | | Resonator connection | | 4.7 | 6.9 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.9 | 7.0 | |
| | | | | | | Resonator connection | | 5.0 | 7.2 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 5.2 | 7.6 | |
| | | | | | | Resonator connection | | 5.2 | 7.7 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 5.5 | 9.3 | |
| | | | | | | Resonator connection | | 5.6 | 9.4 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.2 | 13.3 | |
| | | | | | | Resonator connection | | 6.2 | 13.4 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 8.3 | 46.0 | |
| | | | | | | Resonator connection | | 8.4 | 46.0 | |

(**Notes** and **Remarks** are listed on the next page.)

<R> **Note 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, or $V_{SS}$. The following points apply in the HS (high-speed main) mode.
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into LCD controller/driver, A/D converter, D/A converter, comparator, LVD circuit, USB 2.0 function module, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the real-time clock 2.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

<R> **Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 24 MHz
2.4 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 16 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (48 MHz max.)

**Remark 3.** $f_{IH}$: Main system clock source frequency when the high-speed on-chip oscillator clock divided 1, 2, 4, or 8, or the PLL clock divided by 2, 4, or 8 is selected (24 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 6 | $f_{HOCO}$ = 48 MHz Note 4, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 3.6 V | | 0.77 | 3.4 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.77 | 3.4 | |
| | | | | $f_{HOCO}$ = 24 MHz Note 4, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 3.6 V | | 0.55 | 2.7 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.55 | 2.7 | |
| | | | | $f_{HOCO}$ = 16 MHz Note 4, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 3.6 V | | 0.48 | 1.9 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.47 | 1.9 | |
| | | | HS (high-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.6 V | Square wave input | | 0.35 | 2.10 | mA |
| | | | | | Resonator connection | | 0.51 | 2.20 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.34 | 2.10 | |
| | | | | | Resonator connection | | 0.51 | 2.20 | |
| | | | | $f_{MX}$ = 16 MHz Note 3, $V_{DD}$ = 3.6 V | Square wave input | | 0.30 | 1.25 | |
| | | | | | Resonator connection | | 0.45 | 1.41 | |
| | | | | $f_{MX}$ = 16 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.29 | 1.23 | |
| | | | | | Resonator connection | | 0.45 | 1.41 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.6 V | Square wave input | | 0.23 | 1.10 | |
| | | | | | Resonator connection | | 0.30 | 1.20 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.22 | 1.10 | |
| | | | | | Resonator connection | | 0.30 | 1.20 | |
| | | | HS (High-speed main) mode (PLL operation) | $f_{MX}$ = 48 MHz, $f_{CLK}$ = 24 MHz Note 3 | $V_{DD}$ = 3.6 V | | 0.99 | 2.93 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.99 | 2.92 | |
| | | | | $f_{MX}$ = 48 MHz, $f_{CLK}$ = 12 MHz Note 3 | $V_{DD}$ = 3.6 V | | 0.89 | 2.51 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.89 | 2.50 | |
| | | | | $f_{MX}$ = 48 MHz, $f_{CLK}$ = 6 MHz Note 3 | $V_{DD}$ = 3.6 V | | 0.84 | 2.30 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.84 | 2.29 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = -40°C | Square wave input | | 0.32 | 0.61 | µA |
| | | | | | Resonator connection | | 0.51 | 0.80 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +25°C | Square wave input | | 0.41 | 0.74 | |
| | | | | | Resonator connection | | 0.62 | 0.91 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +50°C | Square wave input | | 0.52 | 2.30 | |
| | | | | | Resonator connection | | 0.75 | 2.49 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +70°C | Square wave input | | 0.82 | 4.03 | |
| | | | | | Resonator connection | | 1.08 | 4.22 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +85°C | Square wave input | | 1.38 | 8.04 | |
| | | | | | Resonator connection | | 1.62 | 8.23 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +105°C | Square wave input | | 3.29 | 41.00 | |
| | | | | | Resonator connection | | 3.63 | 41.00 | |
| | $I_{DD3}$ | STOP mode Note 7 | $T_A$ = -40°C | | | | 0.18 | 0.52 | µA |
| | | | $T_A$ = +25°C | | | | 0.25 | 0.52 | |
| | | | $T_A$ = +50°C | | | | 0.34 | 2.21 | |
| | | | $T_A$ = +70°C | | | | 0.64 | 3.94 | |
| | | | $T_A$ = +85°C | | | | 1.18 | 7.95 | |
| | | | $T_A$ = +105°C | | | | 2.92 | 40.00 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or
<R> $V_{SS}$. The following points apply in the HS (high-speed main) mode.
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into LCD controller/driver, A/D converter, D/A converter, comparator, LVD circuit, USB 2.0 function module, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the real-time clock 2.
In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low
<R> current consumption (AMPHS1 = 1).

**Note 6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 24 MHz
2.4 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 16 MHz

**Note 7.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (48 MHz max.)

**Remark 3.** $f_{IH}$: Main system clock source frequency when the high-speed on-chip oscillator clock divided 1, 2, 4, or 8, or the PLL clock divided by 2, 4, or 8 is selected (24 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

<R> **Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | | | 0.20 | | μA |
| RTC2 operating current | $I_{RTC}$ Notes 1, 3 | | | | | | 0.02 | | μA |
| 12-bit interval timer operating current | $I_{TMKA}$ Notes 1, 2, 4 | | | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 5 | $f_{IL}$ = 15 kHz | | | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 6, 7 | $AV_{DD}$ = 3.0 V, when conversion at maximum speed | | | | | 422 | 720 | μA |
| $AV_{REF(+)}$ current | $I_{AVREF}$ Note 8 | $AV_{DD}$ = 3.0 V, ADREFP1 = 0, ADREFP0 = 0 Note 7 | | | | | 14.0 | 25.0 | μA |
| | | $AV_{REFP}$ = 3.0 V, ADREFP1 = 0, ADREFP0 = 1 Note 10 | | | | | 14.0 | 25.0 | |
| | | ADREFP1 = 1, ADREFP0 = 0 Note 1 | | | | | 14.0 | 25.0 | |
| A/D converter reference voltage current | $I_{ADREF}$ Notes 1, 9 | $V_{DD}$ = 3.0 V | | | | | 75.0 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | | | 78 | | μA |
| D/A converter operating current | $I_{DAC}$ Notes 1, 11 | Per D/A converter channel | | | | | 0.53 | 1.5 | mA |
| Comparator operating current | $I_{CMP}$ Notes 1, 12 | $V_{DD}$ = 3.6 V, Regulator output voltage = 2.1 V | Window mode | | | | 12.5 | | μA |
| | | | Comparator high-speed mode | | | | 4.5 | | μA |
| | | | Comparator low-speed mode | | | | 1.2 | | μA |
| LVD operating current | $I_{LVD}$ Notes 1, 13 | | | | | | 0.06 | | μA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 14 | | | | | | 2.50 | 12.20 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 15 | | | | | | 1.68 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 16 | | | | 0.34 | 1.10 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | | | 0.53 | 2.04 | |
| | | Simplified SPI (CSI)/UART operation | | | | | 0.70 | 1.54 | mA |
| LCD operating current | $I_{LCD1}$ Notes 17, 18 | External resistance division method | $f_{LCD}$ = $f_{SUB}$ LCD clock = 128 Hz | 1/3 bias 4-time slice | $V_{DD}$ = 3.6 V, $L_{V4}$ = 3.6 V | | 0.14 | | μA |
| | $I_{LCD2}$ Note 17 | Internal voltage boosting method | $f_{LCD}$ = $f_{SUB}$ LCD clock = 128 Hz | 1/3 bias 4-time slice | $V_{DD}$ = 3.0 V, $L_{V4}$ = 3.0 V (VLCD = 04H) | | 0.61 | | μA |
| | $I_{LCD3}$ Note 17 | Capacitor split method | $f_{LCD}$ = $f_{SUB}$ LCD clock = 128 Hz | 1/3 bias 4-time slice | $V_{DD}$ = 3.0 V, $L_{V4}$ = 3.0 V | | 0.12 | | μA |
| USB current Note 19 | $I_{USB}$ Note 20 | Operating current during USB communication | | | | | 4.88 | | mA |
| | $I_{USB}$ Note 21 | Operating current in the USB suspended state | | | | | 0.04 | | mA |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Current flowing to $V_{DD}$.

**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**Note 3.** Current flowing only to the real-time clock 2 (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock 2 operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock 2.

**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{TMKA}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the 12-bit interval timer.

**Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer operates in STOP mode.

**Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$, $I_{AVREF}$, $I_{ADREF}$ when the A/D converter operates in an operation mode or the HALT mode.

**Note 7.** Current flowing to the $AV_{DD}$.

**Note 8.** Current flowing from the reference voltage source of A/D converter.

**Note 9.** Operation current flowing to the internal reference voltage.

**Note 10.** Current flowing to the $AV_{REFP}$.

**Note 11.** Current flowing only to the D/A converter. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{DA}$ when the D/A converter operates in an operation mode or the HALT mode.

**Note 12.** Current flowing only to the comparator circuit. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{CMP}$ when the comparator circuit operates in the Operating, HALT or STOP mode.

**Note 13.** Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVI}$ when the LVD circuit operates in the Operating, HALT or STOP mode.

**Note 14.** Current flowing only during self-programming.

**Note 15.** Current flowing only during data flash rewrite.

**Note 16.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/L1C User's Manual..

**Note 17.** Current flowing only to the LCD controller/driver ($V_{DD}$ pin). The current value of the RL78 microcontrollers is the sum of the LCD operating current ($I_{LCD1}$, $I_{LCD2}$ or $I_{LCD3}$) to the supply current ($I_{DD1}$, or $I_{DD2}$) when the LCD controller/driver operates in an operation mode or HALT mode. Not including the current that flows through the LCD panel.

**Note 18.** Not including the current that flows through the external divider resistor divider resistor.

**Note 19.** Current flowing to the $UV_{BUS}$.

**Note 20.** Including the operating current when $f_{PLL}$ = 48 MHz.

**Note 21.** Including the current supplied from the pull-up resistor of the UDP pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.

**Remark 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**Remark 2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 3.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**Remark 4.** Temperature condition of the TYP. value is $T_A$ = 25°C

## 3.4 AC Characteristics

### 3.4.1 Basic operation

**($T_A$ = -40 to +105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (1/2)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 0.0417 | | 1 | μs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | μs |
| | | Subsystem clock ($f_{SUB}$) operation | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | 28.5 | 30.5 | 31.3 | μs |
| | | In the self-programming mode | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 0.0417 | | 1 | μs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | μs |
| External main system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 1.0 | | 16.0 | MHz |
| | $f_{EXT}$ | | | | 32 | | 35 | kHz |
| External main system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 30 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | μs |
| TI00 to TI07 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 | | | ns |

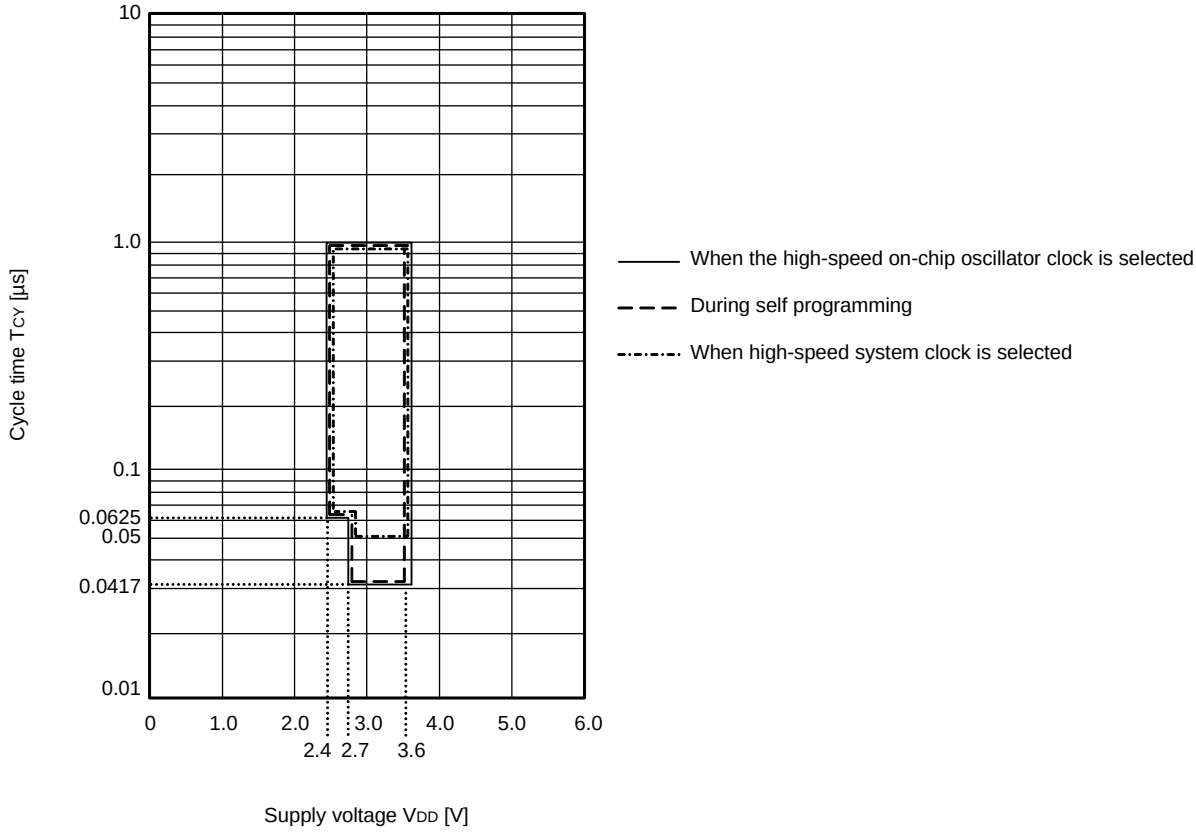
**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 7))

**($T_A$ = -40 to +105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)** **(2/2)**

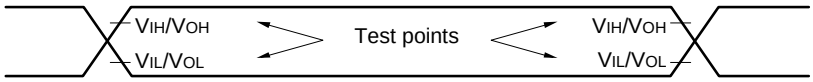
| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| TO00 to TO07, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21 output frequency | $f_{TO}$ | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 8 | MHz |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 8 | MHz |
| PCLBUZ0, PCLBUZ1 output frequency | $f_{PCL}$ | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 8 | MHz |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 8 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 to INTP7 | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | 1 | | | µs |
| Key interrupt input low-level width | $t_{KR}$ | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 250 | | | ns |
| TMKB2 forced output stop input high-level width | $t_{IHR}$ | INTP0 to INTP7 | $f_{CLK}$ > 16 MHz | 125 | | | ns |
| | | | $f_{CLK}$ ≤ 16 MHz | 2 | | | $f_{CLK}$ |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | 10 | | | µs |

Minimum Instruction Execution Time during Main System Clock Operation

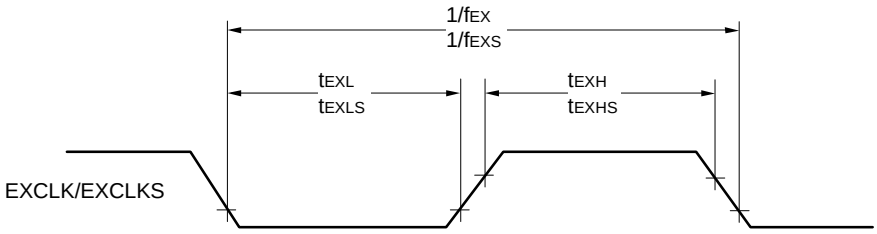
$T_{CY}$ vs $V_{DD}$ (HS (high-speed main) mode)



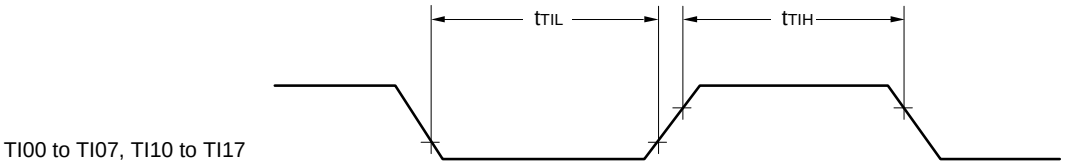
AC Timing Test Points

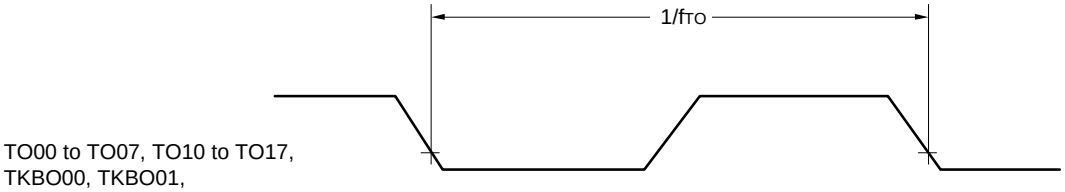



External System Clock Timing

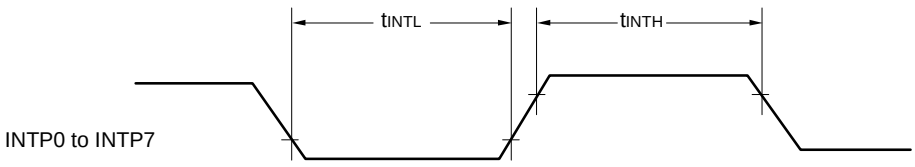



TI/TO Timing

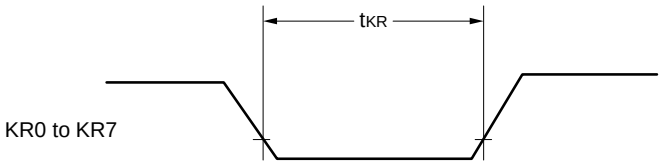


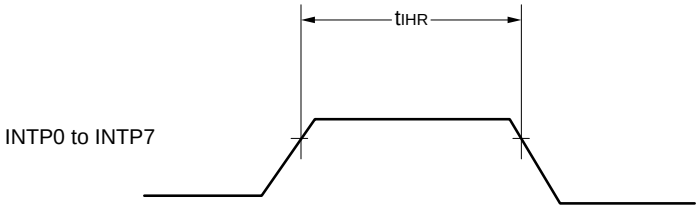

Interrupt Request Input Timing



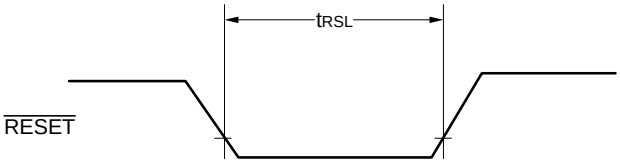
Key Interrupt Input Timing



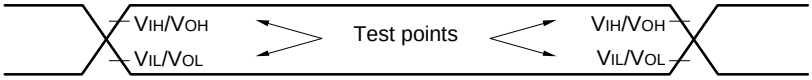

Timer KB2 Input Timing




$\overline{\text{RESET}}$ Input Timing



## 3.5 Peripheral Functions Characteristics




### 3.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Transfer rate Note 1 | | 2.4 V ≤ VDD ≤ 3.6 V | | fMCK/12 Note 2 | bps |
| | | Theoretical value of the maximum transfer rate<br>fMCK = fCLK Note 3 | | 2.0 | Mbps |

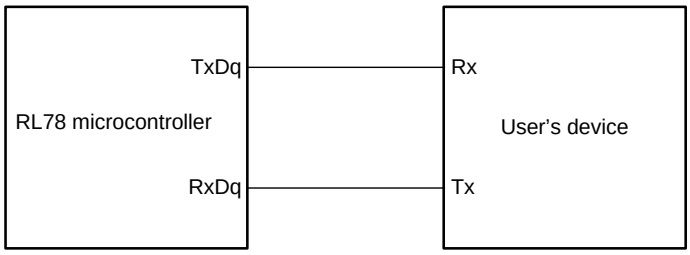
**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**Note 2.** The following conditions are required for low voltage interface.
2.4 V ≤ VDD < 2.7 V: MAX. 1.3 Mbps

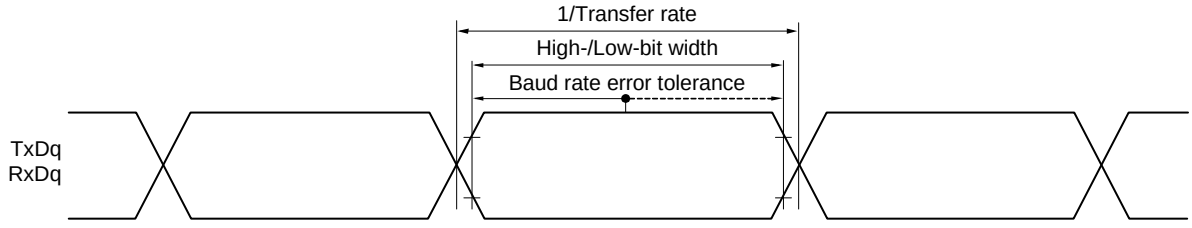
**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ VDD ≤ 3.6 V)
16 MHz (2.4 V ≤ VDD ≤ 3.6 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remark 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 3)

**Remark 2.** fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (2) During communication at same potential (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq f_{CLK}/4$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 250 | | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | $t_{KCY1}$/2 - 36 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | $t_{KCY1}$/2 - 76 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 66 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 133 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | | | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 30 pF Note 4 | | | 50 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0 to 3)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (3) During communication at same potential (Simplified SPI (CSI) mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 2.7 V ≤ $V_{DD}$ < 3.6 V | $f_{MCK}$ > 16 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.6 V | | 12/$f_{MCK}$ and 1000 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | $t_{KCY2}$/2 - 16 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | $t_{KCY2}$/2 - 36 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 2/$f_{MCK}$ + 66 | ns |
| | | | 2.4 V ≤ $V_{DD}$ < 3.6 V | | 2/$f_{MCK}$ + 113 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SOp output lines.

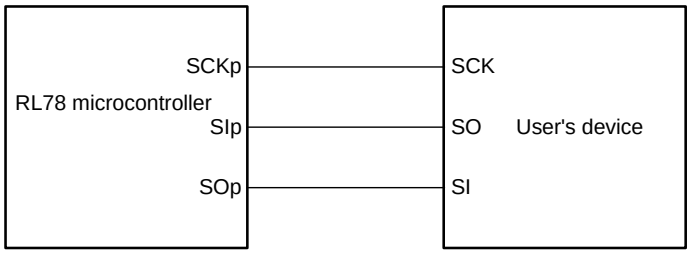
**Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0 to 3)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

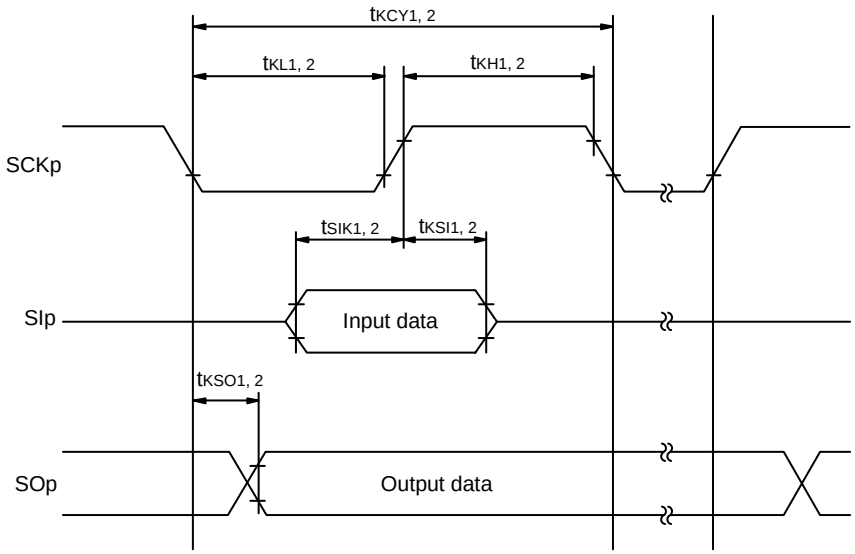
**Simplified SPI (CSI) mode connection diagram (during communication at same potential)**



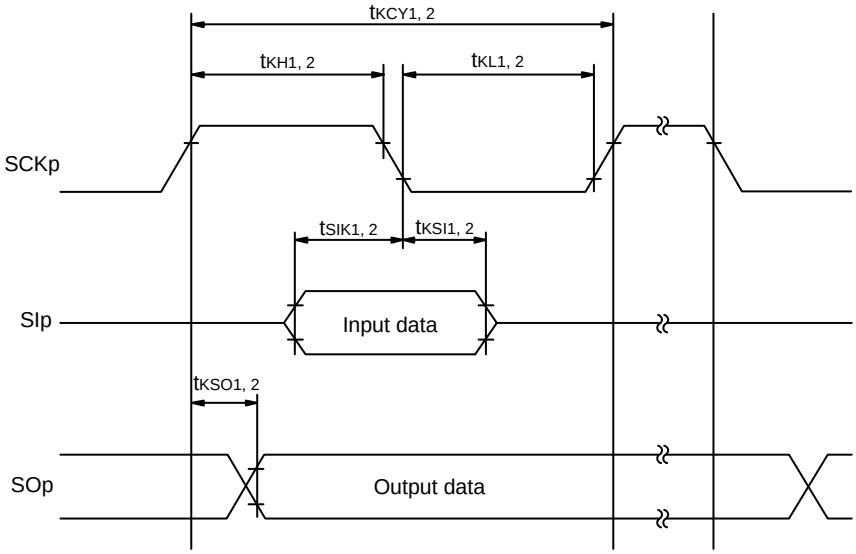

**Remark 1.** p: CSI number (p = 00, 10, 20, 30)

**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 10, 20, 30)
**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

### (4) During communication at same potential (simplified I²C mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

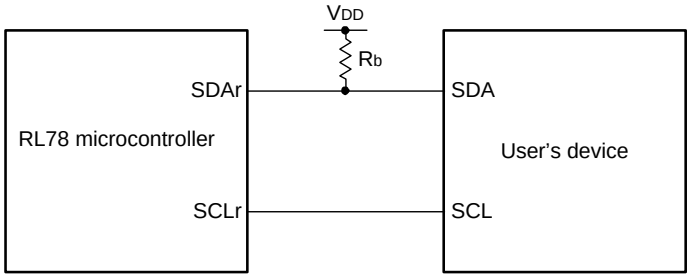
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = "L" | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = "H" | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 200 Note 2 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 580 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD: DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 1420 | ns |

**Note 1.** The value must be equal to or less than $f_{MCK}$/4.

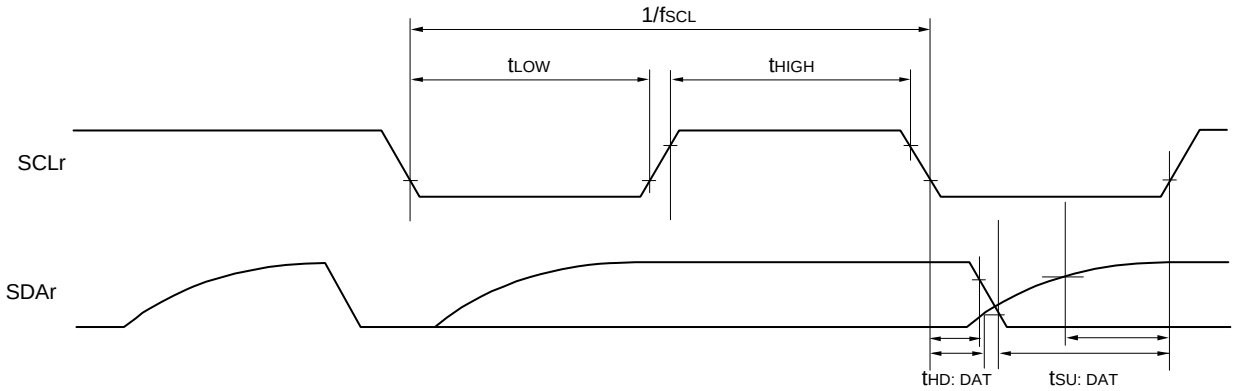
**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

**Simplified I²C mode connection diagram (during communication at same potential)**



**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

**Remark 2.** r: IIC number (r = 00, 10, 20, 30), g: PIM number (g = 0 to 3),
h: POM number (h = 0 to 3)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

### (5) Communication at different potential (1.8 V, 2.5 V) (UART mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| Transfer rate Notes 1, 2 | | Reception | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 2.0 | Mbps |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/12 Notes 1, 2, 3 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 1.3 | Mbps |

**Note 1.** Transfer rate in the SNOOZE mode is 4,800 bps only.

**Note 2.** Use it with $V_{DD} \geq V_b$.

**Note 3.** The following conditions are required for low voltage interface.
2.4 V ≤ $V_{DD}$ < 2.7 V: MAX. 2.6 Mbps

**Note 4.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 3.6 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 3.6 V)

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $V_b$[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 3)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (5) Communication at different potential (1.8 V, 2.5V) (UART mode)

**($T_A$ = -40 to +105°C, 2.4 ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| Transfer rate Note 2 | | Transmission | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 2 | Mbps |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | Notes 3, 4 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 5 | Mbps |

**Note 1.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ $V_{DD}$ < 3.6 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 2.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

**Note 3.** Use it with $V_{DD}$ ≥ $V_b$.

**Note 4.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V ≤ $V_{DD}$ < 3.3 V and 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

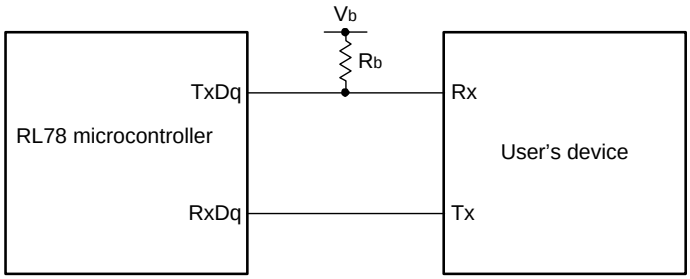
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

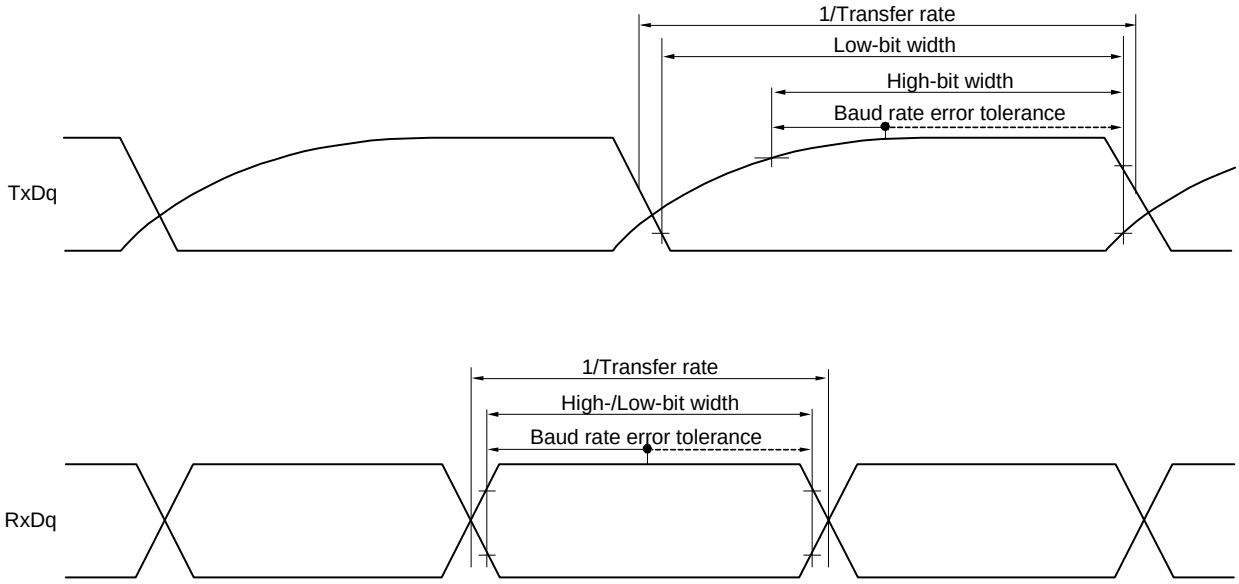
**Note 5.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**UART mode connection diagram (during communication at different potential)**




**UART mode bit width (during communication at different potential) (reference)**




**Remark 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance, $C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 3)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (6) Communication at different potential (1.8 V, 2.5 V) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq f_{CLK}/4$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 1000 Note | | ns |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 1.8 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 2300 Note | | ns |
| SCKp high-level width | $t_{KH1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 340 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 916 | | ns |
| SCKp low-level width | $t_{KL1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 36 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 100 | | ns |

**Note** Use it with $V_{DD} \geq V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

### (6) Communication at different potential (1.8 V, 2.5 V) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 354 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 958 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 390 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 966 | ns |
| SIp setup time (to SCKp↓) Note 2 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 88 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 220 | | ns |
| SIp hold time (from SCKp↓) Note 2 | $t_{KSI1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↑ to SOp output Note 2 | $t_{KSO1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 50 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 50 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

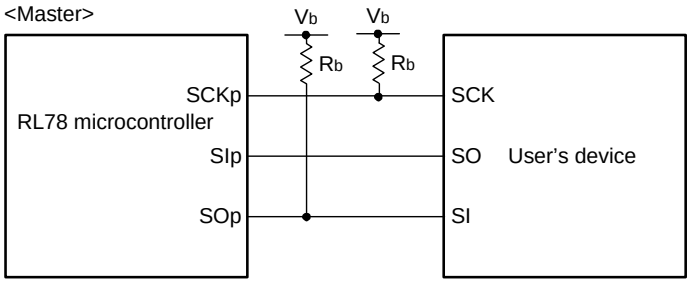
**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** Use it with $V_{DD}$ ≥ $V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Simplified SPI (CSI) mode connection diagram (during communication at different potential)**

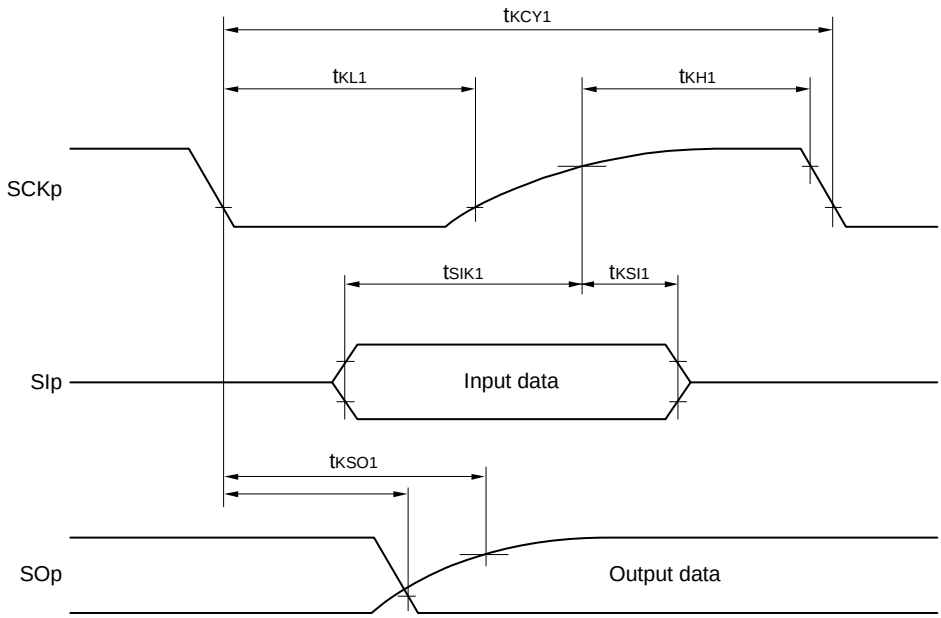



**Remark 1.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

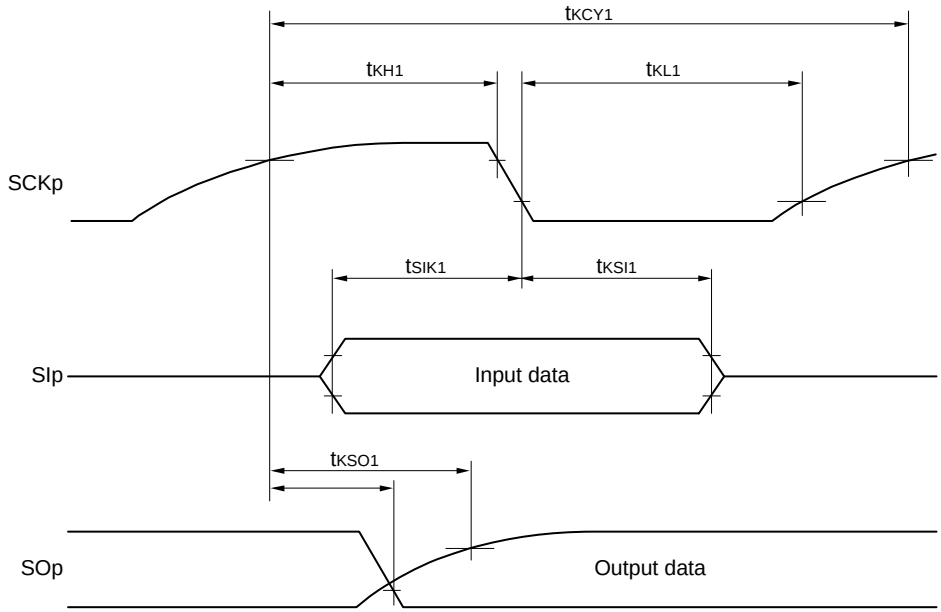
**Remark 2.** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0 to 3)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0 to 3)

### (7) Communication at different potential (1.8 V, 2.5 V) (Simplified SPI (CSI) mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 32/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 28/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 24/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 72/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 64/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 52/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 32/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 20/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 - 36 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | $t_{KCY2}$/2 - 100 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 5 | $t_{KSO2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 1146 | ns |

**Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Note 2.** Use it with $V_{DD} \geq V_b$.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

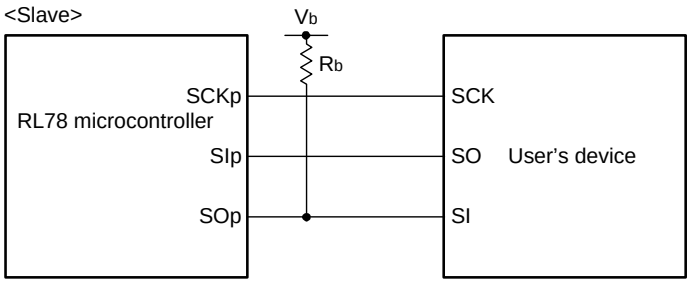
**Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Simplified SPI (CSI) mode connection diagram (during communication at different potential)**

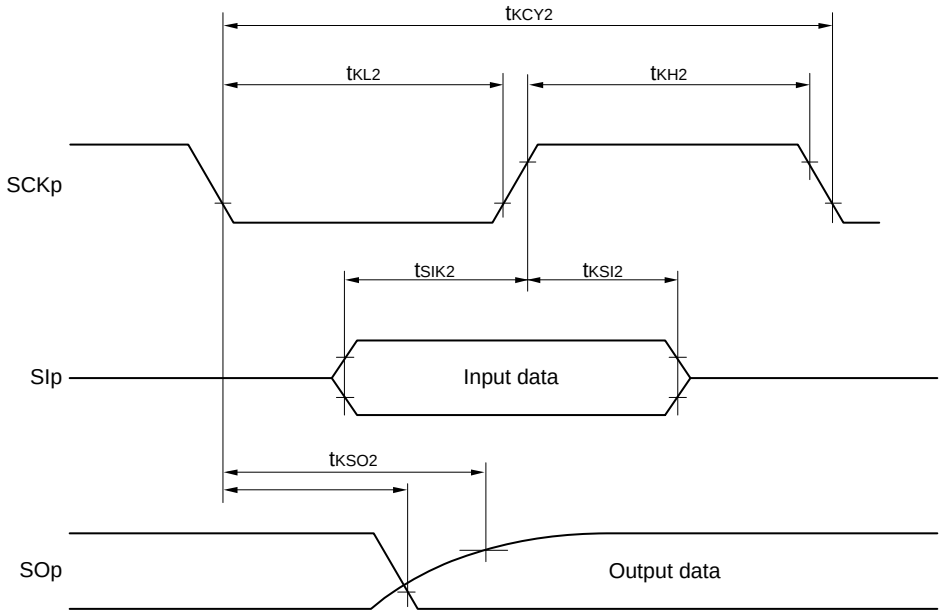



**Remark 1.** $R_b$[Ω]: Communication line (SOp) pull-up resistance, $C_b$[F]: Communication line (SOp) load capacitance, $V_b$[V]: Communication line voltage

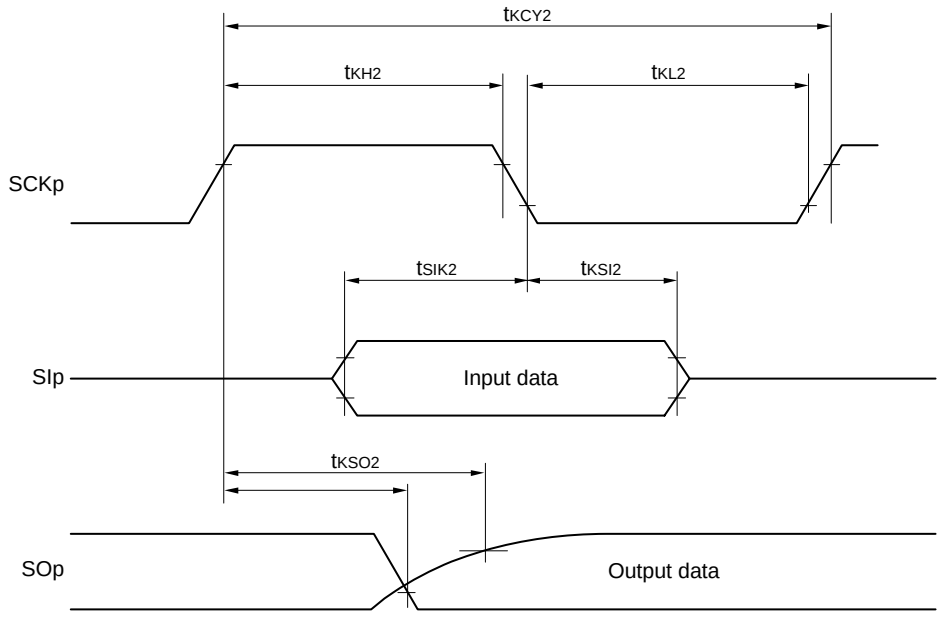
**Remark 2.** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0 to 3)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10, 12))

**Simplified SPI (CSI) mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**Simplified SPI (CSI) mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0 to 3)

### (8) Communication at different potential (1.8 V, 2.5 V) (simplified $I^2C$ mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 100 Note 1 | kHz |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ <2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 4600 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 4650 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 500 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 2400 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1830 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 340 Note 3 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 760 Note 3 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1/$f_{MCK}$ + 570 Note 3 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 1420 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 1215 | ns |

**Note 1.** The value must be equal to or less than $f_{MCK}$/4.

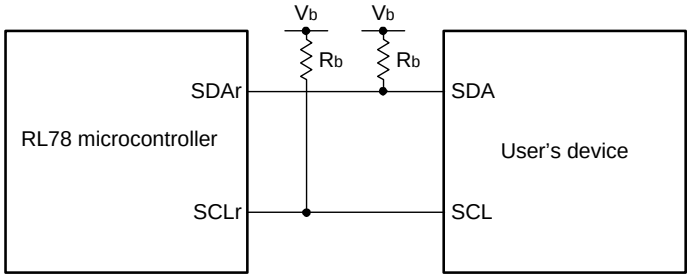
**Note 2.** Use it with $V_{DD}$ ≥ $V_b$.

**Note 3.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

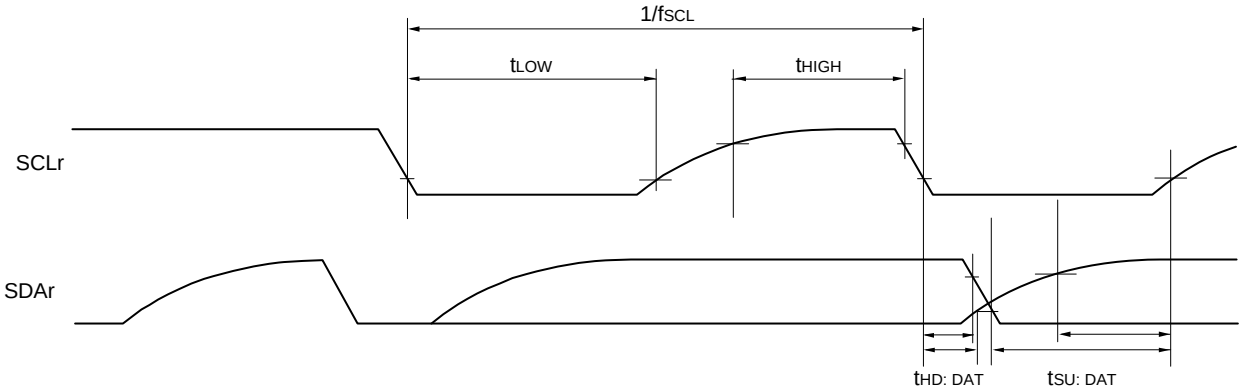
**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** r: IIC number (r = 00, 10, 20, 30), g: PIM, POM number (g = 0 to 3)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00, 02, 10, 12)

## 3.5.2 Serial interface IICA

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Standard mode | | Fast mode | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | — | — | 0 | 400 | kHz |
| | | Standard mode: $f_{CLK}$ ≥ 1 MHz | 0 | 100 | — | — | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | | 4.7 | | 0.6 | | µs |
| Hold time Note 1 | $t_{HD: STA}$ | | 4.0 | | 0.6 | | µs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | | 4.7 | | 1.3 | | µs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | | 4.0 | | 0.6 | | µs |
| Data setup time (reception) | $t_{SU: DAT}$ | | 250 | | 100 | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | | 0 | 3.45 | 0 | 0.9 | µs |
| Setup time of stop condition | $t_{SU: STO}$ | | 4.0 | | 0.6 | | µs |
| Bus-free time | $t_{BUF}$ | | 4.7 | | 1.3 | | µs |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

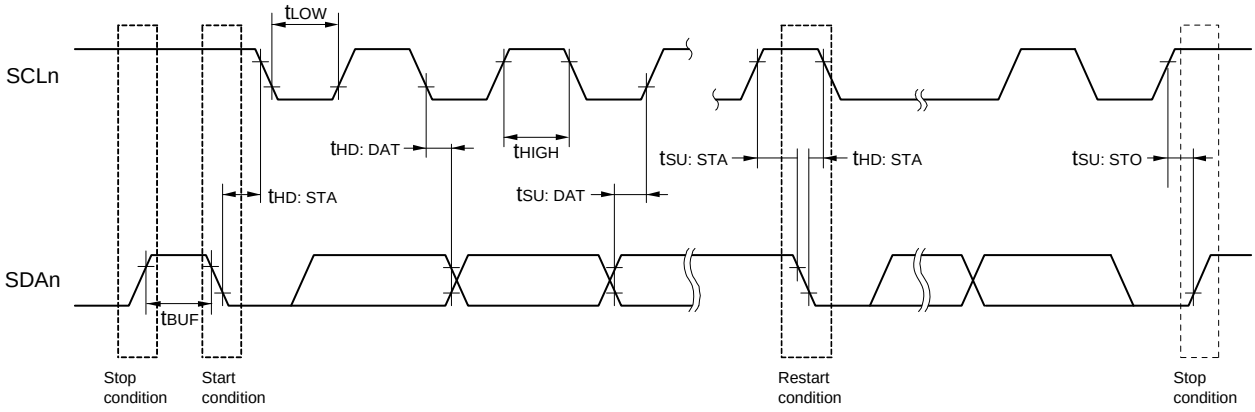
**Note 2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b$ = 400 pF, $R_b$ = 2.7 kΩ

Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**



## 3.5.3 USB

### (1) Electrical specifications

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| UREGC | UREGC output voltage characteristic | UREGC | UVBUS = 4.0 to 5.5 V, PXXCON = VDDUSBE = 1 | 3.0 | 3.3 | 3.6 | V |
| UVBUS | UVBUS input voltage characteristic | UVBUS | Function | 4.35 (4.02 Note) | 5.00 | 5.25 | V |

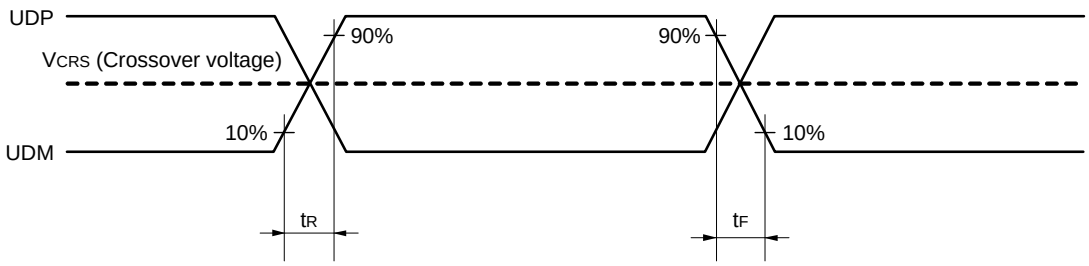
**Note** Value of instantaneous voltage

**($T_A$ = -40 to +105°C, 4.35 V ≤ UVBUS ≤ 5.25 V, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input characteristic (FS/LS receiver) | Input voltage | | VIH | | 2.0 | | | V |
| | | | VIL | | | | 0.8 | V |
| | Difference input sensitivity | | VDI | \| UDP voltage - UDM voltage \| | 0.2 | | | V |
| | Difference common mode range | | VCM | | 0.8 | | 2.5 | V |
| Output characteristic (FS driver) | Output voltage | | VOH | IOH = -200 µA | 2.8 | | 3.6 | V |
| | | | VOL | IOL = 2 mA | 0 | | 0.3 | V |
| | Transition time | Rising | tFR | Rising: From 10% to 90% of amplitude, Falling: From 90% to 10% of amplitude, CL = 50 pF | 4 | | 20 | ns |
| | | Falling | tFF | | 4 | | 20 | ns |
| | Matching (TFR/TFF) | | VFRFM | | 90 | | 111.1 | % |
| | Crossover voltage | | VFCRS | | 1.3 | | 2.0 | V |
| | Output Impedance | | ZDRV | | 28 | | 44 | Ω |
| Output characteristic (LS driver) | Output voltage | | VOH | | 2.8 | | 3.6 | V |
| | | | VOL | | 0 | | 0.3 | V |
| | Transition time | Rising | tLR | Rising: From 10% to 90% of amplitude, Falling: From 90% to 10% of amplitude, CL = 250 pF to 750 pF<br><br>The UDP and UDM pins are individually pulled down via 15 kΩ | 75 | | 300 | ns |
| | | Falling | tLF | | 75 | | 300 | ns |
| | Matching (TFR/TFF) Note | | VLTFM | | 80 | | 125 | % |
| | Crossover voltage Note | | VLCRS | | 1.3 | | 2.0 | V |
| Pull-up, Pull-down | Pull-down resistor | | RPD | | 14.25 | | 24.80 | kΩ |
| | Pull-up resistor | Idle | RPUI | | 0.9 | | 1.575 | kΩ |
| | | Reception | RPUA | | 1.425 | | 3.09 | kΩ |
| UVBUS | UVBUS pull-down resistor | | RVBUS | UVBUS voltage = 5.5 V | | 1000 | | kΩ |
| | UVBUS input voltage | | VIH | | 3.20 | | | V |
| | | | VIL | | | | 0.8 | V |

**Note** Excludes the first signal transition from the idle state.

**Timing of UDP and UDM**




**(2) BC standard**

**($T_A$ = -40 to +105°C, 4.35 V ≤ $UV_{BUS}$ ≤ 5.25 V, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| USB standard BC1.2 | UDP sink current | $I_{DP\_SINK}$ | | 25 | 100 | 175 | μA |
| | UDM sink current | $I_{DM\_SINK}$ | | 25 | 100 | 175 | μA |
| | DCD source current | $I_{DP\_SRC}$ | | 7 | 10 | 13 | μA |
| | Data detection voltage | $V_{DAT\_REF}$ | | 0.25 | 0.325 | 0.4 | V |
| | UDP source voltage | $V_{DP\_SRC}$ | Output current 250 μA | 0.5 | 0.6 | 0.7 | V |
| | UDM source voltage | $V_{DM\_SRC}$ | Output current 250 μA | 0.5 | 0.6 | 0.7 | V |

### (3) BC option standard

**($T_A$ = -40 to +105°C, 4.35 V ≤ $UV_{BUS}$ ≤ 5.25 V, 2.4 V ≤ $V_{DD}$ ≤ 3.6, $V_{SS}$ = 0 V)**

| Parameter | | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| UDP/UDM input reference voltage ($UV_{BUS}$ divider ratio) (Function) | VDSELi [3: 0] (i = 0, 1) | 0000 | $V_{DDET0}$ | | 27 | 32 | 37 | %UVBUS |
| | | 0001 | $V_{DDET1}$ | | 29 | 34 | 39 | %UVBUS |
| | | 0010 | $V_{DDET2}$ | | 32 | 37 | 42 | %UVBUS |
| | | 0011 | $V_{DDET3}$ | | 35 | 40 | 45 | %UVBUS |
| | | 0100 | $V_{DDET4}$ | | 38 | 43 | 48 | %UVBUS |
| | | 0101 | $V_{DDET5}$ | | 41 | 46 | 51 | %UVBUS |
| | | 0110 | $V_{DDET6}$ | | 44 | 49 | 54 | %UVBUS |
| | | 0111 | $V_{DDET7}$ | | 47 | 52 | 57 | %UVBUS |
| | | 1000 | $V_{DDET8}$ | | 51 | 56 | 61 | %UVBUS |
| | | 1001 | $V_{DDET9}$ | | 55 | 60 | 65 | %UVBUS |
| | | 1010 | $V_{DDET10}$ | | 59 | 64 | 69 | %UVBUS |
| | | 1011 | $V_{DDET11}$ | | 63 | 68 | 73 | %UVBUS |
| | | 1100 | $V_{DDET12}$ | | 67 | 72 | 73 | %UVBUS |
| | | 1101 | $V_{DDET13}$ | | 71 | 76 | 81 | %UVBUS |
| | | 1110 | $V_{DDET14}$ | | 75 | 80 | 85 | %UVBUS |
| | | 1111 | $V_{DDET15}$ | | 79 | 84 | 89 | %UVBUS |

## 3.6 Analog Characteristics

### 3.6.1 A/D converter characteristics

**Classification of A/D converter characteristics**

| Reference Voltage / Input Channel | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (-) = $AV_{REFM}$ | Reference voltage (+) = $AV_{DD}$<br>Reference voltage (-) = $AV_{SS}$ | Reference voltage (+) = Internal reference voltage<br>Reference voltage (-) = $AV_{SS}$ |
|---|---|---|---|
| High-accuracy channel; ANI0 to ANI6 (input buffer power supply: $AV_{DD}$) | Refer to **3.6.1 (1)**. | Refer to **3.6.1 (2)**. | Refer to **3.6.1 (5)**. |
| Standard channel; ANI16 to ANI21 (input buffer power supply: $V_{DD}$) | Refer to **3.6.1 (3)**. | Refer to **3.6.1 (4)**. | |
| Internal reference voltage, Temperature sensor output voltage | Refer to **3.6.1 (3)**. | Refer to **3.6.1 (4)**. | — |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), conversion target: ANI2 to ANI6**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| Overall error Note | AINL | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±6.0 | LSB |
| Conversion time | $t_{CONV}$ | ADTYP = 0,<br>12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 3.375 | | | µs |
| Zero-scale error Note | $E_{ZS}$ | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±4.5 | LSB |
| Full-scale error Note | $E_{FS}$ | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±4.5 | LSB |
| Integral linearity error Note | ILE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | LSB |
| Differential linearity error Note | DLE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.5 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $AV_{REFP}$ | V |

**Note** Excludes quantization error (±1/2 LSB).

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

**(2) When reference voltage (+) = $AV_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = $AV_{SS}$ (ADREFM = 0), conversion target: ANI0 to ANI6**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{DD}$, Reference voltage (-) = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| Overall error Note | AINL | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±7.5 | LSB |
| Conversion time | $t_{CONV}$ | ADTYP = 0,<br>12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | 3.375 | | | µs |
| Zero-scale error Note | $E_{ZS}$ | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±6.0 | LSB |
| Full-scale error Note | $E_{FS}$ | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±6.0 | LSB |
| Integral linearity error Note | ILE | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | LSB |
| Differential linearity error Note | DLE | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $AV_{DD}$ | V |

**Note** Excludes quantization error (±1/2 LSB).

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

**(3) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), conversion target ANI16 to ANI21, internal reference voltage, temperature sensor output voltage**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| Overall error Note 1 | AINL | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | ADTYP = 0, 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 4.125 | | | µs |
| Zero-scale error Note 1 | $E_{ZS}$ | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | LSB |
| Full-scale error Note 1 | $E_{FS}$ | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | LSB |
| Integral linearity error Note 1 | ILE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | LSB |
| Differential linearity error Note 1 | DLE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage (2.4 V ≤ $V_{DD}$ ≤ 3.6 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 2 | | | |
| | | Temperature sensor output voltage (2.4 V ≤ $V_{DD}$ ≤ 3.6 V, HS (high-speed main) mode) | | $V_{TMP25}$ Note 2 | | | |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** Refer to **3.6.2 Temperature sensor, internal reference voltage output characteristics**.

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

**(4) When reference voltage (+) = $AV_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = $AV_{SS}$ (ADREFM = 0), conversion target: ANI16 to ANI21, internal reference voltage, temperature sensor output voltage**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{DD}$, Reference voltage (-) = $AV_{SS}$ = 0)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| Overall error Note 1 | AINL | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±8.5 | LSB |
| Conversion time | $t_{CONV}$ | ADTYP = 0,<br>12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | 4.125 | | | μs |
| Zero-scale error Note 1 | $E_{ZS}$ | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±8.0 | LSB |
| Full-scale error Note 1 | $E_{FS}$ | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±8.0 | LSB |
| Integral linearity error Note 1 | ILE | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.5 | LSB |
| Differential linearity error Note 1 | DLE | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.5 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $AV_{DD}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 3.6 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 2 | | | |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 3.6 V, HS (high-speed main) mode) | | $V_{TMP25}$ Note 2 | | | |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** Refer to **3.6.2 Temperature sensor, internal reference voltage output characteristics**.

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

**(5) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVSS (ADREFM = 0), conversion target: ANI0 to ANI6, ANI16 to ANI21**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, 2.4 V ≤ $V_{DD}$, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = internal reference voltage, Reference voltage (-) = $AV_{SS}$ = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | bit |
| Conversion time | tCONV | 8-bit resolution | 16.0 | | | µs |
| Zero-scale error Note | EZS | 8-bit resolution | | | ±4.0 | LSB |
| Integral linearity error Note | ILE | 8-bit resolution | | | ±2.0 | LSB |
| Differential linearity error Note | DLE | 8-bit resolution | | | ±2.5 | LSB |
| Reference voltage (+) | $AV_{REF(+)}$ | = Internal reference voltage ($V_{BGR}$) | 1.38 | 1.45 | 1.5 | V |
| Analog input voltage | VAIN | | 0 | | $V_{BGR}$ | V |

**Note** Excludes quantization error (±1/2 LSB).

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

## 3.6.2 Temperature sensor, internal reference voltage output characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V (HS (high-speed main) mode))**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor output voltage that depends on the temperature | | -3.6 | | mV/°C |
| Operation stabilization wait time | tAMP | | 10 | | | µs |

## 3.6.3 D/A converter characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | | 8 | bit |
| Overall error | AINL | Rload = 4 MΩ | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | | ±2.5 | LSB |
| | | Rload = 8 MΩ | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | | ±2.5 | LSB |
| Settling time | tSET | Cload = 20 pF | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 3 | µs |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 6 | µs |

## 3.6.4 Comparator

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage range | Ivref | | | 0 | | $V_{DD}$ - 1.4 | V |
| | Ivcmp | | | -0.3 | | $V_{DD}$ + 0.3 | V |
| Output delay | td | $V_{DD}$ = 3.0 V<br>Input slew rate > 50 mV/μs | High-speed comparator mode, standard mode | | | 1.2 | μs |
| | | | High-speed comparator mode, window mode | | | 2.0 | μs |
| | | | Low-speed comparator mode, standard mode | | 3 | 5.0 | μs |
| High-electric-potential judgment voltage | VTW+ | High-speed comparator mode, window mode | | | 0.76 $V_{DD}$ | | V |
| Low-electric-potential judgment voltage | VTW- | High-speed comparator mode, window mode | | | 0.24 $V_{DD}$ | | V |
| Operation stabilization wait time | $t_{CMP}$ | | | 100 | | | μs |
| Internal reference voltage Note | $V_{BGR}$ | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, HS (high-speed main) mode | | 1.38 | 1.45 | 1.50 | V |

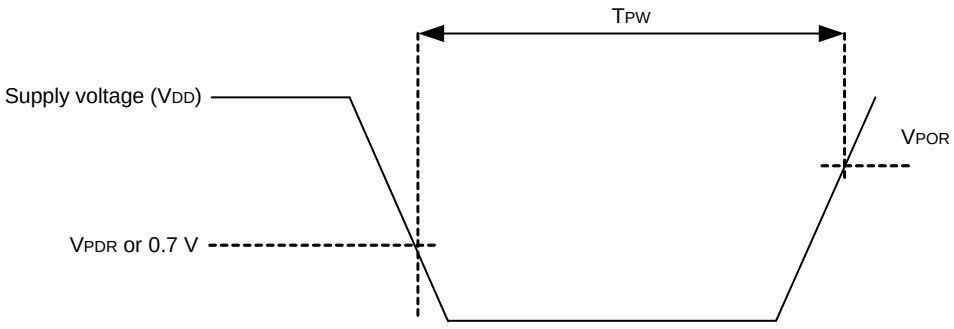
**Note** Not usable in sub-clock operation or STOP mode.

## 3.6.5 POR circuit characteristics

**($T_A$ = -40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Power supply rise time | 1.45 | 1.51 | 1.57 | V |
| | $V_{PDR}$ | Power supply fall time Note | 1.44 | 1.50 | 1.56 | V |
| Minimum pulse width | $T_{PW}$ | | 300 | | | μs |

**Note** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 3.6.6 LVD circuit characteristics

**($T_A$ = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq 3.6$ V $\leq V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | Supply voltage level | $V_{LVD2}$ | Power supply rise time | 3.01 | 3.13 | 3.25 | V |
| | | | Power supply fall time | 2.94 | 3.06 | 3.18 | V |
| | | VLVD3 | Power supply rise time | 2.90 | 3.02 | 3.14 | V |
| | | | Power supply fall time | 2.85 | 2.96 | 3.07 | V |
| | | $V_{LVD4}$ | Power supply rise time | 2.81 | 2.92 | 3.03 | V |
| | | | Power supply fall time | 2.75 | 2.86 | 2.97 | V |
| | | $V_{LVD5}$ | Power supply rise time | 2.71 | 2.81 | 2.92 | V |
| | | | Power supply fall time | 2.64 | 2.75 | 2.86 | V |
| | | $V_{LVD6}$ | Power supply rise time | 2.61 | 2.71 | 2.81 | V |
| | | | Power supply fall time | 2.55 | 2.65 | 2.75 | V |
| | | $V_{LVD7}$ | Power supply rise time | 2.51 | 2.61 | 2.71 | V |
| | | | Power supply fall time | 2.45 | 2.55 | 2.65 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | μs |
| Detection delay time | | | | | | 300 | μs |

**Caution Set the detection voltage ($V_{LVD}$) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.**
**HS (high-speed main) mode: $V_{DD}$ = 2.7 to 3.6 V at 1 MHz to 24 MHz**
**$V_{DD}$ = 2.4 to 3.6 V at 1 MHz to 16 MHz**

**LVD Detection Voltage of Interrupt & Reset Mode**

**($T_A$ = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq$ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDD0}$ | $V_{POC0}$, $V_{POC1}$, $V_{POC2}$ = 0, 1, 1, falling reset voltage: 2.7 V | | | 2.64 | 2.75 | 2.86 | V |
| | $V_{LVDD1}$ | | LVIS0, LVIS1 = 1, 0 | Rising release reset voltage | 2.81 | 2.92 | 3.03 | V |
| | | | | Falling interrupt voltage | 2.75 | 2.86 | 2.97 | V |
| | $V_{LVDD2}$ | | LVIS0, LVIS1 = 0, 1 | Rising release reset voltage | 2.90 | 3.02 | 3.14 | V |
| | | | | Falling interrupt voltage | 2.85 | 2.96 | 3.07 | V |

## 3.7 Power supply voltage rising slope characteristics

**($T_A$ = -40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Power supply voltage rising slope | $SV_{DD}$ | | | 54 | V/ms |

**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 3.4 AC Characteristics.**

## 3.8 LCD Characteristics

### 3.8.1 Resistance division method

**(1) Static display mode**

**($T_A$ = -40 to +105°C, $V_{L4}$ (MIN.) ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| LCD drive voltage | $V_{L4}$ | | 2.0 | | $V_{DD}$ | V |

**(2) 1/2 bias method, 1/4 bias method**

**($T_A$ = -40 to +105°C, $V_{L4}$ (MIN.) ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| LCD drive voltage | $V_{L4}$ | | 2.7 | | $V_{DD}$ | V |

**(3) 1/3 bias method**

**($T_A$ = -40 to +105°C, $V_{L4}$ (MIN.) ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| LCD drive voltage | $V_{L4}$ | | 2.5 | | $V_{DD}$ | V |

## 3.8.2 Internal voltage boosting method

**(1) 1/3 bias method**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| LCD output voltage variation range | $V_{L1}$ | C1 to C4 Note 1 = 0.47 μF Note 2 | VLCD = 04H | 0.90 | 1.00 | 1.08 | V |
| | | | VLCD = 05H | 0.95 | 1.05 | 1.13 | V |
| | | | VLCD = 06H | 1.00 | 1.10 | 1.18 | V |
| | | | VLCD = 07H | 1.05 | 1.15 | 1.23 | V |
| | | | VLCD = 08H | 1.10 | 1.20 | 1.28 | V |
| | | | VLCD = 09H | 1.15 | 1.25 | 1.33 | V |
| | | | VLCD = 0AH | 1.20 | 1.30 | 1.38 | V |
| | | | VLCD = 0BH | 1.25 | 1.35 | 1.43 | V |
| | | | VLCD = 0CH | 1.30 | 1.40 | 1.48 | V |
| | | | VLCD = 0DH | 1.35 | 1.45 | 1.53 | V |
| | | | VLCD = 0EH | 1.40 | 1.50 | 1.58 | V |
| | | | VLCD = 0FH | 1.45 | 1.55 | 1.63 | V |
| | | | VLCD = 10H | 1.50 | 1.60 | 1.68 | V |
| | | | VLCD = 11H | 1.55 | 1.65 | 1.73 | V |
| | | | VLCD = 12H | 1.60 | 1.70 | 1.78 | V |
| | | | VLCD = 13H | 1.65 | 1.75 | 1.83 | V |
| Doubler output voltage | $V_{L2}$ | C1 to C4 Note 1 = 0.47 μF | | 2 $V_{L1}$ - 0.1 | 2 $V_{L1}$ | 2 $V_{L1}$ | V |
| Tripler output voltage | $V_{L3}$ | C1 to C4 Note 1 = 0.47 μF | | 3 $V_{L1}$ - 0.15 | 3 $V_{L1}$ | 3 $V_{L1}$ | V |
| Reference voltage setup time Note 2 | $t_{VWAIT1}$ | | | 5 | | | ms |
| Voltage boost wait time Note 3 | $t_{VWAIT2}$ | C1 to C4 Note 1 = 0.47μF | | 500 | | | ms |

**Note 1.** This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between $V_{L1}$ and GND
C3: A capacitor connected between $V_{L2}$ and GND
C4: A capacitor connected between $V_{L4}$ and GND
C1 = C2 = C3 = C4 = 0.47 μF±30%

**Note 2.** This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

**Note 3.** This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

**(2) 1/4 bias method**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| LCD output voltage variation range | $V_{L1}$ | C1 to C4 Note 1 = 0.47 μF Note 2 | VLCD = 04H | 0.90 | 1.00 | 1.08 | V |
| | | | VLCD = 05H | 0.95 | 1.05 | 1.13 | V |
| | | | VLCD = 06H | 1.00 | 1.10 | 1.18 | V |
| | | | VLCD = 07H | 1.05 | 1.15 | 1.23 | V |
| | | | VLCD = 08H | 1.10 | 1.20 | 1.28 | V |
| | | | VLCD = 09H | 1.15 | 1.25 | 1.33 | V |
| | | | VLCD = 0AH | 1.20 | 1.30 | 1.38 | V |
| Doubler output voltage | $V_{L2}$ | C1 to C4 Note 1 = 0.47 μF | | 2 $V_{L1}$ - 0.08 | 2 $V_{L1}$ | 2 $V_{L1}$ | V |
| Tripler output voltage | $V_{L3}$ | C1 to C4 Note 1 = 0.47 μF | | 3 $V_{L1}$ - 0.12 | 3 $V_{L1}$ | 3 $V_{L1}$ | V |
| Quadruply output voltage | $V_{L4}$ | C1 to C5 Note 1 = 0.47 μF | | 4 $V_{L1}$ - 0.16 | 4 $V_{L1}$ | 4 $V_{L1}$ | V |
| Reference voltage setup time Note 2 | $t_{VWAIT1}$ | | | 5 | | | ms |
| Voltage boost wait time Note 3 | $t_{VWAIT2}$ | C1 to C5 Note 1 = 0.47μF | | 500 | | | ms |

**Note 1.** This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between $V_{L1}$ and GND
C3: A capacitor connected between $V_{L2}$ and GND
C4: A capacitor connected between $V_{L3}$ and GND
C5: A capacitor connected between $V_{L4}$ and GND
C1 = C2 = C3 = C4 = 0.47 μF±30%

**Note 2.** This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

**Note 3.** This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

### 3.8.3 Capacitor split method

**(1) 1/3 bias method**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $V_{L4}$ voltage | $V_{L4}$ | C1 to C4 = 0.47 μF Note 2 | | $V_{DD}$ | | V |
| $V_{L2}$ voltage | $V_{L2}$ | C1 to C4 = 0.47 μF Note 2 | 2/3 $V_{L4}$ - 0.07 | 2/3 $V_{L4}$ | 2/3 $V_{L4}$ + 0.07 | V |
| $V_{L1}$ voltage | $V_{L1}$ | C1 to C4 = 0.47 μF Note 2 | 1/3 $V_{L4}$ - 0.08 | 1/3 $V_{L4}$ | 1/3 $V_{L4}$ + 0.08 | V |
| Capacitor split wait time Note 1 | $t_{VWAIT}$ | | 100 | | | ms |

**Note 1.** This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

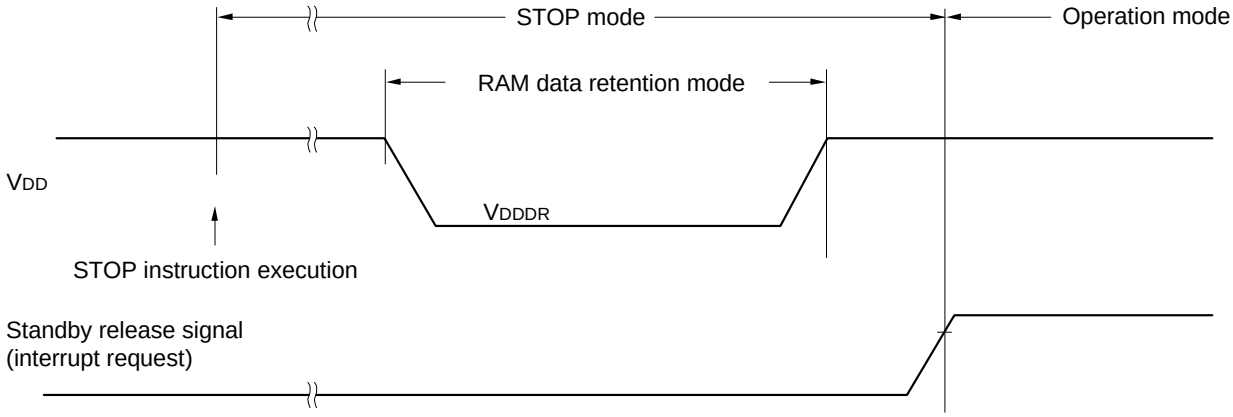
**Note 2.** This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between $V_{L1}$ and GND
C3: A capacitor connected between $V_{L2}$ and GND
C4: A capacitor connected between $V_{L4}$ and GND
C1 = C2 = C3 = C4 = 0.47 μF±30%

## 3.9 RAM Data Retention Characteristics

**($T_A$ = -40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.44 Note | | 3.6 | V |

**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



## 3.10 Flash Memory Programming Characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CPU/peripheral hardware clock frequency | $f_{CLK}$ | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | 1 | | 24 | MHz |
| Number of code flash rewrites Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years $T_A$ = 85°C Note 4 | 1,000 | | | Times |
| Number of data flash rewrites Notes 1, 2, 3 | | Retained for 1 year $T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years $T_A$ = 85°C Note 4 | 100,000 | | | |
| | | Retained for 20 years $T_A$ = 85°C Note 4 | 10,000 | | | |

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**Note 2.** When using flash memory programmer and Renesas Electronics self programming library

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

**Note 4.** This temperature is the average value at which data are retained.

## 3.11 Dedicated Flash Memory Programmer Communication (UART)

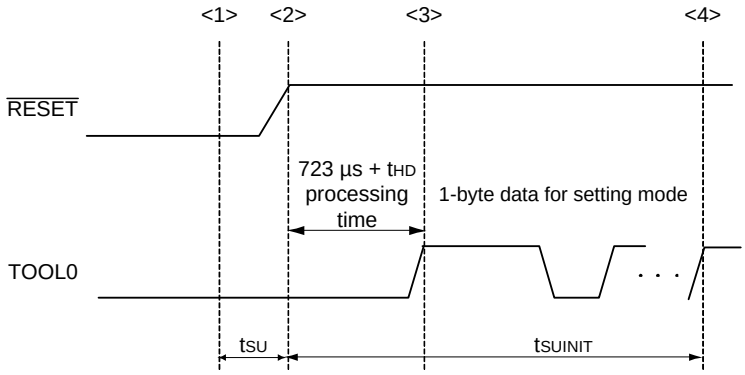
**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 3.12 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| How long from when an external reset ends until the initial communication settings are specified | $t_{SUINIT}$ | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until an external reset ends | $t_{SU}$ | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| Time to hold the TOOL0 pin at the low level after an external reset is released (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must end before the external reset ends. | 1 | | | ms |




<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.
$t_{SU}$: How long from when the TOOL0 pin is placed at the low level until a external reset ends
$t_{HD}$: How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)

# 4. PACKAGE DRAWINGS

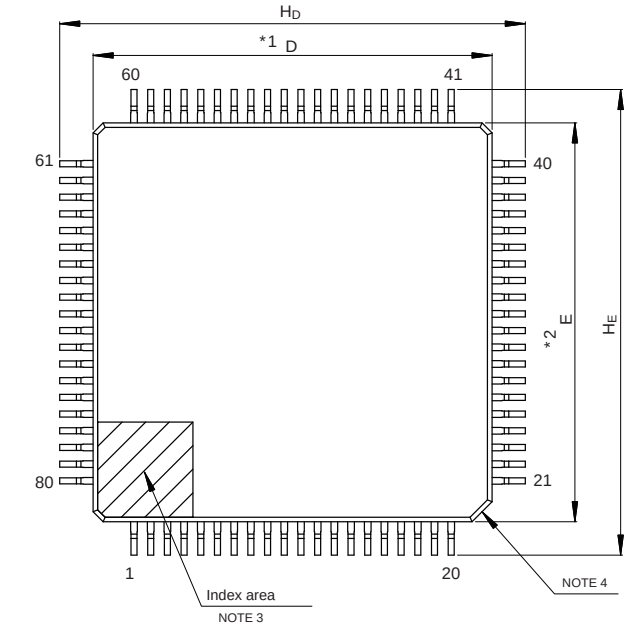
## 4.1 80-pin products

R5F110MEAFB, R5F110MFAFB, R5F110MGAFB, R5F110MHAFB, R5F110MJAFB
R5F111MEAFB, R5F111MFAFB, R5F111MGAFB, R5F111MHAFB, R5F111MJAFB
R5F110MEGFB, R5F110MFGFB, R5F110MGGFB, R5F110MHGFB, R5F110MJGFB
R5F111MEGFB, R5F111MFGFB, R5F111MGGFB, R5F111MHGFB, R5F111MJGFB

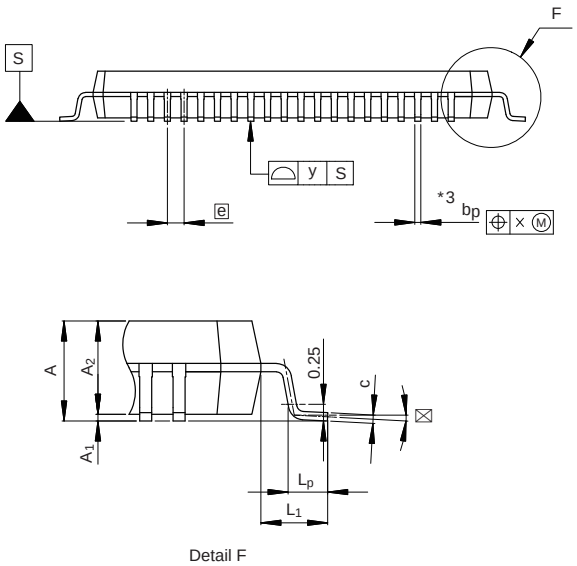
<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP80-12x12-0.50 | PLQP0080KB-B | — | 0.5 |

Unit: mm



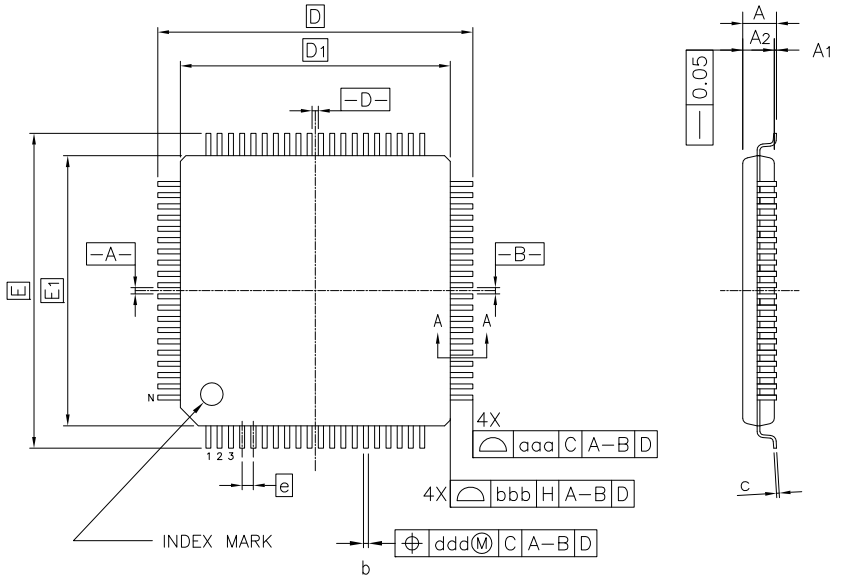

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

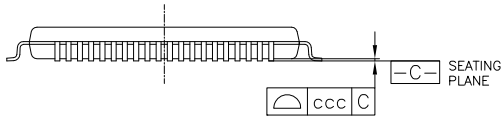


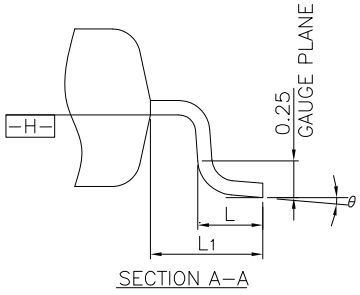

Detail F

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 11.9 | 12.0 | 12.1 |
| E | 11.9 | 12.0 | 12.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 13.8 | 14.0 | 14.2 |
| $H_E$ | 13.8 | 14.0 | 14.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-LFQFP80-12x12-0.50 | PLQP0080KJ-A | 0.49 |



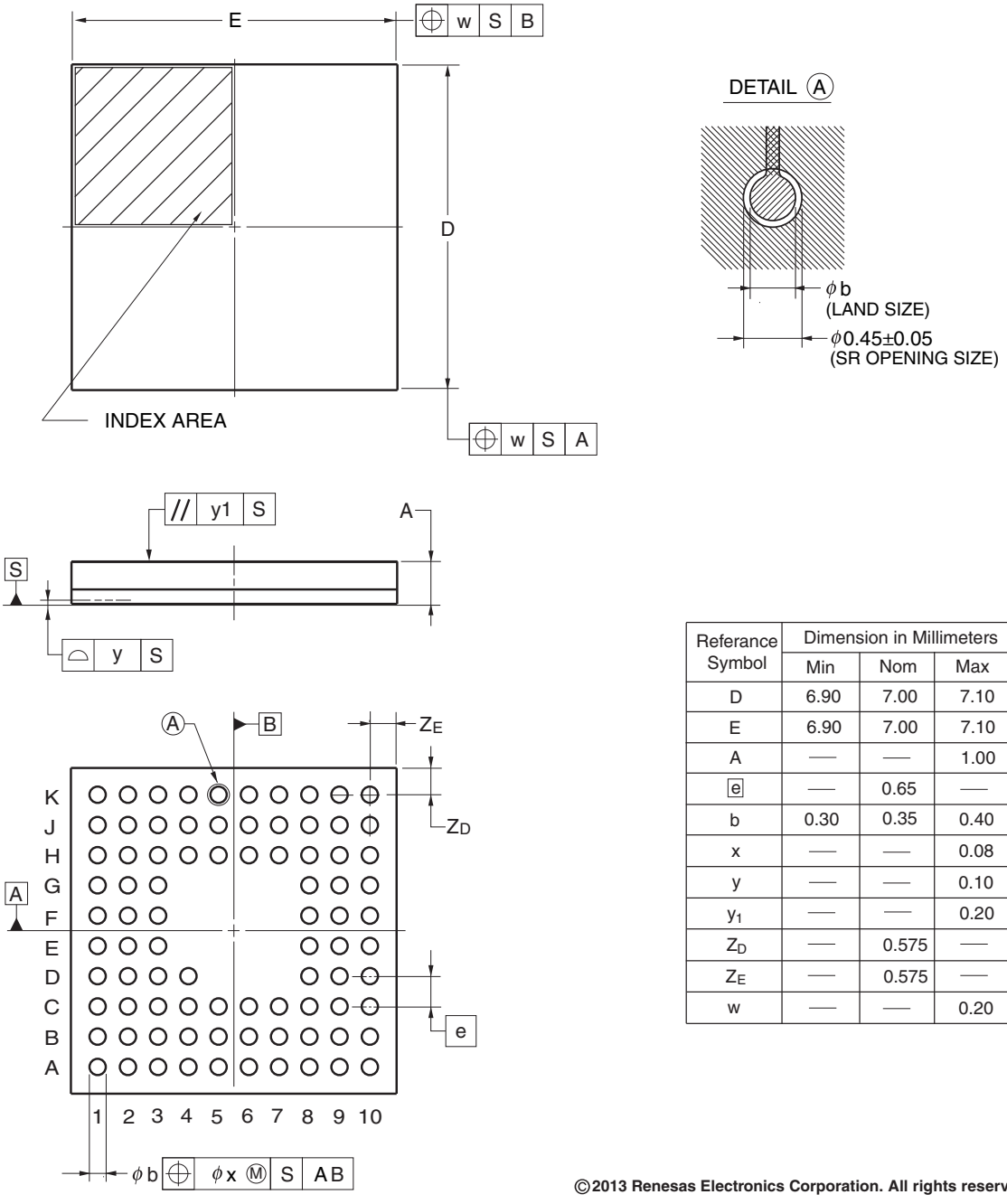




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | – | – | 1.60 |
| $A_1$ | 0.05 | – | 0.15 |
| $A_2$ | 1.35 | 1.40 | 1.45 |
| D | – | 14.00 | – |
| $D_1$ | – | 12.00 | – |
| E | – | 14.00 | – |
| $E_1$ | – | 12.00 | – |
| N | – | 80 | – |
| e | – | 0.50 | – |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | – | 0.20 |
| θ | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 |
| $L_1$ | – | 1.00 | – |
| aaa | – | – | 0.20 |
| bbb | – | – | 0.20 |
| ccc | – | – | 0.08 |
| ddd | – | – | 0.08 |

## 4.2 85-pin products

R5F110NEALA, R5F110NFALA, R5F110NGALA, R5F110NHALA, R5F110NJALA
R5F111NEALA, R5F111NFALA, R5F111NGALA, R5F111NHALA, R5F111NJALA
R5F110NEGLA, R5F110NFGLA, R5F110NGGLA, R5F110NHGLA, R5F110NJGLA
R5F111NEGLA, R5F111NFGLA, R5F111NGGLA, R5F111NHGLA, R5F111NJGLA

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P-VFLGA85-7x7-0.65 | PVLG0085JA-A | P85FC-65-BN4 | 0.1 |



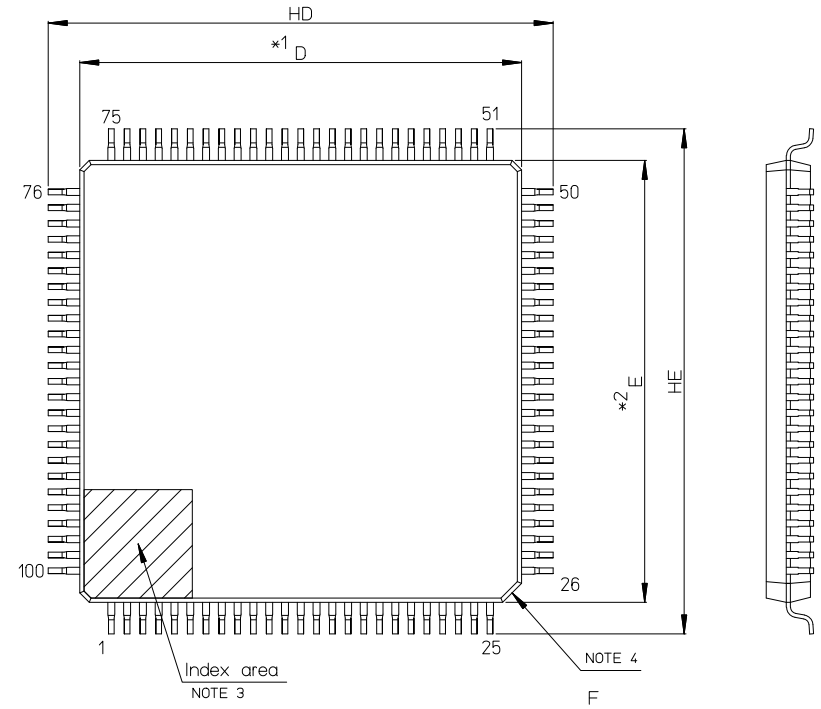

| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 |
| A | — | — | 1.00 |
| e | — | 0.65 | — |
| b | 0.30 | 0.35 | 0.40 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $y_1$ | — | — | 0.20 |
| $Z_D$ | — | 0.575 | — |
| $Z_E$ | — | 0.575 | — |
| w | — | — | 0.20 |

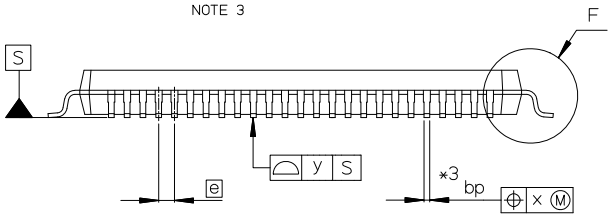
## 4.3 100-pin products

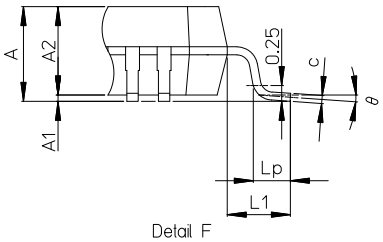
R5F110PEAFB, R5F110PFAFB, R5F110PGAFB, R5F110PHAFB, R5F110PJAFB
R5F111PEAFB, R5F111PFAFB, R5F111PGAFB, R5F111PHAFB, R5F111PJAFB
R5F110PEGFB, R5F110PFGFB, R5F110PGGFB, R5F110PHGFB, R5F110PJGFB
R5F111PEGFB, R5F111PFGFB, R5F111PGGFB, R5F111PHGFB, R5F111PJGFB

<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-B | —— | 0.6g |



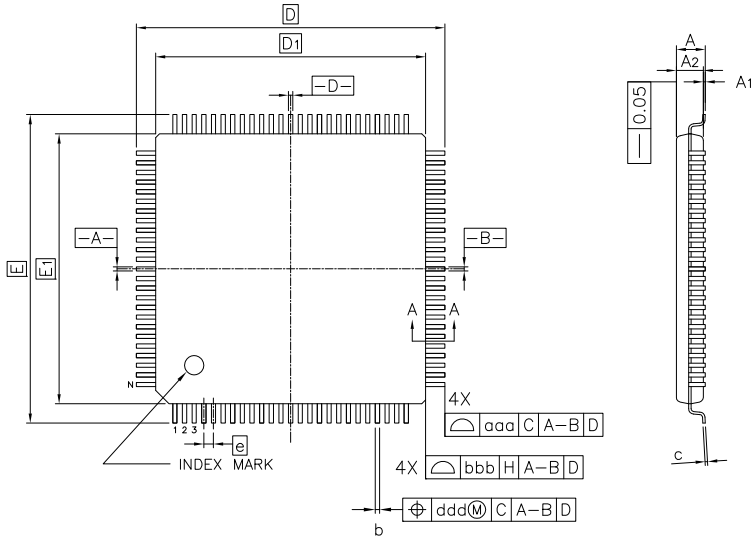



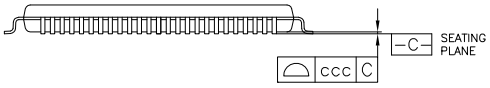



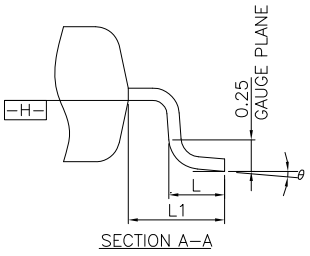

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| A2 | —— | 1.4 | —— |
| HD | 15.8 | 16.0 | 16.2 |
| HE | 15.8 | 16.0 | 16.2 |
| A | —— | —— | 1.7 |
| A1 | 0.05 | —— | 0.15 |
| bp | 0.15 | 0.20 | 0.27 |
| c | 0.09 | —— | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | —— | 0.5 | —— |
| x | —— | —— | 0.08 |
| y | —— | —— | 0.08 |
| Lp | 0.45 | 0.6 | 0.75 |
| L1 | —— | 1.0 | —— |

| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KP-A | 0.67 |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | – | – | 1.60 |
| $A_1$ | 0.05 | – | 0.15 |
| $A_2$ | 1.35 | 1.40 | 1.45 |
| D | – | 16.00 | – |
| $D_1$ | – | 14.00 | – |
| E | – | 16.00 | – |
| $E_1$ | – | 14.00 | – |
| N | – | 100 | – |
| e | – | 0.50 | – |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | – | 0.20 |
| θ | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 |
| $L_1$ | – | 1.00 | – |
| aaa | – | – | 0.20 |
| bbb | – | – | 0.20 |
| ccc | – | – | 0.08 |
| ddd | – | – | 0.08 |

| REVISION HISTORY | RL78/L1C Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.01 | Oct 15, 2012 | — | First Edition issued |
| 1.00 | Nov 18, 2013 | 1, 2 | Modification of 1.1 Features |
| | | 3, 4 | Modification of 1.2 Ordering Information |
| | | 5 to 8 | Modification of package type in 1.3 Pin Configuration (Top View) |
| | | 14 to 17 | Modification of vectored interrupt sources in 1.6 Outline of Functions |
| | | 14 to 17 | Modification of operating ambient temperature in 1.6 Outline of Functions |
| | | 19 to 21 | Modification of description in tables in 2.1 Absolute Maximum Ratings |
| | | 22, 23 | Modification of description in 2.2 Oscillator Characteristics |
| | | 25 | Modification of low-level output current in 2.3.1 Pin characteristics |
| | | 26 | Modification of error of high-level input voltage conditions in 2.3.1 Pin characteristics |
| | | 26 | Modification of error of low-level input voltage conditions in 2.3.1 Pin characteristics |
| | | 27 | Modification of low-level output voltage in 2.3.1 Pin characteristics |
| | | 28 | Modification of error of internal pull-up resistor conditions in 2.3.1 Pin characteristics |
| | | 29 to 34 | Modification of 2.3.2 Supply current characteristics |
| | | 35, 36 | Modification of 2.4 AC Characteristics |
| | | 37, 38 | Addition of minimum instruction execution time during main system clock operation |
| | | 41 to 63 | Addition of LS mode and LV mode characteristics in 2.5.1 Serial array unit |
| | | 64 to 66 | Addition of LS mode and LV mode characteristics in 2.5.2 Serial interface IICA |
| | | 67, 68 | Modification of conditions in 2.5.3 USB |
| | | 69 | Addition of (3) BC option standard in 2.5.3 USB |
| | | 70 to 75 | Addition of characteristics about conversion of internal reference voltage and temperature sensor in 2.6.1 A/D converter characteristics |
| | | 76 | Addition of characteristic in 2.6.4 Comparator |
| | | 76 | Deletion of detection delay in 2.6.5 POR circuit characteristics |
| | | 78 | Modification of 2.7 Power supply voltage rising slope characteristics |
| | | 79 to 82 | Modification of 2.8 LCD Characteristics |
| | | 83 | Modification of 2.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics |
| | | 83 | Modification of 2.10 Flash Memory Programming Characteristics |
| | | 84 | Addition of 2.12 Timing Specs for Switching Modes |
| | | 85 to 144 | Addition of 3. ELECTRICAL SPECIFICATIONS (G: $T_A$ = -40 to +105°C) |
| 2.00 | Feb 21, 2014 | All | Addition of 85-pin product information |
| | | All | Modification from 80-pin to 80/85-pin |
| | | All | Modification from x = M, P to x = M, N, P |
| | | All | Modification from high-accuracy real-time clock to real-time clock 2 |
| | | All | Modification from RTC to RTC2 |
| | | 1 | Modification of 1.1 Features |
| | | 3 | Modification of 1.2 Ordering Information |

| REVISION HISTORY | RL78/L1C Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 2.00 | Feb 21, 2014 | 4 | Modification of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/L1C |
| | | 69 | Modification of (1) Electrical specifications in 2.5.3 USB |
| | | 82 | Modification of note 1 in (1) 1/3 bias method in 2.8.2 Internal voltage boosting method |
| | | 130 | Modification of (1) Electrical specifications in 3.5.3 USB |
| | | 142 | Modification of note 1 in (1) 1/3 bias method in 3.8.2 Internal voltage boosting method |
| 2.10 | Aug 12, 2016 | 5 | Addition of product name (RL78/L1C) and description (Top View) in 1.3.1 80-pin products (with USB) |
| | | 6 | Addition of product name (RL78/L1C) and description (Top View) in 1.3.2 80-pin products (without USB) |
| | | 9 | Addition of product name (RL78/L1C) and description (Top View) in 1.3.5 100-pin products (with USB) |
| | | 10 | Addition of product name (RL78/L1C) and description (Top View) in 1.3.6 100-pin products (without USB) |
| | | 17, 19 | Modification of 1.6 Outline of Functions |
| | | 23 | Modification of description in Absolute Maximum Ratings ($T_A$ = 25°C) |
| | | 26, 27 | Modification of description in 2.3.1 Pin characteristics |
| | | 39, 40 | Modification of the graph for Minimum Instruction Execution Time during Main System Clock Operation |
| | | 72 | Modification of conditions in (1) of 2.6.1 A/D converter characteristics |
| | | 85 | Modification of the title and note in 2.9 RAM Data Retention Characteristics |
| | | 85 | Modification of conditions in 2.10 Flash Memory Programming Characteristics |
| | | 87 | Modification of description in 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A$ = -40 to +105 °C) |
| | | 88, 90 | Modification of description in Absolute Maximum Ratings ($T_A$ = 25°C) |
| | | 93, 94, 96 | Modification of description in 3.3.1 Pin characteristics |
| | | 106 | Modification of the graph for Minimum Instruction Execution Time during Main System Clock Operation |
| | | 144 | Modification of the title and note in 3.9 RAM Data Retention Characteristics |
| | | 145 | Modification of conditions and addition of note 4 in 3.10 Flash Memory Programming Characteristics |
| 2.20 | Dec 28, 2017 | 13 | Modification of figure in 1.5.2 80/85-pin products (without USB) |
| | | 17, 19 | Modification of tables in 1.6 Outline of Functions |
| | | 26, 27 | Modification of table and note 3 in 2.3.1 Pin characteristics |
| | | 85 | Modification of figure in 2.12 Timing of Entry to Flash Memory Programming Modes |
| | | 89 | Modification of table in 3.1 Absolute Maximum Ratings |
| | | 92, 93 | Modification of table and note 3 in 3.3.1 Pin characteristics |
| | | 144 | Modification of figure in 3.12 Timing of Entry to Flash Memory Programming Modes |

| REVISION HISTORY | RL78/L1C Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 2.21 | Nov 30, 2022 | All | The module name for CSI was changed to Simplified SPI(CSI) |
| | | All | “wait” for IIC was modified to “clock stretch” |
| | | 3 | Modification of description in two tables in 1.2 Ordering Information |
| | | 4 | Modification of packaging specification in Figure1-1 |
| | | 146 | Addition of package drawing in 4.1 80-pin Package |
| | | 149 | Addition of package drawing in 4.3 100-pin Package |
| 2.30 | Mar 20, 2023 | 32 | Modification of notes in 2.3.2 Supply current characteristics ($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (1/2) |
| | | 34 | Modification of notes and remark in 2.3.2 Supply current characteristics ($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (2/2) |
| | | 98 | Modification of notes in 3.3.2 Supply current characteristics ($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (1/2) |
| | | 100 | Modification of notes and remark in 3.3.2 Supply current characteristics ($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V) (2/2) |
| | | 145 | Modification of package drawing of PLQP0080KB-B in 4.1 80-pin products |
| | | 148 | Modification of package drawing of PLQP0100KB-B in 4.3 100-pin products |

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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