NEC

Preliminary User's Manual

78K0S/KU1+, 78K0S/KY1+

8-Bit Single-Chip Microcontrollers

μPD78F9200 μPD78F9210
μPD78F9201 μPD78F9211
μPD78F9202 μPD78F9212

Document No. U16994EJ2V0UD00 (2nd edition)
Date Published February 2005 NS CP(K)

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Windows and Windows NT are either registered trademarks or trademarks of Microsoft Corporation in the United States and/or other countries.

PC/AT is a trademark of International Business Machines Corporation.

HP9000 series 700 and HP-UX are trademarks of Hewlett-Packard Company.

SPARCstation is a trademark of SPARC International, Inc.

Solaris and SunOS are trademarks of Sun Microsystems, Inc.

SuperFlash® is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, inc.

- **The information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion, may withdraw the product prior to its production.**
- **Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of a customer's equipment shall be done under the full responsibility of the customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific". The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics products depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.

  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.

  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.

(Note)

(1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.

(2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).

M5D 02. 11-1

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC Electronics product in your application, please contact the NEC Electronics office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

[GLOBAL SUPPORT]
http://www.necel.com/en/support/support.html

NEC Electronics America, Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782

NEC Electronics (Europe) GmbH
Duesseldorf, Germany
Tel: 0211-65030

- **Sucursal en España**
  Madrid, Spain
  Tel: 091-504 27 87
- **Succursale Française**
  Vélizy-Villacoublay, France
  Tel: 01-30-67 58 00
- **Filiale Italiana**
  Milano, Italy
  Tel: 02-66 75 41
- **Branch The Netherlands**
  Eindhoven, The Netherlands
  Tel: 040-244 58 45
- **Tyskland Filial**
  Taeby, Sweden
  Tel: 08-63 80 820
- **United Kingdom Branch**
  Milton Keynes, UK
  Tel: 01908-691-133

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-558-3737

NEC Electronics Shanghai Ltd.
Shanghai, P.R. China
Tel: 021-5888-5400

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377

NEC Electronics Singapore Pte. Ltd.
Novena Square, Singapore
Tel: 6253-8311

J04.1

INTRODUCTION

Target Readers

This manual is intended for user engineers who wish to understand the functions of the 78K0S/KU1+ and 78K0S/KY1+ in order to design and develop its application systems and programs.

The target devices are the following subseries products.

- 78K0S/KU1+: μPD78F9200, 78F9201, 78F9202
- 78K0S/KY1+: μPD78F9210, 78F9211, 78F9212

Purpose

This manual is intended to give users on understanding of the functions described in the **Organization** below.

Organization

Two manuals are available for 78K0S/KU1+ and 78K0S/KY1+: this manual and the Instruction Manual (common to the 78K/0S Series).

78K0S/KU1+, 78K0S/KY1+ User's Manual	78K/0S Series Instructions User's Manual
• Pin functions • Internal block functions • Interrupts • Other internal peripheral functions • Electrical specifications (target)	• CPU function • Instruction set • Instruction description

How to Use This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

◊ To understand the overall functions of the 78K0S/KU1+ and 78K0S/KY1+
  → Read this manual in the order of the **CONTENTS**. The mark ★ shows major revised points.

◊ How to read register formats
  → For a bit number enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0S, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0S.

◊ To learn the detailed functions of a register whose register name is known
  → See **APPENDIX B REGISTER INDEX**.

◊ To learn the details of the instruction functions of the 78K/0S Series
  → Refer to **78K/0S Series Instructions User's Manual (U11047E)** separately available.

◊ To learn the electrical specifications (target) of the 78K0S/KU1+ and 78K0S/KY1+
  → See **CHAPTER 18 ELECTRICAL SPECIFICATIONS (TARGET VALUES)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{\times\times\times}$ (overscore over pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representation:	Binary ... ×××× or ××××B
	Decimal ... ××××
	Hexadecimal ... ××××H

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
78K0S/KU1+, 78K0S/KY1+ User's Manual	This manual
78K/0S Series Instructions User's Manual	U11047E

★ **Documents Related to Development Software Tools (User's Manuals)**

Document Name		Document No.
RA78K0S Assembler Package	Operation	U16656E
	Language	U14877E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U16654E
	Language	U14872E
ID78K0S-NS Ver. 2.52 Integrated Debugger	Operation	U16584E
ID78K0S-QB Ver. 2.81 Integrated Debugger	Operation	U17287E
PM plus Ver.5.20		U16934E

Documents Related to Development Hardware Tools (User's Manuals)

Document Name	Document No.
IE-78K0S-NS In-Circuit Emulator	U13549E
IE-78K0S-NS-A In-Circuit Emulator	U15207E
★ QB-78K0SKX1MINI In-Circuit Emulator	U17272E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Flash Memory Writing

Document Name	Document No.
PG-FP4 Flash Memory Programmer User's Manual	U15260E
★ PG-FPL2 Flash Memory Programmer User's Manual	U17307E

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products and Packages -	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the "Semiconductor Device Mount Manual" website (http://www.necel.com/pkg/en/mount/index.html).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

CONTENTS

CHAPTER 1 OVERVIEW

1.1 Features

O Minimum instruction execution time selectable from high speed (0.2 μs) and low speed (3.2 μs) (with CPU clock of 10 MHz)

O General-purpose registers: 8 bits × 8 registers

O ROM and RAM capacities

Item / Part number	Program Memory (Flash Memory)	Memory (Internal High-Speed RAM)
μPD78F9200, 78F9210	1 KB	128 bytes
μPD78F9201, 78F9211	2 KB	
μPD78F9202, 78F9212	4 KB	

O On-chip power-on clear (POC) circuit and low voltage detector (LVI)

O On-chip watchdog timer (operable on internal low-speed Ring-OSC clock)

O I/O ports

- μPD78F9200, 78F9201, 78F9202: 6
- μPD78F9210, 78F9211, 78F9212: 14

O Timer: 3 channels

- 16-bit timer/event counter: 1 channel
- 8-bit timer: 1 channel
- Watchdog timer: 1 channel

O 10-bit resolution A/D converter: 4 channels

O Supply voltage: V_{DD} = 2.0 to 5.5 V[Note]

O Operating temperature range: T_A = −40 to +85°C

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

1.2 Application Fields

O Automotive electronics

- System control of body instrumentation system (such as power windows and keyless entry reception)
- Sub-microcontroller of control system

O Household appliances

- Electric toothbrushes
- Electric shavers

O Toys

O Industrial equipment

- Sensor and switch control
- Power tools

★ 1.3 Ordering Information

(1) 78K0S/KU1+

Part Number	Package	Quality Grade
μPD78F9200GR(T)-AND	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9200GR(T2)-AND	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9200GR(S)-AND	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9200GR(T)-AND-A	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9200GR(T2)-AND-A	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9200GR(S)-AND-A	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9201GR(T)-AND	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9201GR(T2)-AND	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9201GR(S)-AND	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9201GR(T)-AND-A	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9201GR(T2)-AND-A	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9201GR(S)-AND-A	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9202GR(T)-AND	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9202GR(T2)-AND	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9202GR(S)-AND	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9202GR(T)-AND-A	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9202GR(T2)-AND-A	8-pin plastic SOP (5.75mm (225))	Standard
μPD78F9202GR(S)-AND-A	8-pin plastic SOP (5.75mm (225))	Standard

Remark The μPD78F9200GR(xx)-AND-A, 78F9201GR(xx)-AND-A, and 78F9202GR(xx)-AND-A are lead-free products.
xx : T, T2, S

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The 78K0S/KU1+ standard grade products are further classified as follows.

(T), (T2): General management

(S): Management based on individual contract

(2) 78K0S/KY1+

Part Number	Package	Quality Grade
μPD78F9210GR(T)-JJG	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9210GR(T2)-JJG	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9210GR(S)-JJG	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9210GR(R)-JJG	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9210GR(T)-JJG-A	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9210GR(T2)-JJG-A	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9210GR(S)-JJG-A	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9210GR(R)-JJG-A	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9211GR(T)-JJG	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9211GR(T2)-JJG	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9211GR(S)-JJG	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9211GR(R)-JJG	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9211GR(T)-JJG-A	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9211GR(T2)-JJG-A	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9211GR(S)-JJG-A	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9211GR(R)-JJG-A	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9212GR(T)-JJG	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9212GR(T2)-JJG	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9212GR(S)-JJG	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9212GR(R)-JJG	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9212GR(T)-JJG-A	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9212GR(T2)-JJG-A	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9212GR(S)-JJG-A	16-pin plastic SSOP (5.72 mm (225))	Standard
μPD78F9212GR(R)-JJG-A	16-pin plastic SSOP (5.72 mm (225))	Standard

Remark The μPD78F9210GR(xx)-JJG-A, 78F9211GR(xx)-JJG-A, and 78F9212GR(xx)-JJG-A are lead-free products.
xx : T, T2, S, R

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

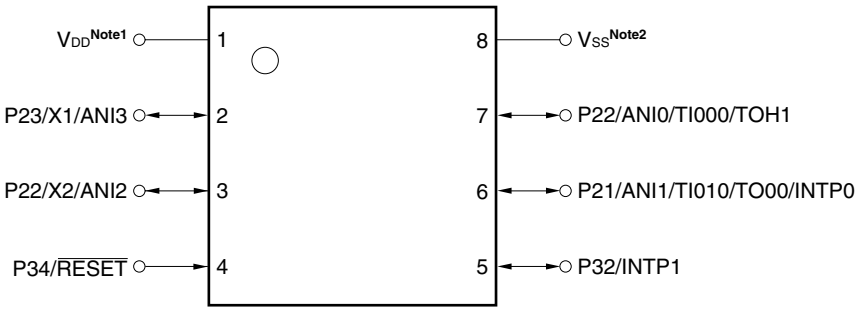
The 78K0S/KY1+ standard grade products are further classified as follows.

(T), (T2): General management
(S): Management based on individual contract
(R): Management for automotive accessories

1.4 Pin Configuration (Top View)

(1) 78K0S/KU1+

8-pin plastic SOP (5.72mm (225))



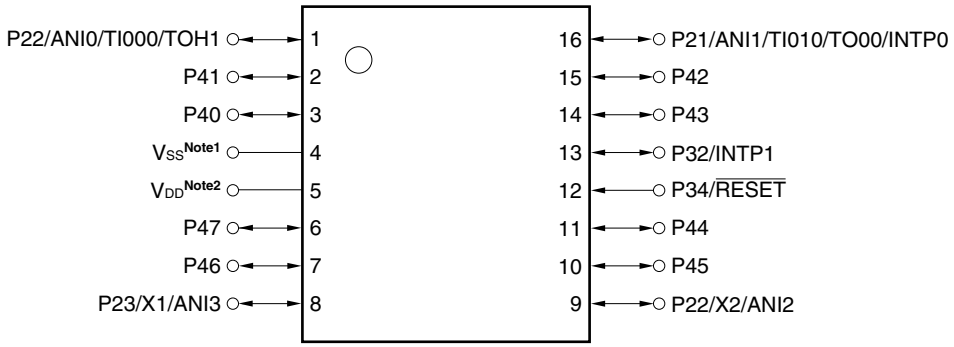
Notes 1. In the 78K0S/KU1+, V_{DD} functions alternately as the A/D converter reference voltage input. When using the A/D converter, stabilize V_{DD} at the supply voltage used (2.7 to 5.5 V).

2. In the 78K0S/KU1+, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

ANI0 to ANI3:	Analog input	TI000, TI010:	Timer input
INTP0, INTP1:	External interrupt input	TO00, TOH1:	Timer output
P20 to P23:	Port 2	V_{DD}:	Power supply
P30, P34:	Port 3	V_{SS}:	Ground
$\overline{\text{RESET}}$:	Reset	X1, X2:	Crystal oscillator (X1 input clock)

(2) 78K0S/KY1+

16-pin plastic SSOP (5.72 mm (225))



Notes 1. In the 78K0S/KY1+, V_{DD} functions alternately as the A/D converter reference voltage input. When using the A/D converter, stabilize V_{DD} at the supply voltage used (2.7 to 5.5 V).

2. In the 78K0S/KY1+, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

ANI0 to ANI3:	Analog input	TI000, TI010:	Timer input
INTP0, INTP1:	External interrupt input	TO00, TOH1:	Timer output
P20 to P23:	Port 2	V_{DD}:	Power supply
P30, P34:	Port 3	V_{SS}:	Ground
P40 to P47:	Port 4	X1, X2:	Crystal oscillator (X1 input clock)
$\overline{\text{RESET}}$:	Reset		

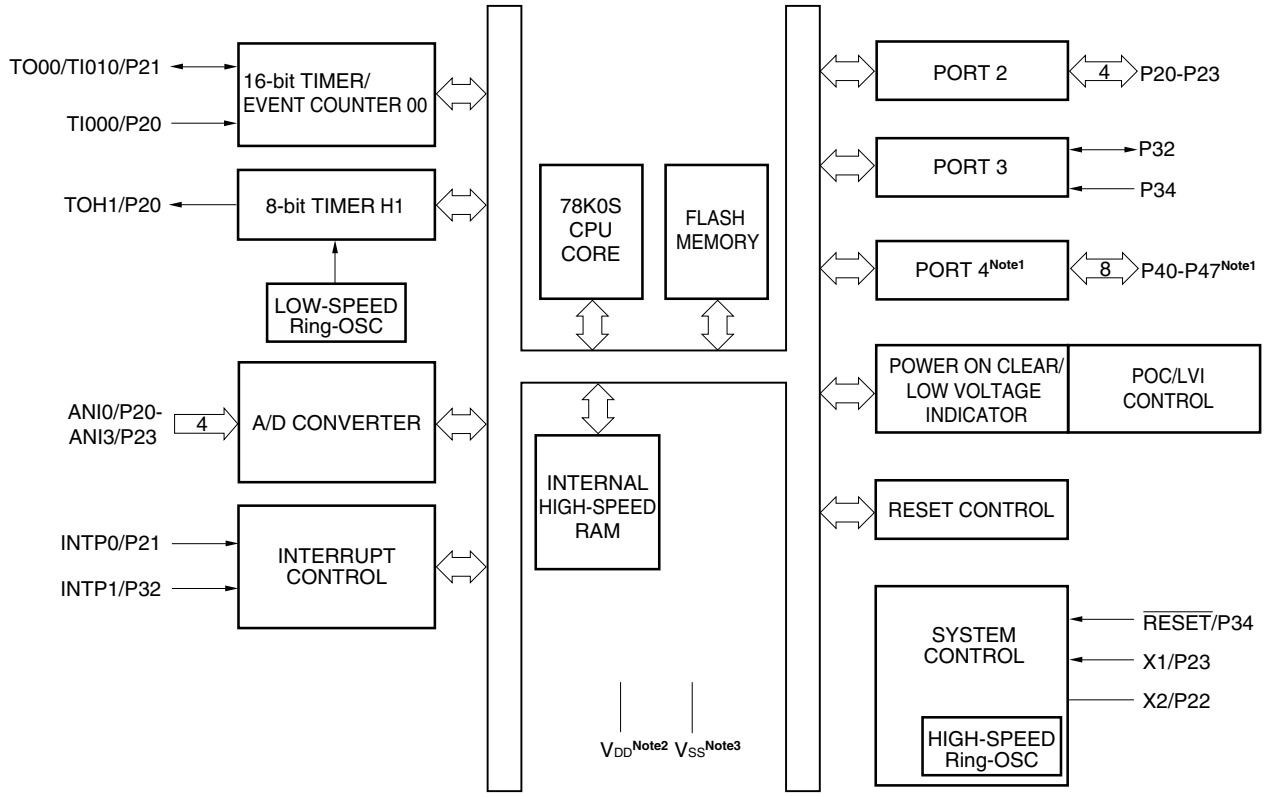
1.5 78K0S/Kx1+ Product Lineup

The following table shows the product lineup of the 78K0S/Kx1+.

Item \ Part Number		78K0S/KU1+	78K0S/KY1+	78K0S/KA1+		78K0S/KB1+
Number of pins		8 pins	16 pins	20 pins		30 pins
Internal memory	Flash memory	1 KB, 2 KB, 4 KB	1 KB, 2 KB, 4 KB	2 KB	4 KB	4 KB, 8 KB
	RAM	128 bytes	128 bytes	128 bytes	256 bytes	256 bytes
Supply voltage		V_{DD} = 2.0 to 5.5 V[Note]				
★ Minimum instruction execution time		0.20 μs (10 MHz, V_{DD} = 4.0 to 5.5 V) 0.33 μs (6 MHz, V_{DD} = 3.0 to 5.5 V) 0.40 μs (5 MHz, V_{DD} = 2.7 to 5.5 V) 1.0 μs (2 MHz, V_{DD} = 2.0 to 5.5 V)				
System clock (oscillation frequency)		Internal high-speed Ring-OSC oscillation (8 MHz (TYP.)) Crystal/ceramic oscillation (1 to 10 MHz) External clock input oscillation (1 to 10 MHz)				
Clock for TMH1 and WDT (oscillation frequency)		Internal low-speed Ring-OSC oscillation (240 kHz (TYP.))				
Port	CMOS I/O	5	13	15		22
	CMOS input	1	1	1		1
	CMOS output	–	–	1		1
Timer	16-bit (TM0)	1 ch				
	8-bit (TMH)	1 ch				
	8-bit (TM8)	–		1 ch		
	WDT	1 ch				
Serial interface		–		LIN-Bus-supporting UART: 1 ch		
A/D converter		10 bits: 4 ch (2.7 to 5.5V)				
Multiplier (8 bits × 8 bits)		–				Provided
Interrupts	External	2		4		
	Internal	5		9		
Reset	$\overline{\text{RESET}}$ pin	Provided				
	POC	2.1 V ±0.1 V				
	LVI	Provided (selectable by software)				
	WDT	Provided				
Operating temperature range		–40 to +85°C				

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on- clear (POC) circuit is 2.1 V ±0.1 V.

1.6 Block Diagram



★ **Notes 1.** 78K0S/KY1+ only. When using the 78K0S/KU1+, set port mode register 4 (PM4) to 00H when initially setting the program.

2. In the 78K0S/KU1+ and 78K0S/KY1+, V_{DD} functions alternately as the A/D converter reference voltage input. When using the A/D converter, stabilize V_{DD} at the supply voltage used (2.7 to 5.5 V).

3. In the 78K0S/KU1+ and 78K0S/KY1+, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

1.7 Functional Outline

Item		78K0S/KU1+	78K0S/KY1+
Internal memory	Flash memory	μPD78F9200: 1 KB μPD78F9201: 2 KB μPD78F9202: 4 KB	μPD78F9210: 1 KB μPD78F9211: 2 KB μPD78F9212: 4 KB
	High-speed RAM	128 bytes	
Memory space		64 KB	
X1 input clock (oscillation frequency)		Crystal/ceramic/external clock input: 10 MHz (V_{DD} = 2.0 to 5.5 V)	
Ring-OSC clock	High speed (oscillation frequency)	Internal Ring oscillation: 8 MHz (TYP.)	
	Low speed (for TMH1 and WDT)	Internal Ring oscillation: 240 kHz (TYP.)	
General-purpose registers		8 bits × 8 registers	
Minimum instruction execution time		0.2 μs/0.4 μs/0.8 μs/1.6 μs/3.2 μs (X1 input clock: f_X = 10 MHz)	
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test), etc.	
I/O port		Total: 6 pins CMOS I/O: 5 pins CMOS input: 1 pin	Total: 14 pins CMOS I/O: 13 pins CMOS input: 1 pin
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer (timer H1): 1 channel • Watchdog timer: 1 channel	
	Timer output	2 pins (PWM: 1 pin)	
A/D converter		10-bit resolution × 4 channels	
Vectored interrupt sources	External	2	
	Internal	5	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on clear • Internal reset by low-voltage detector	
Supply voltage		V_{DD} = 2.0 to 5.5 V[Note]	
Operating temperature range		TA = −40 to +85°C	
Package		8-pin plastic SOP (5.72mm (225))	16-pin plastic SSOP(5.72 mm(225))

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on- clear (POC) circuit is 2.1 V ±0.1 V.

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Function List

(1) Port pins

Pin Name	I/O	Function		After Reset	Alternate-Function Pin
P20	I/O	Port 2. 4-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	ANI0/TI000/TOH1
P21					ANI1/TI010/ TO00/INTP0
P22					X2/ANI2
P23					X1/ANI3
P32	I/O	Port 3	Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.	Input	INTP1
P34	Input		Input only	Input	$\overline{\text{RESET}}$
P40 to P47[Note]	I/O	Port 4. 8-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	–

★ **Note** The P40 to P47 pins are provided only in the 78K0S/KY1+. When using the 78K0S/KU1+, set port mode register 4 (PM4) to 00H when initially setting the program.

Caution The P22/X2/ANI2 and P23/X1/ANI3 pins are pulled down during reset.

(2) Non-port pins

Pin Name	I/O	Function	After Reset	Alternate-Function Pin
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P21/ANI1/TI010/TO00
INTP1				P32
TI000	Input	External count clock input to 16-bit timer/event counter 00. Capture trigger input to capture registers (CR000 and CR010) of 16-bit timer/event counter 00	Input	P20/ANI0/TOH1
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P21/ANI1/TO00/INTP0
TO00	Output	16-bit timer/event counter 00 output	Input	P21/ANI1/TI010/INTP0
TOH1	Output	8-bit timer H1 output	Input	P20/ANI0/TI000
ANI0	Input	Analog input of A/D converter	Input	P20/TI000/TOH1
ANI1				P21/TI010/TO00/INTP0
ANI2				P22/X2
ANI3				P23/X1
$\overline{\text{RESET}}$	Input	System reset input	Input	P34
X1	Input	Connection of crystal/ceramic oscillator for system clock oscillation. External clock input	–	P23/ANI3
X2	–	Connection of crystal/ceramic oscillator for system clock oscillation.	–	P22/ANI2
V_{DD}	–	Positive power supply	–	–
V_{SS}	–	Ground potential	–	–

Caution The P22/X2/ANI2 and P23/X1/ANI3 pins are pulled down during reset.

2.2 Pin Functions

2.2.1 P20 to P23 (Port 2)

P20 to P23 constitute a 4-bit I/O port. In addition to the function as I/O port pins, these pins also have a function to input an analog signal to the A/D converter, input/output a timer signal, and input an external interrupt request signal.

P22 and P23 are also function as the X1 and X2 pins, respectively.

These pins can be set to the following operation modes in 1-bit units.

(1) Port mode

P20 to P23 function as a 4-bit I/O port. Each bit of this port can be set to the input or output mode by using port mode register 2 (PM2). In addition, an on-chip pull-up resistor can be connected to the port by using pull-up resistor option register 2 (PU2).

(2) Control mode

P20 to P23 function to input an analog signal to the A/D converter, input/output a timer signal, and input an external interrupt request signal.

(a) ANI0 to ANI3

These are the analog input pins of the A/D converter. When using these pins as analog input pins, refer to **9.6 Cautions for A/D converter (5) ANI0/P20 to ANI3/P23**.

(b) TI000

This pin inputs an external count clock to 16-bit timer/event counter 00, or a capture trigger signal to the capture registers (CR000 and CR010) of 16-bit timer/event counter 00.

(c) TI010

This pin inputs a capture trigger signal to the capture register (CR000) of 16-bit timer/event counter 00.

(d) TO00

This pin outputs a signal from 16-bit timer/event counter 00.

(e) TOH1

This pin outputs a signal from 8-bit timer H1.

(f) INTP0

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

Caution The P22/X2/ANI2 and P23/X1/ANI3 pins are pulled down during reset.

2.2.2 P32 and P34 (Port 3)

P32 is a 1-bit I/O port. In addition to the function as an I/O port pin, this pin also has a function to input an external interrupt request signal.

P34 is a 1-bit input-only port. This pin is also used as a $\overline{\text{RESET}}$ pin.

P32 can be set to the following operation modes in 1-bit units.

(1) Port mode

P32 functions as a 1-bit I/O port. This pin can be set to the input or output mode by using port mode register 3 (PM3). In addition, an on-chip pull-up resistor can be connected to the port by using pull-up resistor option register 3 (PU3).

P34 functions as a 1-bit input-only port.

(2) Control mode

P32 functions as an external interrupt request input pin (INTP1) for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified. .

2.2.3 P40 to P47 (Port 4)[Note]

P40 to P47 constitute a 8-bit I/O port. Each bit of this port can be set to the input or output mode by using port mode register 4 (PM4). In addition, an on-chip pull-up resistor can be connected to the port by using pull-up resistor option register 4 (PU4).

★ **Note** The P40 to P47 pins are provided only in the 78K0S/KY1+. When using the 78K0S/KU1+, set port mode register 4 (PM4) to 00H when initially setting the program.

2.2.4 $\overline{\text{RESET}}$

This pin inputs an active-low system reset signal.

2.2.5 X1 and X2

These pins connect an oscillator to oscillate the X1 input clock.

Supply an external clock to X1.

Caution P22/X2/ANI2 and P23/X1/ANI3 pins are pulled down during reset.

2.2.6 V_{DD}

This is the positive power supply pin.

In the 78K0S/KU1+ and 78K0S/KY1+, V_{DD} functions alternately as the A/D converter reference voltage input. When using the A/D converter, stabilize V_{DD} at the supply voltage used (2.7 to 5.5 V).

2.2.7 V_{SS}

This is the ground pin.

In the 78K0S/KU1+ and 78K0S/KY1+, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

2.3 Pin I/O Circuits and Connection of Unused Pins

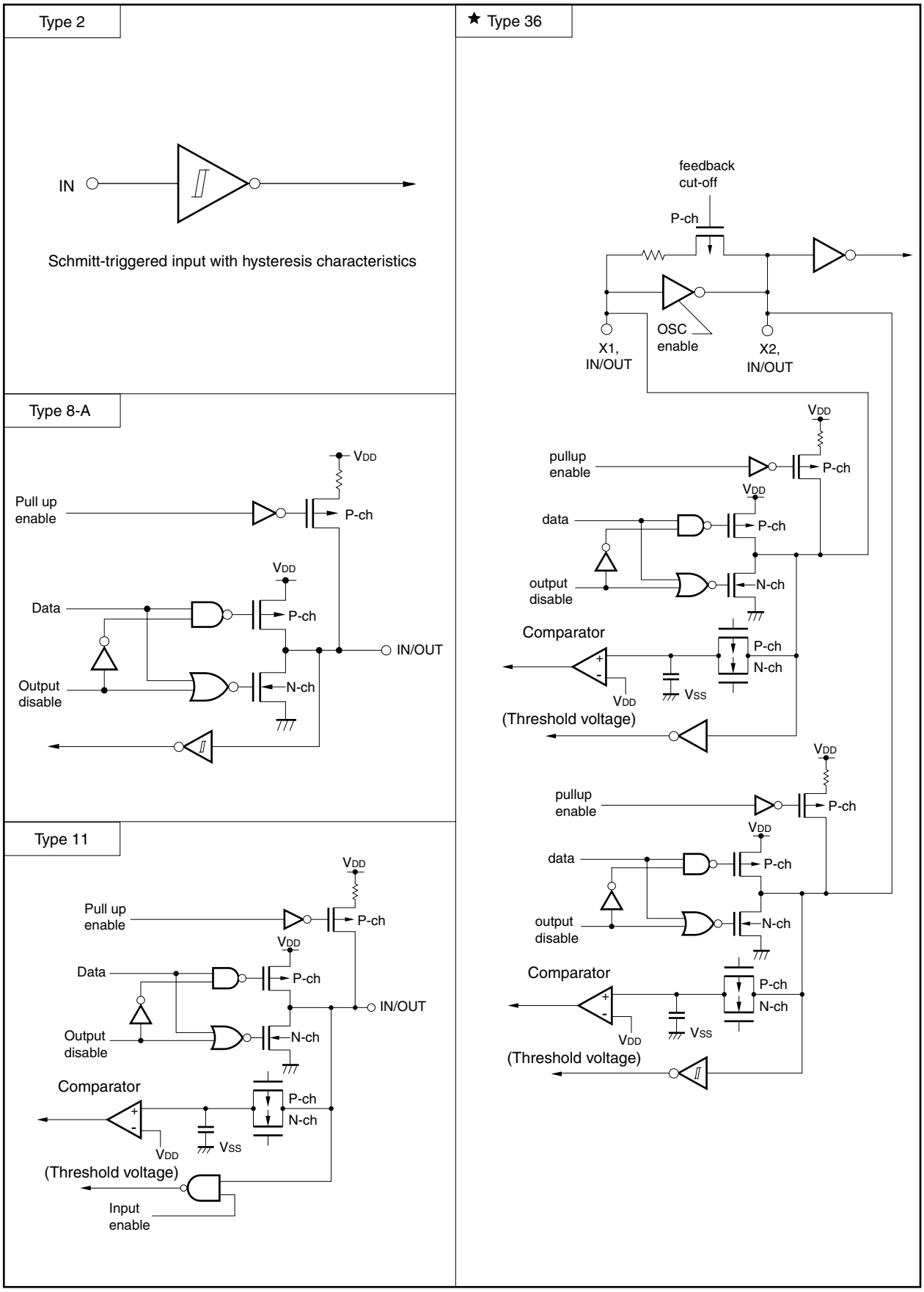
Table 2-1 shows I/O circuit type of each pin and the connections of unused pins.
For the configuration of the I/O circuit of each type, refer to **Figure 2-1**.

Table 2-1. Types of Pin I/O Circuits and Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P20/ANI0/TI000/TOH1	11	I/O	Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave open.
P21/ANI1/TI010/TO00/ INTP0			
P22/ANI2/X2	36		Input: Individually connect to V_{SS} via resistor. Output: Leave open.
P23/ANI3/X1			
P32/INTP1	8-A		Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave open.
P34/$\overline{\text{RESET}}$	2	Input	Connect to V_{DD} via resistor.
P40 to P47[Note]	8-A	I/O	Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave open.

★ **Note** The P40 to P47 pins are provided only in the 78K0S/KY1+. When using the 78K0S/KU1+, set port mode register 4 (PM4) to 00H when initially setting the program.

Figure 2-1. Pin I/O Circuits

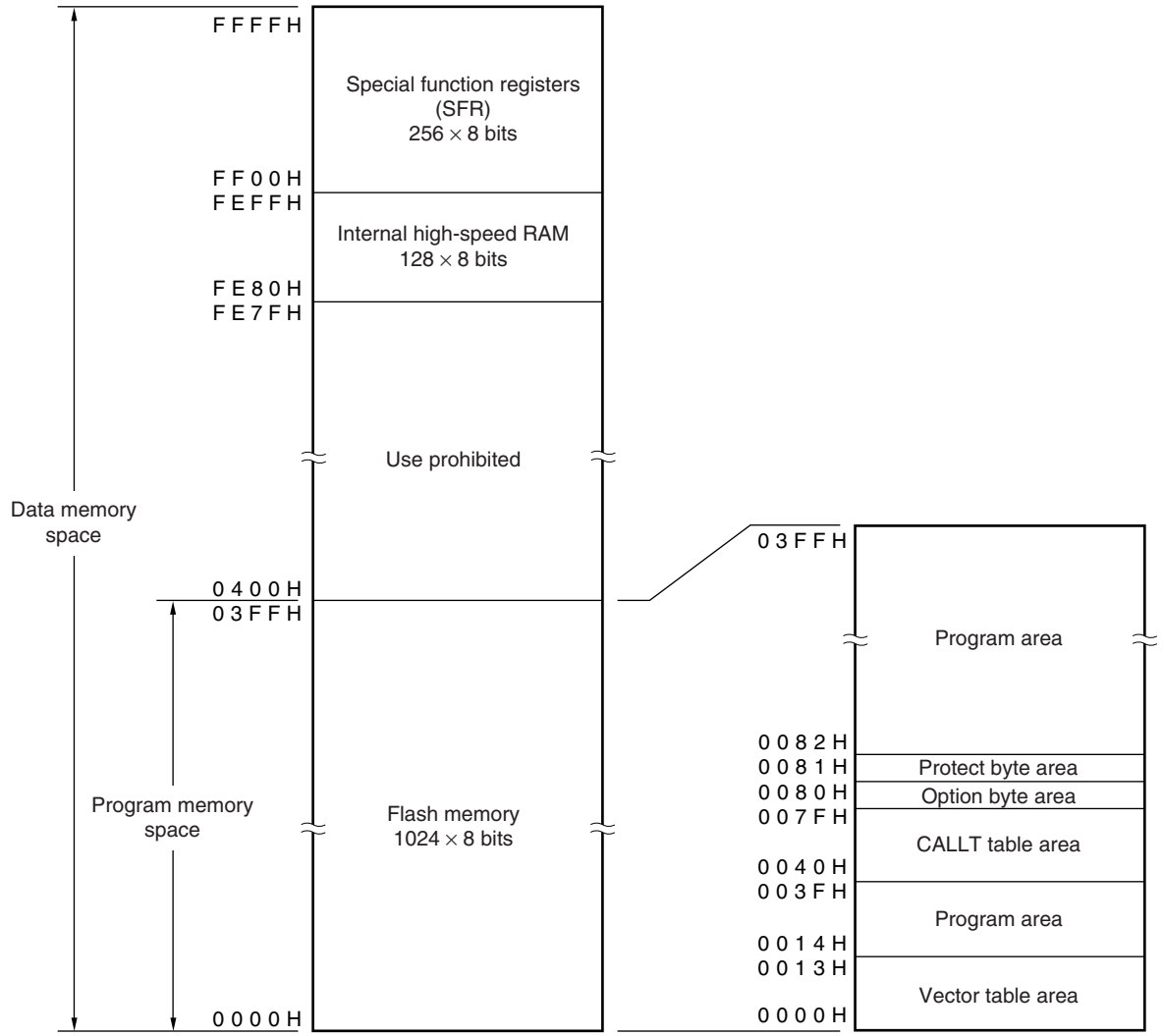


CHAPTER 3 CPU ARCHITECTURE

3.1 Memory Space

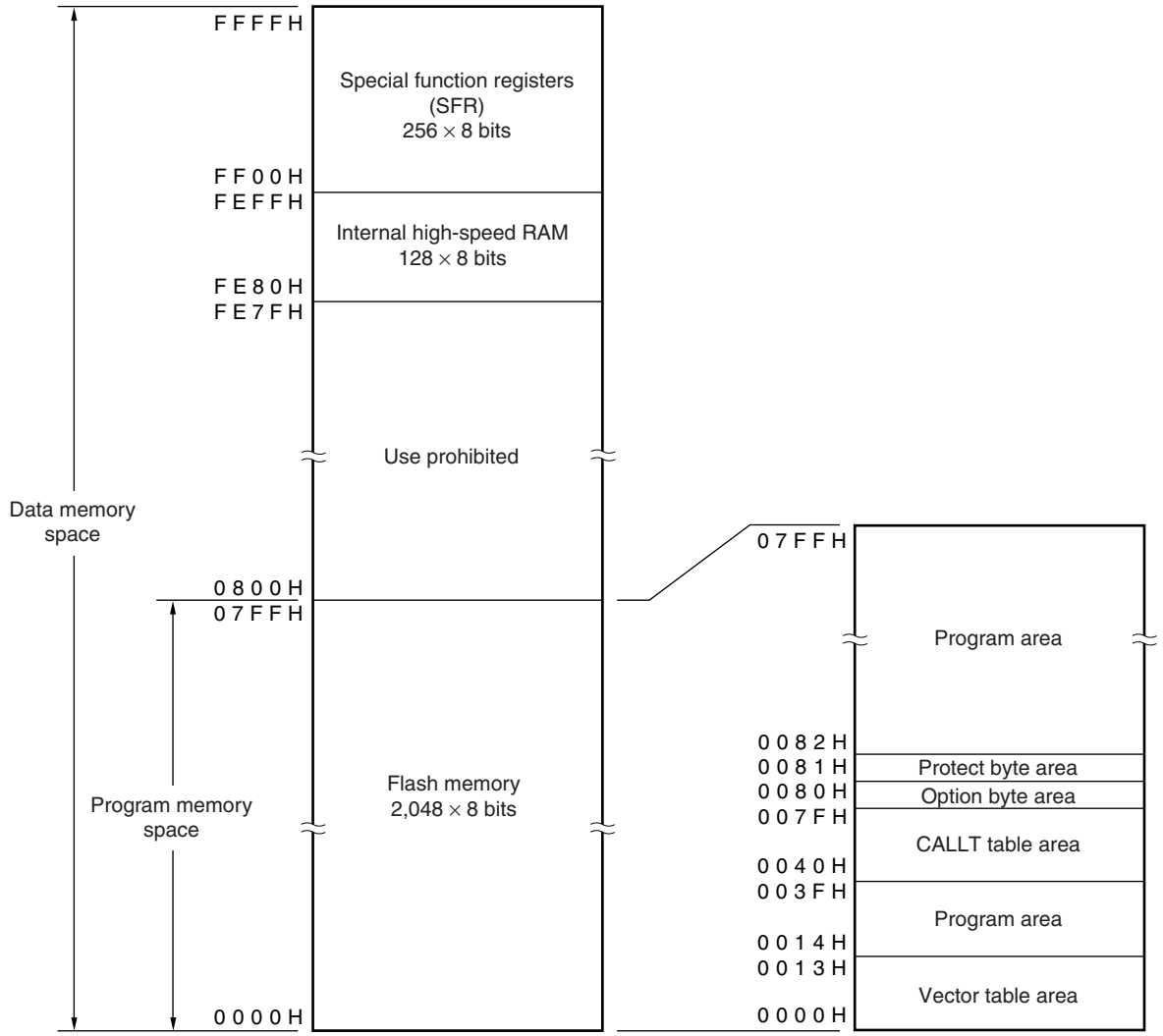
The 78K0S/KU1+ and 78K0S/KY1+ can access up to 64 KB of memory space. Figures 3-1 to 3-3 show the memory maps.

Figure 3-1. Memory Map (μPD78F9200, 78F9210)



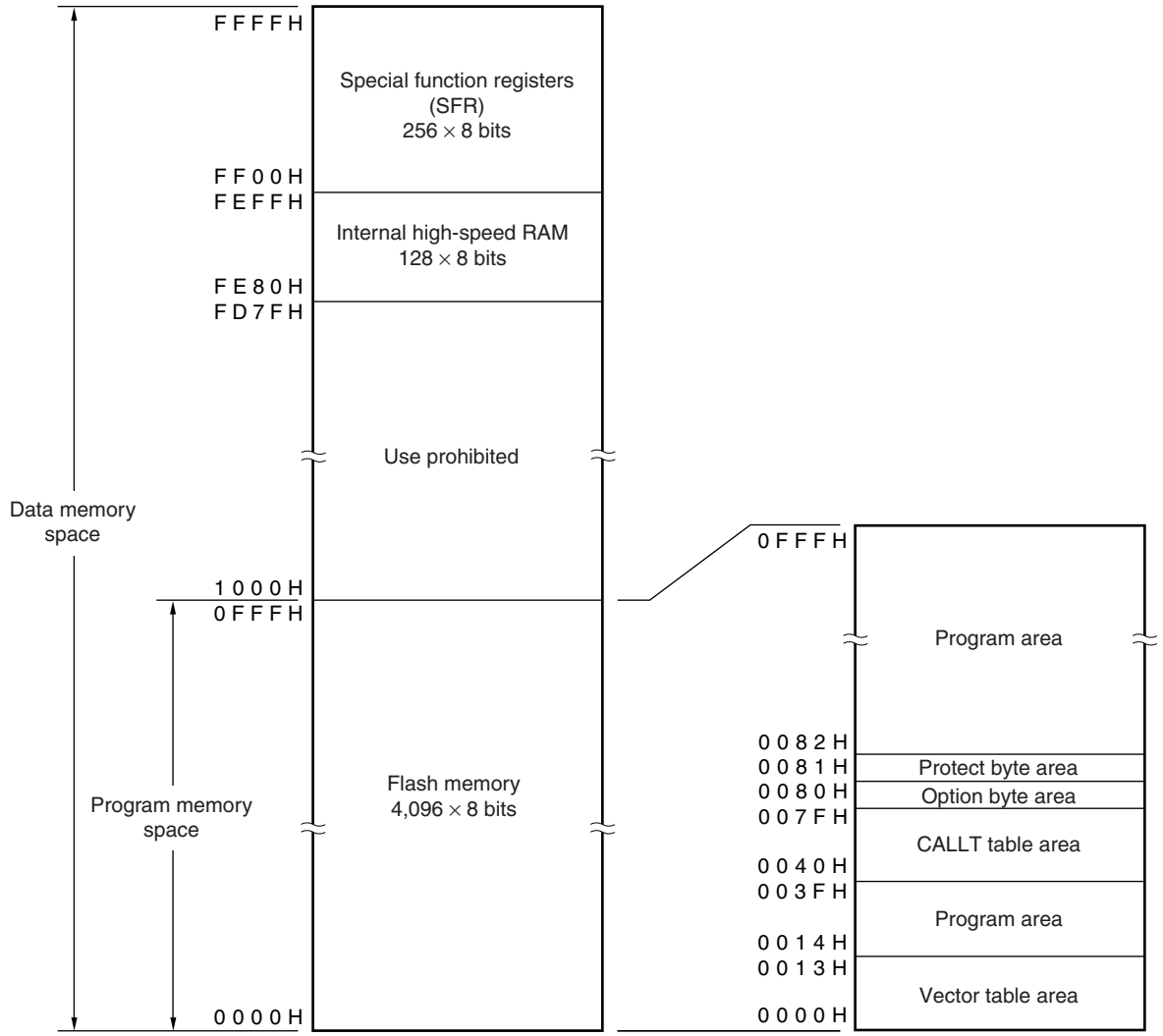
Remark The option byte and protect byte are 1 byte each.

Figure 3-2. Memory Map (μPD78F9201, 78F9211)



Remark The option byte and protect byte are 1 byte each.

Figure 3-3. Memory Map (μPD78F9202, 78F9212)



Remark The option byte and protect byte are 1 byte each.

3.1.1 Internal program memory space

The internal program memory space stores programs and table data. This space is usually addressed by the program counter (PC).

The 78K0S/KU1+ and 78K0S/KY1+ provide the following internal ROMs (or flash memory) containing the following capacities.

Table 3-1. Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
μPD78F9200, 78F9210	Flash memory	1,024 × 8 bits
μPD78F9201, 78F9211		2,048 × 8 bits
μPD78F9202, 78F9212		4,096 × 8 bits

The following areas are allocated to the internal program memory space.

(1) Vector table area

The 20-byte area of addresses 0000H to 0013H is reserved as a vector table area. This area stores program start addresses to be used when branching by $\overline{\text{RESET}}$ input or interrupt request generation. Of a 16-bit address, the lower 8 bits are stored in an even address, and the higher 8 bits are stored in an odd address.

Table 3-2. Vector Table

Vector Table Address	Interrupt Request	Vector Table Address	Interrupt Request
0000H	Reset input	000CH	INTTMH1
0006H	INTLVI	000EH	INTTM000
0008H	INTP0	0010H	INTTM010
000AH	INTP1	0012H	INTAD

(2) CALLT instruction table area

The subroutine entry address of a 1-byte call instruction (CALLT) can be stored in the 64-byte area of addresses 0040H to 007FH.

(3) Option byte area

The option byte area is the 1-byte area of address 0080H. For details, refer to **CHAPTER 15 OPTION BYTE**.

(4) Protect byte area

The protect byte area is the 1-byte area of address 0081H. For details, refer to **CHAPTER 16 FLASH MEMORY**.

3.1.2 Internal data memory space

128-byte internal high-speed RAM is provided in the 78K0S/KU1+ and 78K0S/KY1+.

The internal high-speed RAM can also be used as a stack memory.

3.1.3 Special function register (SFR) area

Special function registers (SFRs) of on-chip peripheral hardware are allocated to the area of FF00H to FFFFH (see **Table 3-3**).

3.1.4 Data memory addressing

The 78K0S/KU1+ and 78K0S/KY1+ are provided with a wide range of addressing modes to make memory manipulation as efficient as possible. The area (FE80H to FEFFH) which contains a data memory and the special function register (SFR) area can be accessed using a unique addressing mode in accordance with each function. Figures 3-4 to 3-6 illustrate the data memory addressing.

Figure 3-4. Data Memory Addressing (μPD78F9200, 78F9210)

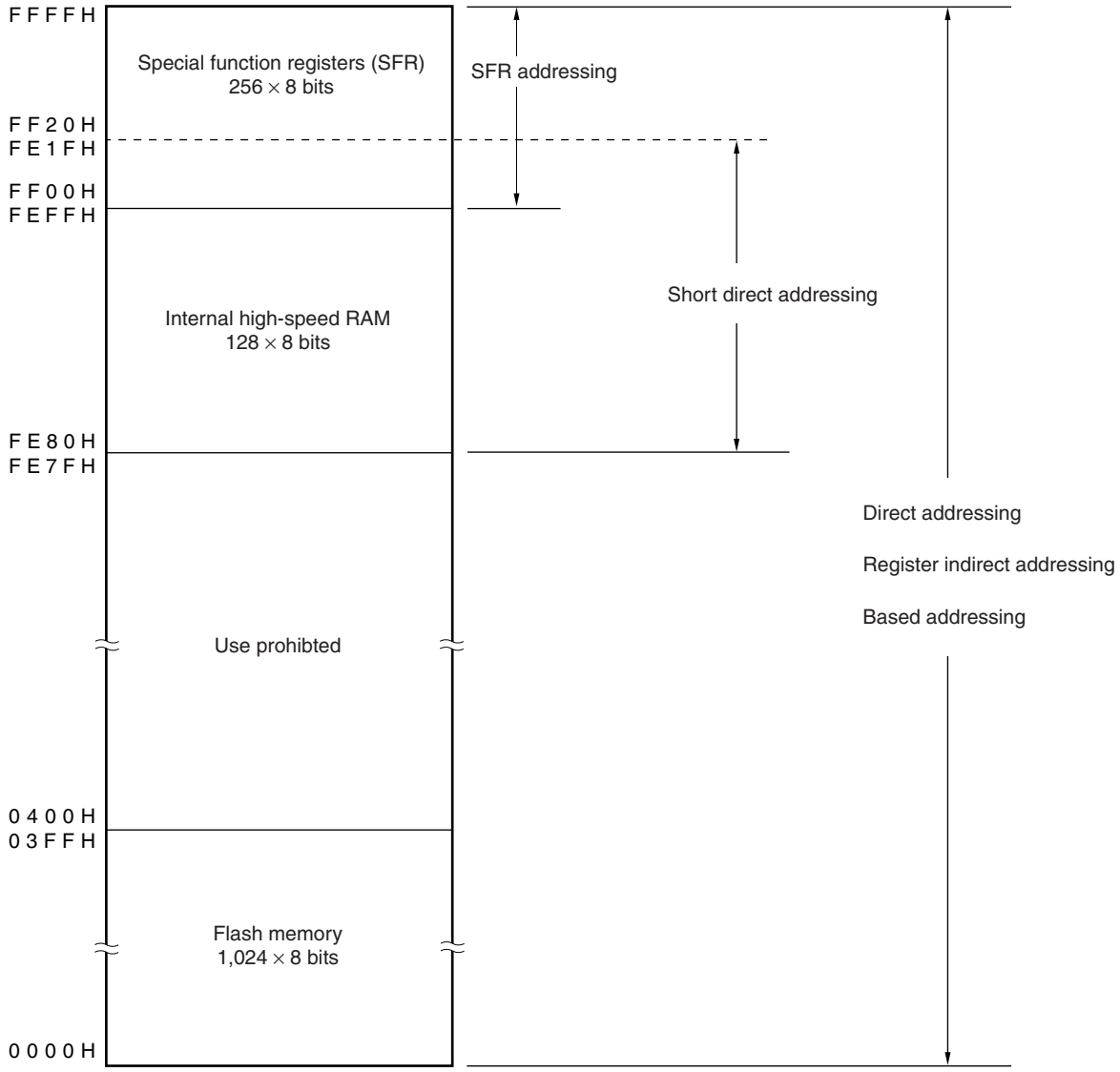


Figure 3-5. Data Memory Addressing (μPD78F9201, 78F9211)

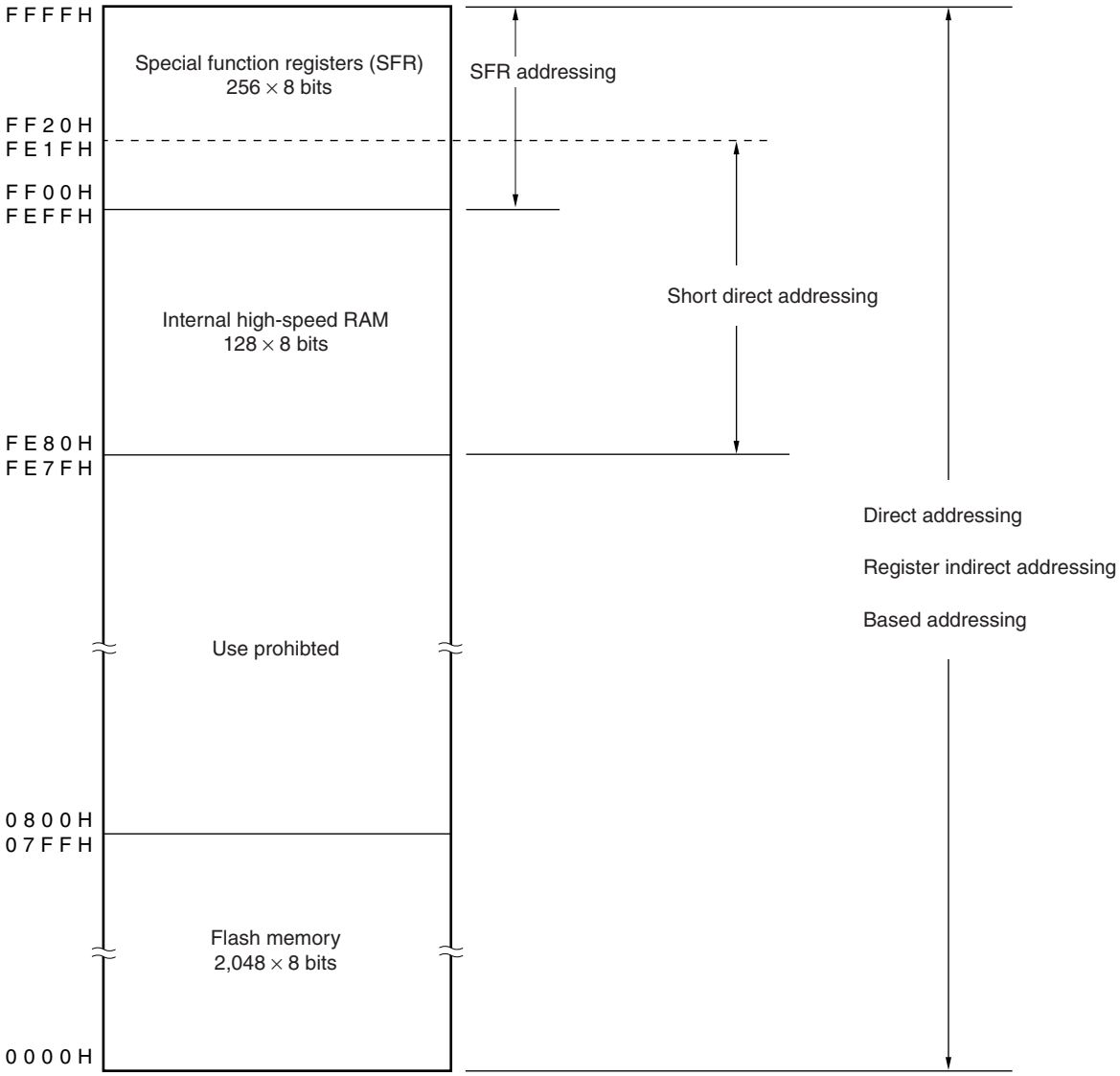
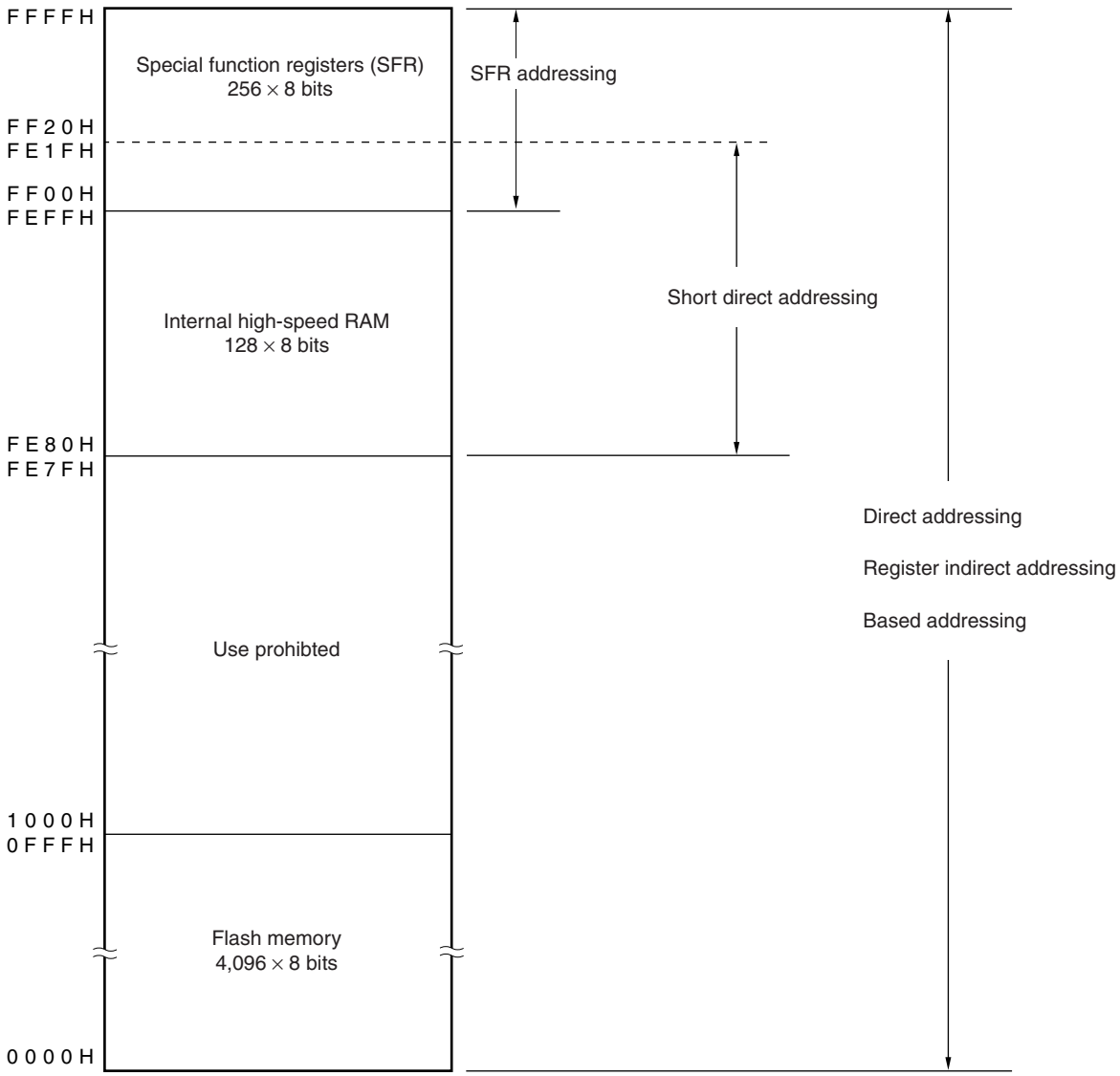


Figure 3-6. Data Memory Addressing (μPD78F9202, 78F9212)



3.2 Processor Registers

The 78K0S/KU1+ and 78K0S/KY1+ provide the following on-chip processor registers.

3.2.1 Control registers

The control registers have special functions to control the program sequence statuses and stack memory. The control registers include a program counter, a program status word, and a stack pointer.

(1) Program counter (PC)

The program counter is a 16-bit register which holds the address information of the next program to be executed.

In normal operation, the PC is automatically incremented according to the number of bytes of the instruction to be fetched. When a branch instruction is executed, immediate data or register contents are set.

$\overline{\text{RESET}}$ input sets the reset vector table values at addresses 0000H and 0001H to the program counter.

Figure 3-7. Program Counter Configuration

	15															0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags to be set/reset by instruction execution.

Program status word contents are automatically stacked upon interrupt request generation or PUSH PSW instruction execution and are automatically restored upon execution of the RETI and POP PSW instructions.

$\overline{\text{RESET}}$ input sets PSW to 02H.

Figure 3-8. Program Status Word Configuration

	7							0
PSW	IE	Z	0	AC	0	0	1	CY

(a) Interrupt enable flag (IE)

This flag controls interrupt request acknowledge operations of the CPU.

When IE = 0, the interrupt disabled (DI) status is set. All interrupt requests except non-maskable interrupt are disabled.

When IE = 1, the interrupt enabled (EI) status is set. Interrupt request acknowledgment is controlled with an interrupt mask flag for various interrupt sources.

This flag is reset to 0 upon DI instruction execution or interrupt acknowledgment and is set to 1 upon EI instruction execution.

(b) Zero flag (Z)

When the operation result is zero, this flag is set to 1. It is reset to 0 in all other cases.

(c) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set to 1. It is reset to 0 in all other cases.

(d) Carry flag (CY)

This flag stores overflow and underflow that have occurred upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal high-speed RAM area can be set as the stack area.

Figure 3-9. Stack Pointer Configuration

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The SP is decremented before writing (saving) to the stack memory and is incremented after reading (restoring) from the stack memory.

Each stack operation saves/restores data as shown in Figures 3-10 and 3-11.

Caution Since reset input makes SP contents undefined, be sure to initialize the SP before using the stack memory.

Figure 3-10. Data to Be Saved to Stack Memory

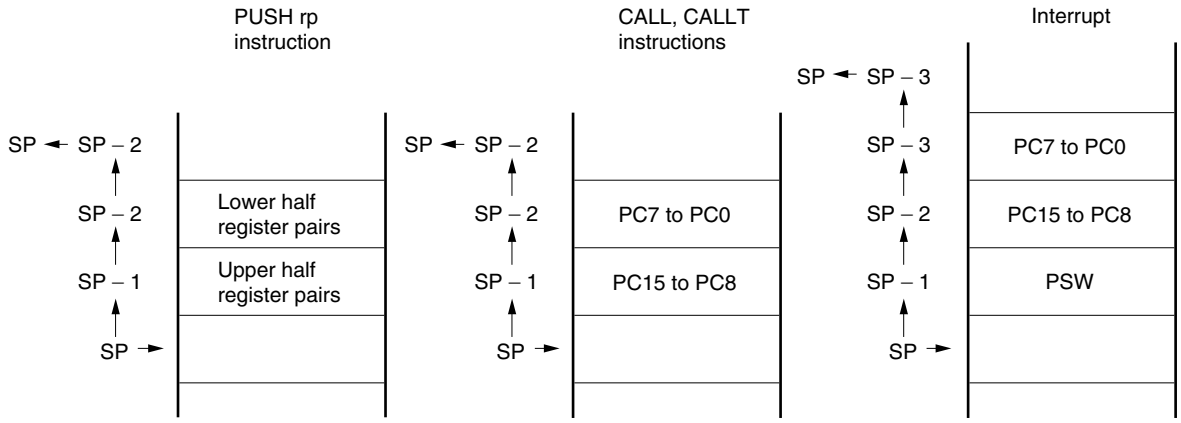
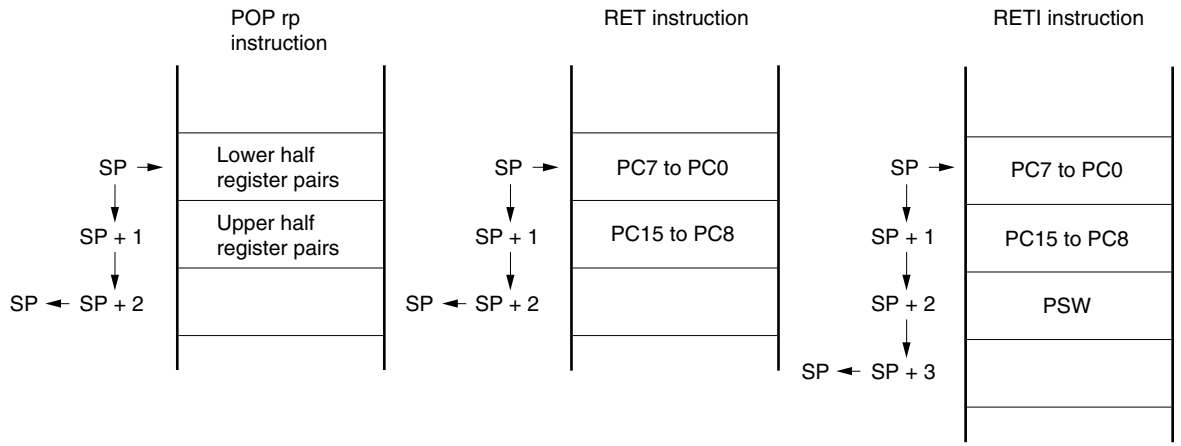


Figure 3-11. Data to Be Restored from Stack Memory



3.2.2 General-purpose registers

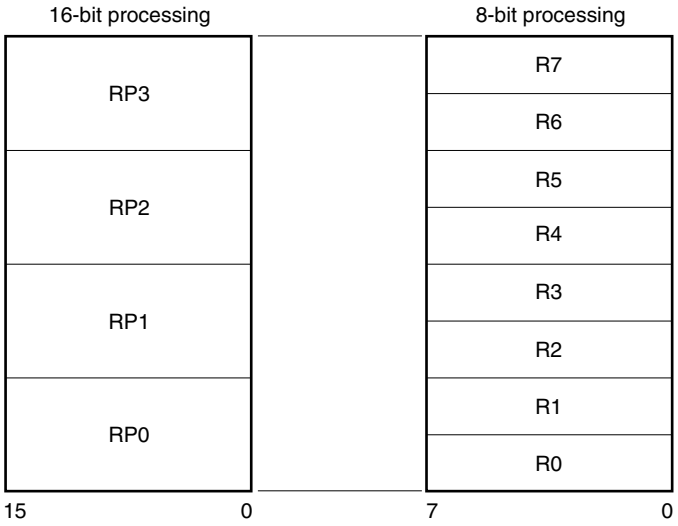
A general-purpose register consists of eight 8-bit registers (X, A, C, B, E, D, L, and H).

In addition each register being used as an 8-bit register, two 8-bit registers in pairs can be used as a 16-bit register (AX, BC, DE, and HL).

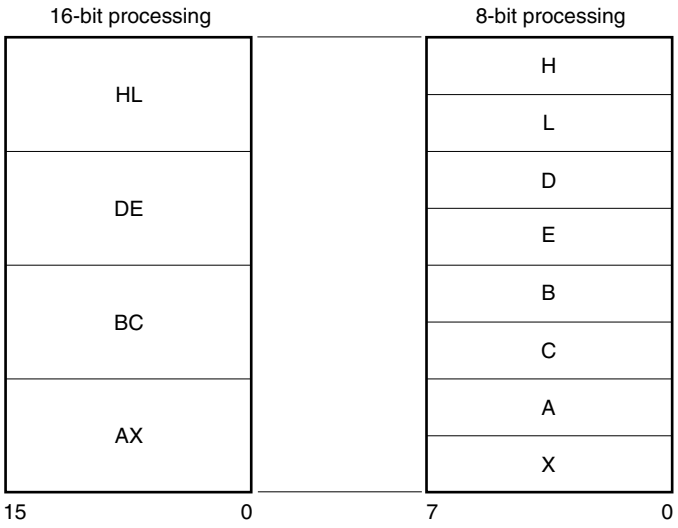
Registers can be described in terms of function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

Figure 3-12. General-Purpose Register Configuration

(a) Absolute names



(b) Function names



3.2.3 Special function registers (SFRs)

Unlike the general-purpose registers, each special function register has a special function.

The special function registers are allocated to the 256-byte area FF00H to FFFFH.

The special function registers can be manipulated, like the general-purpose registers, with operation, transfer, and bit manipulation instructions. Manipulatable bit units (1, 8, and 16) differ depending on the special function register type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describes a symbol reserved by the assembler for the 1-bit manipulation instruction operand (sfr.bit). This manipulation can also be specified with an address.

- 8-bit manipulation
  Describes a symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr). This manipulation can also be specified with an address.

- 16-bit manipulation
  Describes a symbol reserved by the assembler for the 16-bit manipulation instruction operand. When specifying an address, describe an even address.

Table 3-3 lists the special function registers. The meanings of the symbols in this table are as follows:

- Symbol
  Indicates the addresses of the implemented special function registers. It is defined as a reserved word in the RA78K0S, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0S. Therefore, these symbols can be used as instruction operands if an assembler or integrated debugger is used.

- R/W
  Indicates whether the special function register can be read or written.
  R/W: Read/write
  R: Read only
  W: Write only

- Number of bits manipulated simultaneously
  Indicates the bit units (1, 8, and 16) in which the special function register can be manipulated.

- After reset
  Indicates the status of the special function register when a reset is input.

Table 3-3. Special Function Registers (1/2)

Address	Special Function Register (SFR) Name	Symbol	R/W	Number of Bits Manipulated Simultaneously			After Reset
				1 Bit	8 Bits	16 Bits	
FF02H	Port register 2	P2	R/W Note 2	√	√	–	00H
FF03H	Port register 3	P3		√	√	–	
FF04H	Port register 4	P4		√	√	–	
FF0EH	8-bit timer H compare register 01	CMP01	R/W	–	√	–	
FF0FH	8-bit timer H compare register 11	CMP11		–	√	–	
FF12H	16-bit timer counter 00	TM00	R	–	–	√Note 3	0000H
FF13H							
FF14H	16-bit timer capture/compare register 000	CR000	R/W	–	–	√Note 3	0000H
FF15H							
FF16H	16-bit timer capture/compare register 010	CR010		–	–	√Note 3	0000H
FF17H							
FF18H	10-bit A/D conversion result register	ADCR	R	–	–	√Note 3	Undefined
FF19H							
FF1AH	8-bit A/D conversion result register	ADCRH		–	√	–	
FF22H	Port mode register 2	PM2	R/W	√	√	–	FFH
FF23H	Port mode register 3	PM3		√	√	–	
FF24H	Port mode register 4Note 1	PM4Note 1		√	√	–	
FF32H	Pull-up resistance option register 2	PU2		√	√	–	00H
FF33H	Pull-up resistance option register 3	PU3		√	√	–	
FF34H	Pull-up resistance option register 4	PU4		√	√	–	
FF48H	Watchdog timer mode register	WDTM		–	√	–	67H
FF49H	Watchdog timer enable register	WDTE		–	√	–	9AH
FF50H	Low voltage detect register	LVIM		√	√	–	00HNote 4
FF51H	Low voltage detection level select register	LVIS		–	√	–	
FF54H	Reset control flag register	RESF	R	–	√	–	00HNote 5
★ FF58H	Low-speed Ring-OSC mode register	LSRCM	R/W	√	√	–	00H
FF60H	16-bit timer mode control register 00	TMC00		√	√	–	
FF61H	Prescaler mode register 00	PRM00		√	√	–	
FF62H	Capture/compare control register 00	CRC00		√	√	–	
FF63H	16-bit timer output control register 00	TOC00		√	√	–	
FF70H	8-bit timer H mode register 1	TMHMD1		√	√	–	
FF80H	A/D converter mode register	ADM		√	√	–	
FF81H	Analog input channel specify register	ADS		√	√	–	
FF84H	Port mode control register 2	PMC2		√	√	–	

★ **Notes 1.** When using the 78K0S/KU1+, set port mode register 4 (PM4) to 00H when initially setting the program.

2. Only P34 is an input-only port.

3. A 16-bit access is possible only by the short direction addressing.

★ **4.** Retained only after a reset by LVI.

5. Varies depending on the reset cause.

Table 3-3. Special Function Registers (2/2)

Address	Special Function Register (SFR) Name	Symbol	R/W	Number of Bits Manipulated Simultaneously			After Reset
				1 Bit	8 Bits	16 Bits	
FFA0H	Flash Protect Command register	PFCMD	W	–	√	–	Undefined
FFA1H	Flash Status register	PFS	R/W	√	√	–	00H
FFA2H	Flash Programming Mode Control register	FLPMC		√	√	–	Undefined
FFA3H	Flash Programming Command register	FLCMD		√	√	–	00H
FFA4H	Flash Address Pointer L	FLAPL		√	√	–	Undefined
FFA5H	Flash Address Pointer H	FLAPH		√	√	–	
FFA6H	Flash Address Pointer H Compare register	FLAPHC		√	√	–	00H
FFA7H	Flash Address Pointer L Compare register	FLAPLC		√	√	–	
FFA8H	Flash Write buffer register	FLW		–	√	–	
FFE0H	Interrupt request flag register 0	IF0		√	√	–	
FFE4H	Interrupt mask flag register 0	MK0		√	√	–	FFH
FFECH	External interrupt mode register 0	INTM0		–	√	–	00H
FFF3H	Preprocessor clock control register	PPCC		√	√	–	02H
FFF4H	Oscillation stabilization time selection register	OSTS		–	√	–	Undefined Note
FFFBH	Processor clock control register	PCC		√	√	–	02H

Note The oscillation stabilization time that elapses after release of reset is selected by the option byte. For details, refer to **CHAPTER 15 OPTION BYTE**.

3.3 Instruction Address Addressing

An instruction address is determined by the program counter (PC) contents. The PC contents are normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination address information is set to the PC to branch by the following addressing (for details of each instruction, refer to **78K/0S Series Instructions User's Manual (U11047E)**).

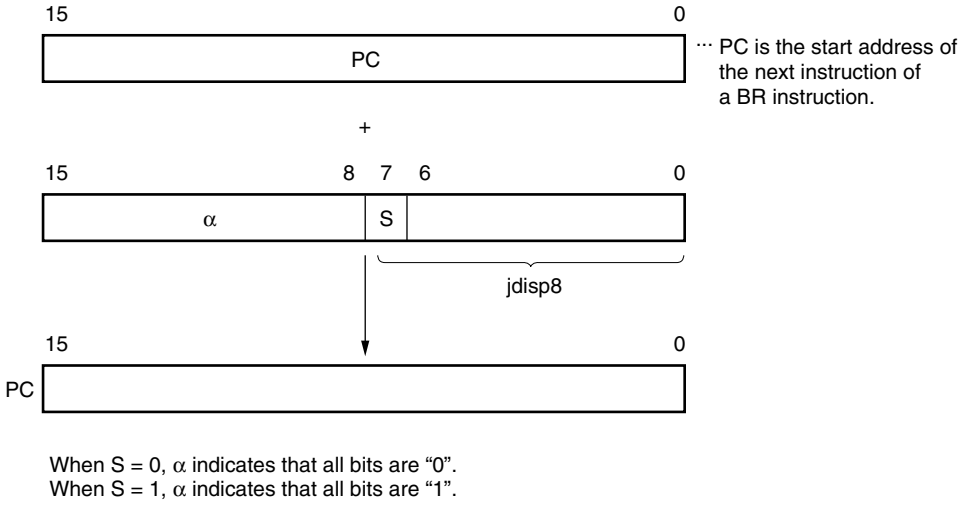
3.3.1 Relative addressing

[Function]

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) to branch. The displacement value is treated as signed two's complement data (–128 to +127) and bit 7 becomes the sign bit. In other words, the range of branch in relative addressing is between –128 and +127 of the start address of the following instruction.

This function is carried out when the BR $addr16 instruction or a conditional branch instruction is executed.

[Illustration]



When S = 0, α indicates that all bits are "0".
When S = 1, α indicates that all bits are "1".

3.3.2 Immediate addressing

[Function]

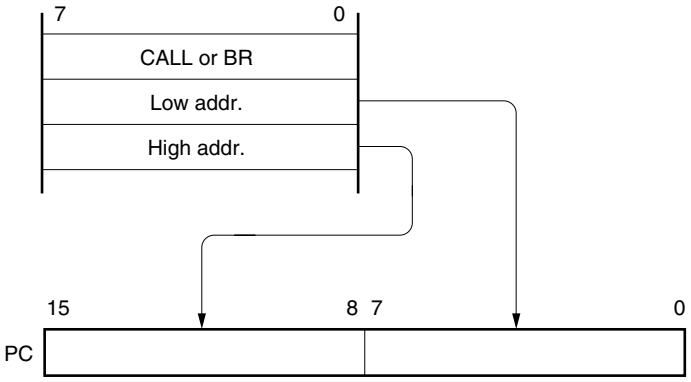
Immediate data in the instruction word is transferred to the program counter (PC) to branch.

This function is carried out when the CALL !addr16 and BR !addr16 instructions are executed.

CALL !addr16 and BR !addr16 instructions can be used to branch to all the memory spaces.

[Illustration]

In case of CALL !addr16 and BR !addr16 instructions



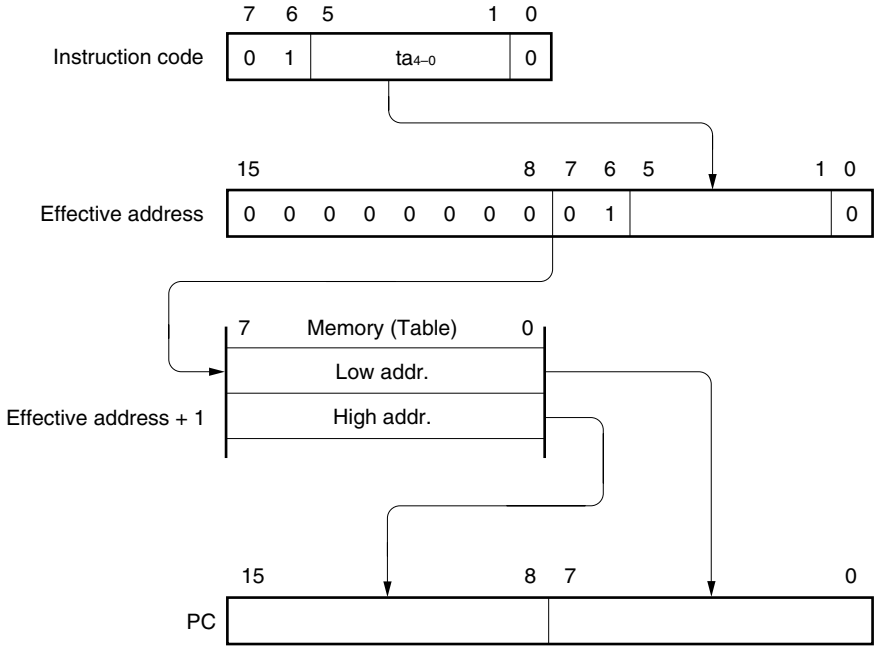
3.3.3 Table indirect addressing

[Function]

The table contents (branch destination address) of the particular location to be addressed by the immediate data of an instruction code from bit 1 to bit 5 are transferred to the program counter (PC) to branch.

Table indirect addressing is carried out when the CALLT [addr5] instruction is executed. This instruction can be used to branch to all the memory spaces according to the address stored in the memory table 40H to 7FH.

[Illustration]



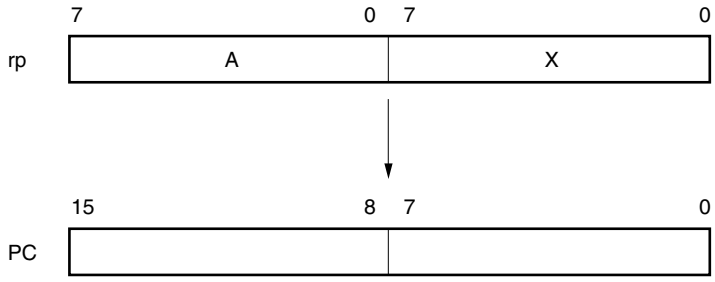
3.3.4 Register addressing

[Function]

The register pair (AX) contents to be specified with an instruction word are transferred to the program counter (PC) to branch.

This function is carried out when the BR AX instruction is executed.

[Illustration]



3.4 Operand Address Addressing

The following methods (addressing) are available to specify the register and memory to undergo manipulation during instruction execution.

3.4.1 Direct addressing

[Function]

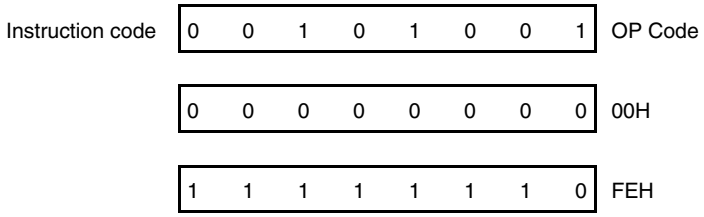
The memory indicated by immediate data in an instruction word is directly addressed.

[Operand format]

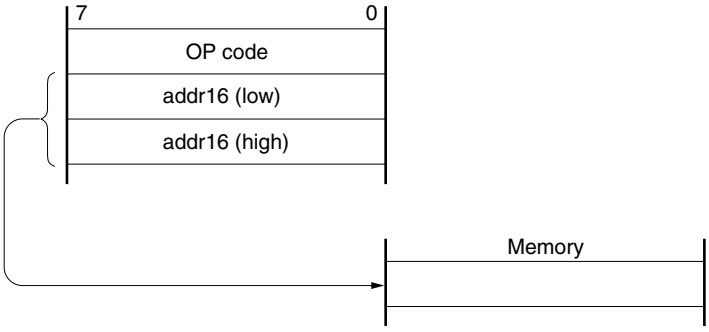
Identifier	Description
addr16	Label or 16-bit immediate data

[Description example]

MOV A, !FE00H; When setting !addr16 to FE00H



[Illustration]



3.4.2 Short direct addressing

[Function]

The memory to be manipulated in the fixed space is directly addressed with the 8-bit data in an instruction word.

The fixed space where this addressing is applied is the 256-byte space FE20H to FF1FH. An internal high-speed RAM is mapped at FE20H to FEFFH and the special function registers (SFR) are mapped at FF00H to FF1FH.

The SFR area where short direct addressing is applied (FF00H to FF1FH) is a part of the total SFR area. In this area, ports which are frequently accessed in a program and a compare register of the timer counter are mapped, and these SFRs can be manipulated with a small number of bytes and clocks.

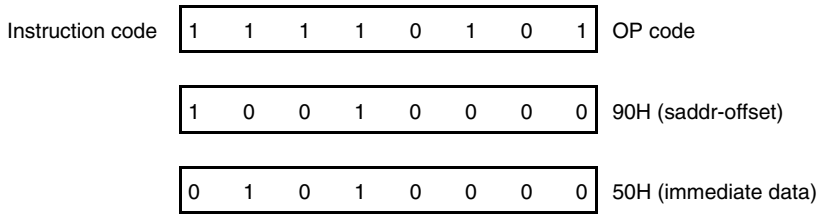
When 8-bit immediate data is at 20H to FFH, bit 8 of an effective address is cleared to 0. When it is at 00H to 1FH, bit 8 is set to 1. See **[Illustration]** below.

[Operand format]

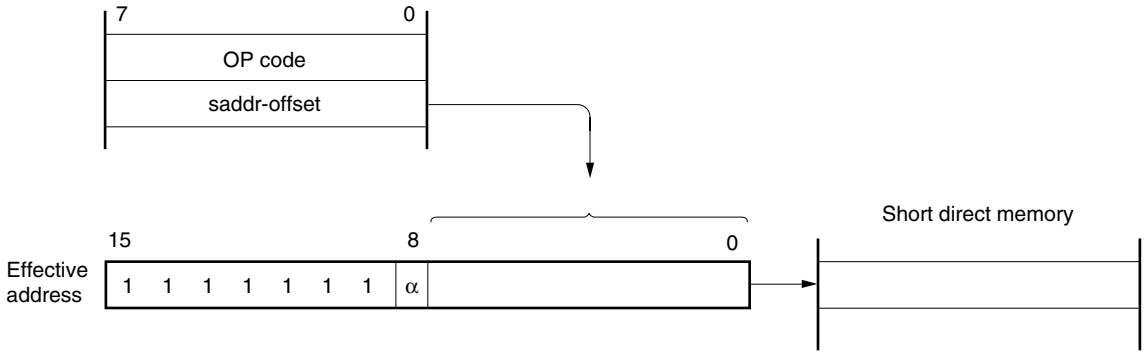
Identifier	Description
saddr	Label or FE20H to FF1FH immediate data
saddrp	Label or FE20H to FF1FH immediate data (even address only)

[Description example]

MOV FE90H, #50H; When setting saddr to FE90H and the immediate data to 50H



[Illustration]



When 8-bit immediate data is 20H to FFH, $\alpha = 0$.
When 8-bit immediate data is 00H to 1FH, $\alpha = 1$.

3.4.3 Special function register (SFR) addressing

[Function]

A memory-mapped special function register (SFR) is addressed with the 8-bit immediate data in an instruction word.

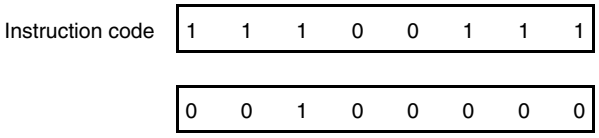
This addressing is applied to the 256-byte space FF00H to FFFFH. However, SFRs mapped at FF00H to FF1FH are accessed with short direct addressing.

[Operand format]

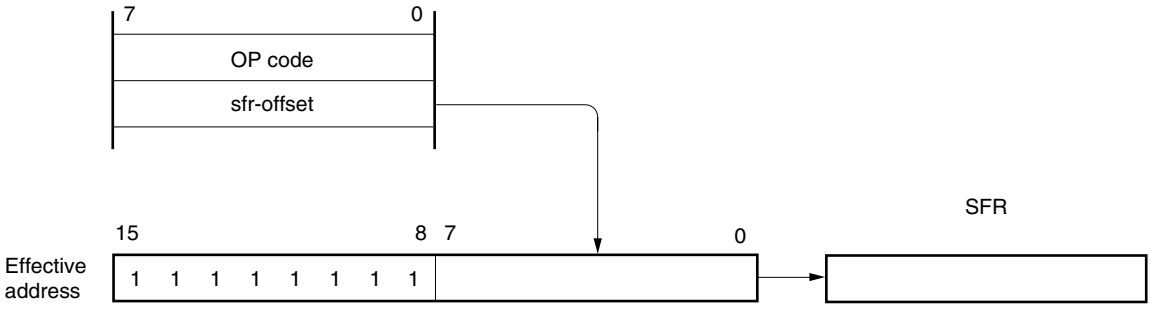
Identifier	Description
sfr	Special function register name

[Description example]

MOV PM0, A; When selecting PM0 for sfr



[Illustration]



3.4.4 Register addressing

[Function]

A general-purpose register is accessed as an operand.

The general-purpose register to be accessed is specified with the register specify code and functional name in the instruction code.

Register addressing is carried out when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the instruction code.

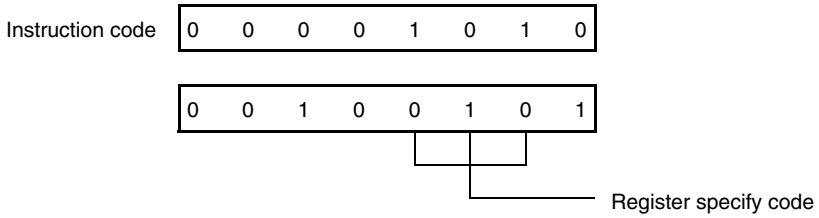
[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

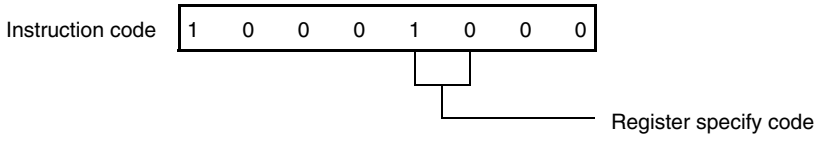
'r' and 'rp' can be described with absolute names (R0 to R7 and RP0 to RP3) as well as function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL).

[Description example]

MOV A, C; When selecting the C register for r



INCW DE; When selecting the DE register pair for rp



3.4.5 Register indirect addressing

[Function]

The memory is addressed with the contents of the register pair specified as an operand. The register pair to be accessed is specified with the register pair specify code in the instruction code. This addressing can be carried out for all the memory spaces.

[Operand format]

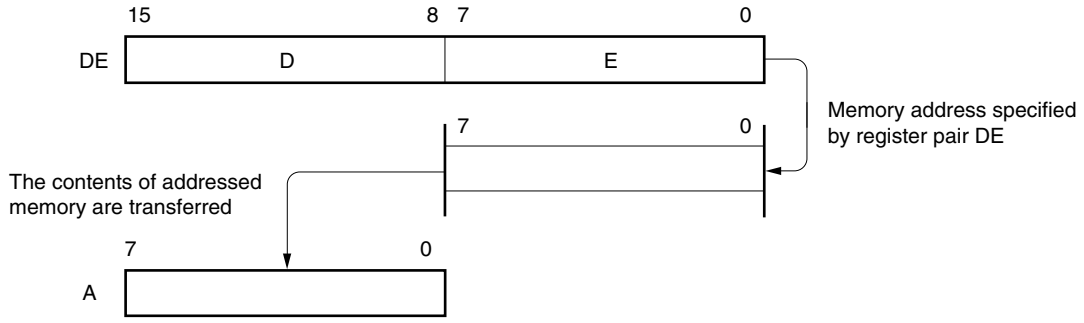
Identifier	Description
–	[DE], [HL]

[Description example]

MOV A, [DE]; When selecting register pair [DE]

Instruction code	0	0	1	0	1	0	1	1

[Illustration]



3.4.6 Based addressing

[Function]

8-bit immediate data is added to the contents of the base register, that is, the HL register pair, and the sum is used to address the memory. Addition is performed by expanding the offset data as a positive number to 16 bits. A carry from the 16th bit is ignored. This addressing can be carried out for all the memory spaces.

[Operand format]

Identifier	Description
–	[HL+byte]

[Description example]

MOV A, [HL+10H]; When setting byte to 10H

Instruction code	0	0	1	0	1	1	0	1
	0	0	0	1	0	0	0	0

3.4.7 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, subroutine call, and return instructions are executed or the register is saved/restored upon interrupt request generation.

Stack addressing can be used to access the internal high-speed RAM area only.

[Description example]

In the case of PUSH DE

Instruction code	1	0	1	0	1	0	1	0

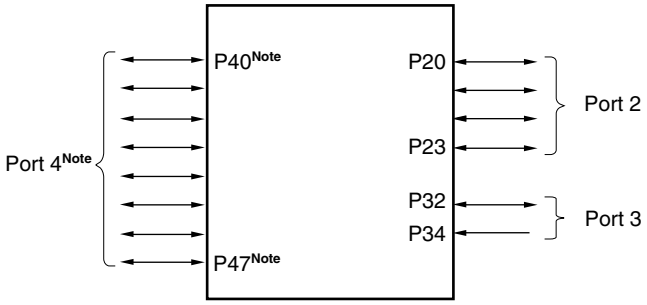
CHAPTER 4 PORT FUNCTIONS

4.1 Functions of Ports

The 78K0S/KU1+ and 78K0S/KY1+ have the ports shown in Figure 4-1, which can be used for various control operations. Table 4-1 shows the functions of each port.

In addition to digital I/O port functions, each of these ports has an alternate function. For details, refer to **CHAPTER 2 PIN FUNCTIONS**.

Figure 4-1. Port Functions



★ **Note** The P40 to P47 pins are provided only in the 78K0S/KY1+. When using the 78K0S/KU1+, set port mode register 4 (PM4) to 00H when initially setting the program.

Table 4-1. Port Functions

Pin Name	I/O	Function		After Reset	Alternate-Function Pin
P20	I/O	Port 2. 4-bit I/O port. Can be set to input or output mode in 1-bit units. On-chip pull-up resistor can be connected by setting software.		Input	ANI0/TI000/TOH1
P21					ANI1/TI010/TO00/INTP0
P22					X2/ANI2
P23					X1/ANI3
P32	I/O	Port 3	Can be set to input or output mode in 1-bit units. On-chip pull-up resistor can be connected by setting software.	Input	INTP1
P34	Input		Input only	Input	$\overline{\text{RESET}}$
P40 to P47Note	I/O	Port 4. 8-bit I/O port. Can be set to input or output mode in 1-bit units. On-chip pull-up resistor can be connected setting software.		Input	–

★ **Note** The P40 to P47 pins are provided only in the 78K0S/KY1+. When using the 78K0S/KU1+, set port mode register 4 (PM4) to 00H when initially setting the program.

Caution The P22/X2/ANI2 and P23/X1/ANI3 pins are pulled down during reset.

Remarks 1. P22 and P23 can be allocated when the high-speed Ring-OSC is selected as the system clock.

★ **2.** P22 can be allocated when an external clock input is selected as the system clock.

4.2 Port Configuration

Ports consist of the following hardware units.

Table 4-2. Configuration of Ports

Item	Configuration
Control registers	Port mode registers (PM2 to PM4) Port registers (P3, P4) Port mode control register 2 (PMC2) Pull-up resistor option registers (PU2 to PU4)
Ports	78K0S/KU1+ Total: 6 (CMOS I/O: 5, CMOS input: 1) 78K0S/KY1+ Total: 14 (CMOS I/O: 13, CMOS input: 1)
Pull-up resistor	78K0S/KU1+ Total: 5 78K0S/KY1+ Total: 13

4.2.1 Port 2

Port 2 is a 4-bit I/O port with an output latch. Each bit of this port can be set to the input or output mode by using port mode register 2 (PM2). When the P20 to P23 pins are used as an input port, an on-chip pull-up resistor can be connected in 1-bit units by using pull-up resistor option register 2 (PU2).

This port can also be used for A/D converter analog input, timer I/O, and external interrupt request input.

The P22 and P23 pins are also used as the X2 and X1 pins of the system clock oscillator. The functions of the P22 and P23 pins differ, therefore, depending on the selected system clock oscillator. The following three system clock oscillators can be used.

(1) High-speed Ring-OSC circuit

The P22 and P23 pins can be used as I/O port pins or analog input pins to the A/D converter.

(2) Crystal/ceramic oscillator

The P22 and P23 pins cannot be used as I/O port pins or analog input pins to the A/D converter because they are used as the X2 and X1 pins.

(3) External clock input

The P22 pin can be used as an I/O port pin or an analog input pin to the A/D converter.

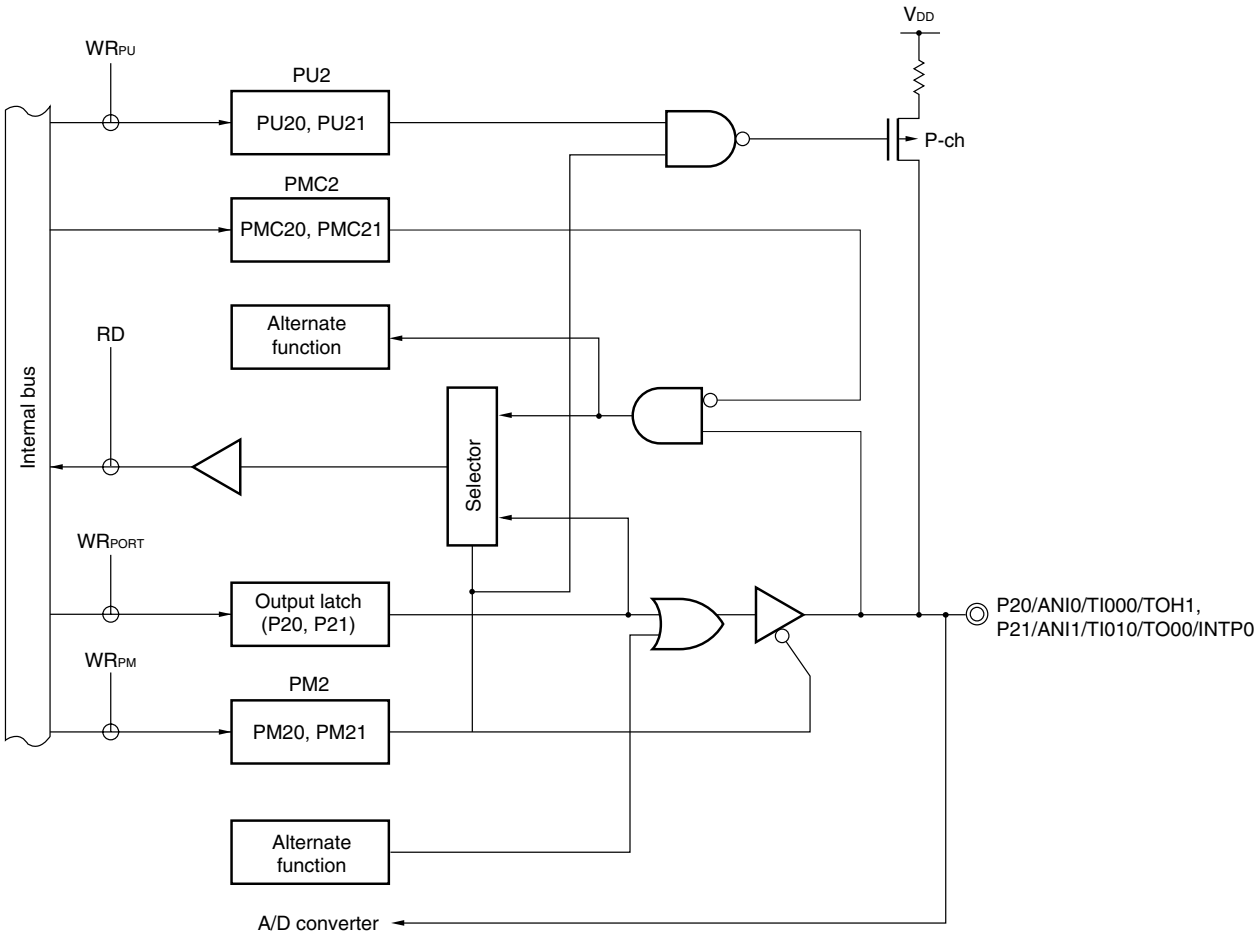
The P23 pin is used as the X1 pin to input an external clock, and therefore it cannot be used as an I/O port pin or an analog input pin to the A/D converter.

The system clock oscillation is selected by the option byte. For details, refer to **CHAPTER 15 OPTION BYTE**.

Reset input sets port 2 to the input mode.

Figure 4-2 and 4-3 show the block diagrams of port 2.

Figure 4-2. Block Diagram of P20 and P21



PU2: Pull-up resistor option register 2
PM2: Port mode register 2
PMC2: Port mode control register 2
RD: Read signal
WR××: Write signal

★ **Figure 4-3. Block Diagram of P22**

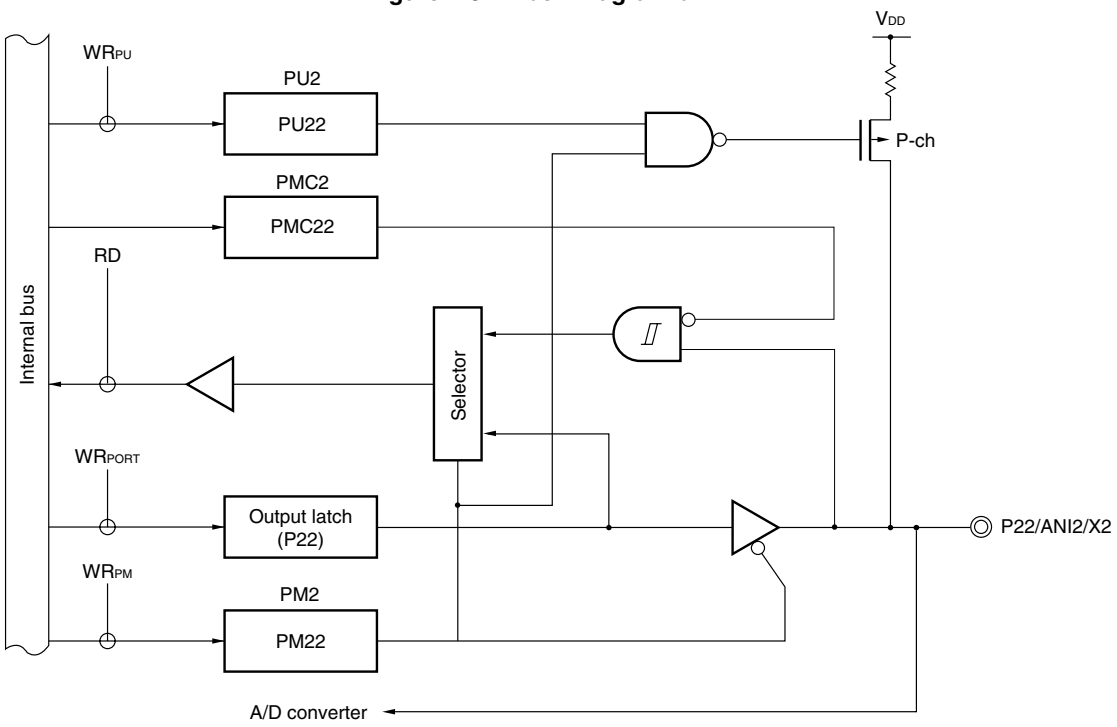
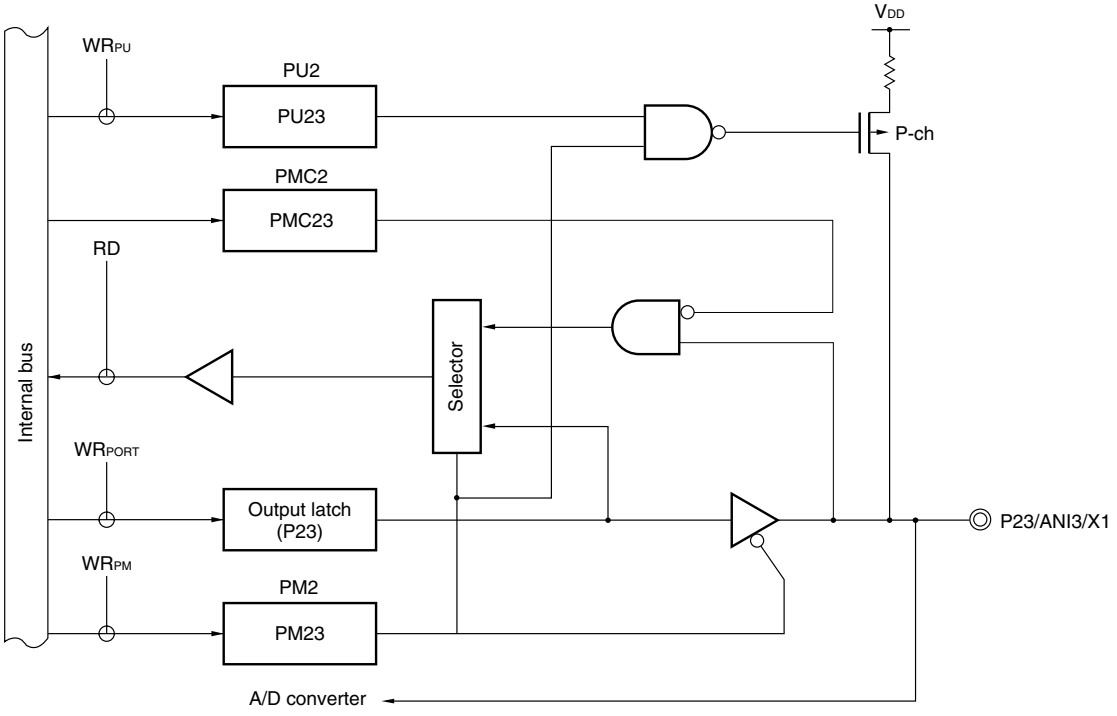


Figure 4-4. Block Diagram of P23



PU2: Pull-up resistor option register 2
PM2: Port mode register 2
PMC2: Port mode control register 2
RD: Read signal
WR××: Write signal

4.2.2 Port 3

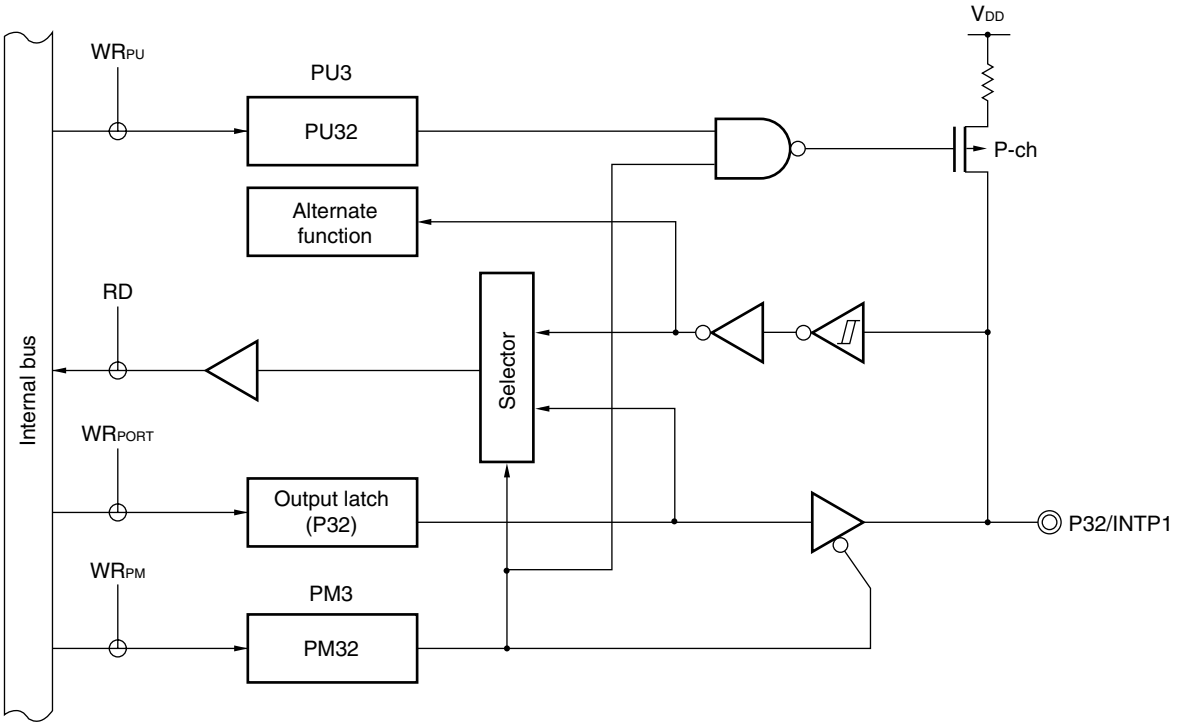
The P32 pin is a 1-bit I/O port with an output latch. This pin can be set to the input or output mode by using port mode register 3 (PM3). When this pin is used as an input port, an on-chip pull-up resistor can be connected in 1-bit units by using pull-up resistor option register 3 (PU3). This pin can also be used for external interrupt request input.

The P34 pin is a 1-bit input-only port and can also be used for the $\overline{\text{RESET}}$ input.

Reset input sets port 3 to the input mode.

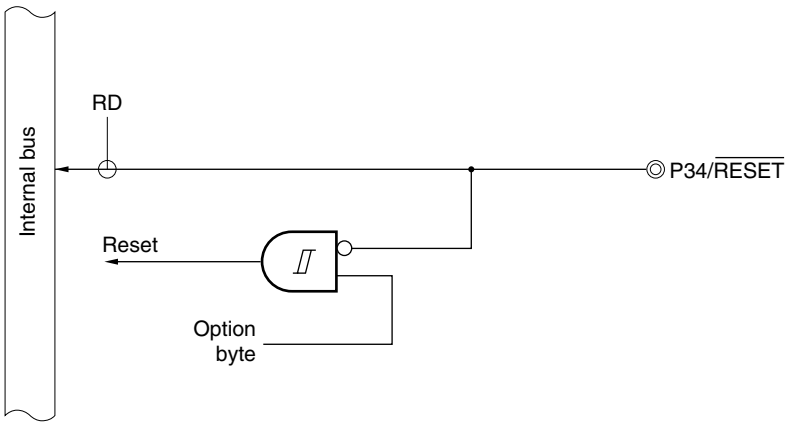
Figures 4-5 and 4-6 show the block diagrams of port 3.

Figure 4-5. Block Diagram of P32



PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Figure 4-6. Block Diagram of P34



RD: Read signal

Caution Because the P34 pin functions alternately as the $\overline{\text{RESET}}$ pin, if it is used as an input port pin, the function to input an external reset signal to the $\overline{\text{RESET}}$ pin cannot be used. The function of the port is selected by the option byte. For details, refer to CHAPTER 15 OPTION BYTE.
If a low level is input to the $\overline{\text{RESET}}$ pin before the option byte is referenced again after reset is released by the POC circuit, the 78K0S/KU1+ and 78K0S/KY1+ are reset and are held in the reset state until a high level is input to the $\overline{\text{RESET}}$ pin.

4.2.3 Port 4 (78K0S/KY1+ only)

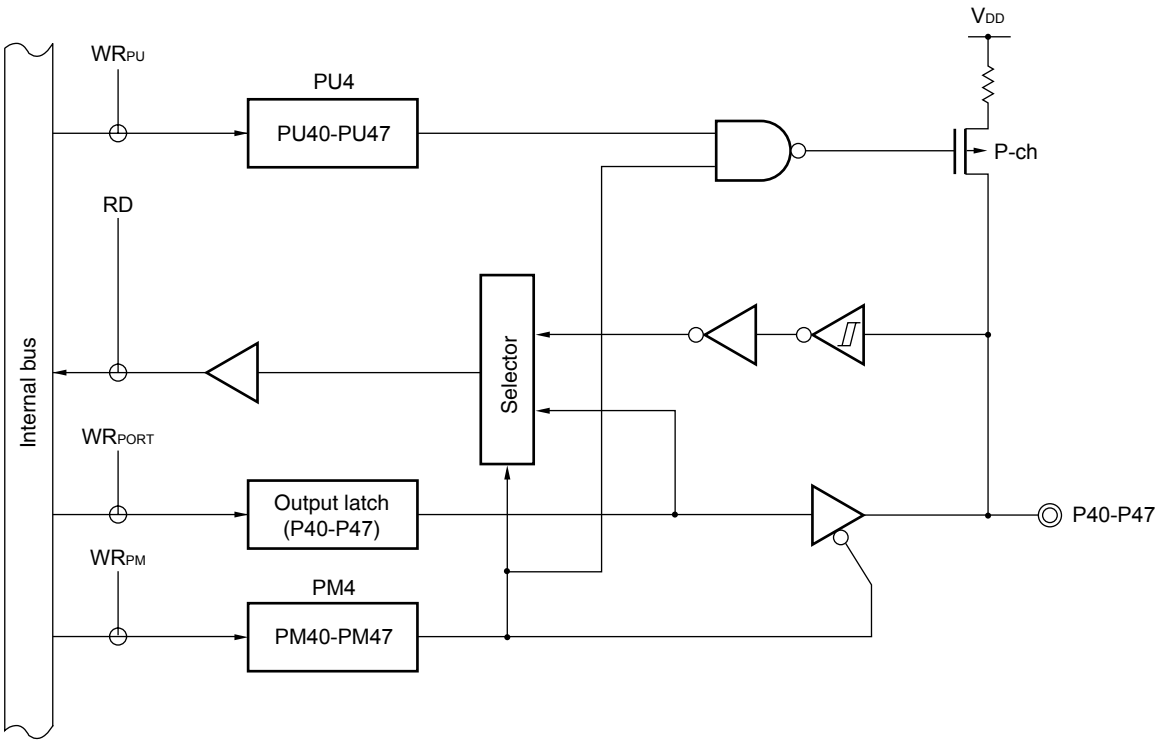
Port 4 is a 8-bit I/O port with an output latch. Each bit of this port can be set to the input or output mode by using port mode register 4 (PM4). When the P40 to P47 pins[Note] are used as an input port, an on-chip pull-up resistor can be connected in 1-bit units by using pull-up resistor option register 4 (PU4).

Reset input sets port 4 to the input mode.

Figures 4-6 shows the block diagram of port 4.

★ **Note** The P40 to P47 pins are provided only in the 78K0S/KY1+. When using the 78K0S/KU1+, set port mode register 4 (PM4) to 00H when initially setting the program.

Figure 4-7. Block Diagram of P40 and P47 (78K0S/KY1+ only)



PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

4.3 Registers Controlling Port Functions

The ports are controlled by the following four types of registers.

- Port mode registers (PM2 to PM4)
- Port registers (P2 to P4)
- Port mode control register 2 (PMC2)
- Pull-up resistor option registers (PU2 to PU4)

(1) Port mode registers (PM2 to PM4[Note])

These registers are used to set the corresponding port to the input or output mode in 1-bit units.

Each port mode register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset input sets these registers to FFH.

When a port pin is used as an alternate-function pin, set its port mode register and output latch as shown in Table 4-3.

★ **Note** When using the 78K0S/KU1+, set port mode register 4 (PM4) to 00H when initially setting the program.

Caution Because P21 and P32 are also used as external interrupt pins, the corresponding interrupt request flag is set if each of these pins is set to the output mode and its output level is changed. To use the port pin in the output mode, therefore, set the corresponding interrupt mask flag to 1 in advance.

Figure 4-8. Format of Port Mode Register

Address: FF22H, After reset: FFH, R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	1	1	PM23	PM22	PM21	PM20

Address: FF23H, After reset: FFH, R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	1	PM32	1	1

Address: FF24H, After reset: FFH, R/W

Symbol	7	6	5	4	3	2	1	0
PM4[Note]	PM47[Note]	PM46[Note]	PM45[Note]	PM44[Note]	PM43[Note]	PM42[Note]	PM41[Note]	PM40[Note]

PMmn	Selection of I/O mode of Pmn pin (m = 2 to 4; n = 0 to 7)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

★ **Note** When using the 78K0S/KU1+, set port mode register 4 (PM4) to 00H when initially setting the program.

(2) Port registers (P2 to P4)

These registers are used to write data to be output from the corresponding port pin to an external device connected to the chip.

When a port register is read, the pin level is read in the input mode, and the value of the output latch of the port is read in the output mode.

P20 to P23, P32, and P40 to P47 are set by using a 1-bit or 8-bit memory manipulation instruction.

Reset input sets these registers to 00H.

Figure 4-9. Format of Port Register

Address: FF02H, After reset: 00H (Output latch) R/W

Symbol	7	6	5	4	3	2	1	0
P2	0	0	0	0	P23	P22	P21	P20

Address: FF03H, After reset: 00H[Note] (Output latch) R/W[Note]

Symbol	7	6	5	4	3	2	1	0
P3	0	0	0	P34	0	P32	0	0

Address: FF04H, After reset: 00H (Output latch) R/W

Symbol	7	6	5	4	3	2	1	0
P4	P47	P46	P45	P44	P43	P42	P41	P40

Pmn	m = 2 to 4; n = 0 to 7	
	Controls of output data (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Note Because P34 is read-only, its reset value is undefined.

(3) Port mode control register 2 (PMC2)

This register specifies the port/alternate function (except the A/D converter function) mode or the A/D converter mode.

Each bit of the PMC2 register corresponds to each pin of port 2 and can be specified in 1-bit units.

PMC2 is set by using a 1-bit or 8-bit memory manipulation instruction.

Reset input sets PMC2 to 00H.

Figure 4-10. Format of Port Mode Control Register 2

Address: FF84H, After reset: R/W

Symbol	7	6	5	4	3	2	1	0
PMC2	0	0	0	0	PMC23	PMC22	PMC21	PMC20

PMC2n	Specification of operation mode (n = 0 to 3)
0	Port/alternate-function (except the A/D converter function) mode
1	A/D converter mode

Table 4-3. Setting of Port Mode Register, Port Register (Output Latch), and Port Mode Control Register When Alternate Function Is Used

Pin Name	Alternate-Function Pin		PM××	P××	PMC2n (n = 0 to 3)
	Name	I/O			
P20	ANI0	Input	1	×	1
	TI000	Input	1	×	0
	TOH1	Output	0	0	0
P21	ANI1	Input	1	×	1
	TI010	Input	1	×	0
	TO00	Output	0	0	0
	INTP0	Input	1	×	0
P22	ANI2	Input	1	×	1
P23	ANI3	Input	1	×	1
P32	INTP1	Input	1	×	–

Remark ×: don't care

PM××: Port mode register, P××: Port register (output latch of port)

PMC2×: Port mode control register

(4) Pull-up resistor option registers (PU2 to PU4)

These registers are used to specify whether an on-chip pull-up resistor is connected to P20 to P23, P32, and P40 to P47. By setting PU2 to PU4, an on-chip pull-up resistor can be connected to the port pin corresponding to the bit of PU2 to PU4.

PU2 to PU4 are set by using a 1-bit or 8-bit memory manipulation instruction.

Reset input set these registers to 00H.

Figure 4-11. Format of Pull-up Resistor Option Register

Address: FF32H, After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU2	0	0	0	0	PU23	PU22	PU21	PU20

Address: FF33H, After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU3	0	0	0	0	0	PU32	0	0

Address: FF34H, After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU4	PU47	PU46	PU45	PU44	PU43	PU42	PU41	PU40

PUmn	Selection of connection of on-chip pull-up resistor of Pmn (m = 2 to 4; n = 0 to 7)
0	Does not connect on-chip pull-up resistor
1	Connects on-chip pull-up resistor

4.4 Operation of Port Function

The operation of a port differs, as follows, depending on the setting of the I/O mode.

Caution Although a 1-bit memory manipulation instruction manipulates 1 bit, it accesses a port in 8-bit units. Therefore, the contents of the output latch of a pin in the input mode, even if it is not subject to manipulation by the instruction, are undefined in a port with a mixture of inputs and outputs.

4.4.1 Writing to I/O port

(1) In output mode

A value can be written to the output latch by a transfer instruction. In addition, the contents of the output latch are output from the pin. Once data is written to the output latch, it is retained until new data is written to the output latch.

Reset input cleans the data in the output latch.

(2) In input mode

A value can be written to the output latch by a transfer instruction. Because the output buffer is off, however, the pin status remains unchanged.

Once data is written to the output latch, it is retained until new data is written to the output latch.

4.4.2 Reading from I/O port

(1) In output mode

The contents of the output latch can be read by a transfer instruction. The contents of the output latch remain unchanged.

(2) In input mode

The pin status can be read by a transfer instruction. The contents of the output latch remain unchanged.

4.4.3 Operations on I/O port

(1) In output mode

An operation is performed on the contents of the output latch and the result is written to the output latch. The contents of the output latch are output from the pin.

Once data is written to the output latch, it is retained until new data is written to the output latch.

Reset input clears the data in the output latch.

(2) In input mode

The pin level is read and an operation is performed on its contents. The operation result is written to the output latch. However, the pin status remains unchanged because the output buffer is off.

CHAPTER 5 CLOCK GENERATORS

5.1 Functions of Clock Generators

The clock generators include a circuit that generates a clock (system clock) to be supplied to the CPU and peripheral hardware, and a circuit that generates a clock (interval time generation clock) to be supplied to the watchdog timer and 8-bit timer H1 (TMH1).

5.1.1 System clock oscillators

The following three types of system clock oscillators are used.

- High-speed Ring-OSC oscillator
  This circuit internally oscillates a clock of 8 MHz (TYP.). Its oscillation can be stopped by execution of the STOP instruction.
  If the high-speed Ring-OSC oscillator is selected to supply the system clock, the X1 and X2 pins can be used as I/O port pins.

- Crystal/ceramic oscillator
  This circuit oscillates a clock with a crystal/ceramic oscillator connected across the X1 and X2 pins. It can ★ oscillate a clock of 1 MHz to 10 MHz. Oscillation of this circuit can be stopped by execution of the STOP instruction.

- External clock input circuit
  ★ This circuit supplies a clock from an external IC to the X1 pin. A clock of 1 MHz to 10 MHz can be supplied. Internal clock supply can be stopped by execution of the STOP instruction.
  If the external clock input is selected as the system clock, the X2 pin can be used as an I/O port pin.

The system clock source is selected by using the option byte. For details, refer to **CHAPTER 15 OPTION BYTE**.
When using the X1 and X2 pins as I/O port pins, refer to **CHAPTER 4 PORT FUNCTIONS** for details.

5.1.2 Clock oscillator for interval time generation

The following circuit is used as a clock oscillator for interval time generation.

- Low-speed Ring-OSC oscillator
  This circuit oscillates a clock of 240 kHz (TYP.). Its oscillation can be stopped by using the low-speed Ring-OSC mode register (LSRCM) when it is specified by the option byte that its oscillation can be stopped by software.

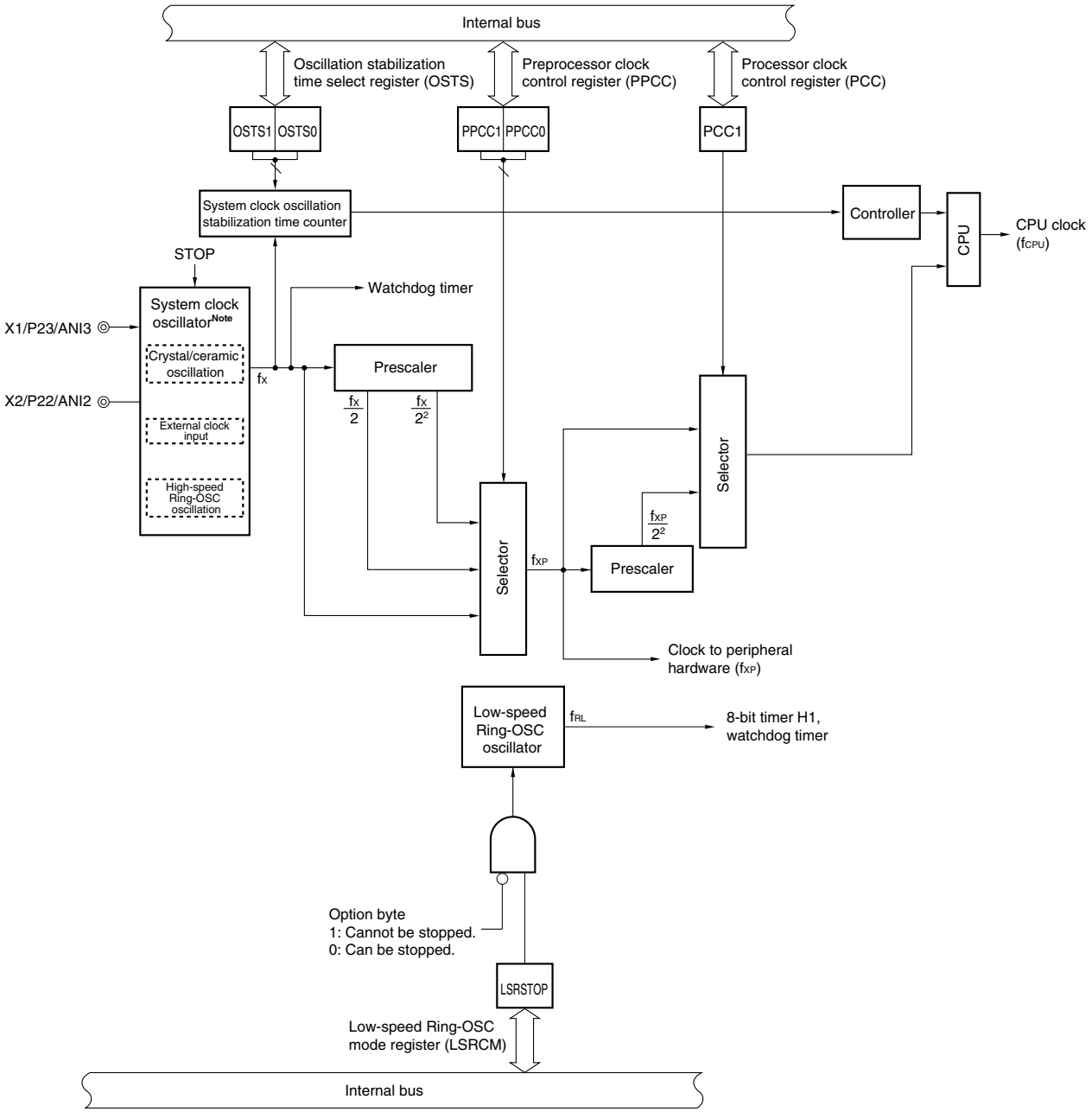
5.2 Configuration of Clock Generators

The clock generators consist of the following hardware.

Table 5-1. Configuration of Clock Generators

Item	Configuration
Control registers	Processor clock control register (PCC) Preprocessor clock control register (PPCC) Low-speed Ring-OSC mode register (LSRCM) Oscillation stabilization time select register (OSTS)
Oscillators	Crystal/ceramic oscillator High-speed Ring-OSC oscillator External clock input circuit Low-speed Ring-OSC oscillator

★ **Figure 5-1. Block Diagram of Clock Generators**



Note Select the high-speed Ring-OSC oscillator, crystal/ceramic oscillator, or external clock input as the system clock source by using the option byte.

5.3 Registers Controlling Clock Generators

The clock generators are controlled by the following four registers.

- Processor clock control register (PCC)
- Preprocessor clock control register (PPCC)
- Low-speed Ring-OSC mode register (LSRCM)
- Oscillation stabilization time select register (OSTS)

(1) Processor clock control register (PCC) and preprocessor clock control register (PPCC)

These registers are used to specify the division ratio of the system clock.

PCC and PPCC are set by using a 1-bit or 8-bit memory manipulation instruction.

Reset input sets PCC and PPCC to 02H.

Figure 5-2. Format of Processor Clock Control Register (PCC)

Address: FFFBH, After reset: 02H, R/W

Symbol	7	6	5	4	3	2	1	0
PCC	0	0	0	0	0	0	PCC1	0

Figure 5-3. Format of Preprocessor Clock Control Register (PPCC)

Address: FFF3H, After reset: 02H, R/W

Symbol	7	6	5	4	3	2	1	0
PPCC	0	0	0	0	0	0	PPCC1	PPCC0

PPCC1	PPCC0	PCC1	Selection of CPU clock (f_{CPU})
0	0	0	f_X
0	1	0	$f_X/2$ Note 1
0	0	1	$f_X/2^2$
1	0	0	$f_X/2^2$ Note 2
0	1	1	$f_X/2^3$ Note 1
1	0	1	$f_X/2^4$ Note 2
Other than above			Setting prohibited

Notes 1. If PPCC = 01H, the clock (f_{XP}) supplied to the peripheral hardware is $f_X/2$.

2. If PPCC = 02H, the clock (f_{XP}) supplied to the peripheral hardware is $f_X/2^2$.

The fastest instruction of the 78K0S/KU1+ and 78K0S/KY1+ is executed in two CPU clocks. Therefore, the relationship between the CPU clock (f_{CPU}) and the minimum instruction execution time is as shown in Table 5-2.

Table 5-2. Relationship between CPU Clock and Minimum Instruction Execution Time

CPU Clock (f_{CPU}) Note	Minimum Instruction Execution Time: $2/f_{CPU}$	
	High-speed Ring-OSC clock (at 8.0 MHz (TYP.))	Crystal/ceramic oscillation clock or external clock input (at 10.0 MHz)
f_X	0.25 μs	0.2 μs
$f_X/2$	0.5 μs	0.4 μs
$f_X/2^2$	1.0 μs	0.8 μs
$f_X/2^3$	2.0 μs	1.6 μs
$f_X/2^4$	4.0 μs	3.2 μs

Note The CPU clock (high-speed Ring-OSC clock, crystal/ceramic oscillation clock, or external clock input) is selected by the option byte.

(2) Low-speed Ring-OSC mode register (LSRCM)

This register is used to select the operation mode of the low-speed Ring-OSC oscillator (240 kHz (TYP.)).

This register is valid when it is specified by the option byte that the low-speed Ring-OSC oscillator can be stopped by software. If it is specified by the option byte that the low-speed Ring-OSC oscillator cannot be stopped by software, setting of this register is invalid, and the low-speed Ring-OSC oscillator continues oscillating. In addition, the source clock of WDT is fixed to the low-speed Ring-OSC oscillator. For details, refer to **CHAPTER 8 WATCHDOG TIMER**.

LSRCM can be set by using a 1-bit or 8-bit memory manipulation instruction.

Reset input sets LSRCM to 00H.

Figure 5-4. Format of Low-Speed Ring-OSC Mode Register (LSRCM)

Address: FF58H, After reset: 00H, R/W

Symbol	7	6	5	4	3	2	1	<0>
LSRCM	0	0	0	0	0	0	0	LSRSTOP

LSRSTOP	Oscillation/stop of low-speed Ring-OSC
0	Low-speed Ring-OSC oscillates
1	Low-speed Ring-OSC stops

(3) Oscillation stabilization time select register (OSTS)

This register is used to select oscillation stabilization time of the clock supplied from the oscillator when the STOP mode is released. The wait time set by OSTS is valid only when the crystal/ceramic oscillation clock is selected as the system clock and after the STOP mode is released. If the high-speed Ring-OSC oscillator or external clock input is selected as the system clock source, no wait time elapses.

The system clock oscillator and the oscillation stabilization time that elapses after power application or release of reset are selected by the option byte. For details, refer to **CHAPTER 15 OPTION BYTE**.

OSTS is set by using an 8-bit memory manipulation instruction.

Figure 5-5. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFF4H, After reset: Undefined, R/W

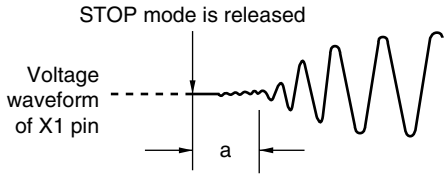
Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	0	OSTS1	OSTS0

OSTS1	OSTS0	Selection of oscillation stabilization time
0	0	$2^{10}/f_X$ (102.4 μs)
0	1	$2^{12}/f_X$ (409.6 μs)
1	0	$2^{15}/f_X$ (3.27 ms)
1	1	$2^{17}/f_X$ (13.1 ms)

Cautions 1. To set and then release the STOP mode, set the oscillation stabilization time as follows.

Expected oscillation stabilization time of resonator ≤ Oscillation stabilization time set by OSTS

2. The wait time after the STOP mode is released does not include the time from the release of the STOP mode to the start of clock oscillation (“a” in the next figure), regardless of whether STOP mode was released by reset input or interrupt generation.



3. The oscillation stabilization time that elapses on power application or after release of reset is selected by the option byte. For details, refer to CHAPTER 15 OPTION BYTE.

Remarks 1. ( ): f_X = 10 MHz

2. Determine the oscillation stabilization time of the resonator by checking the characteristics of the resonator to be used.

5.4 System Clock Oscillators

The following three types of system clock oscillators are available.

- High-speed Ring-OSC oscillator: Internally oscillates a clock of 8 MHz (TYP.).
- ★ • Crystal/ceramic oscillator: Oscillates a clock of 1 MHz to 10 MHz.
- ★ • External clock input circuit: Supplies a clock of 1 MHz to 10 MHz to the X1 pin.

5.4.1 High-speed Ring-OSC oscillator

The 78K0S/KU1+ and 78K0S/KY1+ include a high-speed Ring-OSC oscillator (8 MHz (TYP.)).

If the high-speed Ring-OSC is selected by the option byte as the clock source, the X1 and X2 pins can be used as I/O port pins.

For details of the option byte, refer to **CHAPTER 15 OPTION BYTE**. For details of I/O ports, refer to **CHAPTER 4 PORT FUNCTIONS**.

5.4.2 Crystal/ceramic oscillator

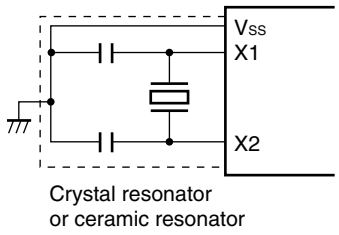
The crystal/ceramic oscillator oscillates using a crystal or ceramic resonator connected between the X1 and X2 pins.

If the crystal/ceramic oscillator is selected by the option byte as the system clock source, the X1 and X2 pins are used as crystal or ceramic resonator connection pins.

For details of the option byte, refer to **CHAPTER 15 OPTION BYTE**. For details of I/O ports, refer to **CHAPTER 4 PORT FUNCTIONS**.

Figure 5-6 shows the external circuit of the crystal/ceramic oscillator.

Figure 5-6. External Circuit of Crystal/Ceramic Oscillator



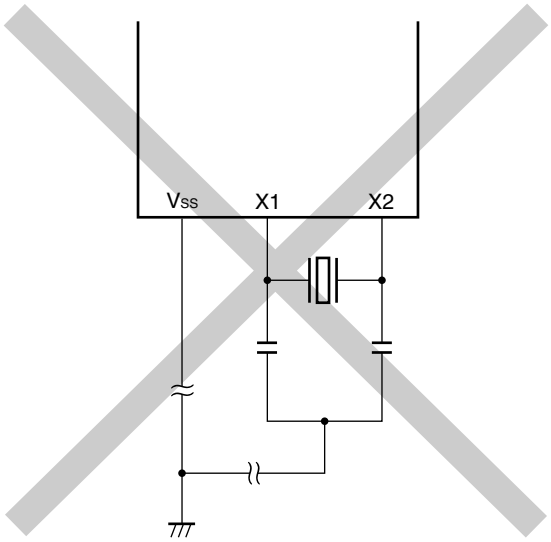
Caution When using the crystal/ceramic oscillator, wire as follows in the area enclosed by the broken lines in Figure 5-6 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as Vss. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

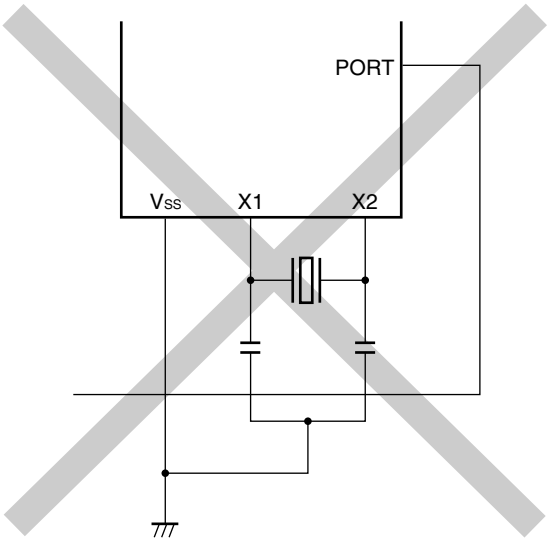
Figure 5-7 shows examples of incorrect resonator connection.

Figure 5-7. Examples of Incorrect Resonator Connection (1/2)

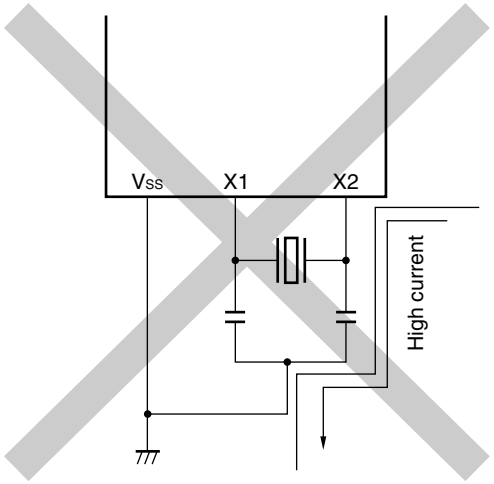
(a) Too long wiring of connected circuit



(b) Crossed signal lines



(c) Wiring near high fluctuating current



(d) Current flowing through ground line of oscillator
(Potential at points A, B, and C fluctuates.)

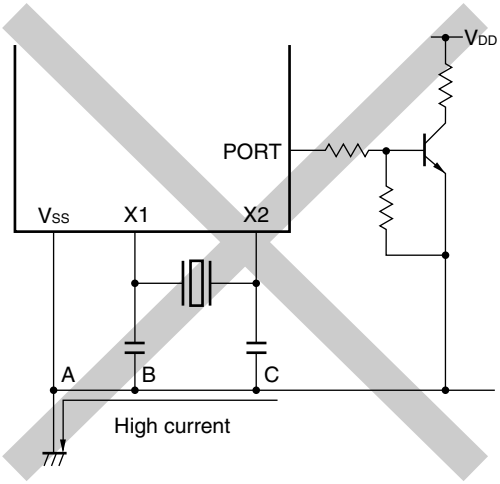
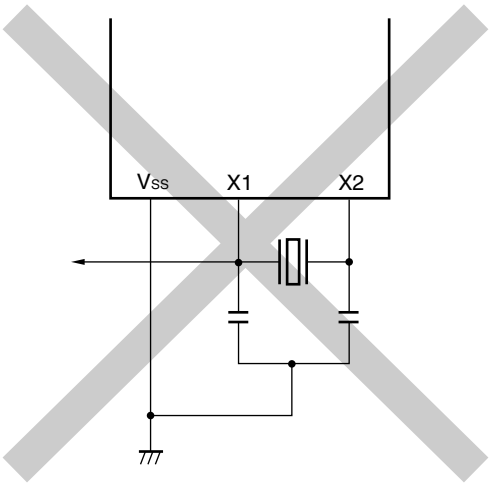


Figure 5-7. Examples of Incorrect Resonator Connection (2/2)

(e) Signals are fetched



5.4.3 External clock input circuit

This circuit supplies a clock from an external IC to the X1 pin.

If external clock input is selected by the option byte as the system clock source, the X2 pin can be used as an I/O port pin.

For details of the option byte, refer to **CHAPTER 15 OPTION BYTE**. For details of I/O ports, refer to **CHAPTER 4 PORT FUNCTIONS**.

5.4.4 Prescaler

The prescaler divides the clock (f_X) output by the system clock oscillator to generate a clock (f_{XP}) to be supplied to the peripheral hardware. It also divides the clock to peripheral hardware (f_{XP}) to generate a clock to be supplied to the CPU.

Remark The clock output by the oscillator selected by the option byte (high-speed Ring-OSC oscillator, crystal/ceramic oscillator, or external clock input circuit) is divided. For details of the option byte, refer to **CHAPTER 15 OPTION BYTE**.

5.5 Operation of CPU Clock Generator

A clock (f_{CPU}) is supplied to the CPU from the system clock (f_X) oscillated by one of the following three types of oscillators.

- High-speed Ring-OSC oscillator: Internally oscillates a clock of 8 MHz (TYP.).
- ★ • Crystal/ceramic oscillator: Oscillates a clock of 1 MHz to 10 MHz.
- ★ • External clock input circuit: Supplies a clock of 1 MHz to 10 MHz to X1 pin.

The system clock oscillator is selected by the option byte. For details of the option byte, refer to **CHAPTER 15 OPTION BYTE**.

(1) High-speed Ring-OSC oscillator

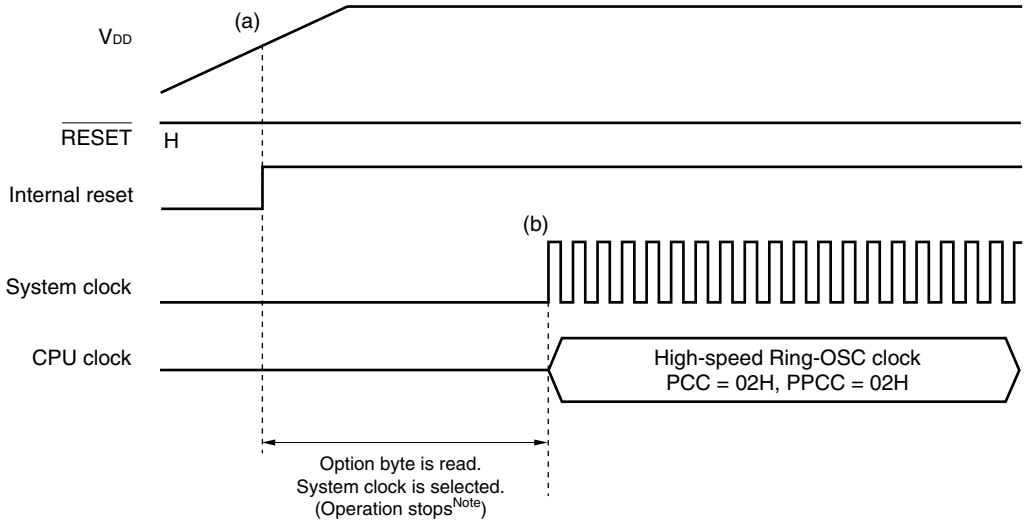
When the high-speed Ring-OSC oscillator is selected by the option byte, the following is possible.

- Shortening of start time
  If the high-speed Ring-OSC oscillator is selected as the oscillator, the CPU can be started without having to wait for the oscillation stabilization time of the system clock. Therefore, the start time can be shortened.
- Improvement of expandability
  If the high-speed Ring-OSC oscillator is selected as the oscillator, the X1 and X2 pins can be used as I/O port pins. For details, refer to **CHAPTER 4 PORT FUNCTIONS**.

Figures 5-8 and 5-9 show the timing chart and status transition diagram of the default start by the high-speed Ring-OSC oscillator.

Remark When the high-speed Ring-OSC oscillator is used, the clock accuracy is ±5%.

Figure 5-8. Timing Chart of Default Start by High-Speed Ring-OSC Oscillator

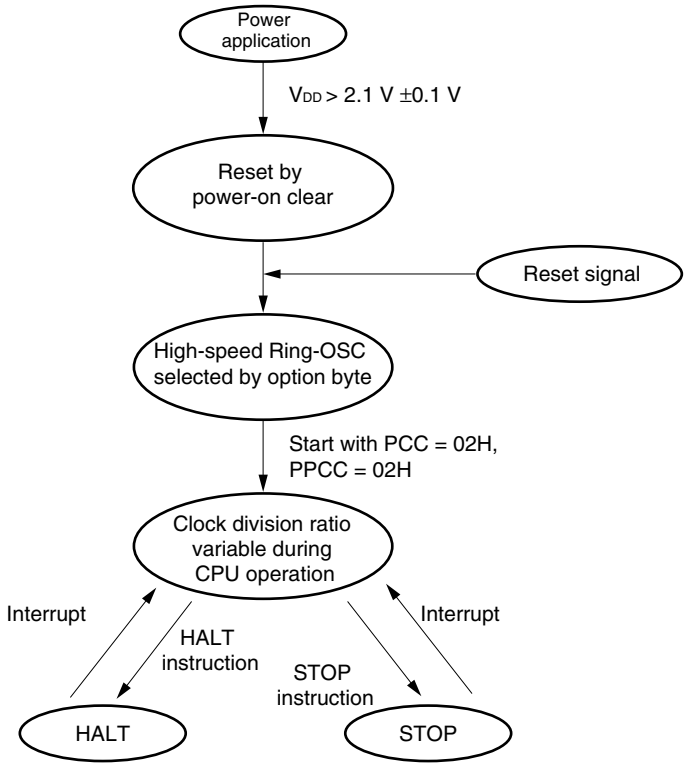


★ **Note** Operation stop time is 277 μs (MIN.), 544 μs (TYP.), and 1.075 ms (MAX.).

(a) The internal reset signal is generated by the power-on clear function on power application, the option byte is referenced after reset, and the system clock is selected.

(b) The option byte is referenced and the system clock is selected. Then the high-speed Ring-OSC clock operates as the system clock.

Figure 5-9. Status Transition of Default Start by High-Speed Ring-OSC



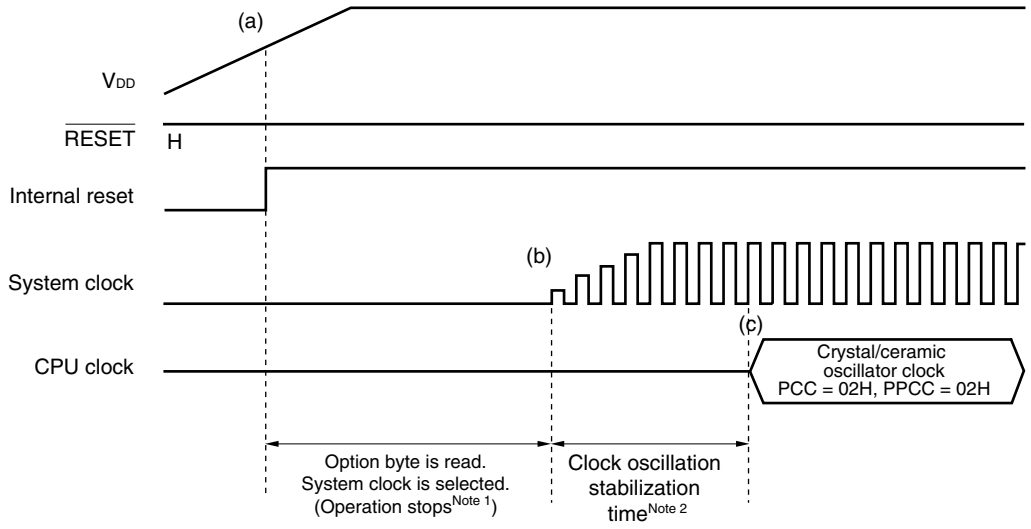
Remark PCC: Processor clock control register
PPCC: Preprocessor clock control register

(2) Crystal/ceramic oscillator

If crystal/ceramic oscillation is selected by the option byte, a clock frequency of 1 MHz to 10 MHz can be selected and the accuracy of processing is improved because the frequency deviation is small, as compared with high-speed Ring-OSC oscillation (8 MHz (TYP.)).

Figures 5-10 and 5-11 show the timing chart and status transition diagram of default start by the crystal/ceramic oscillator.

Figure 5-10. Timing Chart of Default Start by Crystal/Ceramic Oscillator



★ **Notes 1.** Operation stop time is 276 μs (MIN.), 544 μs (TYP.), and 1.074 ms (MAX.).

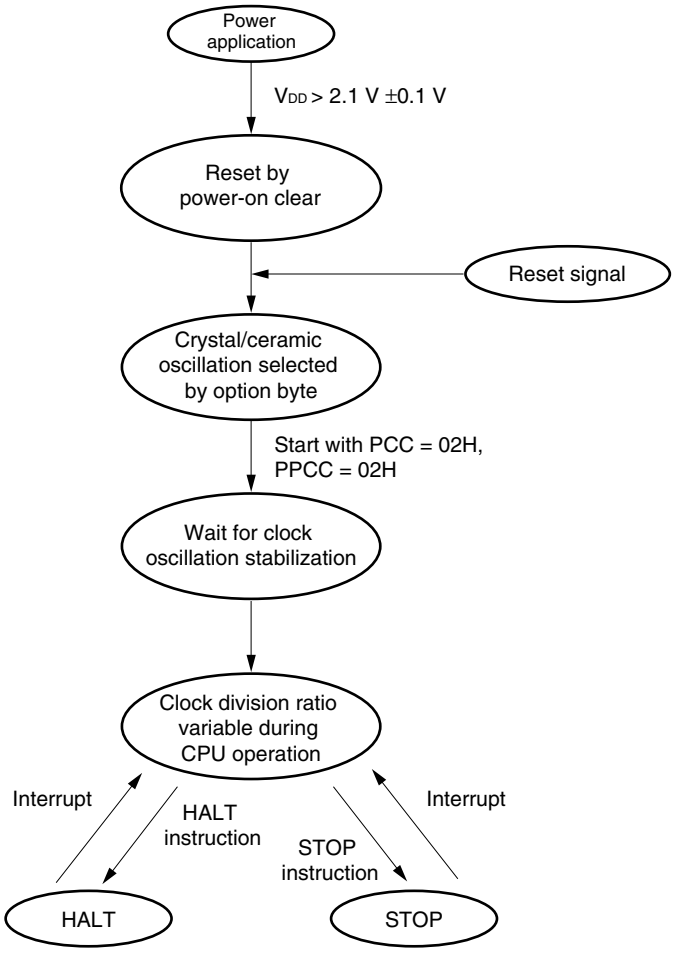
2. The clock oscillation stabilization time for default start is selected by the option byte. For details, refer to **CHAPTER 15 OPTION BYTE**. The oscillation stabilization time that elapses after the STOP mode is released is selected by the oscillation stabilization time select register (OSTS).

(a) The internal reset signal is generated by the power-on clear function on power application, the option byte is referenced after reset, and the system clock is selected.

(b) After high-speed Ring-OSC clock is generated, the option byte is referenced and the system clock is selected. In this case, the crystal/ceramic oscillator clock is selected as the system clock.

(c) If the system clock is the crystal/ceramic oscillator clock, it starts operating as the CPU clock after clock oscillation is stabilized. The wait time is selected by the option byte. For details, refer to **CHAPTER 15 OPTION BYTE**.

Figure 5-11. Status Transition of Default Start by Crystal/Ceramic Oscillation



Remark PCC: Processor clock control register
PPCC: Preprocessor clock control register

(3) External clock input circuit

If external clock input is selected by the option byte, the following is possible.

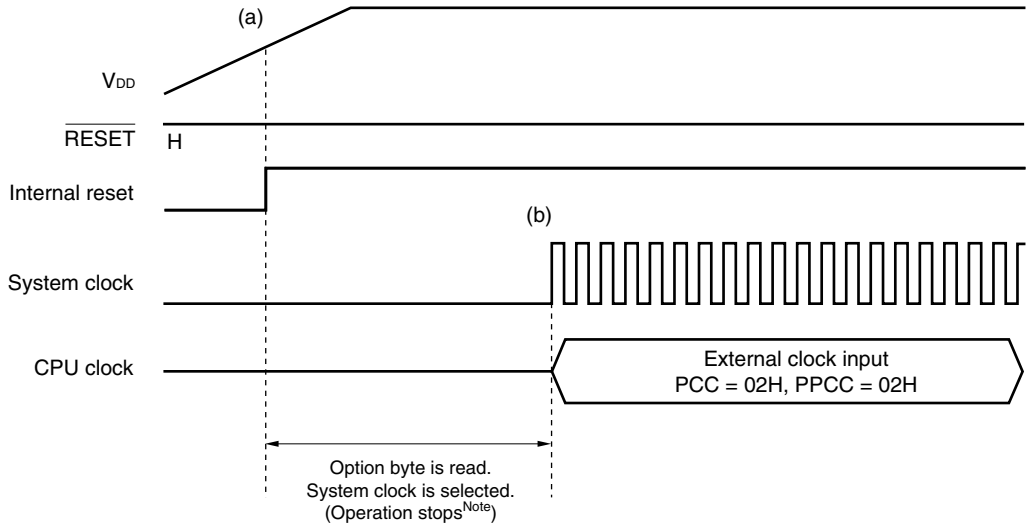
- High-speed operation

  The accuracy of processing is improved as compared with high-speed Ring-OSC oscillation (8 MHz (TYP.)) ★ because an oscillation frequency of 1 MHz to 10 MHz can be selected and an external clock with a small frequency deviation can be supplied.
- Improvement of expandability

  If the external clock input circuit is selected as the oscillator, the X2 pin can be used as an I/O port pin. For details, refer to **CHAPTER 4 PORT FUNCTIONS**.

Figures 5-12 and 5-13 show the timing chart and status transition diagram of default start by external clock input.

Figure 5-12. Timing of Default Start by External Clock Input

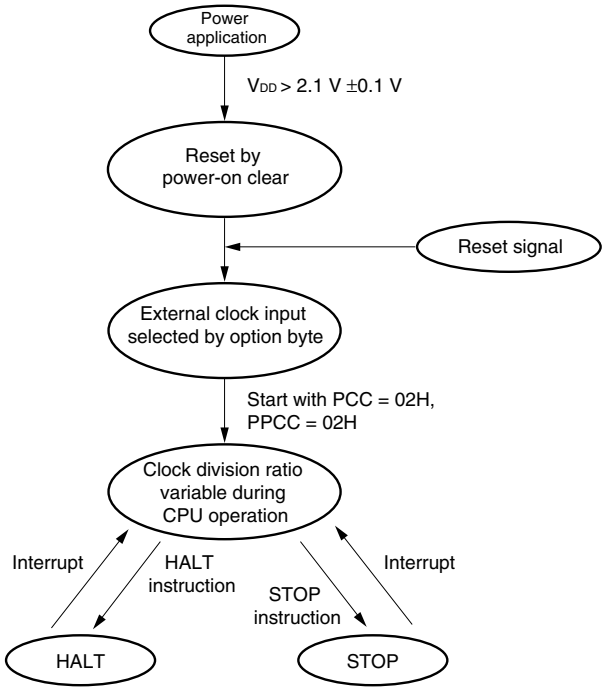


★ **Note** Operation stop time is 277 μs (MIN.), 544 μs (TYP.), and 1.075 ms (MAX.).

(a) The internal reset signal is generated by the power-on clear function on power application, the option byte is referenced after reset, and the system clock is selected.

(b) The option byte is referenced and the system clock is selected. Then the external clock operates as the system clock.

Figure 5-13. Status Transition of Default Start by External Clock Input



Remark PCC: Processor clock control register
PPCC: Preprocessor clock control register

5.6 Operation of Clock Generator Supplying Clock to Peripheral Hardware

The following two types of clocks are supplied to the peripheral hardware.

- Clock to peripheral hardware (f_{XP})
- Low-speed Ring-OSC clock (f_{RL})

(1) Clock to peripheral hardware

The clock to the peripheral hardware is supplied by dividing the system clock (f_X). The division ratio is selected by the pre-processor clock control register (PPCC).

Three types of frequencies are selectable: "f_X", "$f_X/2$", and "$f_X/2^2$". Table 5-3 lists the clocks supplied to the peripheral hardware.

Table 5-3. Clocks to Peripheral Hardware

PPCC1	PPCC0	Selection of clock to peripheral hardware (f_{XP})
0	0	f_X
0	1	$f_X/2$
1	0	$f_X/2^2$
1	1	Setting prohibited

(2) Low-speed Ring-OSC clock

The low-speed Ring-OSC oscillator of the clock oscillator for interval time generation is always started after release of reset, and oscillates at 240 kHz (TYP.).

It can be specified by the option byte whether the low-speed Ring-OSC oscillator can or cannot be stopped by software. If it is specified that the low-speed Ring-OSC oscillator can be stopped by software, oscillation can be started or stopped by using the low-speed Ring-OSC mode register (LSRCM). If it is specified that it cannot be stopped by software, the clock source of WDT is fixed to the low-speed Ring-OSC clock (f_{RL}).

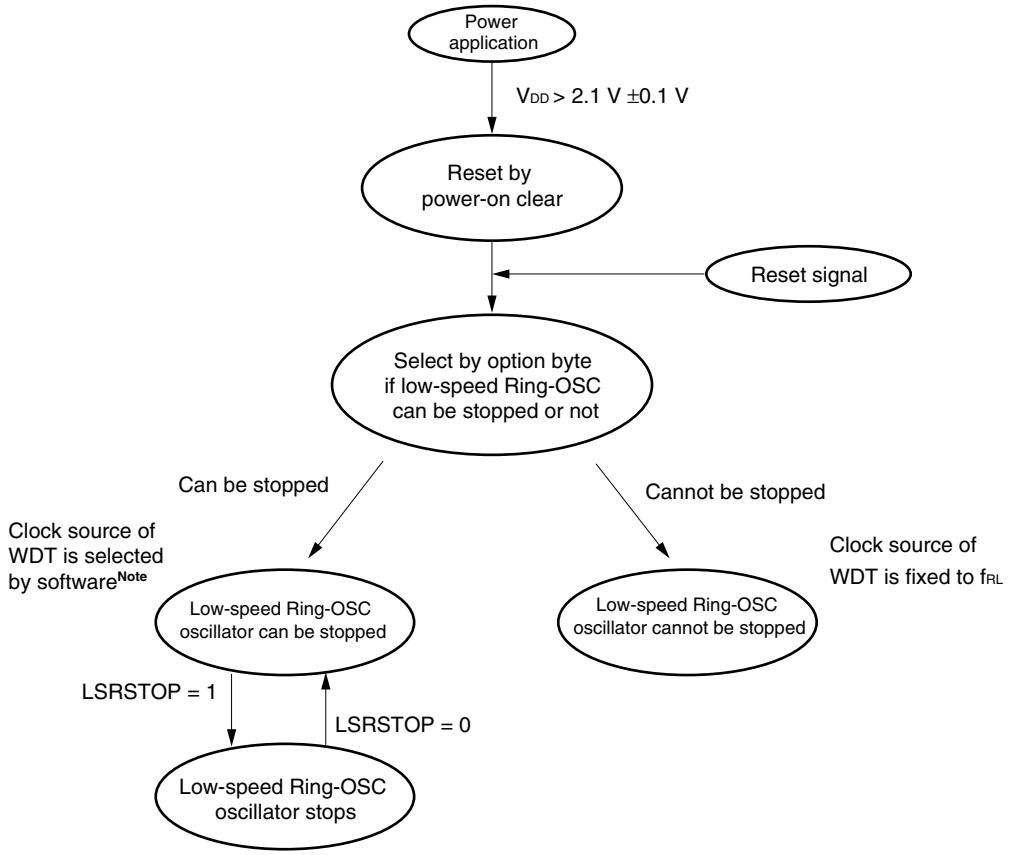
The low-speed Ring-OSC oscillator is independent of the CPU clock. If it is used as the source clock of WDT, therefore, a hang-up can be detected even if the CPU clock is stopped. If the low-speed Ring-OSC oscillator is used as a count clock source of 8-bit timer H1, 8-bit timer H1 can operate even in the standby status.

Table 5-4 shows the operation status of the low-speed Ring-OSC oscillator when it is selected as the source clock of WDT and the count clock of 8-bit timer H1. Figure 5-14 shows the status transition of the low-speed Ring-OSC oscillator.

Table 5-4. Operation Status of Low-Speed Ring-OSC Oscillator

Option Byte Setting		CPU Status	WDT Status	TMH1 Status
Can be stopped by software	LSRSTOP = 1	Operation mode	Stopped	Stopped
	LSRSTOP = 0		Operates	Operates
	LSRSTOP = 1	Standby	Stopped	Stopped
	LSRSTOP = 0		Stopped	Operates
Cannot be stopped		Operation mode	Operates	
		Standby		

Figure 5-14. Status Transition of Low-Speed Ring-OSC Oscillator



Note The clock source of the watchdog timer (WDT) is selected from f_X or f_{RL}, or it may be stopped. For details, refer to **CHAPTER 8 WATCHDOG TIMER**.

CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00

6.1 Functions of 16-Bit Timer/Event Counter 00

16-bit timer/event counter 00 has the following functions.

(1) Interval timer

16-bit timer/event counter 00 generates interrupt requests at the preset time interval.

- Number of counts: 2 to 65536

(2) External event counter

16-bit timer/event counter 00 can measure the number of pulses with a high-/low-level width of a signal input externally.

- Valid level pulse width: $16/f_{XP}$ or more

(3) Pulse width measurement

16-bit timer/event counter 00 can measure the pulse width of an externally input signal.

- Valid level pulse width: $2/f_{XP}$ or more

(4) Square-wave output

16-bit timer/event counter 00 can output a square wave with any selected frequency.

- Cycle: $(2 \times 2$ to $65536 \times 2) \times$ count clock cycle

(5) PPG output

16-bit timer/event counter 00 can output a square wave that have arbitrary cycle and pulse width.

- 1 < Pulse width < Cycle ≤ (FFFF + 1) H

(6) One-shot pulse output

16-bit timer/event counter 00 can output a one-shot pulse for which output pulse width can be set to any desired value.

6.2 Configuration of 16-Bit Timer/Event Counter 00

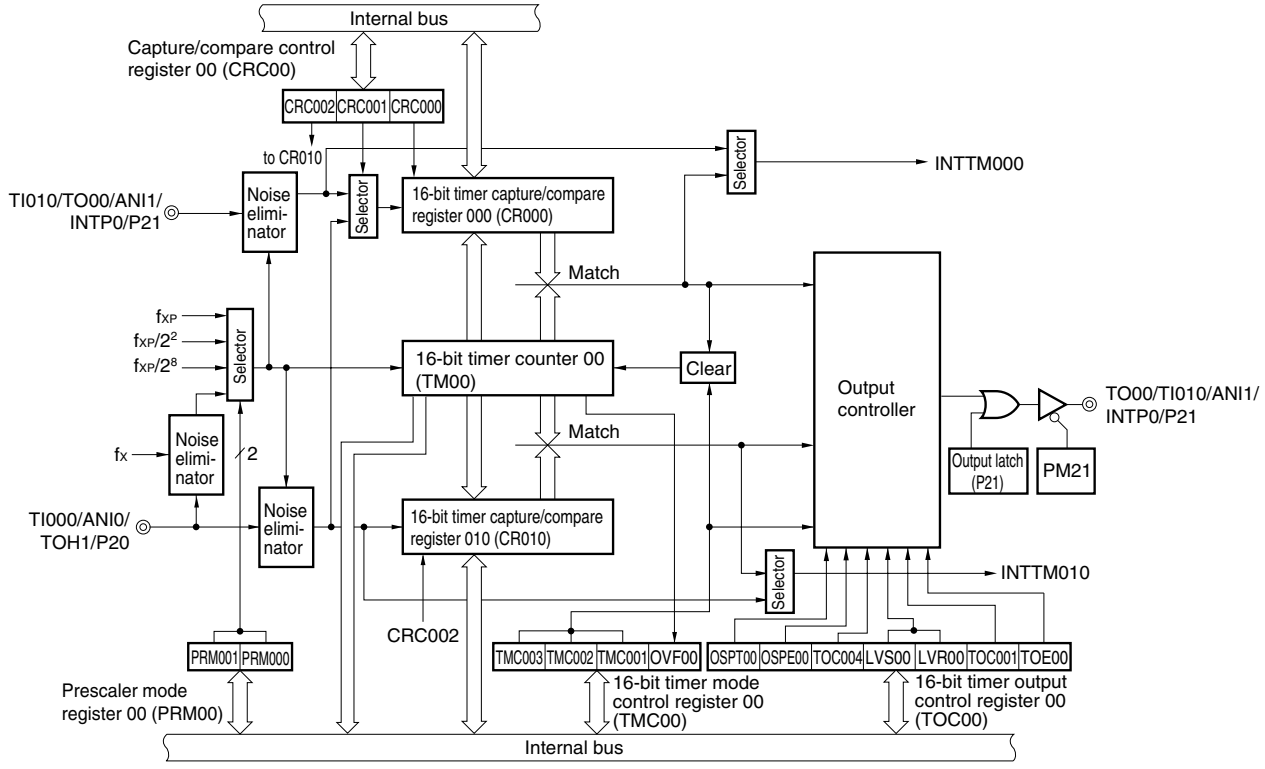
16-bit timer/event counter 00 consists of the following hardware.

Table 6-1. Configuration of 16-Bit Timer/Event Counter 00

Item	Configuration
Timer counter	16-bit timer counter 00 (TM00)
Register	16-bit timer capture/compare registers 000, 010 (CR000, CR010)
Timer input	TI000, TI010
Timer output	TO00, output controller
Control registers	16-bit timer mode control register 00 (TMC00) Capture/compare control register 00 (CRC00) 16-bit timer output control register 00 (TOC00) Prescaler mode register 00 (PRM00) Port mode register 2 (PM2) Port register 2 (P2) Port mode control register 2 (PMC2)

Figures 6-1 shows a block diagram of these counters.

Figure 6-1. Block Diagram of 16-Bit Timer/Event Counter 00

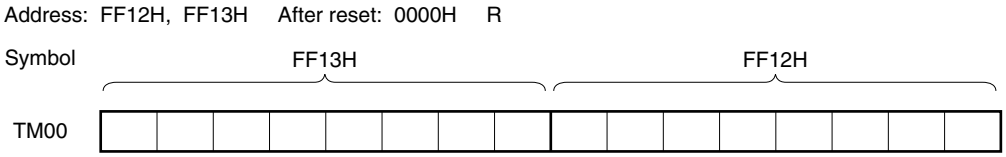


(1) 16-bit timer counter 00 (TM00)

TM00 is a 16-bit read-only register that counts count pulses.

The counter is incremented in synchronization with the rising edge of the count clock. If the count value is read during operation, input of the count clock is temporarily stopped, and the count value at that point is read.

Figure 6-2. Format of 16-Bit Timer Counter 00 (TM00)



The count value is reset to 0000H in the following cases.

<1> At reset input
<2> If TMC003 and TMC002 are cleared
<3> If the valid edge of TI000 is input in the clear & start mode entered by inputting the valid edge of TI000
<4> If TM00 and CR000 match in the clear & start mode entered on a match between TM00 and CR000
<5> If OSPT00 is set to 1 in the one-shot pulse output mode

★ **Cautions 1. Even if TM00 is read, the value is not captured by CR010.**

★ **2. The count clock does not stop while TM00 is being read.**

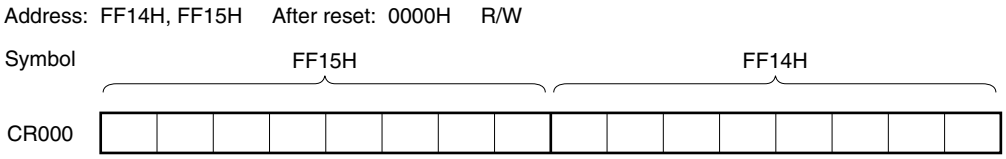
(2) 16-bit timer capture/compare register 000 (CR000)

CR000 is a 16-bit register which has the functions of both a capture register and a compare register. Whether it is used as a capture register or as a compare register is set by bit 0 (CRC000) of capture/compare control register 00 (CRC00).

CR000 is set by 16-bit memory manipulation instruction.

A reset clears CR000 to 0000H.

Figure 6-3. Format of 16-Bit Timer Capture/Compare Register 000 (CR000)



- **When CR000 is used as a compare register**

  The value set in CR000 is constantly compared with the 16-bit timer/counter 00 (TM00) count value, and an interrupt request (INTTM000) is generated if they match. It can also be used as the register that holds the interval time then TM00 is set to interval timer operation.

- **When CR000 is used as a capture register**

  It is possible to select the valid edge of the TI000 pin or the TI010 pin as the capture trigger. Setting of the TI000 or TI010 valid edge is performed by means of prescaler mode register 00 (PRM00) (refer to **Table 6-2**).

Table 6-2. CR000 Capture Trigger and Valid Edges of TI000 and TI010 Pins

(1) TI000 pin valid edge selected as capture trigger (CRC001 = 1, CRC000 = 1)

CR000 Capture Trigger	TI000 Pin Valid Edge		
		ES010	ES000
Falling edge	Rising edge	0	1
Rising edge	Falling edge	0	0
No capture operation	Both rising and falling edges	1	1

(2) TI010 pin valid edge selected as capture trigger (CRC001 = 0, CRC000 = 1)

CR000 Capture Trigger	TI010 Pin Valid Edge		
		ES110	ES100
Falling edge	Falling edge	0	0
Rising edge	Rising edge	0	1
Both rising and falling edges	Both rising and falling edges	1	1

Remarks 1. Setting ES010, ES000 = 1, 0 and ES110, ES100 = 1, 0 is prohibited.

2. ES010, ES000: Bits 5 and 4 of prescaler mode register 00 (PRM00)
ES110, ES100: Bits 7 and 6 of prescaler mode register 00 (PRM00)
CRC001, CRC000: Bits 1 and 0 of capture/compare control register 00 (CRC00)

Cautions 1. Set CR000 to other than 0000H in the clear & start mode entered on match between TM00 and CR000. This means a 1-pulse count operation cannot be performed when this register is used as an external event counter. However, in the free-running mode and in the clear & start mode using the valid edge of TI000, if CR000 is set to 0000H, an interrupt request (INTTM000) is generated when CR000 changes from 0000H to 0001H following overflow (FFFFH).

2. If the new value of CR000 is less than the value of 16-bit timer counter 0 (TM00), TM00 continues counting, overflows, and then starts counting from 0 again. If the new value of CR000 is less than the old value, therefore, the timer must be reset to be restarted after the value of CR000 is changed.

★ **3. The value of CR000 after 16-bit timer/event counter 00 has stopped is not guaranteed.**

★ **4. The capture operation may not be performed for CR000 set in compare mode even if a capture trigger is input.**

5. When P21 is used as the input pin for the valid edge of TI010, it cannot be used as a timer output (TO00). Moreover, when P21 is used as TO00, it cannot be used as the input pin for the valid edge of TI010.

6. If the register read period and the input of the capture trigger conflict when CR000 is used as a capture register, the read data is undefined (the capture data itself is a normal value). Also, if the count stop of the timer and the input of the capture trigger conflict, the capture trigger is undefined.

7. Changing the CR000 setting may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-Bit Timer/Event Counter 00 (17) Changing compare register during timer operation.

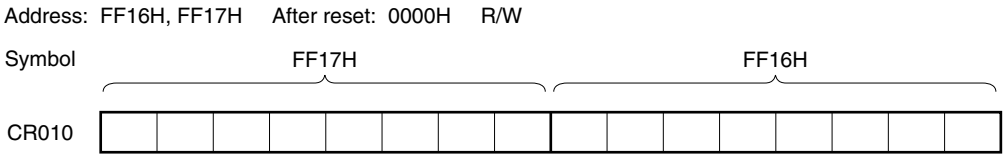
(3) 16-bit timer capture/compare register 010 (CR010)

CR010 is a 16-bit register which has the functions of both a capture register and a compare register. Whether it is used as a capture register or a compare register is set by bit 2 (CRC002) of capture/compare control register 00 (CRC00).

CR010 is set by 16-bit memory manipulation instruction.

Reset input clears CR010 to 0000H.

Figure 6-4. Format of 16-Bit Timer Capture/Compare Register 010 (CR010)



- **When CR010 is used as a compare register**

  The value set in CR010 is constantly compared with the 16-bit timer counter 00 (TM00) count value, and an interrupt request (INTTM010) is generated if they match.

- **When CR010 is used as a capture register**

  It is possible to select the valid edge of the TI000 pin as the capture trigger. The TI000 valid edge is set by means of prescaler mode register 00 (PRM00) (refer to **Table 6-3**).

Table 6-3. CR010 Capture Trigger and Valid Edge of TI000 Pin (CRC002 = 1)

CR010 Capture Trigger	TI000 Pin Valid Edge		
		ES010	ES000
Falling edge	Falling edge	0	0
Rising edge	Rising edge	0	1
Both rising and falling edges	Both rising and falling edges	1	1

Remarks 1. Setting ES010, ES000 = 1, 0 is prohibited.

2. ES010, ES000: Bits 5 and 4 of prescaler mode register 00 (PRM00)
CRC002: Bit 2 of capture/compare control register 00 (CRC00)

Cautions 1. In the free-running mode and in the clear & start mode using the valid edge of the TI000 pin, if CR010 is set to 0000H, an interrupt request (INTTM010) is generated when CR010 changes from 0000H to 0001H following overflow (FFFFH).

2. If the new value of CR010 is less than the value of 16-bit timer counter 00 (TM00), TM00 continues counting, overflows, and then starts counting from 0 again. If the new value of CR010 is less than the old value, therefore, the timer must be reset to be restarted after the value of CR010 is changed.

★ **3. The value of CR010 after 16-bit timer/event counter 00 has stopped is not guaranteed.**

★ **4. The capture operation may not be performed for CR010 set in compare mode even if a capture trigger is input.**

5. If the register read period and the input of the capture trigger conflict when CR000 is used as a capture register, the capture trigger input takes precedence and the read data is undefined. Also, if the timer count stop and the input of the capture trigger conflict, the capture data is undefined.

Cautions 6. Changing the CR010 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-Bit Timer/Event Counter 00 (17) Changing compare register during timer operation.

6.3 Registers to Control 16-Bit Timer/Event Counter 00

The following seven types of registers are used to control 16-bit timer/event counter 00.

- 16-bit timer mode control register 00 (TMC00)
- Capture/compare control register 00 (CRC00)
- 16-bit timer output control register 00 (TOC00)
- Prescaler mode register 00 (PRM00)
- Port mode register 2 (PM2)
- Port register 2 (P2)
- Port mode control register 2 (PMC2)

(1) 16-bit timer mode control register 00 (TMC00)

This register sets the 16-bit timer operating mode, the 16-bit timer counter 00 (TM00) clear mode, and output timing, and detects an overflow.

TMC00 is set by a 1-bit or 8-bit memory manipulation instruction.

Reset input sets the value of TMC00 to 00H.

Caution 16-bit timer counter 00 (TM00) starts operation at the moment TMC002 and TMC003 (operation stop mode) are set to a value other than 0, 0, respectively. Set TMC002 and TMC003 to 0, 0 to stop the operation.

Figure 6-5. Format of 16-Bit Timer Mode Control Register 00 (TMC00)

Address: FF60H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
TMC00	0	0	0	0	TMC003	TMC002	TMC001	OVF00

TMC003	TMC002	TMC001	Operating mode and clear mode selection	TO00 inversion timing selection	Interrupt request generation
0	0	0	Operation stop (TM00 cleared to 0)	No change	Not generated
0	0	1			
0	1	0	Free-running mode	Match between TM00 and CR000 or match between TM00 and CR010	< When operating as compare register > Generated on match between TM00 and CR000, or match between TM00 and CR010 < When operating as capture register > Generated on TI000 pin and TI010 pin valid edge
0	1	1		Match between TM00 and CR000, match between TM00 and CR010 or TI000 pin valid edge	
1	0	0	Clear & start occurs on valid edge of TI000 pin	–	
1	0	1			
1	1	0	Clear & start occurs on match between TM00 and CR000	Match between TM00 and CR000 or match between TM00 and CR010	
1	1	1		Match between TM00 and CR000, match between TM00 and CR010 or TI000 pin valid edge	

OVF00	Overflow detection of 16-bit timer counter 00 (TM00)
0	Overflow not detected
1	Overflow detected

Cautions 1. The timer operation must be stopped before writing to bits other than the OVF00 flag.

★ **2. Regardless of the CPU's operation mode, when the timer stops, the signals input to pins TI000/TI010 are not acknowledged.**

★ **3. Except when TI000 pin valid edge is selected as the count clock, stop the timer operation before setting STOP mode or system clock stop mode; otherwise the timer may malfunction when the system clock starts.**

★ **4. Set the valid edge of the TI000 pin with bits 4 and 5 of prescaler mode register 00 (PRM00) after stopping the timer operation.**

5. If the clear & start mode entered on a match between TM00 and CR000, clear & start mode at the valid edge of the TI000 pin, or free-running mode is selected, when the set value of CR000 is FFFFH and the TM00 value changes from FFFFH to 0000H, the OVF00 flag is set to 1.

★ **6. Even if the OVF00 flag is cleared before the next count clock is counted (before TM00 becomes 0001H) after the occurrence of a TM00 overflow, the OVF00 flag is re-set newly and clear is disabled.**

★ **7. The capture operation is performed at the fall of the count clock. An interrupt request input (INTTM0n0), however, occurs at the rise of the next count clock.**

Remark TM00: 16-bit timer counter 00
CR000: 16-bit timer capture/compare register 000
CR010: 16-bit timer capture/compare register 010

(2) Capture/compare control register 00 (CRC00)

This register controls the operation of the 16-bit capture/compare registers (CR000, CR010).
CRC00 is set by a 1-bit or 8-bit memory manipulation instruction.
Reset input sets the value of CRC00 to 00H.

Figure 6-6. Format of Capture/Compare Control Register 00 (CRC00)

Address: FF62H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CRC00	0	0	0	0	0	CRC002	CRC001	CRC000

CRC002	CR010 operating mode selection
0	Operate as compare register
1	Operate as capture register

CRC001	CR000 capture trigger selection
0	Capture on valid edge of TI010 pin
1	Capture on valid edge of TI000 pin by reverse phase[Note]

CRC000	CR000 operating mode selection
0	Operate as compare register
1	Operate as capture register

Note If both the rising and falling edges have been selected as the valid edges of the TI000 pin, capture is not performed.

Cautions 1. The timer operation must be stopped before setting CRC00.
2. When the clear & start mode entered on a match between TM00 and CR000 is selected by 16-bit timer mode control register 00 (TMC00), CR000 should not be specified as a capture register.
3. To ensure the reliability of the capture operation, the capture trigger requires a pulse longer than two cycles of the count clock selected by prescaler mode register 00 (PRM00) (refer to Figure 6-17).

(3) 16-bit timer output control register 00 (TOC00)

This register controls the operation of the 16-bit timer/event counter output controller. It sets timer output F/F set/reset, output inversion enable/disable, 16-bit timer/event counter 00 timer output enable/disable, one-shot pulse output operation enable/disable, and output trigger of one-shot pulse by software.

TOC00 is set by a 1-bit or 8-bit memory manipulation instruction.

Reset input sets the value of TOC00 to 00H.

Figure 6-7. Format of 16-Bit Timer Output Control Register 00 (TOC00)

Address: FF63H After reset: 00H R/W

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>
TOC00	0	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00

OSPT00	One-shot pulse output trigger control via software
0	No one-shot pulse output trigger
1	One-shot pulse output trigger

OSPE00	One-shot pulse output operation control
0	Successive pulse output mode
1	One-shot pulse output mode[Note]

TOC004	Timer output F/F control using match of CR010 and TM00
0	Disables inversion operation
1	Enables inversion operation

LVS00	LVR00	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F reset (0)
1	0	Timer output F/F set (1)
1	1	Setting prohibited

TOC001	Timer output F/F control using match of CR000 and TM00
0	Disables inversion operation
1	Enables inversion operation

TOE00	Timer output control
0	Disables output (output fixed to level 0)
1	Enables output

Note The one-shot pulse output mode operates correctly only in the free-running mode and the mode in which clear & start occurs at the TI000 pin valid edge. In the mode in which clear & start occurs on a match between TM00 and CR000, one-shot pulse output is not possible because an overflow does not occur.

Cautions 1. Timer operation must be stopped before setting other than OSPT00.

2. If LVS00 and LVR00 are read, 0 is read.

3. OSPT00 is automatically cleared after data is set, so 0 is read.

4. Do not set OSPT00 to 1 other than in one-shot pulse output mode.

5. A write interval of two cycles or more of the count clock selected by prescaler mode register 00 (PRM00) is required to write to OSPT00 successively.

★ **Cautions 6. When the TOE00 is 0, set the TOE00, LVS00, and LVR00 at the same time with the 8-bit memory manipulation instruction. When the TOE00 is 1, the LVS00 and LVR00 can be set with the 1-bit memory manipulation instruction.**

(4) Prescaler mode register 00 (PRM00)

This register is used to set the 16-bit timer counter 00 (TM00) count clock and the TI000, TI010 pin input valid edges.

PRM00 is set by a 1-bit or 8-bit memory manipulation instruction.

Reset input sets the value of PRM00 to 00H.

Figure 6-8. Format of Prescaler Mode Register 00 (PRM00)

Address: FF61H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PRM00	ES110	ES100	ES010	ES000	0	0	PRM001	PRM000

ES110	ES100	TI010 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES010	ES000	TI000 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

PRM001	PRM000	Count clock selection
0	0	f_{XP} (10 MHz)
0	1	$f_{XP}/2^2$ (2.5 MHz)
1	0	$f_{XP}/2^8$ (39.06 kHz)
1	1	TI000 pin valid edge[Note]

Remarks 1. f_{XP}: Oscillation frequency of clock supplied to peripheral hardware

2. ( ): f_{XP} = 10 MHz

Note The external clock requires a pulse longer than two cycles of the internal count clock (f_{XP}).

Cautions 1. Always set data to PRM00 after stopping the timer operation.

2. If the valid edge of the TI000 pin is to be set as the count clock, do not set the clear/start mode and the capture trigger at the valid edge of the TI000 pin.

★ **Cautions 3. In the following cases, note with caution that the valid edge of the TI0n0 pin is detected.**

<1> Immediately after a system reset, if a high level is input to the TI0n0 pin, the operation of the 16-bit timer counter 00 (TM00) is enabled

→ If the rising edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.

<2> If the TM00 operation is stopped while the TI0n0 pin is high level, TM00 operation is then enabled after a low level is input to the TI0n0 pin

→ If the falling edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a falling edge is detected immediately after the TM00 operation is enabled.

<3> If the TM00 operation is stopped while the TI0n0 pin is low level, TM00 operation is then enabled after a high level is input to the TI0n0 pin

→ If the rising edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.

★ **4. The sampling clock used to eliminate noise differs when a TI000 valid edge is used as the count clock and when it is used as a capture trigger. In the former case, the count clock is f_{XP}, and in the latter case the count clock is selected by prescaler mode register 00 (PRM00). The capture operation is not performed until the valid edge is sampled and the valid level is detected twice, thus eliminating noise with a short pulse width.**

5. When using P21 as the input pin (TI010) of the valid edge, it cannot be used as a timer output (TO00). When using P21 as the timer output pin (TO00), it cannot be used as the input pin (TI010) of the valid edge.

Remark n = 0, 1

(5) Port mode register 2 (PM2) and port mode control register 2 (PMC2)

When using the P21/TO00/TI010/ANI1/INTP0 pin for timer output, clear PM21, the output latch of P21, and PMC21 to 0.

When using the P20/TI000/TOH1/ANI0 and P21/TO00/TI010/ANI1/INTP0 pins as a timer input, set PM20 and PM21 to 1, and clear PMC20 and PMC21 to 0.

At this time, the output latches of P20 and P21 can be either 0 or 1.

PM2 and PMC2 are set by a 1-bit or 8-bit memory manipulation instruction.

Reset input sets the value of PM2 to FFH, and clears the value of PMC2 to 00H.

Figure 6-9. Format of Port Mode Register 2 (PM2)

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	1	1	PM23	PM22	PM21	PM20

PM2n	P2n pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 6-10. Format of Port Mode Control Register 2 (PMC2)

Address: FF84H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PMC2	0	0	0	0	PMC23	PMC22	PMC21	PMC20

PMC2n	Specification of operation mode (n = 0 to 3)
0	Port/Alternate-function (except A/D converter) mode
1	A/D converter mode

6.4 Operation of 16-Bit Timer/Event Counter 00

6.4.1 Interval timer operation

Setting 16-bit timer mode control register 00 (TMC00) and capture/compare control register 00 (CRC00) as shown in Figure 6-11 allows operation as an interval timer.

Setting

The basic operation setting procedure is as follows.

<1> Set the CRC00 register (see **Figure 6-11** for the set value).
<2> Set any value to the CR000 register.
<3> Set the count clock by using the PRM00 register.
<4> Set the TMC00 register to start the operation (see **Figure 6-11** for the set value).

Caution Changing the CR000 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-Bit Timer/Event Counter 00 (17) Changing compare register during timer operation.

Remark For how to enable the INTTM000 interrupt, see **CHAPTER 10 INTERRUPT FUNCTIONS**.

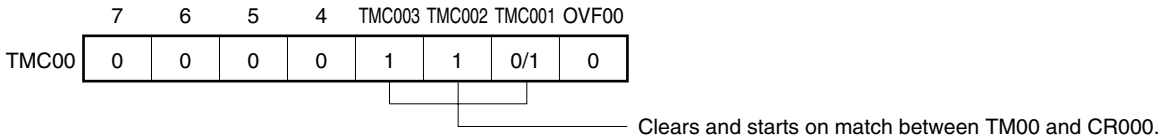
Interrupt requests are generated repeatedly using the count value set in 16-bit timer capture/compare register 000 (CR000) beforehand as the interval.

When the count value of 16-bit timer counter 00 (TM00) matches the value set to CR000, counting continues with the TM00 value cleared to 0 and the interrupt request signal (INTTM000) is generated.

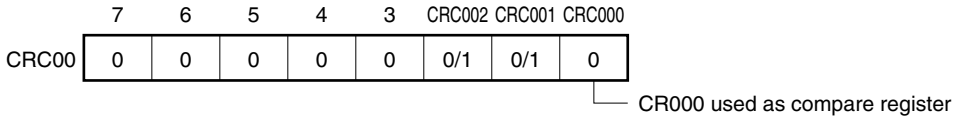
The count clock of the 16-bit timer/event counter can be selected using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00).

Figure 6-11. Control Register Settings for Interval Timer Operation

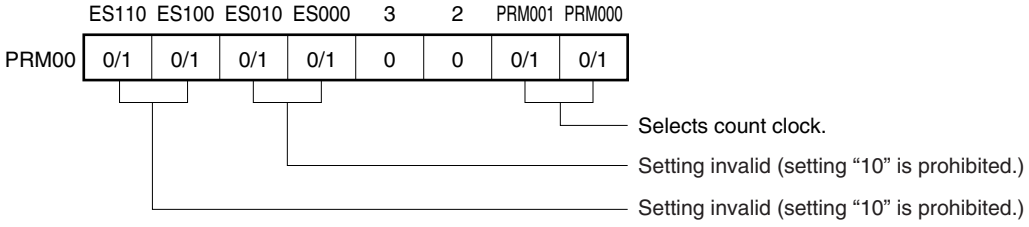
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)

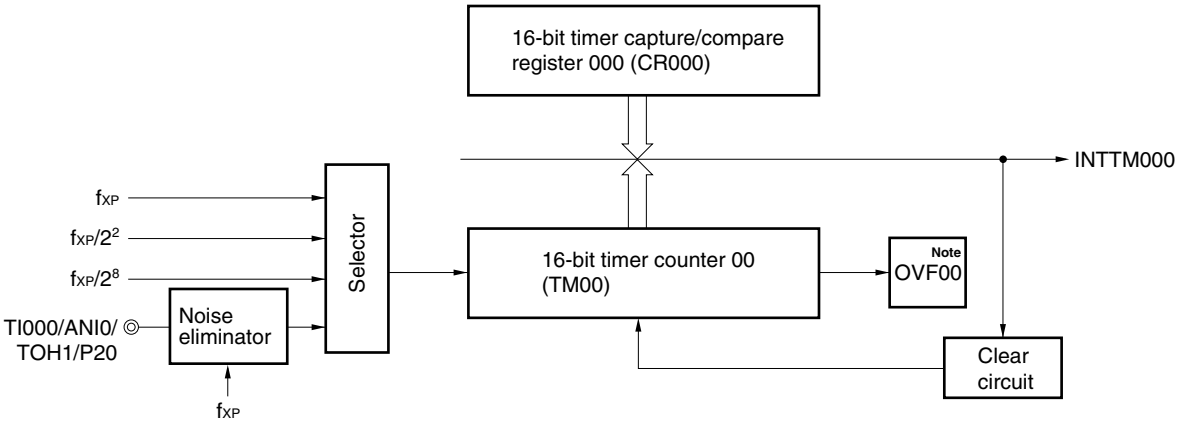


(c) Prescaler mode register 00 (PRM00)



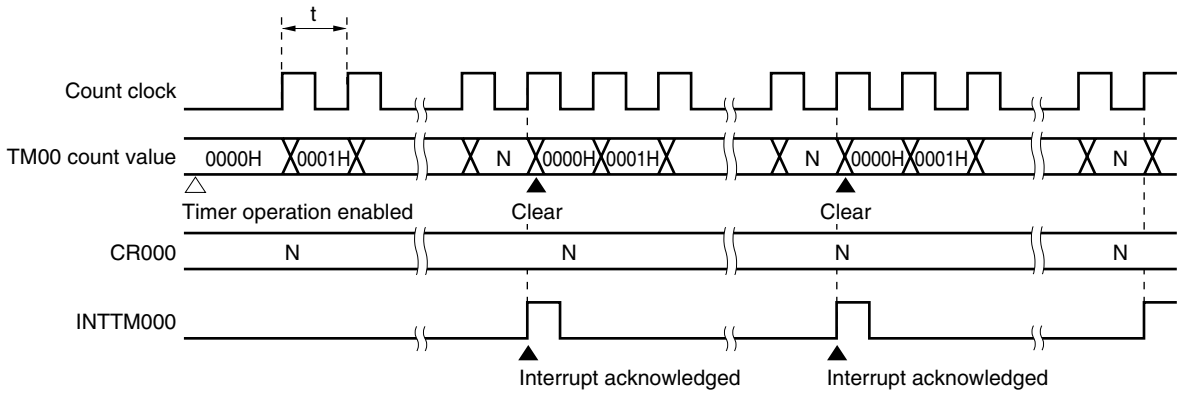
Remark 0/1: Setting 0 or 1 allows another function to be used simultaneously with the interval timer. See the description of the respective control registers for details.

Figure 6-12. Interval Timer Configuration Diagram



Note OVF00 is set to 1 only when 16-bit timer capture/compare register 000 is set to FFFFH.

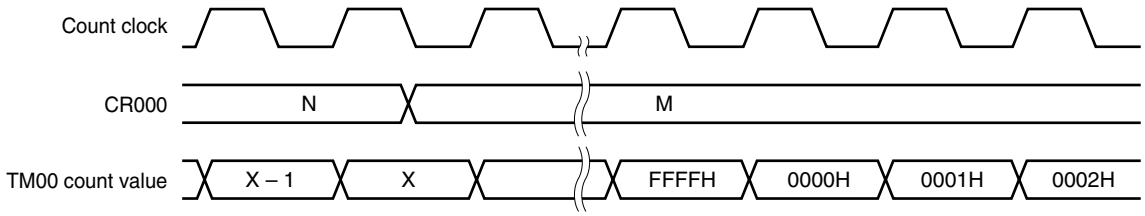
Figure 6-13. Timing of Interval Timer Operation



Remark Interval time = (N + 1) × t
N = 0001H to FFFFH (settable range)

When the compare register is changed during timer count operation, if the value after 16-bit timer capture/compare register 000 (CR000) is changed is smaller than that of 16-bit timer counter 00 (TM00), TM00 continues counting, overflows and then restarts counting from 0. Thus, if the value (M) after the CR000 change is smaller than that (N) before the change, it is necessary to restart the timer after changing CR000.

Figure 6-14. Timing After Change of Compare Register During Timer Count Operation (N → M: N > M)



Remark N > X > M

6.4.2 External event counter operation

Setting

The basic operation setting procedure is as follows.

<1> Set the CRC00 register (see **Figure 6-15** for the set value).
<2> Set the count clock by using the PRM00 register.
<3> Set any value to the CR000 register (0000H cannot be set).
<4> Set the TMC00 register to start the operation (see **Figure 6-15** for the set value).

Remarks 1. For the setting of the TI000 pin, see **6.3 (5) Port mode register 2 (PM2) and port mode control register 2 (PMC2)**.
2. For how to enable the INTTM000 interrupt, see **CHAPTER 10 INTERRUPT FUNCTIONS**.

The external event counter counts the number of external clock pulses to be input to the TI000 pin with using 16-bit timer counter 00 (TM00).

TM00 is incremented each time the valid edge specified by prescaler mode register 00 (PRM00) is input.

When the TM00 count value matches the 16-bit timer capture/compare register 000 (CR000) value, TM00 is cleared to 0 and the interrupt request signal (INTTM000) is generated.

Input a value other than 0000H to CR000. (A count operation with a pulse cannot be carried out.)

The rising edge, the falling edge, or both edges can be selected using bits 4 and 5 (ES000 and ES010) of prescaler mode register 00 (PRM00).

Because an operation is carried out only when the valid edge of the TI000 pin is detected twice after sampling with the internal clock (f_{XP}), noise with a short pulse width can be removed.

Figure 6-15. Control Register Settings in External Event Counter Mode (with Rising Edge Specified)

(a) 16-bit timer mode control register 00 (TMC00)

	7	6	5	4	TMC003	TMC002	TMC001	OVF00
TMC00	0	0	0	0	1	1	0/1	0

Clears and starts on match between TM00 and CR000.

(b) Capture/compare control register 00 (CRC00)

	7	6	5	4	3	CRC002	CRC001	CRC000
CRC00	0	0	0	0	0	0/1	0/1	0

CR000 used as compare register

(c) Prescaler mode register 00 (PRM00)

	ES110	ES100	ES010	ES000	3	2	PRM001	PRM000
PRM00	0/1	0/1	0	1	0	0	1	1

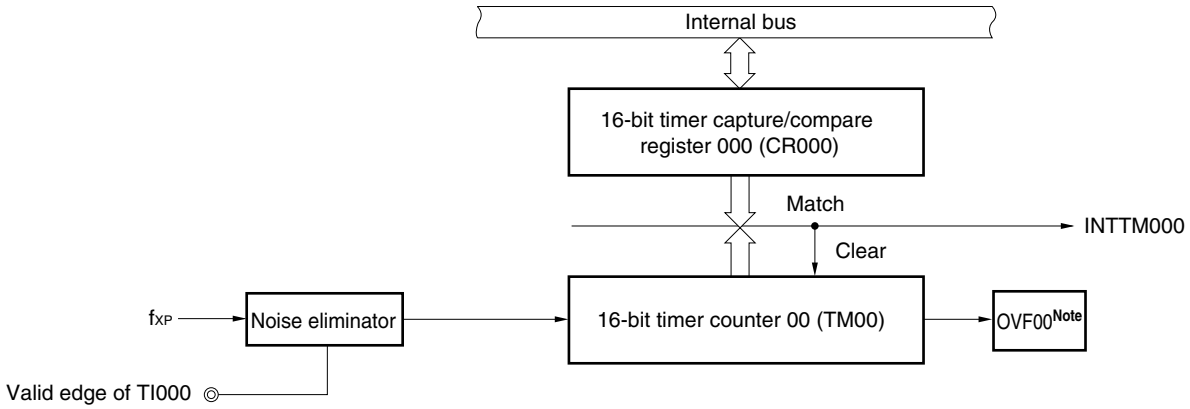
Selects external clock.

Specifies rising edge for pulse width detection.

Setting invalid (setting “10” is prohibited.)

Remark 0/1: Setting 0 or 1 allows another function to be used simultaneously with the external event counter. See the description of the respective control registers for details.

Figure 6-16. External Event Counter Configuration Diagram

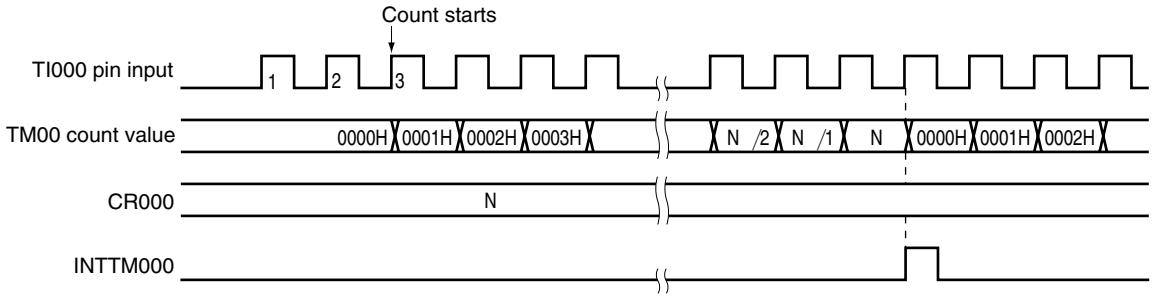


Note OVF00 is 1 only when 16-bit timer capture/compare register 000 is set to FFFFH.

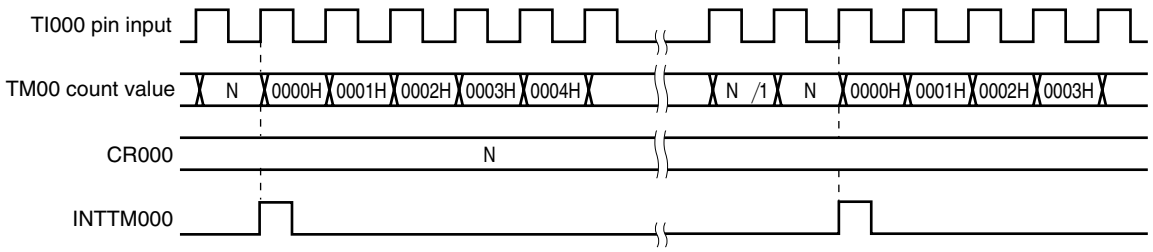
Figure 6-17. External Event Counter Operation Timing (with Rising Edge Specified)

★ **(1) INTTM000 generation timing immediately after operation starts**

Counting is started after a valid edge is detected twice.



(2) INTTM000 generation timing after INTTM000 has been generated twice



Caution When reading the external event counter count value, TM00 should be read.

6.4.3 Pulse width measurement operations

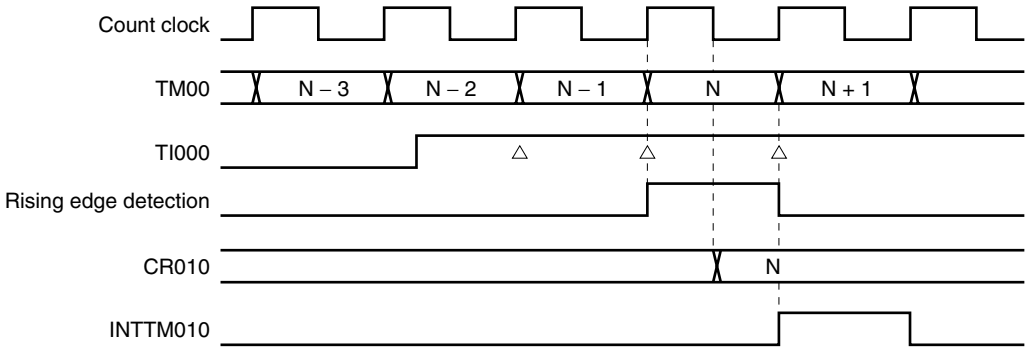
It is possible to measure the pulse width of the signals input to the TI000 pin and TI010 pin using 16-bit timer counter 00 (TM00).

There are two measurement methods: measuring with TM00 used in free-running mode, and measuring by restarting the timer in synchronization with the edge of the signal input to the TI000 pin.

When an interrupt occurs, read the valid value of the capture register, check the overflow flag, and then calculate the necessary pulse width. Clear the overflow flag after checking it.

The capture operation is not performed until the signal pulse width is sampled in the count clock cycle selected by prescaler mode register 00 (PRM00) and the valid level of the TI000 or TI010 pin is detected twice, thus eliminating noise with a short pulse width.

Figure 6-18. CR010 Capture Operation with Rising Edge Specified



Setting

The basic operation setting procedure is as follows.

<1> Set the CRC00 register (see **Figures 6-19**, **6-22**, **6-24**, and **6-26** for the set value).
<2> Set the count clock by using the PRM00 register.
<3> Set the TMC00 register to start the operation (see **Figures 6-19**, **6-22**, **6-24**, and **6-26** for the set value).

Caution To use two capture registers, set the TI000 and TI010 pins.

Remarks 1. For the setting of the TI000 (or TI010) pin, see **6.3 (5) Port mode register 2 (PM2) and port mode control register 2 (PMC2)**.

2. For how to enable the INTTM000 (or INTTM010) interrupt, see **CHAPTER 10 INTERRUPT FUNCTIONS**.

(1) Pulse width measurement with free-running counter and one capture register

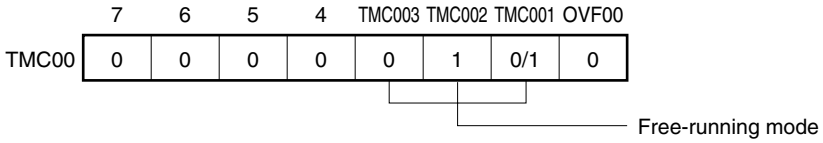
When 16-bit timer counter 00 (TM00) is operated in free-running mode, and the edge specified by prescaler mode register 00 (PRM00) is input to the TI000 pin, the value of TM00 is taken into 16-bit timer capture/compare register 010 (CR010) and an external interrupt request signal (INTTM010) is set.

Specify both the rising and falling edges by using bits 4 and 5 (ES000 and ES010) of PRM00.

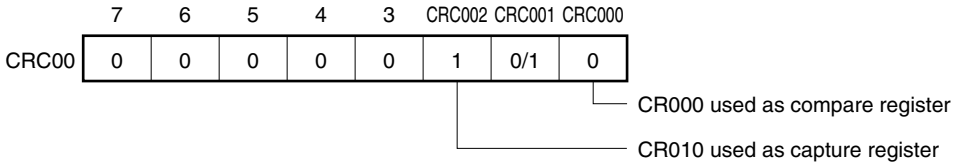
Sampling is performed using the count clock selected by PRM00, and a capture operation is only performed when a valid level of the TI000 pin is detected twice, thus eliminating noise with a short pulse width.

Figure 6-19. Control Register Settings for Pulse Width Measurement with Free-Running Counter and One Capture Register (When TI000 and CR010 Are Used)

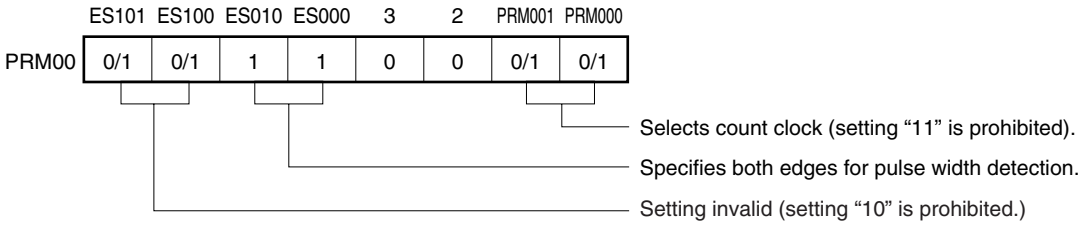
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) Prescaler mode register 00 (PRM00)



Remark 0/1: Setting 0 or 1 allows another function to be used simultaneously with pulse width measurement. See the description of the respective control registers for details.

Figure 6-20. Configuration Diagram for Pulse Width Measurement by Free-Running Counter

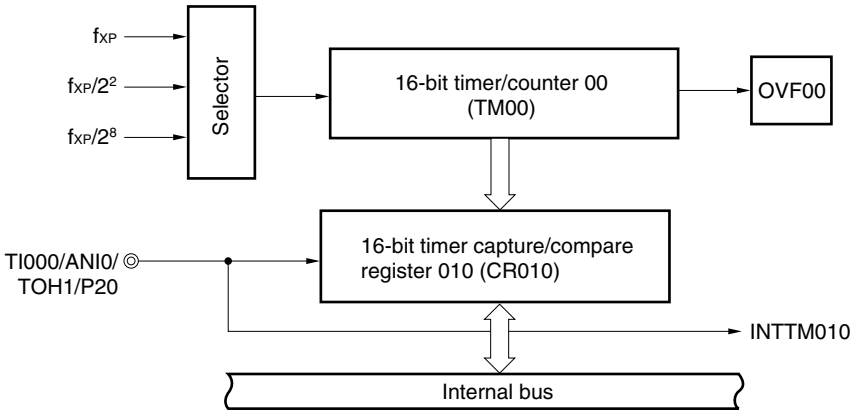
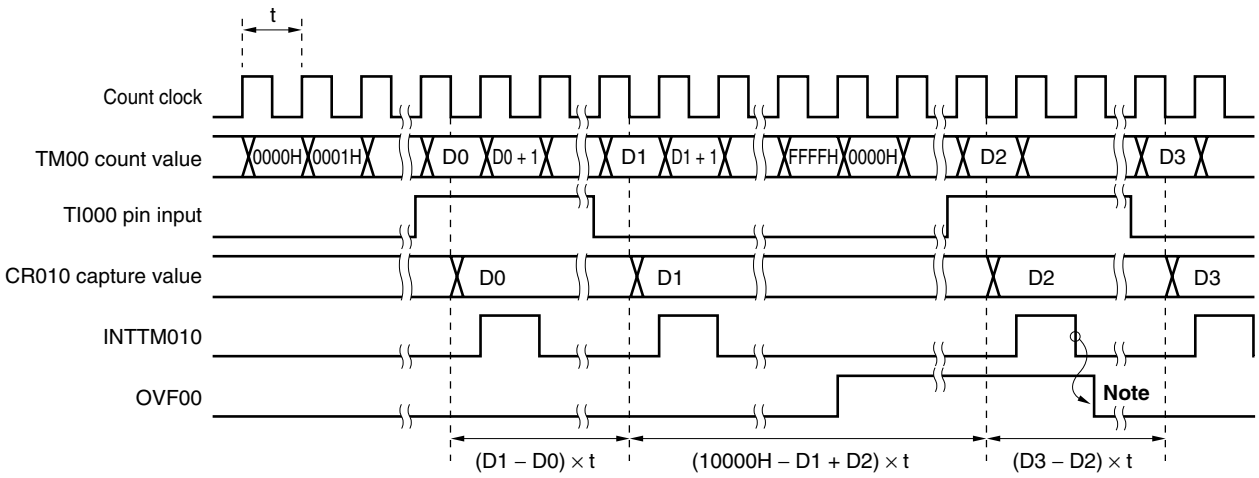


Figure 6-21. Timing of Pulse Width Measurement Operation by Free-Running Counter and One Capture Register (with Both Edges Specified)



Note OVF00 must be cleared by software.

(2) Measurement of two pulse widths with free-running counter

When 16-bit timer counter 00 (TM00) is operated in free-running mode, it is possible to simultaneously measure the pulse widths of the two signals input to the TI000 pin and the TI010 pin.

When the edge specified by bits 4 and 5 (ES000 and ES010) of prescaler mode register 00 (PRM00) is input to the TI000 pin, the value of TM00 is taken into 16-bit timer capture/compare register 010 (CR010) and an interrupt request signal (INTTM010) is set.

Also, when the edge specified by bits 6 and 7 (ES100 and ES110) of PRM00 is input to the TI010 pin, the value of TM00 is taken into 16-bit timer capture/compare register 000 (CR000) and an interrupt request signal (INTTM000) is set.

Specify both the rising and falling edges as the edges of the TI000 and TI010 pins, by using bits 4 and 5 (ES000 and ES010) and bits 6 and 7 (ES100 and ES110) of PRM00.

Sampling is performed using the count clock cycle selected by prescaler mode register 00 (PRM00), and a capture operation is only performed when a valid level of the TI000 or TI010 pin is detected twice, thus eliminating noise with a short pulse width.

Figure 6-22. Control Register Settings for Measurement of Two Pulse Widths with Free-Running Counter

(a) 16-bit timer mode control register 00 (TMC00)

	7	6	5	4	TMC003	TMC002	TMC001	OVF00
TMC00	0	0	0	0	0	1	0/1	0

Free-running mode

(b) Capture/compare control register 00 (CRC00)

	7	6	5	4	3	CRC002	CRC001	CRC000
CRC00	0	0	0	0	0	1	0	1

CR000 used as capture register

Captures valid edge of TI010 pin to CR000.

CR010 used as capture register

(c) Prescaler mode register 00 (PRM00)

	ES110	ES100	ES010	ES000	3	2	PRM001	PRM000
PRM00	1	1	1	1	0	0	0/1	0/1

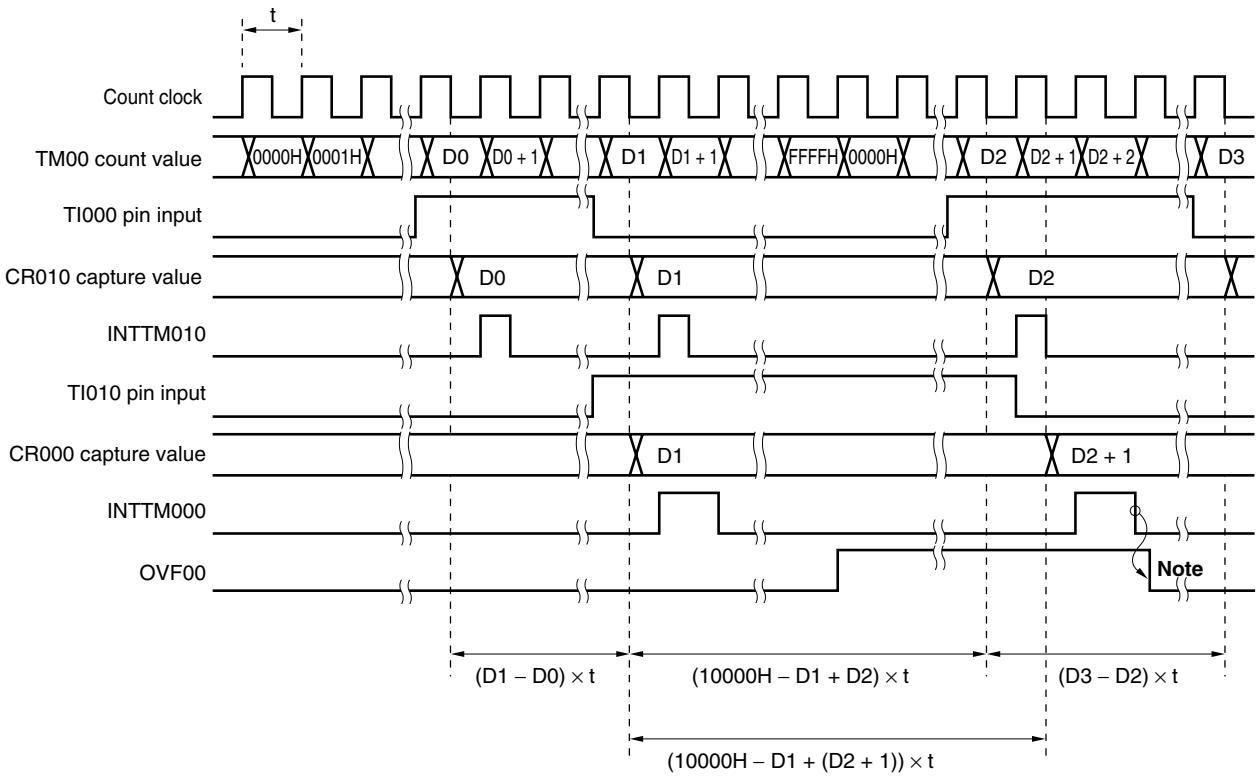
Selects count clock (setting “11” is prohibited).

Specifies both edges for pulse width detection.

Specifies both edges for pulse width detection.

Remark 0/1: Setting 0 or 1 allows another function to be used simultaneously with pulse width measurement. See the description of the respective control registers for details.

Figure 6-23. Timing of Pulse Width Measurement Operation with Free-Running Counter (with Both Edges Specified)



Note OVF00 must be cleared by software.

(3) Pulse width measurement with free-running counter and two capture registers

When 16-bit timer counter 00 (TM00) is operated in free-running mode, it is possible to measure the pulse width of the signal input to the TI000 pin.

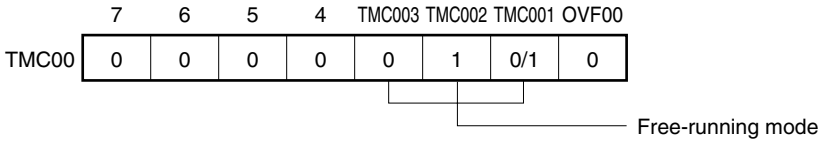
When the rising or falling edge specified by bits 4 and 5 (ES000 and ES010) of prescaler mode register 00 (PRM00) is input to the TI000 pin, the value of TM00 is taken into 16-bit timer capture/compare register 010 (CR010) and an interrupt request signal (INTTM010) is set.

Also, when the inverse edge to that of the capture operation is input into CR010, the value of TM00 is taken into 16-bit timer capture/compare register 000 (CR000).

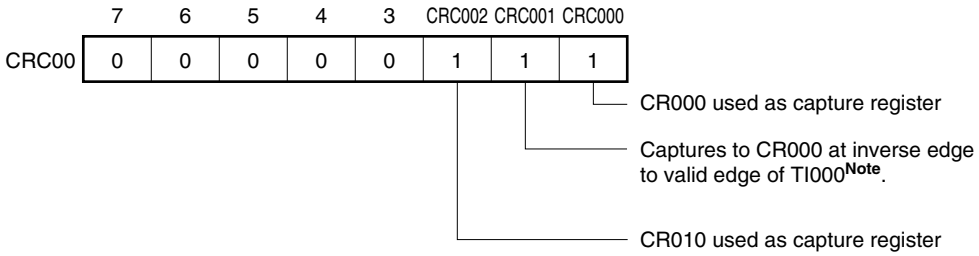
Sampling is performed using the count clock cycle selected by prescaler mode register 00 (PRM00), and a capture operation is only performed when a valid level of the TI000 pin is detected twice, thus eliminating noise with a short pulse width.

Figure 6-24. Control Register Settings for Pulse Width Measurement with Free-Running Counter and Two Capture Registers (with Rising Edge Specified)

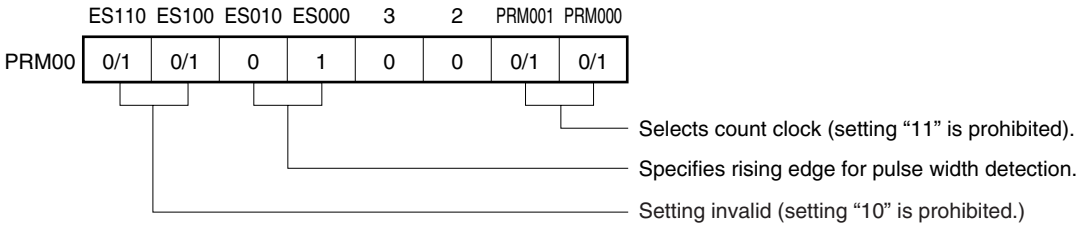
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) Prescaler mode register 00 (PRM00)

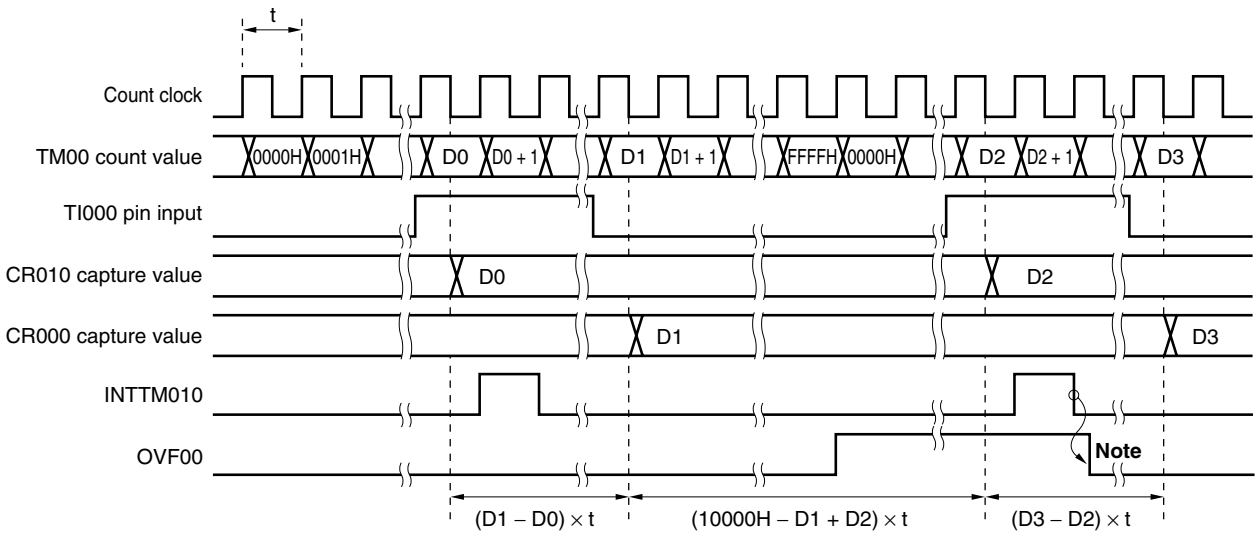


Note If the valid edge of TI000 is specified to be both the rising and falling edges, 16-bit timer capture/compare register 000 (CR000) cannot perform the capture operation. When the CRC001 bit value is 1, the TM00 count value is not captured in the CR000 register when a valid edge of the TI010 pin is detected, but the input from the TI010 pin can be used as an external interrupt source because INTTM000 is generated at that timing.

★

Remark 0/1: Setting 0 or 1 allows another function to be used simultaneously with pulse width measurement. See the description of the respective control registers for details.

Figure 6-25. Timing of Pulse Width Measurement Operation by Free-Running Counter and Two Capture Registers (with Rising Edge Specified)



Note OVF00 must be cleared by software.

(4) Pulse width measurement by means of restart

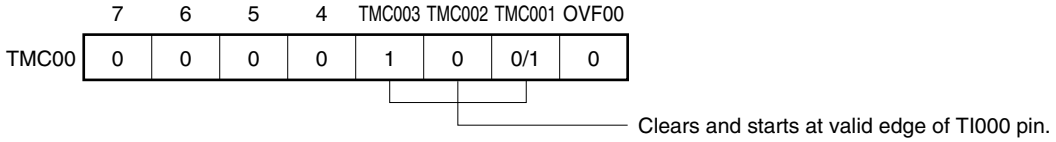
When input of a valid edge to the TI000 pin is detected, the count value of 16-bit timer/counter 00 (TM00) is taken into 16-bit timer capture/compare register 010 (CR010), and then the pulse width of the signal input to the TI000 pin is measured by clearing TM00 and restarting the count.

The edge specification can be selected from two types, rising or falling edges, by bits 4 and 5 (ES000 and ES010) of prescaler mode register 00 (PRM00)

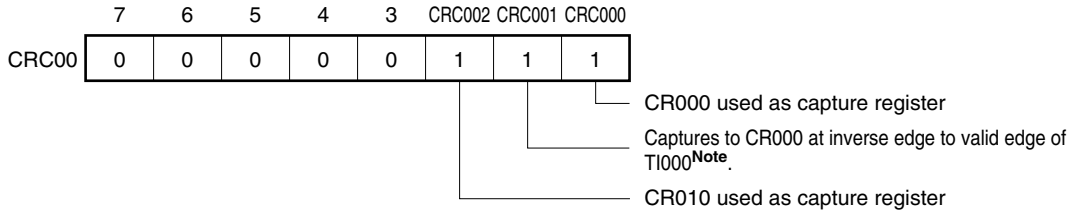
Sampling is performed at the interval selected by prescaler mode register 00 (PRM00) and a capture operation is only performed when a valid level of the TI000 pin is detected twice, thus eliminating noise with a short pulse width.

Figure 6-26. Control Register Settings for Pulse Width Measurement by Means of Restart (with Rising Edge Specified)

(a) 16-bit timer mode control register 00 (TMC00)



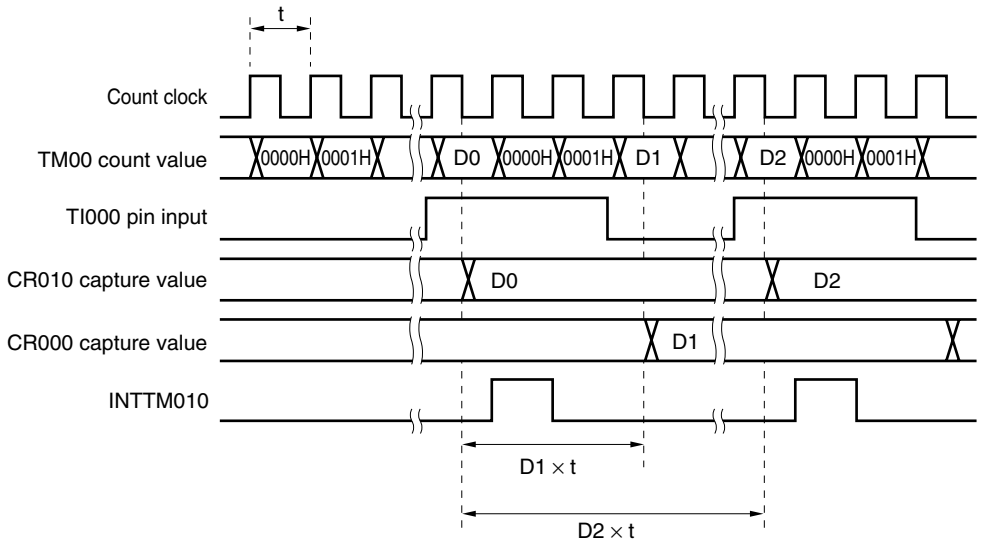
(b) Capture/compare control register 00 (CRC00)



(c) Prescaler mode register 00 (PRM00)

Note If the valid edge of TI000 is specified to be both the rising and falling edges, 16-bit timer capture/compare register 000 (CR000) cannot perform the capture operation.

Figure 6-27. Timing of Pulse Width Measurement Operation by Means of Restart (with Rising Edge Specified)



6.4.4 Square-wave output operation

Setting

The basic operation setting procedure is as follows.

<1> Set the count clock by using the PRM00 register.
<2> Set the CRC00 register (see **Figure 6-28** for the set value).
<3> Set the TOC00 register (see **Figure 6-28** for the set value).
<4> Set any value to the CR000 register (0000H cannot be set).
<5> Set the TMC00 register to start the operation (see **Figure 6-28** for the set value).

Caution Changing the CR000 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-Bit Timer/Event Counter 00 (17) Changing compare register during timer operation.

Remarks 1. For the setting of the TO00 pin, see **6.3 (5) Port mode register 2 (PM2) and port mode control register 2 (PMC2)**.
2. For how to enable the INTTM000 interrupt, see **CHAPTER 10 INTERRUPT FUNCTIONS**.

A square wave with any selected frequency can be output at intervals determined by the count value preset to 16-bit timer capture/compare register 000 (CR000).

The TO00 pin output status is reversed at intervals determined by the count value preset to CR000 + 1 by setting bit 0 (TOE00) and bit 1 (TOC001) of 16-bit timer output control register 00 (TOC00) to 1. This enables a square wave with any selected frequency to be output.

Figure 6-28. Control Register Settings in Square-Wave Output Mode (1/2)

(a) 16-bit timer mode control register 00 (TMC00)

	7	6	5	4	TMC003	TMC002	TMC001	OVF00
TMC00	0	0	0	0	1	1	0	0

Clears and starts on match between TM00 and CR000.

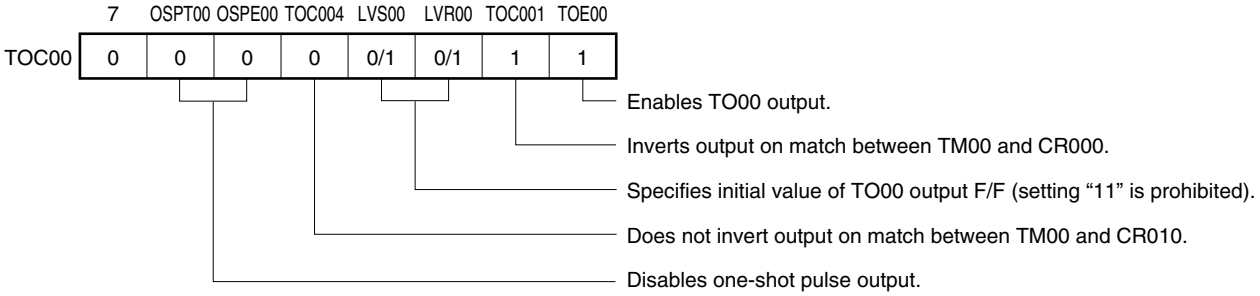
(b) Capture/compare control register 00 (CRC00)

	7	6	5	4	3	CRC002	CRC001	CRC000
CRC00	0	0	0	0	0	0/1	0/1	0

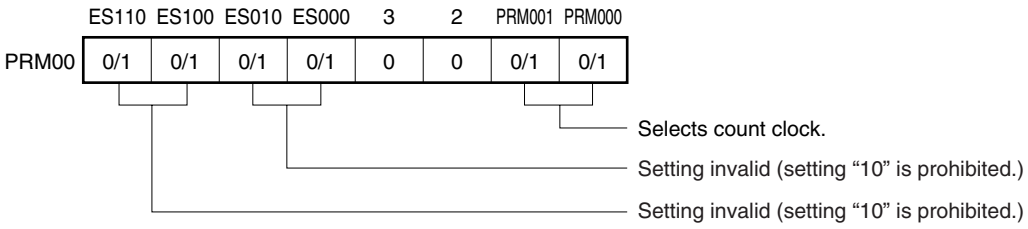
CR000 used as compare register

Figure 6-28. Control Register Settings in Square-Wave Output Mode (2/2)

(c) 16-bit timer output control register 00 (TOC00)

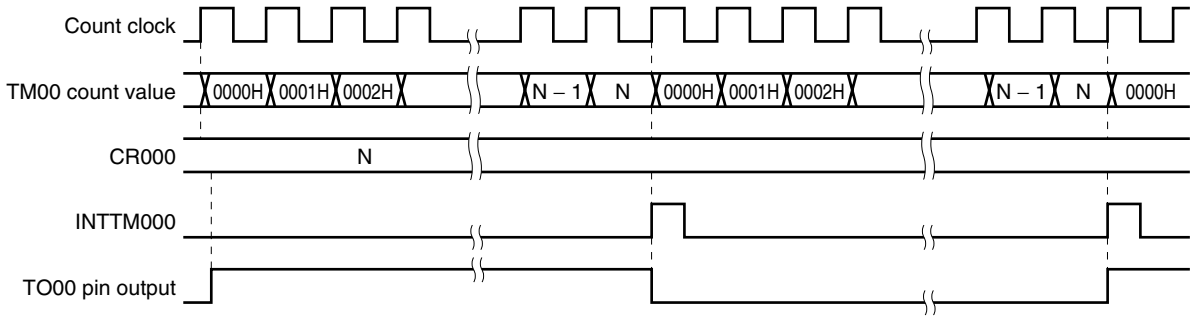


(d) Prescaler mode register 00 (PRM00)



Remark 0/1: Setting 0 or 1 allows another function to be used simultaneously with square-wave output. See the description of the respective control registers for details.

Figure 6-29. Square-Wave Output Operation Timing



6.4.5 PPG output operations

Setting 16-bit timer mode control register 00 (TMC00) and capture/compare control register 00 (CRC00) as shown in Figure 6-30 allows operation as PPG (Programmable Pulse Generator) output.

Setting

The basic operation setting procedure is as follows.

<1> Set the CRC00 register (see **Figure 6-30** for the set value).
<2> Set any value to the CR000 register as the cycle.
<3> Set any value to the CR010 register as the duty factor.
<4> Set the TOC00 register (see **Figure 6-30** for the set value).
<5> Set the count clock by using the PRM00 register.
<6> Set the TMC00 register to start the operation (see **Figure 6-30** for the set value).

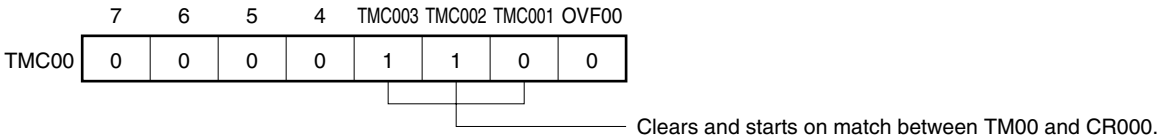
Caution Changing the CRC0n0 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-Bit Timer/Event Counter 00 (17) Changing compare register during timer operation.

Remarks 1. For the setting of the TO00 pin, see **6.3 (5) Port mode register 2 (PM2) and port mode control register 2 (PMC2)**.
2. For how to enable the INTTM000 interrupt, see **CHAPTER 10 INTERRUPT FUNCTIONS**.
3. n = 0 or 1

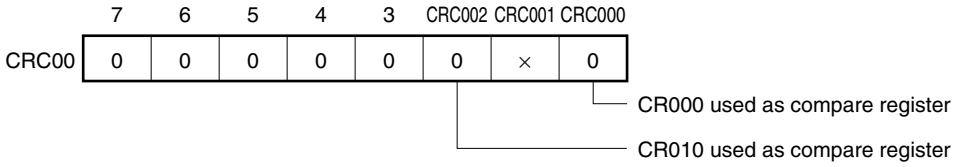
In the PPG output operation, rectangular waves are output from the TO00 pin with the pulse width and the cycle that correspond to the count values preset in 16-bit timer capture/compare register 010 (CR010) and in 16-bit timer capture/compare register 000 (CR000), respectively.

Figure 6-30. Control Register Settings for PPG Output Operation

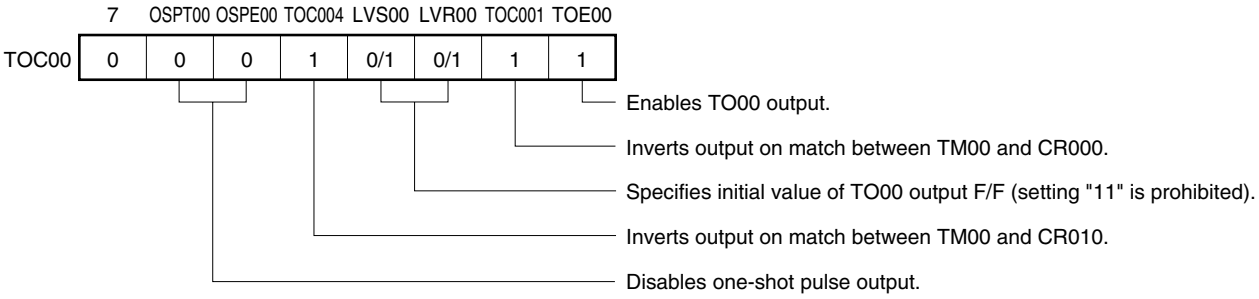
(a) 16-bit timer mode control register 00 (TMC00)



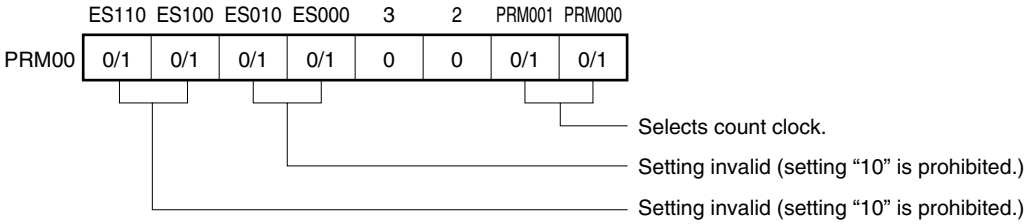
(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



(d) Prescaler mode register 00 (PRM00)



Cautions 1. Values in the following range should be set in CR000 and CR010:
0000H < CR010 < CR000 ≤ FFFFH
2. The cycle of the pulse generated through PPG output (CR000 setting value + 1) has a duty of (CR010 setting value + 1)/(CR000 setting value + 1).

Remark ×: Don’t care

Figure 6-31. Configuration Diagram of PPG Output

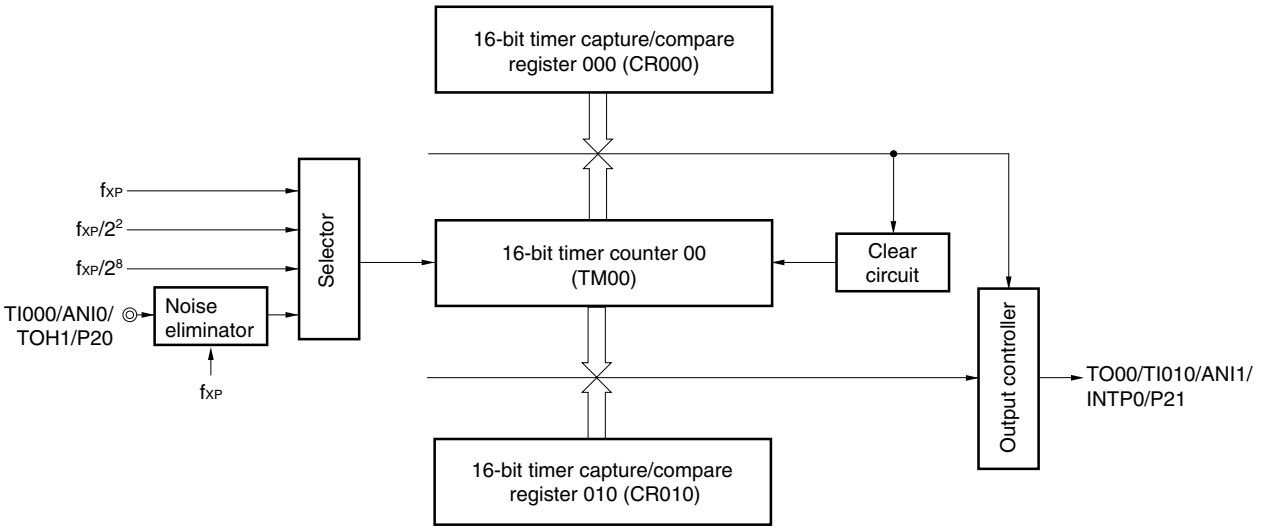
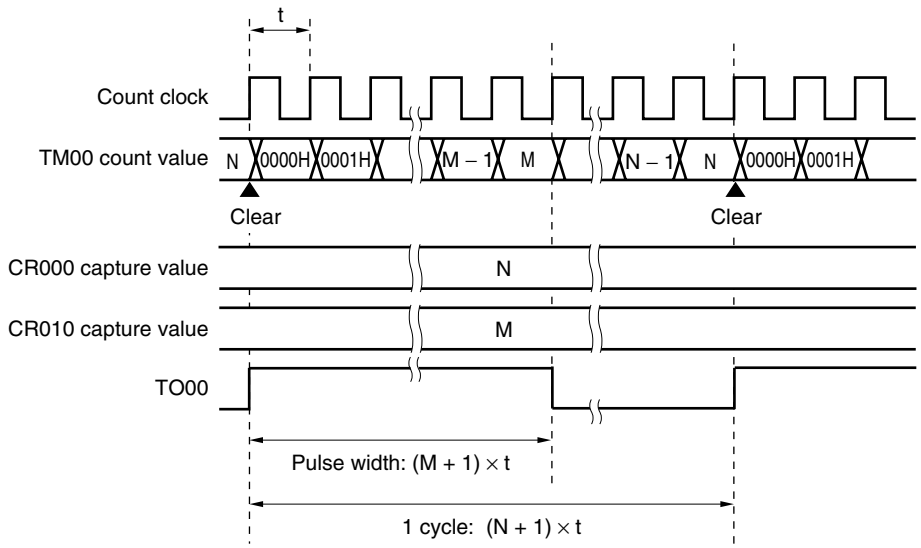


Figure 6-32. PPG Output Operation Timing



Remark 0000H < M < N ≤ FFFFH

6.4.6 One-shot pulse output operation

16-bit timer/event counter 00 can output a one-shot pulse in synchronization with a software trigger or an external trigger (TI000 pin input).

Setting

The basic operation setting procedure is as follows.

<1> Set the count clock by using the PRM00 register.
<2> Set the CRC00 register (see **Figures 6-33** and **6-35** for the set value).
<3> Set the TOC00 register (see **Figures 6-33** and **6-35** for the set value).
<4> Set any value to the CR000 and CR010 registers (0000H cannot be set).
<5> Set the TMC00 register to start the operation (see **Figures 6-33** and **6-35** for the set value).

Remarks 1. For the setting of the TO00 pin, see **6.3 (5) Port mode register 2 (PM2)**.

2. For how to enable the INTTM000 (if necessary, INTTM010) interrupt, see **CHAPTER 10 INTERRUPT FUNCTIONS**.

(1) One-shot pulse output with software trigger

A one-shot pulse can be output from the TO00 pin by setting 16-bit timer mode control register 00 (TMC00), capture/compare control register 00 (CRC00), and 16-bit timer output control register 00 (TOC00) as shown in Figure 6-33, and by setting bit 6 (OSPT00) of the TOC00 register to 1 by software.

By setting the OSPT00 bit to 1, 16-bit timer/event counter 00 is cleared and started, and its output becomes active at the count value (N) set in advance to 16-bit timer capture/compare register 010 (CR010). After that, the output becomes inactive at the count value (M) set in advance to 16-bit timer capture/compare register 000 (CR000)[Note].

Even after the one-shot pulse has been output, the TM00 register continues its operation. To stop the TM00 register, the TMC003 and TMC002 bits of the TMC00 register must be cleared to 00.

Note The case where N < M is described here. When N > M, the output becomes active with the CR000 register and inactive with the CR010 register. Do not set N to M.

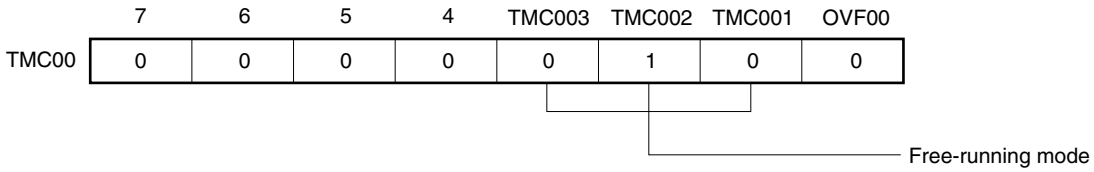
Cautions 1. Do not set the OSPT00 bit to 1 again while the one-shot pulse is being output. To output the one-shot pulse again, wait until the current one-shot pulse output is completed.

2. When using the one-shot pulse output of 16-bit timer/event counter 00 with a software trigger, do not change the level of the TI000 pin or its alternate-function port pin.

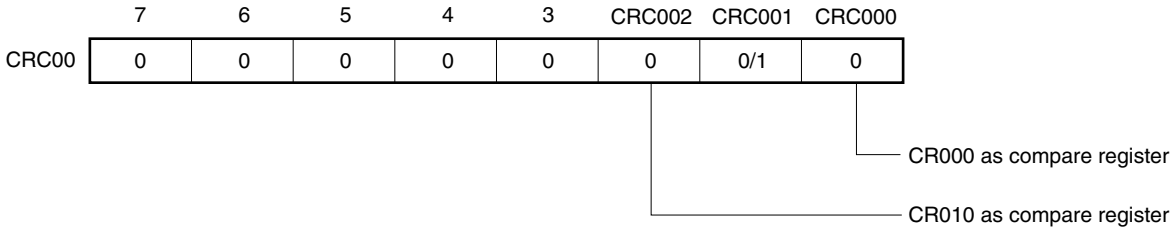
Because the external trigger is valid even in this case, the timer is cleared and started even at the level of the TI000 pin or its alternate-function port pin, resulting in the output of a pulse at an undesired timing.

Figure 6-33. Control Register Settings for One-Shot Pulse Output with Software Trigger

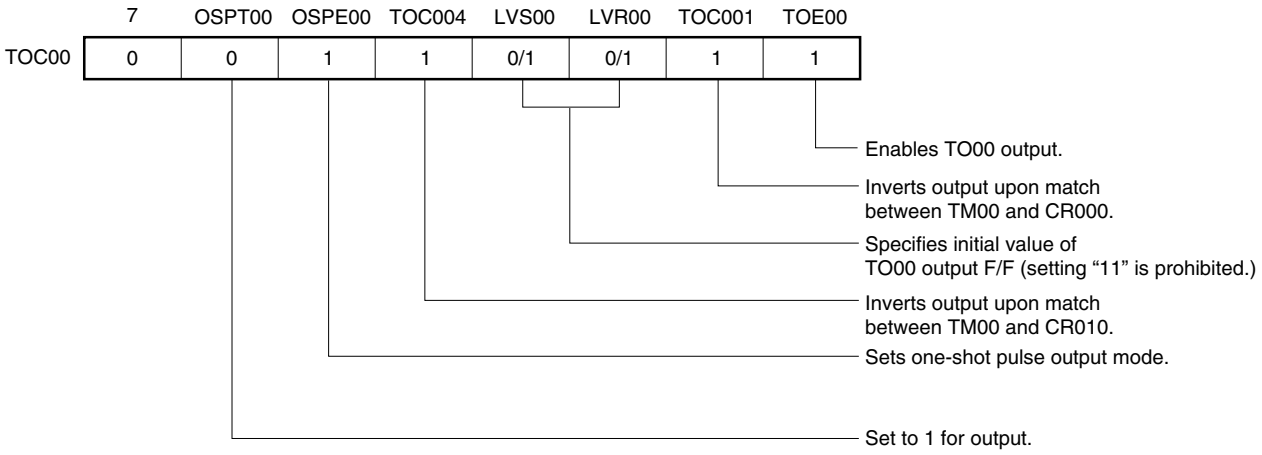
(a) 16-bit timer mode control register 00 (TMC00)



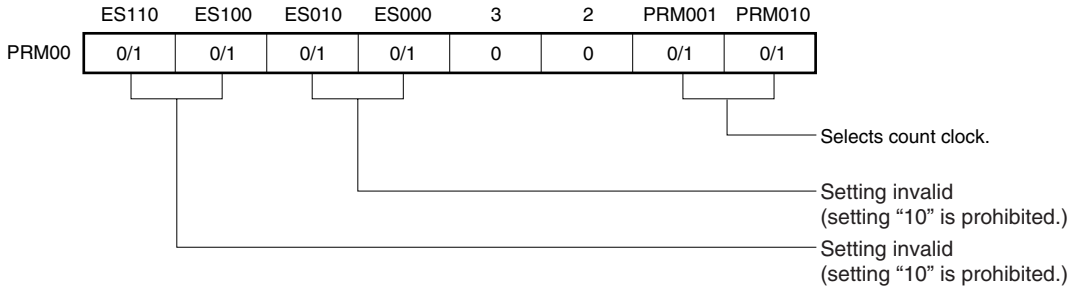
(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)

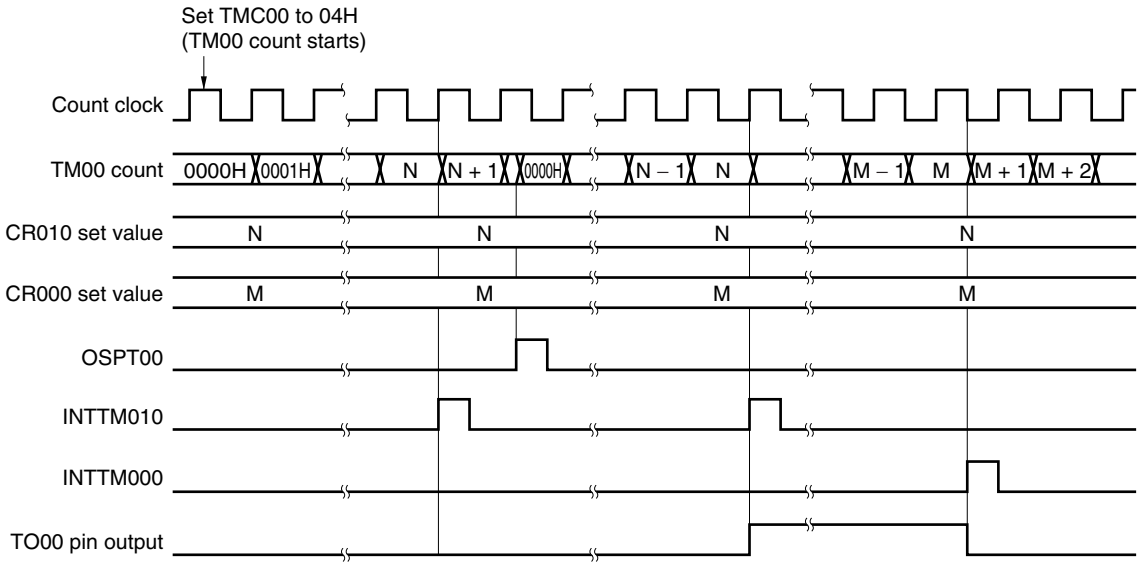


(d) Prescaler mode register 00 (PRM00)



Caution Do not set 0000H to the CR000 and CR010 registers.

Figure 6-34. Timing of One-Shot Pulse Output Operation with Software Trigger



Caution 16-bit timer counter 00 starts operating as soon as a value other than 00 (operation stop mode) is set to the TMC003 and TMC002 bits.

Remark N < M

(2) One-shot pulse output with external trigger

A one-shot pulse can be output from the TO00 pin by setting 16-bit timer mode control register 00 (TMC00), capture/compare control register 00 (CRC00), and 16-bit timer output control register 00 (TOC00) as shown in Figure 6-35, and by using the valid edge of the TI000 pin as an external trigger.

The valid edge of the TI000 pin is specified by bits 4 and 5 (ES000, ES010) of prescaler mode register 00 (PRM00). The rising, falling, or both the rising and falling edges can be specified.

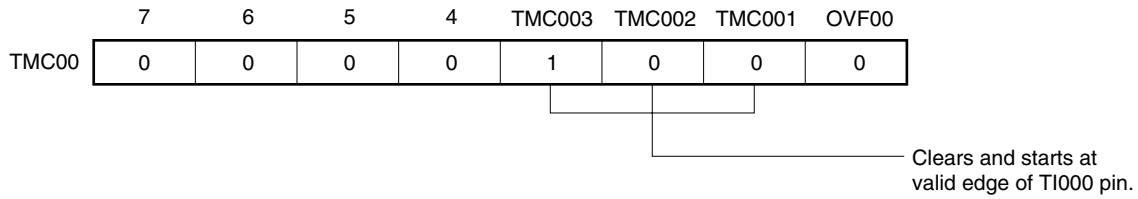
When the valid edge of the TI000 pin is detected, the 16-bit timer/event counter is cleared and started, and the output becomes active at the count value set in advance to 16-bit timer capture/compare register 010 (CR010). After that, the output becomes inactive at the count value set in advance to 16-bit timer capture/compare register 000 (CR000)[Note].

Note The case where N < M is described here. When N > M, the output becomes active with the CR000 register and inactive with the CR010 register. Do not set N to M.

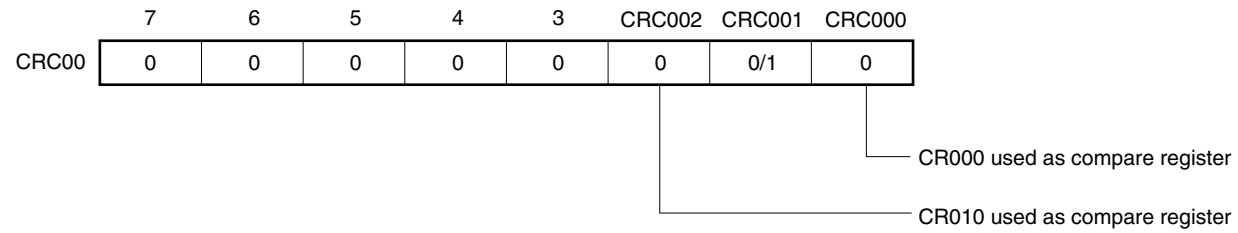
Caution Do not input the external trigger again while the one-shot pulse is output.
To output the one-shot pulse again, wait until the current one-shot pulse output is completed.

Figure 6-35. Control Register Settings for One-Shot Pulse Output with External Trigger (with Rising Edge Specified)

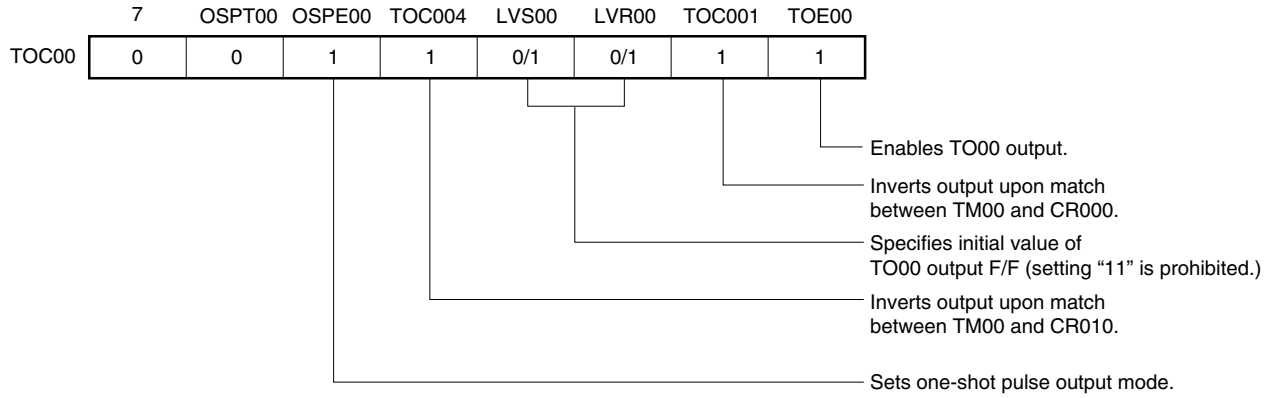
(a) 16-bit timer mode control register 00 (TMC00)



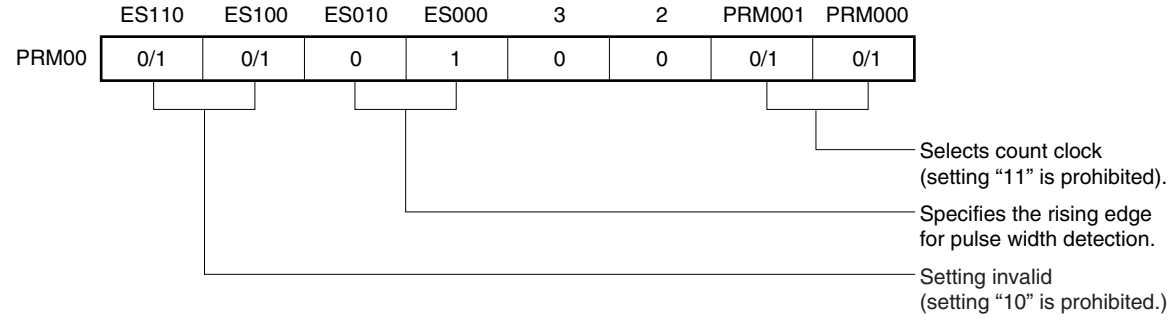
(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)

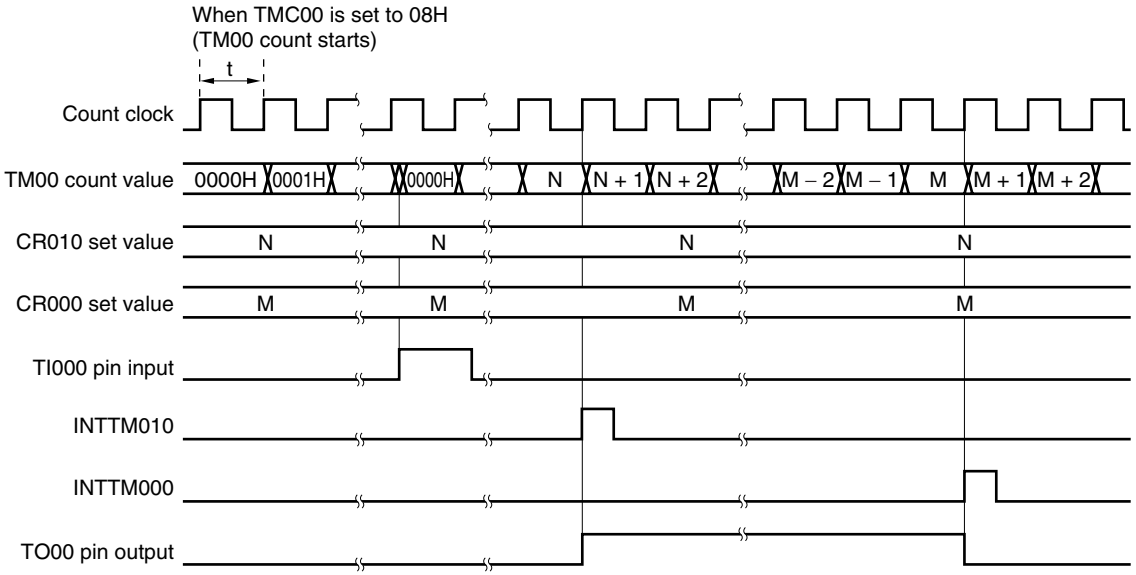


(d) Prescaler mode register 00 (PRM00)



Caution Do not set 0000H to the CR000 and CR010 registers.

Figure 6-36. Timing of One-Shot Pulse Output Operation with External Trigger (with Rising Edge Specified)



Caution 16-bit timer counter 00 starts operating as soon as a value other than 00 (operation stop mode) is set to the TMC002 and TMC003 bits.

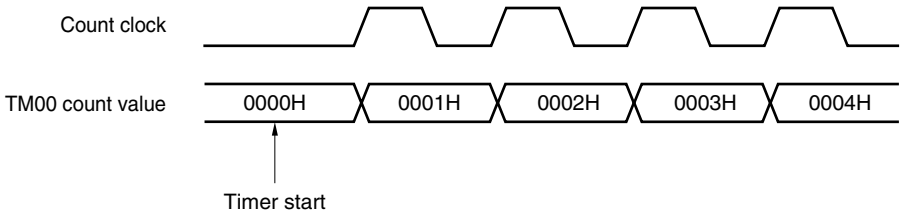
Remark N < M

6.5 Cautions Related to 16-Bit Timer/Event Counter 00

(1) Timer start errors

An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because 16-bit timer counter 00 (TM00) is started asynchronously to the count clock.

Figure 6-37. Start Timing of 16-Bit Timer Counter 00 (TM00)



(2) 16-bit timer counter 00 (TM00) operation

<1> 16-bit timer counter 00 (TM00) starts operation at the moment TMC002 and TMC003 (operation stop mode) are set to a value other than 0, 0, respectively. Set TMC002 and TMC003 to 0, 0 to stop the operation.

<2> Even if TM00 is read, the value is not captured by 16-bit timer capture/compare register 010 (CR010).

<3> During TM00 is read, the count clock is stopped.

<4> Regardless of the CPU's operation mode, when the timer stops, the signals input to pins TI000/TI010 are not acknowledged.

(3) Setting of 16-bit timer capture/compare registers 000, 010 (CR000, CR010)

<1> Set 16-bit timer capture/compare register 000 (CR000) to other than 0000H in the clear & start mode entered on match between TM00 and CR000. This means a 1-pulse count operation cannot be performed when this register is used as an external event counter.

★ <2> When the clear & start mode entered on a match between TM00 and CR000 is selected, CR000 should not be specified as a capture register.

★ <3> In the free-running mode and in the clear & start mode using the valid edge of the TI000 pin, if CR0n0 is set to 0000H, an interrupt request (INTTM0n0) is generated when CR0n0 changes from 0000H to 0001H following overflow (FFFFH).

★ <4> If the new value of CR0n0 is less than the value of TM00, TM00 continues counting, overflows, and then starts counting from 0 again. If the new value of CR0n0 is less than the old value, therefore, the timer must be reset to be restarted after the value of CR0n0 is changed.

(4) Capture register data retention

The values of 16-bit timer capture/compare registers 0n0 (CR0n0) after 16-bit timer/event counter 00 has stopped are not guaranteed.

Remark n = 0, 1

★ **(5) Setting of 16-bit timer mode control register 00 (TMC00)**

The timer operation must be stopped before writing to bits other than the OVF flag.

★ **(6) Setting of capture/compare control register 00 (CRC00)**

The timer operation must be stopped before setting CRC00.

★ **(7) Setting of 16-bit timer output control register 00 (TOC00)**

<1> Timer operation must be stopped before setting other than OSPT00.

<2> If LVS00 and LVR00 are read, 0 is read.

<3> OSPT00 is automatically cleared after data is set, so 0 is read.

<4> Do not set OSPT00 to 1 other than in one-shot pulse output mode.

<5> A write interval of two cycles or more of the count clock selected by prescaler mode register 00 (PRM00) is required to write to OSPT00 successively.

★ **(8) Setting of prescaler mode register 00 (PRM00)**

Always set data to PRM00 after stopping the timer operation.

(9) Valid edge setting

★ Set the valid edge of the TI000 pin with bits 4 and 5 (ES000 and ES010) of prescaler mode register 00 (PRM00) after stopping the timer operation.

(10) One-shot pulse output

One-shot pulse output normally operates only in the free-running mode or in the clear & start mode at the valid edge of the TI000 pin. Because an overflow does not occur in the clear & start mode on a match between TM00 and CR000, one-shot pulse output is not possible.

(11) One-shot pulse output by software

<1> Do not set the OSPT00 bit to 1 again while the one-shot pulse is being output. To output the one-shot pulse again, wait until the current one-shot pulse output is completed.

★ <2> When using the one-shot pulse output of 16-bit timer/event counter 00 with a software trigger, do not change the level of the TI000 pin or its alternate function port pin.

Because the external trigger is valid even in this case, the timer is cleared and started even at the level of the TI000 pin or its alternate function port pin, resulting in the output of a pulse at an undesired timing.

★ <3> Do not set the 16-bit timer capture/compare registers 000 and 010 (CR000 and CR010) to 0000H.

(12) One-shot pulse output with external trigger

<1> Do not input the external trigger again while the one-shot pulse is output.
To output the one-shot pulse again, wait until the current one-shot pulse output is completed.

★ <2> Do not set the 16-bit timer capture/compare registers 000 and 010 (CR000 and CR010) to 0000H.

(13) Operation of OVF00 flag

<1> The OVF00 flag is also set to 1 in the following case.
Either of the clear & start mode entered on a match between TM00 and CR000, clear & start at the valid edge of the TI000 pin, or free-running mode is selected.

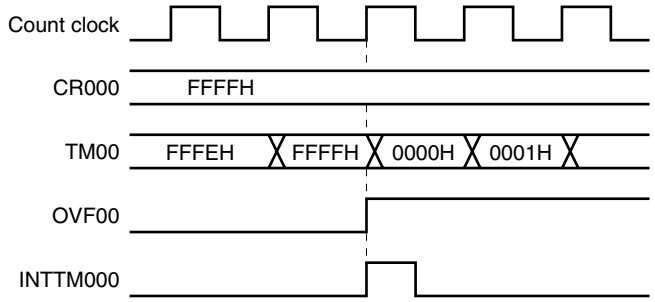
↓

CR000 is set to FFFFH.

↓

When TM00 is counted up from FFFFH to 0000H.

Figure 6-38. Operation Timing of OVF00 Flag

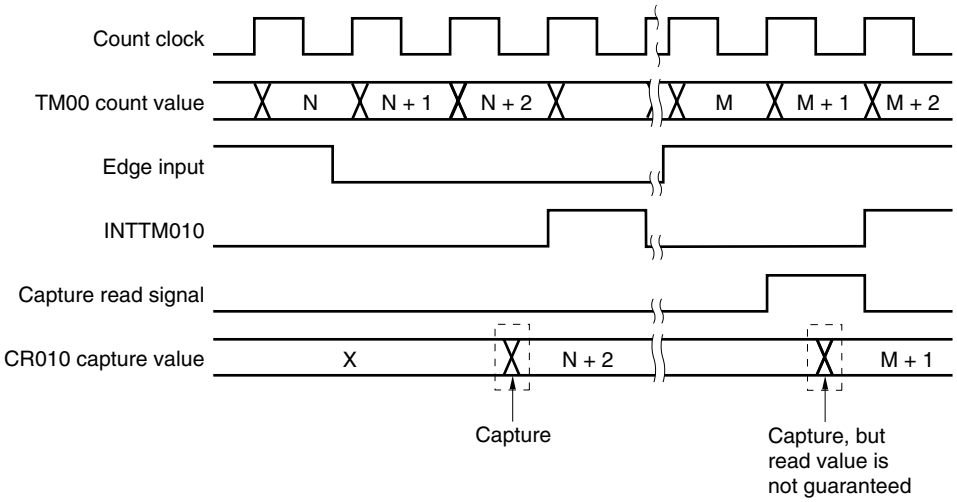


<2> Even if the OVF00 flag is cleared before the next count clock is counted (before TM00 becomes 0001H) after the occurrence of a TM00 overflow, the OVF00 flag is reset newly and clear is disabled.

(14) Conflicting operations

If the register read period and the input of the capture trigger conflict when CR000/CR010 is used as a capture register, the capture trigger input takes precedence and the read data is undefined. Also, if the count stop of the timer and the input of the capture trigger conflict, the captured data is undefined.

Figure 6-39. Capture Register Data Retention Timing



(15) Capture operation

<1> If the TI000 pin is specified as the valid edge of the count clock, a capture operation by the capture register specified as the trigger for the TI000 pin is not possible.

<2> If both the rising and falling edges are selected as the valid edges of the TI000 pin, capture is not performed.

★ <3> When the CRC001 bit value is 1, the TM00 count value is not captured in the CR000 register when a valid edge of the TI010 pin is detected, but the input from the TI010 pin can be used as an external interrupt source because INTTM000 is generated at that timing.

<4> To ensure the reliability of the capture operation, the capture trigger requires a pulse longer than two cycles of the count clock selected by prescaler mode register 00 (PRM00).

<5> The capture operation is performed at the fall of the count clock. A interrupt request input (INTTM0n0), however, occurs at the rise of the next count clock.

★ <6> To use two capture registers, set the TI000 and TI010 pins.

Remark n = 0, 1

(16) Compare operation

The capture operation may not be performed for CR0n0 set in compare mode even if a capture trigger is input.

Remark n = 0, 1

★ (17) Changing compare register during timer operation

<1> With the 16-bit timer capture/compare register 0n0 (CR0n0) used as a compare register, when changing CR0n0 around the timing of a match between 16-bit timer counter 00 (TM00) and 16-bit timer capture/compare register 0n0 (CR0n0) during timer counting, the change timing may conflict with the timing of the match, so the operation is not guaranteed in such cases. To change CR0n0 during timer counting, follow the procedure below using an INTTM000 interrupt.

<Changing cycle (CR000)>

1. Disable the timer output inversion operation at the match between TM00 and CR000 (TOC001 = 0).
2. Disable the INTTM000 interrupt (TMMK000 = 1).
3. Rewrite CR000.
4. Wait for 1 cycle of the TM00 count clock.
5. Enable the timer output inversion operation at the match between TM00 and CR000 (TOC001 = 1).
6. Clear the interrupt request flag of INTTM000 (TMIF000 = 0).
7. Enable the INTTM000 interrupt (TMMK000 = 0).

<Changing duty (CR010)>

1. Disable the timer output inversion operation at the match between TM00 and CR010 (TOC004 = 0).
2. Disable the INTTM000 interrupt (TMMK000 = 1).
3. Rewrite CR010.
4. Wait for 1 cycle of the TM00 count clock.
5. Enable the timer output inversion operation at the match between TM00 and CR010 (TOC004 = 1).
6. Clear the interrupt request flag of INTTM000 (TMIF000 = 0).
7. Enable the INTTM000 interrupt (TMMK000 = 0).

While interrupts and timer output inversion are disabled (1 to 4 above), timer counting is continued. If the value to be set in CR0n0 is small, the value of TM00 may exceed CR0n0. Therefore, set the value, considering the time lapse of the timer clock and CPU after an INTTM000 interrupt has been generated.

Remark n = 0 or 1

<2> If CR010 is changed during timer counting without performing processing <1> above, the value in CR010 may be rewritten twice or more, causing an inversion of the output level of the TO00 pin at each rewrite.

(18) Edge detection

★ <1> In the following cases, note with caution that the valid edge of the TI0n0 pin is detected.

(a) Immediately after a system reset, if a high level is input to the TI0n0 pin, the operation of the 16-bit timer counter 00 (TM00) is enabled

→ If the rising edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.

(b) If the TM00 operation is stopped while the TI0n0 pin is high level, TM00 operation is then enabled after a low level is input to the TI0n0 pin

→ If the falling edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a falling edge is detected immediately after the TM00 operation is enabled.

(c) When the TM00 operation is stopped while the TI0n0 pin is low level, TM00 operation is then enabled after a high level is input to the TI0n0 pin

→ If the rising edge or both rising and falling edges are specified as the valid edge, of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.

Remark n = 0, 1

<2> The sampling clock used to remove noise differs when a TI000 valid edge is used as the count clock and when it is used as a capture trigger. In the former case, the count clock is f_{XP}, and in the latter case the count clock is selected by prescaler mode register 00 (PRM00). The capture operation is not performed until the valid edge is sampled and the valid level is detected twice, thus eliminating, noise with a short pulse width.

(19) External event counter

When reading the external event counter count value, TM00 should be read.

★ **(20) PPG output**

<1> Values in the following range should be set in CR000 and CR010:
0000H < CR010 < CR000 ≤ FFFFH (setting CR000 to 0000H is prohibited)

<2> The cycle of the pulse generated through PPG output (CR000 setting value + 1) has a duty of (CR010 setting value + 1)/(CR000 setting value + 1).

(21) STOP mode or system clock stop mode setting

Except when TI000 pin valid edge is selected as the count clock, stop the timer operation before setting STOP mode or system clock stop mode; otherwise the timer may malfunction when the system clock starts.

★ **(22) P21/TI010/TO00 pin**

When using P21 as the input pin (TI010) of the valid edge, it cannot be used as a timer output pin (TO00). When using P21 as the timer output pin (TO00), it cannot be used as the input pin (TI010) of the valid edge.

CHAPTER 7 8-BIT TIMER H1

7.1 Functions of 8-Bit Timer H1

8-bit timer H1 has the following functions.

- Interval timer
- PWM output mode
- Square-wave output

7.2 Configuration of 8-Bit Timer H1

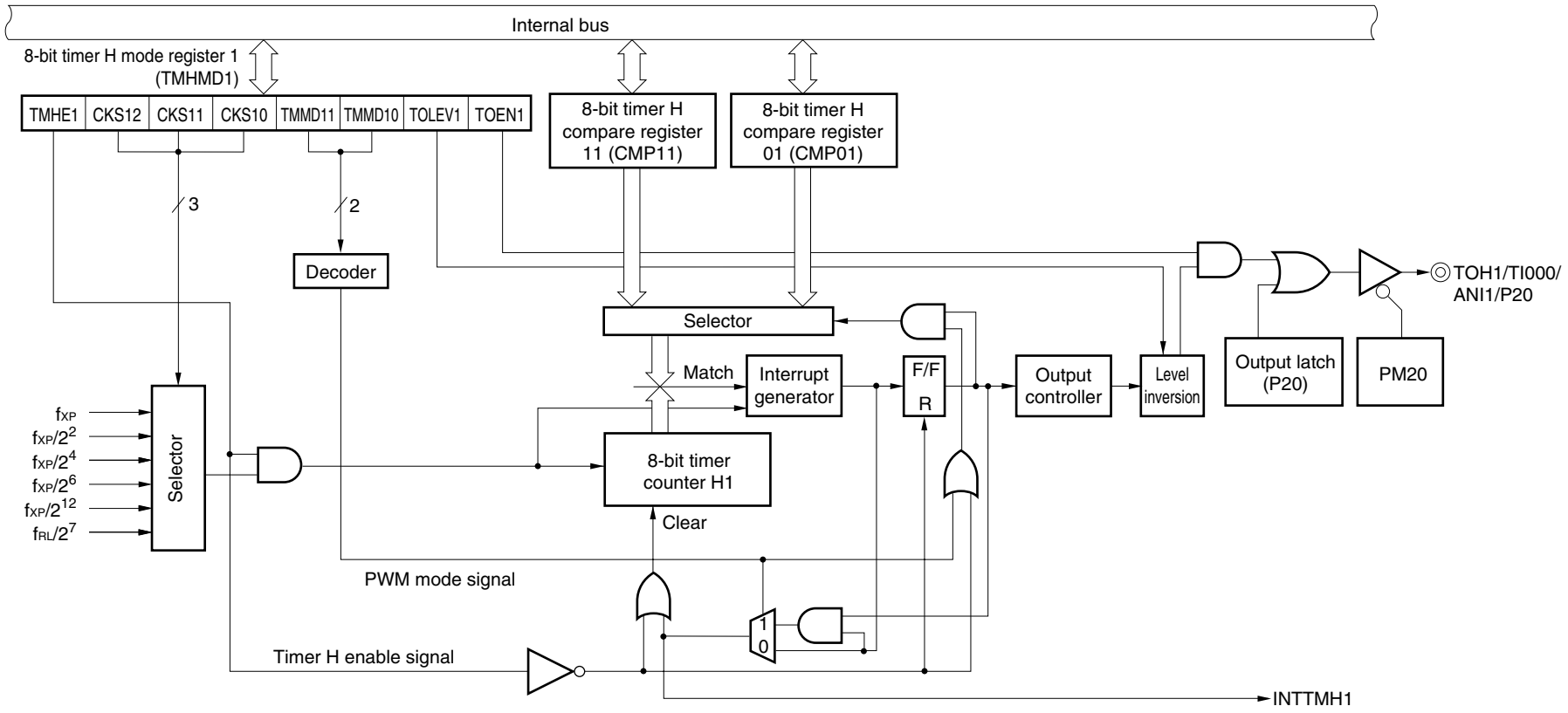
8-bit timer H1 consists of the following hardware.

Table 7-1. Configuration of 8-Bit Timer H1

Item	Configuration
Timer register	8-bit timer counter H1
Registers	8-bit timer H compare register 01 (CMP01) 8-bit timer H compare register 11 (CMP11)
Timer output	TOH1
Control registers	8-bit timer H mode register 1 (TMHMD1) Port mode register 2 (PM2) Port register 2 (P2) Port mode control register 2 (PMC2)

Figure 7-1 shows a block diagram.

Figure 7-1. Block Diagram of 8-Bit Timer H1



(1) 8-bit timer H compare register 01 (CMP01)

This register can be read or written by an 8-bit memory manipulation instruction.

Reset input clears this register to 00H.

Figure 7-2. Format of 8-Bit Timer H Compare Register 01 (CMP01)

Address: FF0EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMP01								

Caution CMP01 cannot be rewritten during timer count operation.

(2) 8-bit timer H compare register 11 (CMP11)

This register can be read or written by an 8-bit memory manipulation instruction.

Reset input clears this register to 00H.

Figure 7-3. Format of 8-Bit Timer H Compare Register 11 (CMP11)

Address: FF0FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMP11								

CMP11 can be rewritten during timer count operation.

If the CMP11 value is rewritten during timer operation, transferring is performed at the timing at which the count value and CMP11 value match. If the transfer timing and writing from CPU to CMP11 conflict, transfer is not performed.

Caution In the PWM output mode, be sure to set CMP11 when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to CMP11).

7.3 Registers Controlling 8-Bit Timer H1

The following four registers are used to control 8-Bit Timer H1.

- 8-bit timer H mode register 1 (TMHMD1)
- Port mode register 2 (PM2)
- Port register 2 (P2)
- Port mode control register 2 (PMC2)

(1) 8-bit timer H mode register 1 (TMHMD1)

This register controls the mode of timer H.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset input clears this register to 00H.

Figure 7-4. Format of 8-Bit Timer H Mode Register 1 (TMHMD1)

Address: FF70H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	<1>	<0>
TMHMD1	TMHE1	CKS12	CKS11	CKS10	TMMD11	TMMD10	TOLEV1	TOEN1

TMHE1	Timer operation enable
0	Stop timer count operation (counter is cleared to 0)
1	Enable timer count operation (count operation started by inputting clock)

CKS12	CKS11	CKS10	Count clock (f_{CNT}) selection
0	0	0	f_{XP} (10 MHz)
0	0	1	$f_{XP}/2^2$ (2.5 MHz)
0	1	0	$f_{XP}/2^4$ (625 kHz)
0	1	1	$f_{XP}/2^6$ (156.25 kHz)
1	0	0	$f_{XP}/2^{12}$ (2.44 kHz)
1	0	1	$f_{RL}/2^7$ (1.88 kHz (TYP.))
Other than above			Setting prohibited

TMMD11	TMMD10	Timer operation mode
0	0	Interval timer mode
1	0	PWM output mode
Other than above		Setting prohibited

TOLEV1	Timer output level control (in default mode)
0	Low level
1	High level

TOEN1	Timer output control
0	Disable output
1	Enable output

Cautions 1. When TMHE1 = 1, setting the other bits of the TMHMD1 register is prohibited.

2. In the PWM output mode, be sure to set 8-bit timer H compare register 11 (CMP11) when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).

Remarks 1. f_{XP}: Oscillation frequency of clock to peripheral hardware

2. f_{RL}: Low-speed Ring-OSC clock oscillation frequency

3. Figures in parentheses apply to operation at f_{XP} = 10 MHz, f_{RL} = 240 kHz (TYP.).

(2) Port mode register 2 (PM2) and port mode control register 2 (PMC2)

When using the P20/TOH1/TI000/ANI0 pin for timer output, clear PM20, the output latch of P20, and PMC20 to 0.

PM2 and PMC2 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset input sets PM2 to FFH, and clears PMC2 to 00H.

Figure 7-5. Format of Port Mode Register 2 (PM2)

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	1	1	PM23	PM22	PM21	PM20

PM2n	P2n pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 7-6. Format of Port Mode Control Register 2 (PMC2)

Address: FF84H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PMC2	0	0	0	0	PMC23	PMC22	PMC21	PMC20

PMC2n	Specification of operation mode (n = 0 to 3)
0	Port/Alternate-function (except A/D converter) mode
1	A/D converter mode

7.4 Operation of 8-Bit Timer H1

7.4.1 Operation as interval timer/square-wave output

When 8-bit timer counter H1 and compare register 01 (CMP01) match, an interrupt request signal (INTTMH1) is generated and 8-bit timer counter H1 is cleared to 00H.

Compare register 11 (CMP11) is not used in interval timer mode. Since a match of 8-bit timer counter H1 and the CMP11 register is not detected even if the CMP11 register is set, timer output is not affected.

By setting bit 0 (TOEN1) of timer H mode register 1 (TMHMD1) to 1, a square wave of any frequency (duty = 50%) is output from TOH1.

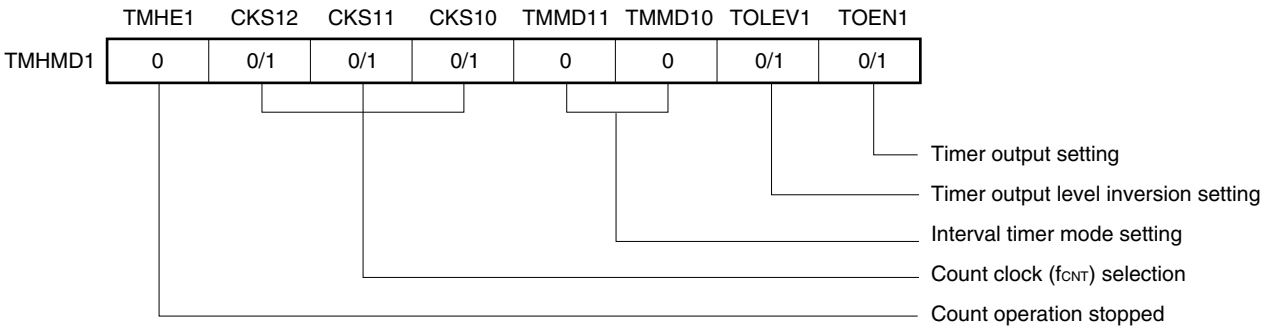
(1) Usage

Generates the INTTMH1 signal repeatedly at the same interval.

<1> Set each register.

Figure 7-7. Register Setting During Interval Timer/Square-Wave Output Operation

(i) Setting timer H mode register 1 (TMHMD1)



(ii) CMP01 register setting

- Compare value (N)

<2> Count operation starts when TMHE1 = 1.

<3> When the values of 8-bit timer counter H1 and the CMP01 register match, the INTTMH1 signal is generated and 8-bit timer counter H1 is cleared to 00H.

Interval time = (N +1)/f_{CNT}

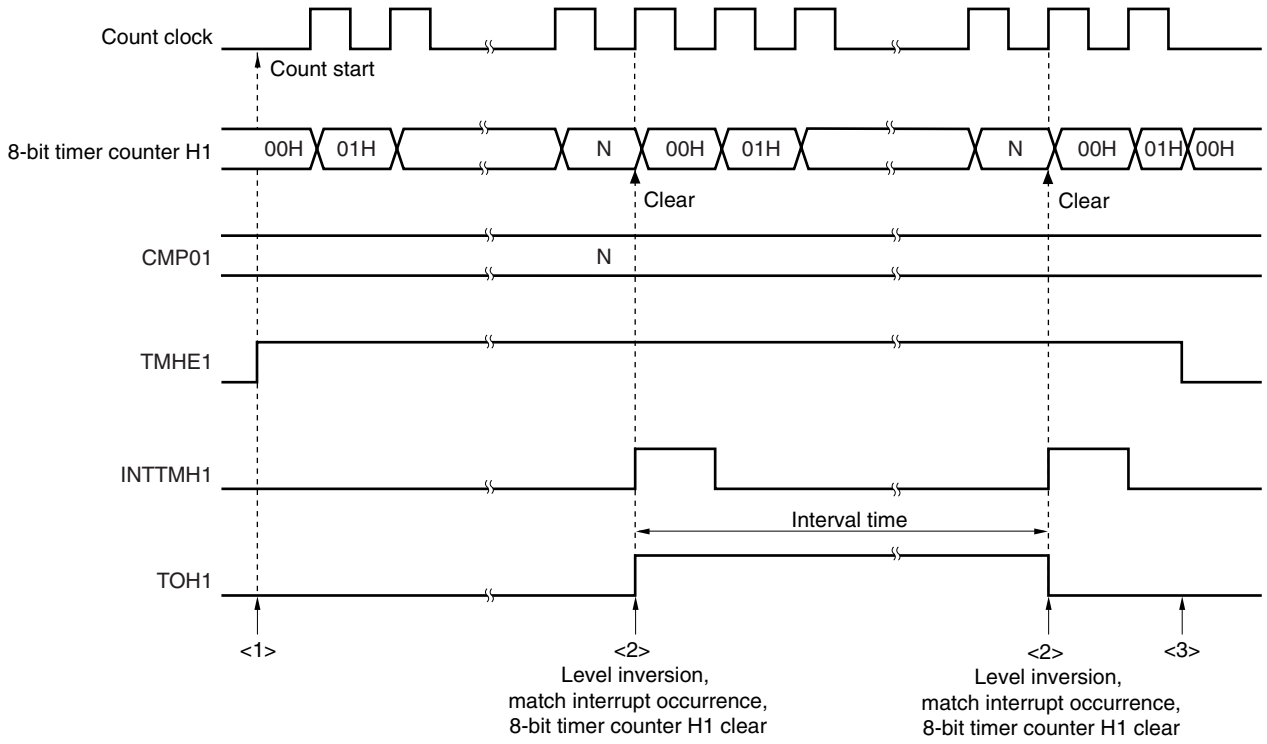
<4> Subsequently, the INTTMH1 signal is generated at the same interval. To stop the count operation, clear TMHE1 to 0.

(2) Timing chart

The timing of the interval timer/square-wave output operation is shown below.

Figure 7-8. Timing of Interval Timer/Square-Wave Output Operation (1/2)

(a) Basic operation



<1> The count operation is enabled by setting the TMHE1 bit to 1. The count clock starts counting no more than 1 clock after the operation is enabled.

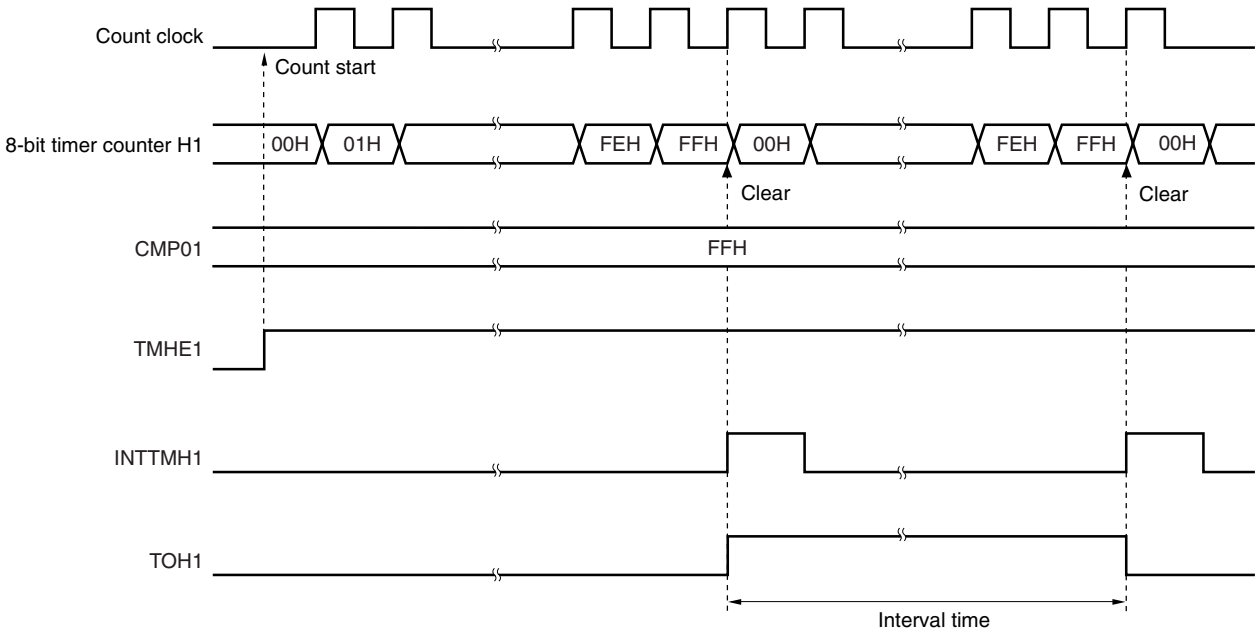
<2> When the values of 8-bit timer counter H1 and the CMP01 register match, the value of 8-bit timer counter H1 is cleared, the TOH1 output level is inverted, and the INTTMH1 signal is output.

<3> The INTTMH1 signal and TOH1 output become inactive by clearing the TMHE1 bit to 0 during timer H1 operation. If these are inactive from the first, the level is retained.

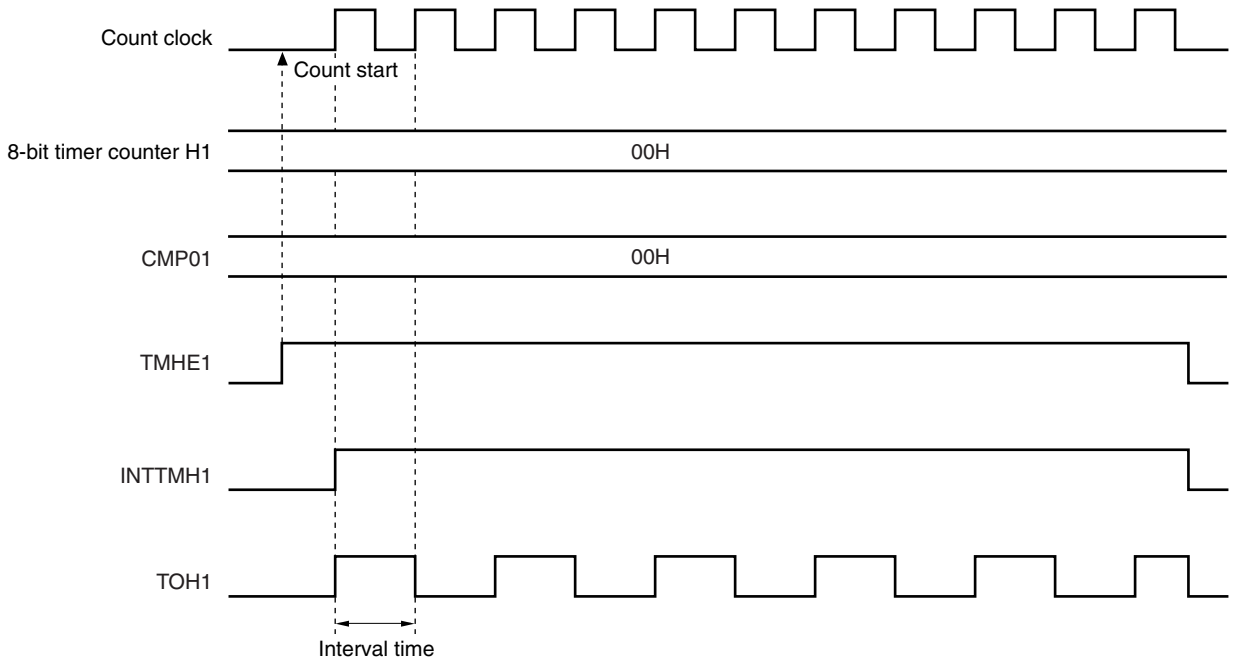
Remark N = 01H to FEH

Figure 7-8. Timing of Interval Timer/Square-Wave Output Operation (2/2)

(b) Operation when CMP01 = FFH



(c) Operation when CMP01 = 00H



7.4.2 Operation as PWM output mode

In PWM output mode, a pulse with an arbitrary duty and arbitrary cycle can be output.

8-bit timer compare register 01 (CMP01) controls the cycle of timer output (TOH1). Rewriting the CMP01 register during timer operation is prohibited.

8-bit timer compare register 11 (CMP11) controls the duty of timer output (TOH1). Rewriting the CMP11 register during timer operation is possible.

The operation in PWM output mode is as follows.

TOH1 output becomes active and 8-bit timer counter H1 is cleared to 0 when 8-bit timer counter H1 and the CMP01 register match after the timer count is started. TOH1 output becomes inactive when 8-bit timer counter H1 and the CMP11 register match.

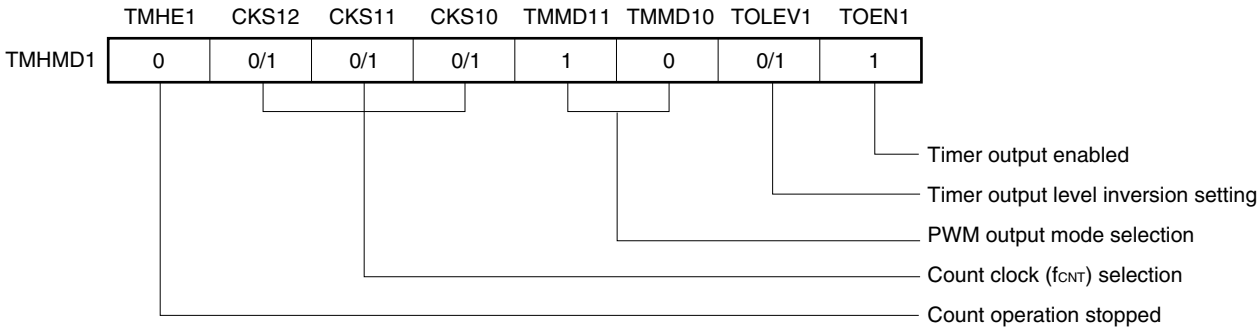
(1) Usage

In PWM output mode, a pulse for which an arbitrary duty and arbitrary cycle can be set is output.

<1> Set each register.

Figure 7-9. Register Setting in PWM Output Mode

(i) Setting timer H mode register 1 (TMHMD1)



(ii) Setting CMP01 register

- Compare value (N): Cycle setting

(iii) Setting CMP11 register

- Compare value (M): Duty setting

Remark 00H ≤ CMP11 (M) < CMP01 (N) ≤ FFH

<2> The count operation starts when TMHE1 = 1.

<3> The CMP01 register is the compare register that is to be compared first after count operation is enabled. When the values of 8-bit timer counter H1 and the CMP01 register match, 8-bit timer counter H1 is cleared, an interrupt request signal (INTTMH1) is generated, and TOH1 output becomes active. At the same time, the compare register to be compared with 8-bit timer counter H1 is changed from the CMP01 register to the CMP11 register.

<4> When 8-bit timer counter H1 and the CMP11 register match, TOH1 output becomes inactive and the compare register to be compared with 8-bit timer counter H1 is changed from the CMP11 register to the CMP01 register. At this time, 8-bit timer counter H1 is not cleared and the INTTMH1 signal is not generated.

<5> By performing procedures <3> and <4> repeatedly, a pulse with an arbitrary duty can be obtained.

<6> To stop the count operation, set TMHE1 = 0.

If the setting value of the CMP01 register is N, the setting value of the CMP11 register is M, and the count clock frequency is f_{CNT}, the PWM pulse output cycle and duty are as follows.

PWM pulse output cycle = $(N+1)/f_{CNT}$
Duty = Active width : Total width of PWM = (M + 1) : (N + 1)

Cautions 1. In PWM output mode, three operation clocks (signal selected using the CKS12 to CKS10 bits of the TMHMD1 register) are required to transfer the CMP11 register value after rewriting the register.

2. Be sure to set the CMP11 register when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).

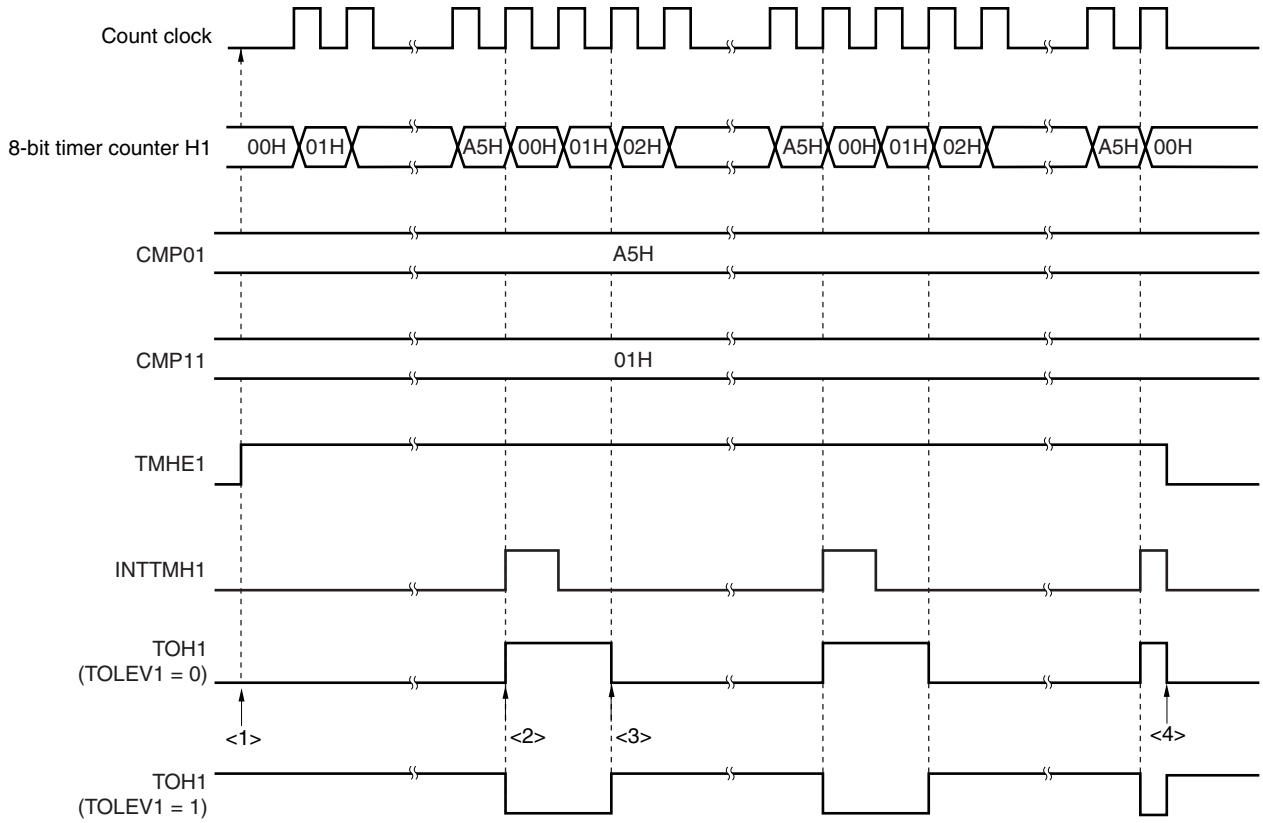
(2) Timing chart

The operation timing in PWM output mode is shown below.

Caution Make sure that the CMP11 register setting value (M) and CMP01 register setting value (N) are within the following range.
00H ≤ CMP11 (M) < CMP01 (N) ≤ FFH

Figure 7-10. Operation Timing in PWM Output Mode (1/4)

(a) Basic operation



<1> The count operation is enabled by setting the TMHE1 bit to 1. Start 8-bit timer counter H1 by masking one count clock to count up. At this time, TOH1 output remains inactive (when TOLEV1 = 0).

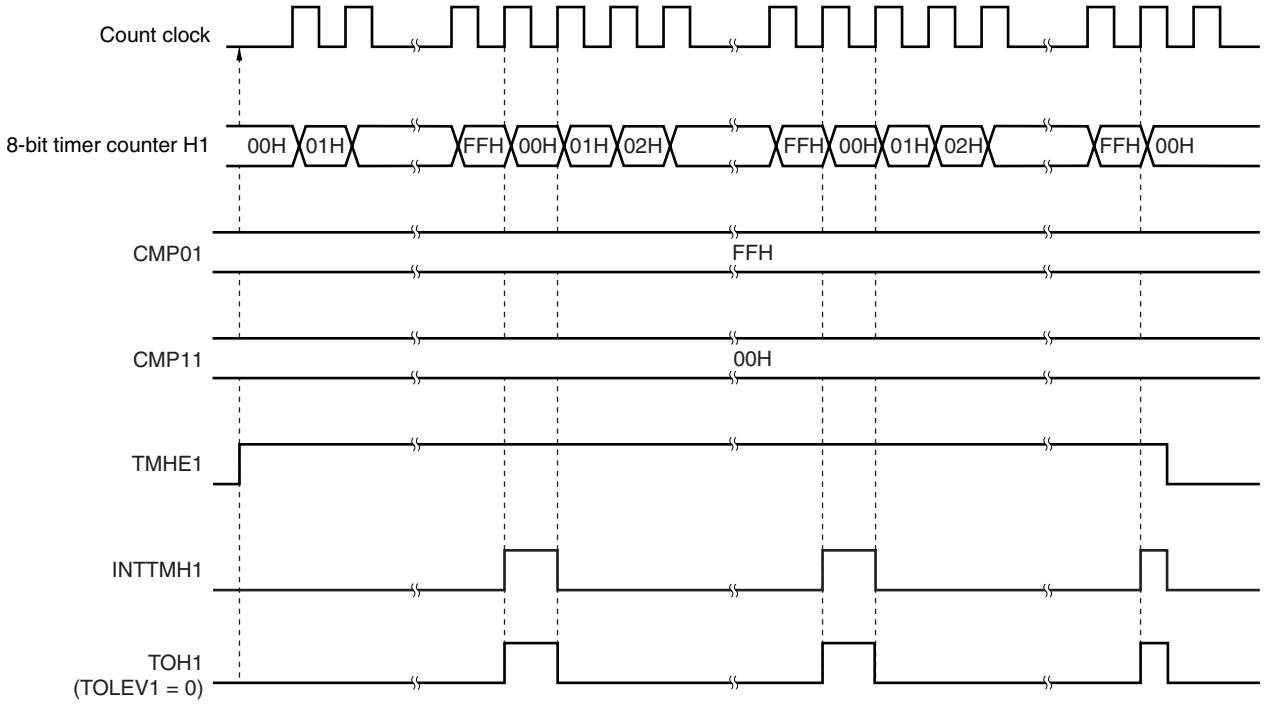
<2> When the values of 8-bit timer counter H1 and the CMP01 register match, the TOH1 output level is inverted, the value of 8-bit timer counter H1 is cleared, and the INTTMH1 signal is output.

<3> When the values of 8-bit timer counter H1 and the CMP11 register match, the level of the TOH1 output is returned. At this time, the 8-bit timer counter value is not cleared and the INTTMH1 signal is not output.

<4> Clearing the TMHE1 bit to 0 during timer H1 operation makes the INTTMH1 signal and TOH1 output inactive.

Figure 7-10. Operation Timing in PWM Output Mode (2/4)

(b) Operation when CMP01 = FFH, CMP11 = 00H



(c) Operation when CMP01 = FFH, CMP11 = FEH

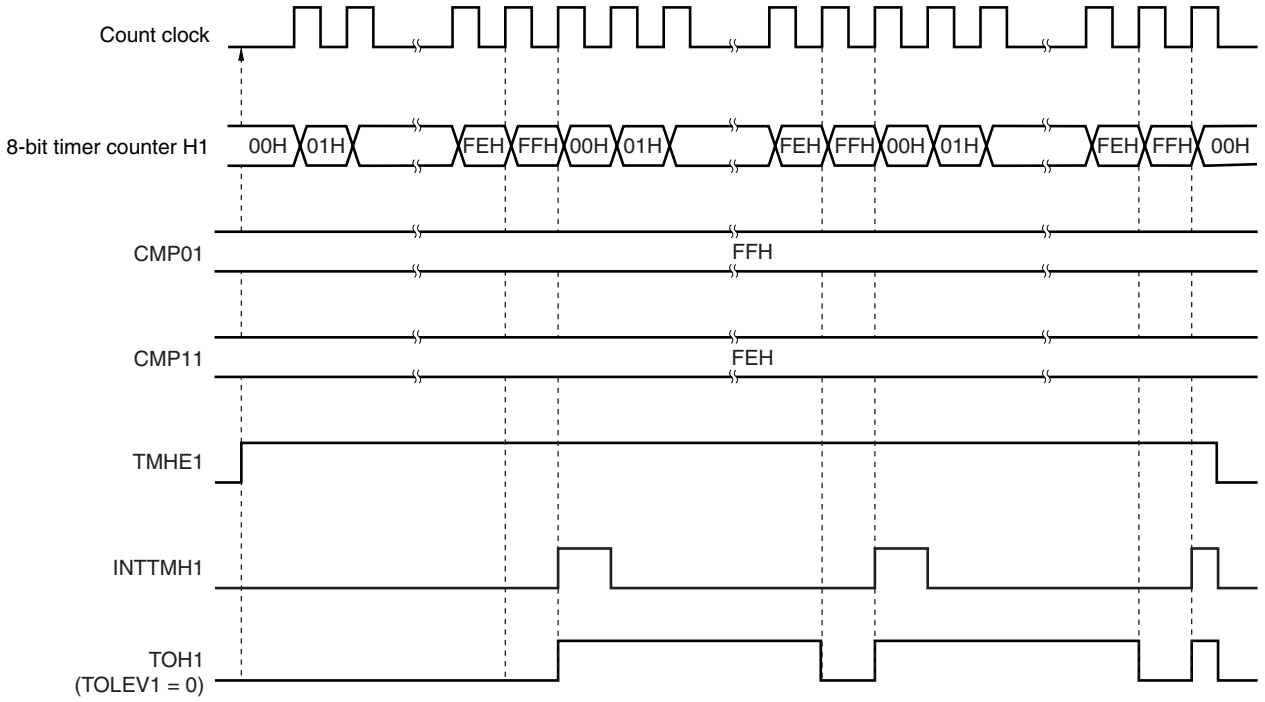


Figure 7-10. Operation Timing in PWM Output Mode (3/4)

(d) Operation when CMP01 = 01H, CMP11 = 00H

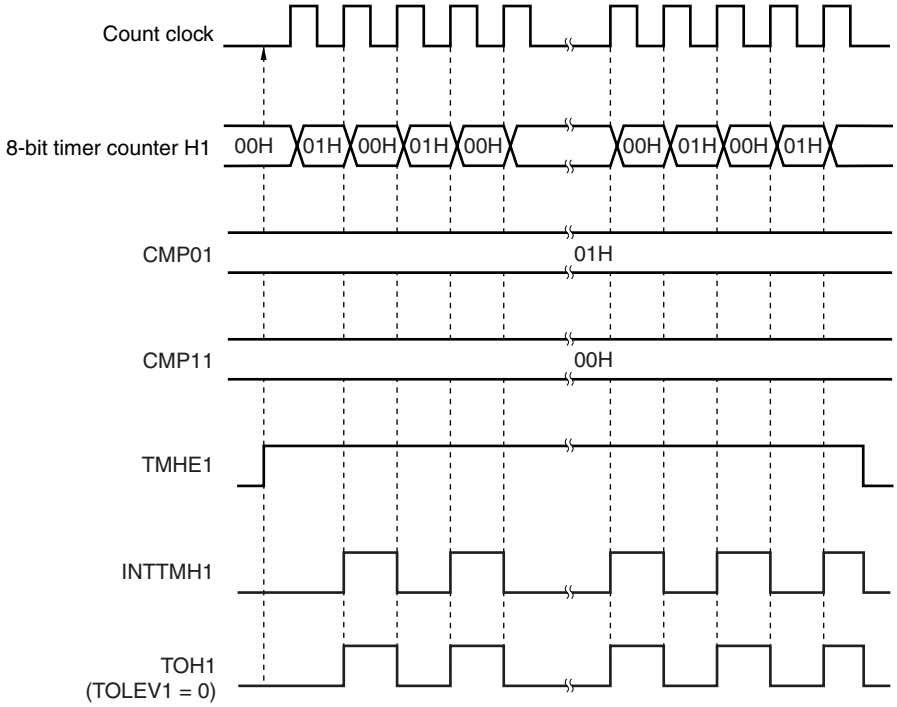
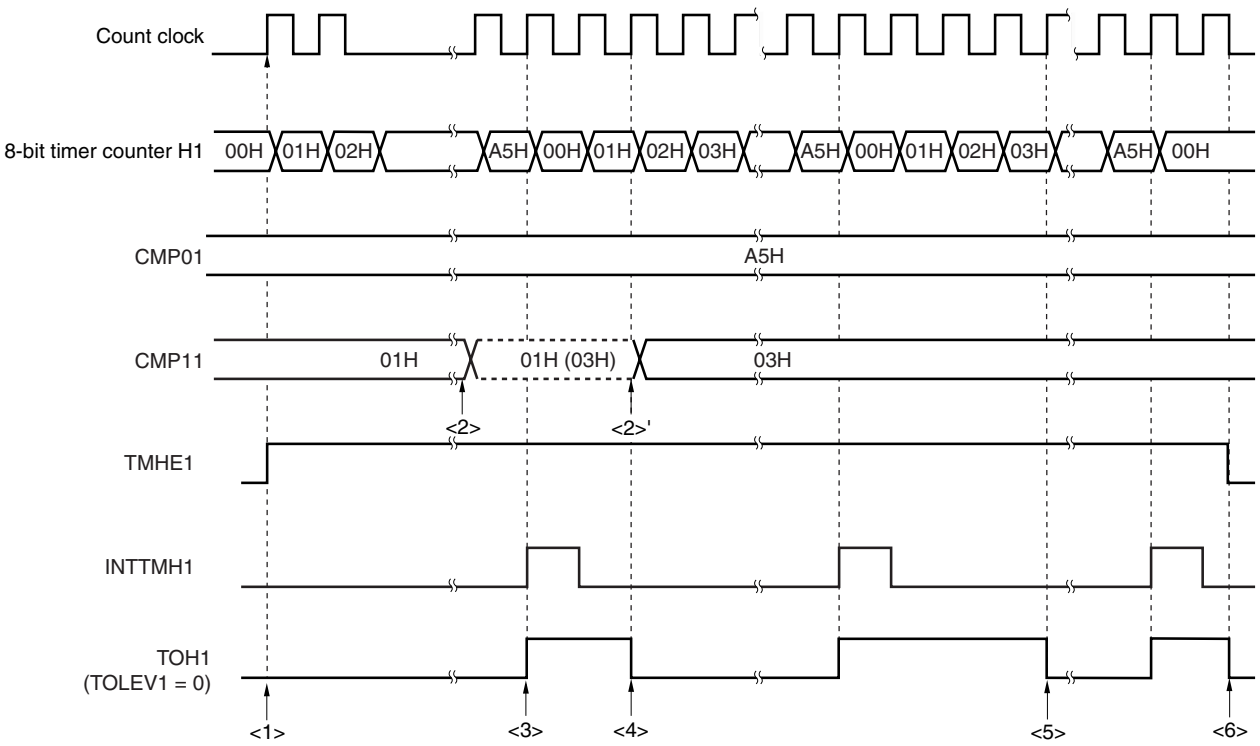


Figure 7-10. Operation Timing in PWM Output Mode (4/4)

(e) Operation by changing CMP11 (CMP11 = 01H → 03H, CMP01 = A5H)



<1> The count operation is enabled by setting TMHE1 = 1. Start 8-bit timer counter H1 by masking one count clock to count up. At this time, the TOH1 output remains inactive (when TOLEV1 = 0).

<2> The CMP11 register value can be changed during timer counter operation. This operation is asynchronous to the count clock.

<3> When the values of 8-bit timer counter H1 and the CMP01 register match, the value of 8-bit timer counter H1 is cleared, the TOH1 output becomes active, and the INTTMH1 signal is output.

<4> If the CMP11 register value is changed, the value is latched and not transferred to the register. When the values of 8-bit timer counter H1 and the CMP11 register before the change match, the value is transferred to the CMP11 register and the CMP11 register value is changed (<2>').

However, three count clocks or more are required from when the CMP11 register value is changed to when the value is transferred to the register. If a match signal is generated within three count clocks, the changed value cannot be transferred to the register.

<5> When the values of 8-bit timer counter H1 and the CMP11 register after the change match, the TOH1 output becomes inactive. 8-bit timer counter H1 is not cleared and the INTTMH1 signal is not generated.

<6> Clearing the TMHE1 bit to 0 during timer H1 operation makes the INTTMH1 signal and TOH1 output inactive.

CHAPTER 8 WATCHDOG TIMER

8.1 Functions of Watchdog Timer

The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

When a reset occurs due to the watchdog timer, bit 4 (WDTRF) of the reset control flag register (RESF) is set to 1. For details of RESF, see **CHAPTER 12 RESET FUNCTION**.

★ **Table 8-1. Loop Detection Time of Watchdog Timer**

Loop Detection Time	
During Low-Speed Ring-OSC Clock Operation	During System Clock Operation
$2^{11}/f_{RL}$ (4.27 ms)	$2^{13}/f_X$ (819.2 μs)
$2^{12}/f_{RL}$ (8.53 ms)	$2^{14}/f_X$ (1.64 ms)
$2^{13}/f_{RL}$ (17.07 ms)	$2^{15}/f_X$ (3.28 ms)
$2^{14}/f_{RL}$ (34.13 ms)	$2^{16}/f_X$ (6.55 ms)
$2^{15}/f_{RL}$ (68.27 ms)	$2^{17}/f_X$ (13.11 ms)
$2^{16}/f_{RL}$ (136.53 ms)	$2^{18}/f_X$ (26.21 ms)
$2^{17}/f_{RL}$ (273.07 ms)	$2^{19}/f_X$ (52.43 ms)
$2^{18}/f_{RL}$ (546.13 ms)	$2^{20}/f_X$ (104.86 ms)

Remarks 1. f_{RL}: Low-speed Ring-OSC clock oscillation frequency

2. f_X: System clock oscillation frequency

3. Figures in parentheses apply to operation at f_{RL} = 480 kHz (MAX.), f_X = 10 MHz.

The operation mode of the watchdog timer (WDT) is switched according to the option byte setting of the on-chip low-speed Ring-OSC oscillator as shown in Table 8-2.

Table 8-2. Option Byte Setting and Watchdog Timer Operation Mode

	Option Byte Setting	
	Low-Speed Ring-OSC Cannot Be Stopped	Low-Speed Ring-OSC Can Be Stopped by Software
Watchdog timer clock source	Fixed to f_{RL} Note 1.	• Selectable by software (f_X, f_{RL} or stopped) • When reset is released: f_{RL}
★ Operation after reset	Operation starts with the maximum interval ($2^{18}/f_{RL}$).	Operation starts with the maximum interval ($2^{18}/f_{RL}$).
Operation mode selection	The interval can be changed only once.	The clock selection/interval can be changed only once.
Features	The watchdog timer cannot be stopped.	The watchdog timer can be stopped Note 2.

Notes 1. As long as power is being supplied, low-speed Ring-OSC oscillation cannot be stopped (except in the reset period).

2. The conditions under which clock supply to the watchdog timer is stopped differ depending on the clock source of the watchdog timer.

<1> If the clock source is f_X, clock supply to the watchdog timer is stopped under the following conditions.
- When f_X is stopped
- In HALT/STOP mode
- During oscillation stabilization time

<2> If the clock source is f_{RL}, clock supply to the watchdog timer is stopped under the following conditions.
- If the CPU clock is f_X and if f_{RL} is stopped by software before execution of the STOP instruction
- In HALT/STOP mode

Remarks 1. f_{RL}: Low-speed Ring-OSC clock oscillation frequency

2. f_X: System clock oscillation frequency

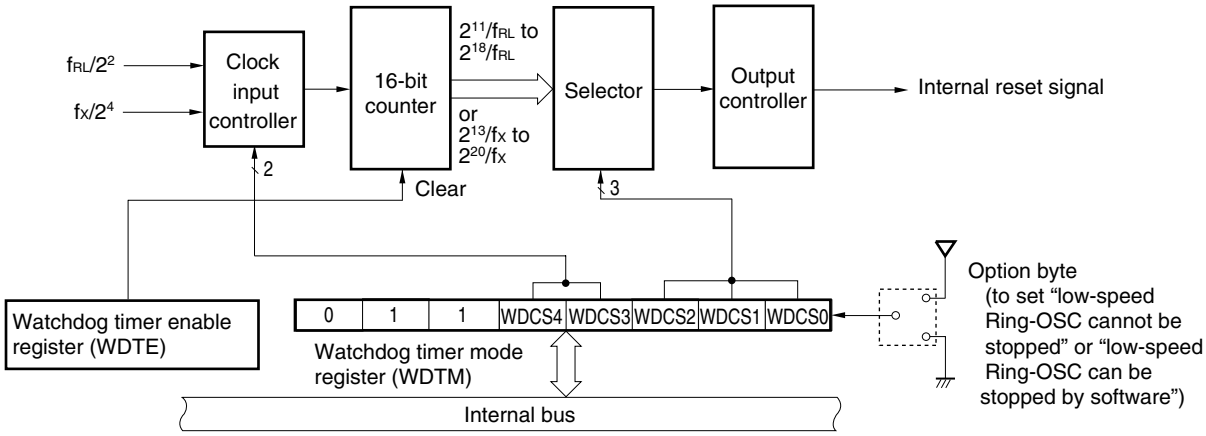
8.2 Configuration of Watchdog Timer

The watchdog timer consists of the following hardware.

Table 8-3. Configuration of Watchdog Timer

Item	Configuration
Control registers	Watchdog timer mode register (WDTM) Watchdog timer enable register (WDTE)

★ **Figure 8-1. Block Diagram of Watchdog Timer**



Remarks 1. f_{RL}: Low-speed Ring-OSC clock oscillation frequency

2. f_X: System clock oscillation frequency

8.3 Registers Controlling Watchdog Timer

The watchdog timer is controlled by the following two registers.

- Watchdog timer mode register (WDTM)
- Watchdog timer enable register (WDTE)

(1) Watchdog timer mode register (WDTM)

This register sets the overflow time and operation clock of the watchdog timer.

This register can be set by an 8-bit memory manipulation instruction and can be read many times, but can be written only once after reset is released.

Reset input sets this register to 67H.

Figure 8-2. Format of Watchdog Timer Mode Register (WDTM)

Address: FF48H After reset: 67H R/W

Symbol	7	6	5	4	3	2	1	0
WDTM	0	1	1	WDCS4	WDCS3	WDCS2	WDCS1	WDCS0

WDCS4[Note 1]	WDCS3[Note 1]	Operation clock selection
0	0	Low-speed Ring-OSC clock (f_{RL})
0	1	System Clock (f_X)
1	×	Watchdog timer operation stopped

★

WDCS2[Note 2]	WDCS1[Note 2]	WDCS0[Note 2]	Overflow time setting	
			During low-speed Ring-OSC clock operation	During system clock operation
0	0	0	$2^{11}/f_{RL}$ (4.27 ms)	$2^{13}/f_X$ (819.2 μs)
0	0	1	$2^{12}/f_{RL}$ (8.53 ms)	$2^{14}/f_X$ (1.64 ms)
0	1	0	$2^{13}/f_{RL}$ (17.07 ms)	$2^{15}/f_X$ (3.28 ms)
0	1	1	$2^{14}/f_{RL}$ (34.13 ms)	$2^{16}/f_X$ (6.55 ms)
1	0	0	$2^{15}/f_{RL}$ (68.27 ms)	$2^{17}/f_X$ (13.11 ms)
1	0	1	$2^{16}/f_{RL}$ (136.53 ms)	$2^{18}/f_X$ (26.21 ms)
1	1	0	$2^{17}/f_{RL}$ (273.07 ms)	$2^{19}/f_X$ (52.43 ms)
1	1	1	$2^{18}/f_{RL}$ (546.13 ms)	$2^{20}/f_X$ (104.86 ms)

Notes 1. If “low-speed Ring-OSC cannot be stopped” is specified by the option byte, this cannot be set. The low-speed Ring-OSC clock will be selected no matter what value is written.

2. Reset is released at the maximum cycle (WDCS2, 1, 0 = 1, 1, 1).

Cautions 1. Set bits 7, 6, and 5 to 0, 1, and 1, respectively (when “low-speed Ring-OSC cannot be stopped” is selected by the option byte, other values are ignored).

2. After reset is released, WDTM can be written only once by an 8-bit memory manipulation instruction. If writing is attempted a second time, an internal reset signal is generated.

3. WDTM cannot be set by a 1-bit memory manipulation instruction.

★ **Cautions 4. When using the flash memory self programming by self writing, set the overflow time for the watchdog timer so that enough everflow time is secured (Example 1-byte writing: 200 μs MIN., 1-block deletion: 10 ms MIN.).**

Remarks 1. f_{RL}: Low-speed Ring-OSC clock oscillation frequency

2. f_X: System clock oscillation frequency

3. ×: Don't care

★ **4.** Figures in parentheses apply to operation at f_{RL} = 480 kHz (MAX.), f_X = 10 MHz.

(2) Watchdog timer enable register (WDTE)

Writing ACH to WDTE clears the watchdog timer counter and starts counting again.

This register can be set by an 8-bit memory manipulation instruction.

Reset input sets this register to 9AH.

Figure 8-3. Format of Watchdog Timer Enable Register (WDTE)

Address: FF49H After reset: 9AH R/W

Symbol	7	6	5	4	3	2	1	0
WDTE								

Cautions 1. If a value other than ACH is written to WDTE, an internal reset signal is generated.

2. If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated.

3. The value read from WDTE is 9AH (this differs from the written value (ACH)).

8.4 Operation of Watchdog Timer

8.4.1 Watchdog timer operation when "low-speed Ring-OSC cannot be stopped" is selected by option byte

The operation clock of watchdog timer is fixed to low-speed Ring-OSC.

After reset is released, operation is started at the maximum cycle (bits 2, 1, and 0 (WDCS2, WDCS1, WDCS0) of the watchdog timer mode register (WDTM) = 1, 1, 1). The watchdog timer operation cannot be stopped.

The following shows the watchdog timer operation after reset release.

1. The status after reset release is as follows.
   - Operation clock: Low-speed Ring-OSC clock
   - ★ Cycle: $2^{18}/f_{RL}$ (546.13 ms: At operation with f_{RL} = 480 kHz (MAX.))
   - Counting starts
2. The following should be set in the watchdog timer mode register (WDTM) by an 8-bit memory manipulation instruction[Notes 1, 2].
   - Cycle: Set using bits 2 to 0 (WDCS2 to WDCS0)
3. After the above procedures are executed, writing ACH to WDTE clears the count to 0, enabling recounting.

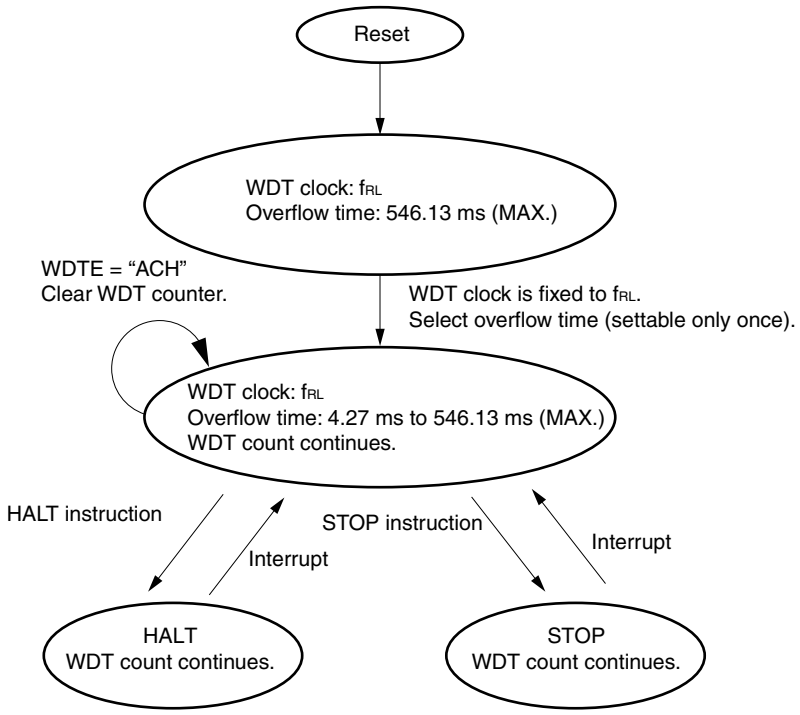
Notes 1. The operation clock (low-speed Ring-OSC clock) cannot be changed. If any value is written to bits 3 and 4 (WDCS3, WDCS4) of WDTM, it is ignored.

2. As soon as WDTM is written, the counter of the watchdog timer is cleared.

Caution In this mode, operation of the watchdog timer cannot be stopped even during STOP instruction execution. For 8-bit timer H1 (TMH1), a division of the low-speed Ring-OSC clock can be selected as the count source, so clear the watchdog timer using the interrupt request of TMH1 before the watchdog timer overflows after STOP instruction execution. If this processing is not performed, an internal reset signal is generated when the watchdog timer overflows after STOP instruction execution.

A status transition diagram is shown below

★ **Figure 8-4. Status Transition Diagram When "Low-Speed Ring-OSC Cannot Be Stopped" Is Selected by Option Byte**



8.4.2 Watchdog timer operation when "low-speed Ring-OSC can be stopped by software" is selected by option byte

The operation clock of the watchdog timer can be selected as either the low-speed Ring-OSC clock or system clock.

After reset is released, operation is started at the maximum cycle of the low-speed Ring-OSC clock (bits 2, 1, and 0 (WDCS2, WDCS1, WDCS0) of the watchdog timer mode register (WDTM) = 1, 1, 1).

The following shows the watchdog timer operation after reset release.

1. The status after reset release is as follows.
   - Operation clock: Low-speed Ring-OSC clock
   - ★ Cycle: $2^{18}/f_{RL}$ (546.13 ms: At operation with f_{RL} = 480 kHz (MAX.))
   - Counting starts
2. The following should be set in the watchdog timer mode register (WDTM) by an 8-bit memory manipulation instruction[Notes 1, 2, 3].
   - Operation clock: Any of the following can be selected using bits 3 and 4 (WDCS3 and WDCS4).
     Low-speed Ring-OSC clock (f_{RL})
     Syatem clock (f_X)
     Watchdog timer operation stopped
   - Cycle: Set using bits 2 to 0 (WDCS2 to WDCS0)
3. After the above procedures are executed, writing ACH to WDTE clears the count to 0, enabling recounting.

Notes 1. As soon as WDTM is written, the counter of the watchdog timer is cleared.

2. Set bits 7, 6, and 5 to 0, 1, 1, respectively. Do not set the other values.

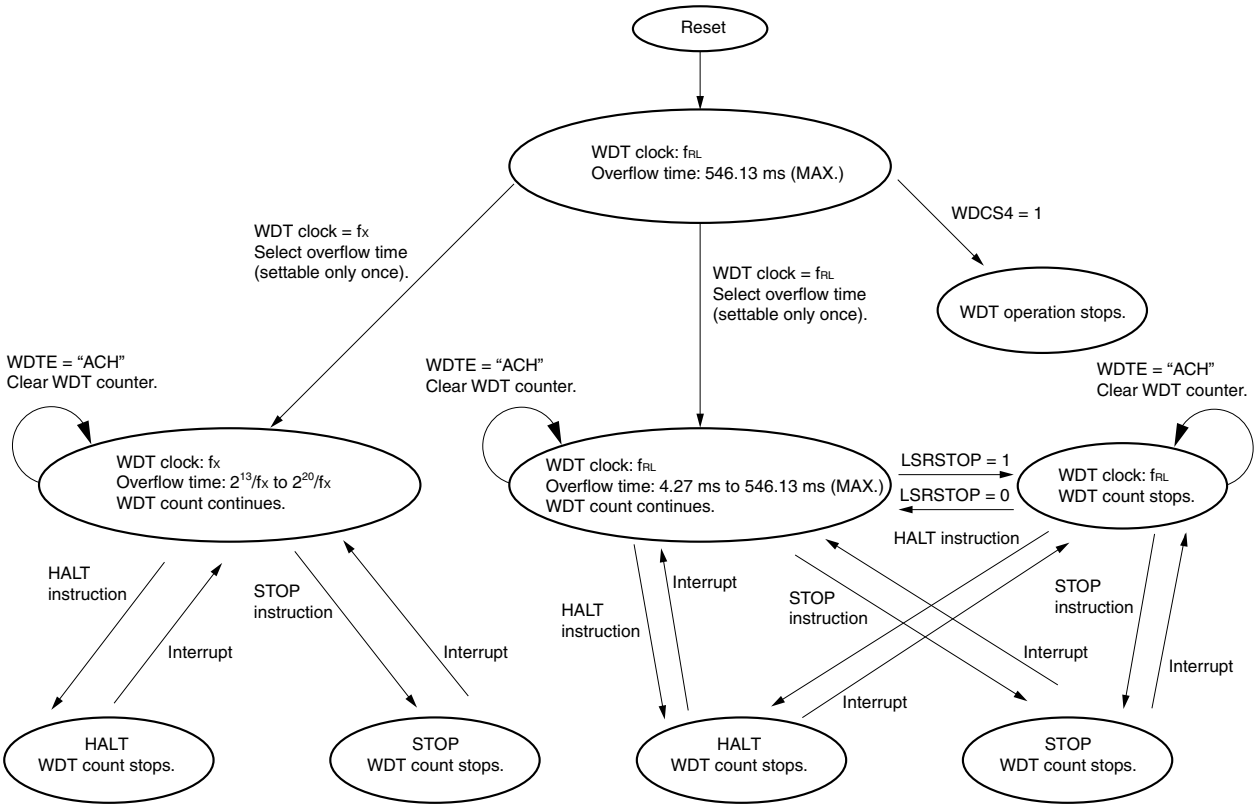
3. If the watchdog timer is stopped by setting WDCS4 and WDCS3 to 1 and ×, respectively, an internal reset signal is not generated even if the following processing is performed.
   - WDTM is written a second time.
   - A 1-bit memory manipulation instruction is executed to WDTE.
   - A value other than ACH is written to WDTE.

Caution In this mode, watchdog timer operation is stopped during HALT/STOP instruction execution. After HALT/STOP mode is released, counting is started again using the operation clock of the watchdog timer set before HALT/STOP instruction execution by WDTM. At this time, the counter is not cleared to 0 but holds its value.

For the watchdog timer operation during STOP mode and HALT mode in each status, see **8.4.3 Watchdog timer operation in STOP mode** and **8.4.4 Watchdog timer operation in HALT mode**.

A status transition diagram is shown below.

★ **Figure 8-5. Status Transition Diagram When "Low-Speed Ring-OSC Can Be Stopped by Software" Is Selected by Option Byte**



8.4.3 Watchdog timer operation in STOP mode (when "low-speed Ring-OSC can be stopped by software" is selected by option byte)

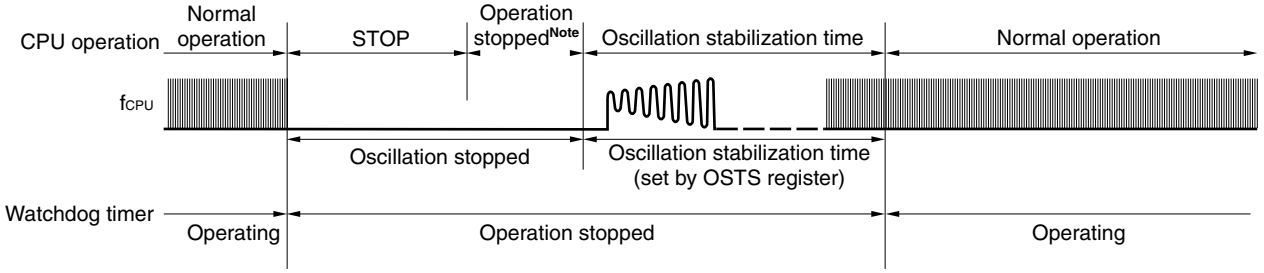
The watchdog timer stops counting during STOP instruction execution regardless of whether the system clock or low-speed Ring-OSC clock is being used.

(1) When the watchdog timer operation clock is the system clock (fx) when the STOP instruction is executed

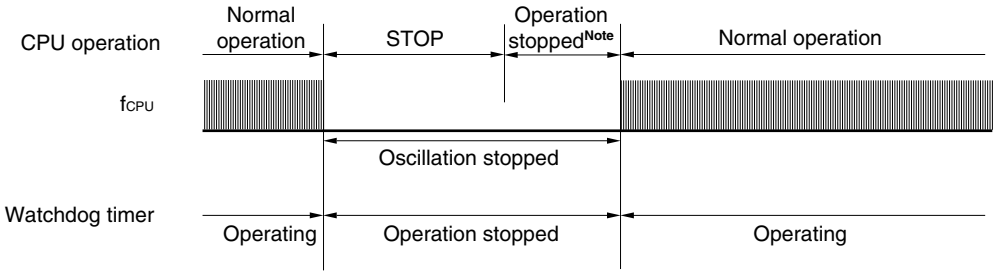
When STOP instruction is executed, operation of the watchdog timer is stopped. After STOP mode is released, ★ operation stops for 34 μs (TYP.) (after waiting for the oscillation stabilization time set by the oscillation stabilization time select register (OSTS) after operation stops in the case of crystal/ceramic oscillation) and then counting is started again using the operation clock before the operation was stopped. At this time, the counter is not cleared to 0 but holds its value.

Figure 8-6. Operation in STOP Mode (WDT Operation Clock: Clock to Peripheral Hardware)

<1> CPU clock: Crystal/ceramic oscillation clock



<2> CPU clock: High-speed Ring-OSC clock or external clock input



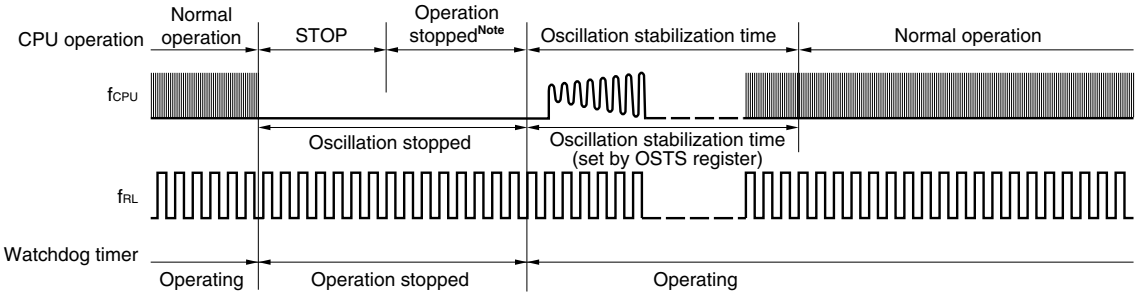
★ **Note** The operation stop time is 17 μs (MIN.), 34 μs (TYP.), and 67 μs (MAX.).

(2) When the watchdog timer operation clock is the low-speed Ring-OSC clock (f_{RL}) when the STOP instruction is executed

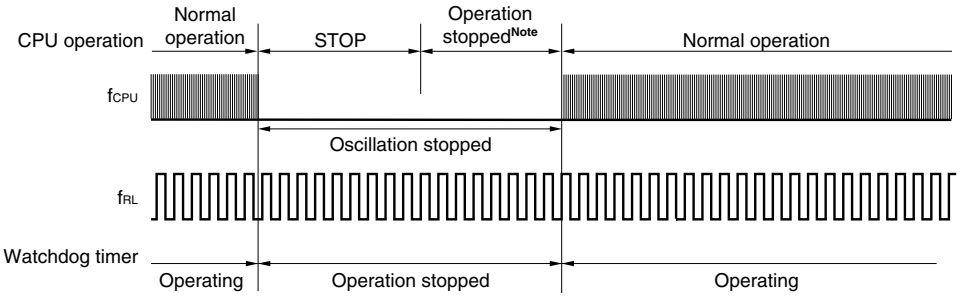
When the STOP instruction is executed, operation of the watchdog timer is stopped. After STOP mode is ★ released, operation stops for 34 μs (TYP.) and then counting is started again using the operation clock before the operation was stopped. At this time, the counter is not cleared to 0 but holds its value.

Figure 8-7. Operation in STOP Mode (WDT Operation Clock: Low-Speed Ring-OSC Clock)

<1> CPU clock: Crystal/ceramic oscillation clock



<2> CPU clock: High-speed Ring-OSC clock or external clock input

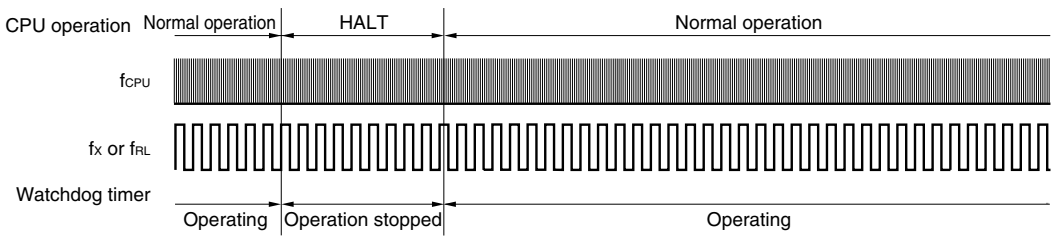


★ **Note** The operation stop time is 17 μs (MIN.), 34 μs (TYP.), and 67 μs (MAX.).

8.4.4 Watchdog timer operation in HALT mode (when "low-speed Ring-OSC can be stopped by software" is selected by option byte)

The watchdog timer stops counting during HALT instruction execution regardless of whether the operation clock of the watchdog timer is the system clock (f_X) or low-speed Ring-OSC clock (f_{RL}). After HALT mode is released, counting is started again using the operation clock before the operation was stopped. At this time, the counter is not cleared to 0 but holds its value.

Figure 8-8. Operation in HALT Mode



CHAPTER 9 A/D CONVERTER

9.1 Functions of A/D Converter

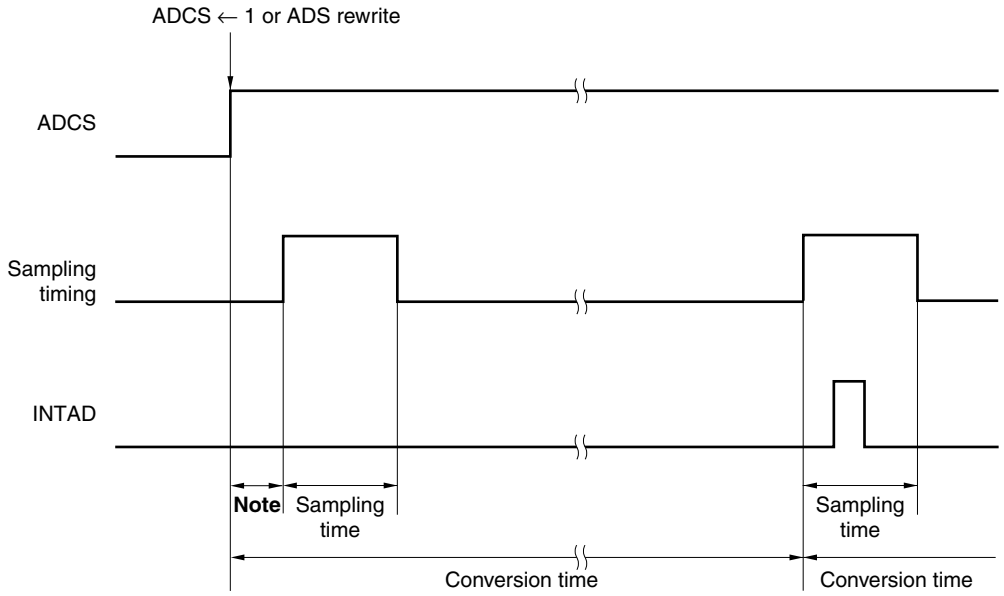
The A/D converter converts an analog input signal into a digital value, and consists of up to four channels (ANI0 to ANI3) with a resolution of 10 bits.

The A/D converter has the following function.

- **10-bit resolution A/D conversion**
  10-bit resolution A/D conversion is carried out repeatedly for one channel selected from analog inputs ANI0 to ANI3. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated.

★ Figure 9-1 shows the timing of sampling and A/D conversion, and Table 9-1 shows the sampling time and A/D conversion time.

Figure 9-1. Timing of A/D Converter Sampling and A/D Conversion



★ **Note** 2 or 3 clocks are required from the ADCS rising to sampling start.

★ **Table 9-1. Sampling Time and A/D Conversion Time**

FR2	FR1	FR0	Reference Voltage Range[Note 1]	Sampling Time[Note 2]	Conversion Time[Note 3]	f_{XP} = 8 MHz		f_{XP} = 10 MHz	
						Sampling Time[Note 2]	Conversion Time[Note 3]	Sampling Time[Note 2]	Conversion Time[Note 3]
0	0	0	$V_{DD} \geq 4.5$ V	$12/f_{XP}$	$36/f_{XP}$	1.5 μs	4.5 μs	1.2 μs	3.6 μs
0	0	1	$V_{DD} \geq 2.85$ V	$24/f_{XP}$	$48/f_{XP}$	3.0 μs	6.0 μs	Setting prohibited (2.4 μs)	Setting prohibited (4.8 μs)
0	1	0	$V_{DD} \geq 2.7$ V	$48/f_{XP}$	$72/f_{XP}$	Setting prohibited (6.0 μs)	Setting prohibited (9.0 μs)	Setting prohibited (4.8 μs)	Setting prohibited (7.2 μs)
0	1	1	$V_{DD} \geq 2.7$ V	$88/f_{XP}$	$112/f_{XP}$	11.0 μs	14.0 μs	Setting prohibited (8.8 μs)	Setting prohibited (11.2 μs)
1	0	0	$V_{DD} \geq 4.5$ V	$24/f_{XP}$	$72/f_{XP}$	3.0 μs	9.0 μs	2.4 μs	7.2 μs
1	0	1	$V_{DD} \geq 2.85$ V	$48/f_{XP}$	$96/f_{XP}$	6.0 μs	12.0 μs	4.8 μs	9.6 μs
1	1	0	$V_{DD} \geq 2.7$ V	$96/f_{XP}$	$144/f_{XP}$	12.0 μs	18.0 μs	Setting prohibited (9.6 μs)	Setting prohibited (14.4 μs)
1	1	1	$V_{DD} \geq 2.7$ V	$176/f_{XP}$	$224/f_{XP}$	22.0 μs	28.0 μs	17.6 μs	22.4 μs

★ **Notes 1.** Be sure to set the FR2, FR1, and FR0 in accordance with the reference voltage range and satisfy **Notes 2** and **3** below.

Example When $V_{DD} \geq 2.7$ V

- Set FR2, FR1, and FR0 = 0, 1, 1 or 1, 1, 1.
- The sampling time is 11.0 μs or more and the A/D conversion time is 14.0 μs or more and less than 100 μs.

2. Set the sampling time as follows.

- $V_{DD} \geq 4.5$ V: 1.0 μs or more
- $V_{DD} \geq 4.0$ V: 2.4 μs or more
- $V_{DD} \geq 2.85$ V: 3.0 μs or more
- $V_{DD} \geq 2.7$ V: 11.0 μs or more

3. Set the A/D conversion time as follows.

- $V_{DD} \geq 4.5$ V: 3.0 μs or more and less than 100 μs
- $V_{DD} \geq 4.0$ V: 4.8 μs or more and less than 100 μs
- $V_{DD} \geq 2.85$ V: 6.0 μs or more and less than 100 μs
- $V_{DD} \geq 2.7$ V: 14.0 μs or more and less than 100 μs

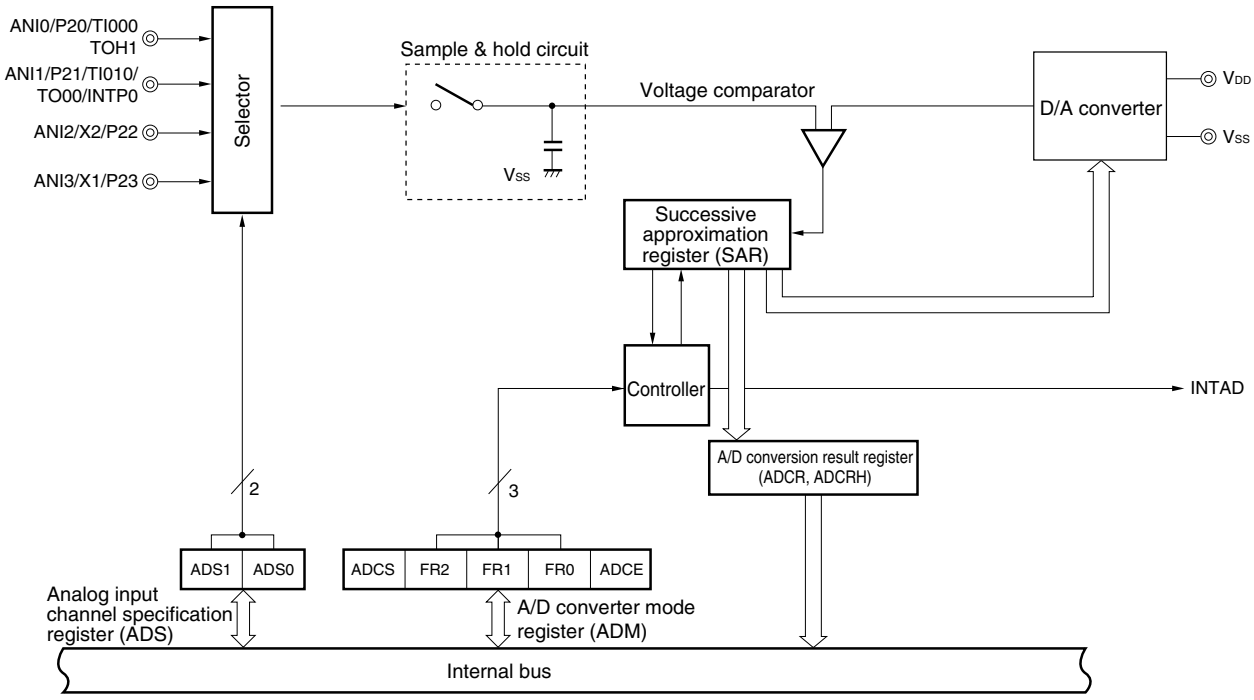
Caution The above sampling time and conversion time do not include the clock frequency error. Select the conversion time taking the clock frequency error into consideration.

Remarks 1. f_{XP}: Oscillation frequency of clock to peripheral hardware

★ **2.** The conversion time refers to the total of the sampling time and the time from successively comparing with the sampling value until the conversion result is output.

Figure 9-2 shows the block diagram of A/D converter.

★ **Figure 9-2. Block Diagram of A/D Converter**



Cautions 1. In the 78K0S/KU1+ and 78K0S/KY1+, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

2. In the 78K0S/KU1+ and 78K0S/KY1+, V_{DD} functions alternately as the A/D converter reference voltage input. When using the A/D converter, stabilize V_{DD} at the supply voltage used (2.7 to 5.5 V).

9.2 Configuration of A/D Converter

The A/D converter consists of the following hardware.

Table 9-2. Registers of A/D Converter Used on Software

Item	Configuration
Registers	10-bit A/D conversion result register (ADCR) 8-bit A/D conversion result register (ADCRH) A/D converter mode register (ADM) Analog input channel specification register (ADS) Port mode register 2 (PM2) Port mode control register 2 (PMC2)

(1) ANI0 to ANI3 pins

These are the analog input pins of the 4-channel A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin by the analog input channel specification register (ADS) can be used as input port pins.

(2) Sample & hold circuit

The sample & hold circuit samples the input signal of the analog input pin selected by the selector when A/D conversion is started, and holds the sampled analog input voltage value during A/D conversion.

★ **(3) D/A converter**

The D/A converter is connected between V_{DD} and V_{SS}, and generates a voltage to be compared with the analog input signal.

(4) Voltage comparator

The voltage comparator compares the sampled analog input voltage and the output voltage of the D/A converter.

(5) Successive approximation register (SAR)

This register compares the sampled analog voltage and the voltage of the D/A converter, and converts the result, starting from the most significant bit (MSB).

When the voltage value is converted into a digital value down to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register are transferred to the A/D conversion result register (ADCR).

(6) 10-bit A/D conversion result register (ADCR)

The result of A/D conversion is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCR register holds the result of A/D conversion in its lower 10 bits (the higher 6 bits are fixed to 0).

(7) 8-bit A/D conversion result register (ADCRH)

The result of A/D conversion is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register holds the result of A/D conversion in its higher 8 bits.

(8) Controller

When A/D conversion has been completed, INTAD is generated.

(9) V_{DD} pin

This is the positive power supply pin.

In the 78K0S/KU1+ and 78K0S/KY1+, V_{DD} functions alternately as the A/D converter reference voltage input. When using the A/D converter, stabilize V_{DD} at the supply voltage used (2.7 to 5.5 V).

(10) V_{SS} pin

This is the ground potential pin.

In the 78K0S/KU1+ and 78K0S/KY1+, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

(11) A/D converter mode register (ADM)

This register is used to set the conversion time of the analog input signal to be converted, and to start or stop the conversion operation.

(12) Analog input channel specification register (ADS)

This register is used to specify the port that inputs the analog voltage to be converted into a digital signal.

(13) Port mode control register 2 (PMC2)

This register is used when the P20/ANI0/TI000/TOH1, P21/ANI1/TI010/TO00/INTP0, P22/ANI2, and P23/ANI3 pins are used as the analog input pins of the A/D converter.

9.3 Registers Used by A/D Converter

The A/D converter uses the following six registers.

- A/D converter mode register (ADM)
- Analog input channel specification register (ADS)
- 10-bit A/D conversion result register (ADCR)
- 8-bit A/D conversion result register (ADCRH)
- Port mode register 2 (PM2)
- Port mode control register 2 (PMC2)

(1) A/D converter mode register (ADM)

This register sets the conversion time for analog input to be A/D converted, and starts/stops conversion.

ADM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset input clears this register to 00H.

Figure 9-3. Format of A/D Converter Mode Register (ADM)

Address: FF80H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
ADM	ADCS	0	FR2	FR1	FR0	0	0	ADCE

ADCS	A/D conversion operation control
0	Stops conversion operation
1 Note 1	Starts conversion operation

★

FR2	FR1	FR0	Reference Voltage Range Note 2	Sampling Time Note 3	Conversion Time Note 4	f_{XP} = 8 MHz		f_{XP} = 10 MHz	
						Sampling Time Note 3	Conversion Time Note 4	Sampling Time Note 3	Conversion Time Note 4
0	0	0	$V_{DD} \geq$ 4.5 V	$12/f_{XP}$	$36/f_{XP}$	1.5 μs	4.5 μs	1.2 μs	3.6 μs
0	0	1	$V_{DD} \geq$ 2.85 V	$24/f_{XP}$	$48/f_{XP}$	3.0 μs	6.0 μs	Setting prohibited (2.4 μs)	Setting prohibited (4.8 μs)
0	1	0	$V_{DD} \geq$ 2.7 V	$48/f_{XP}$	$72/f_{XP}$	Setting prohibited (6.0 μs)	Setting prohibited (9.0 μs)	Setting prohibited (4.8 μs)	Setting prohibited (7.2 μs)
0	1	1	$V_{DD} \geq$ 2.7 V	$88/f_{XP}$	$112/f_{XP}$	11.0 μs	14.0 μs	Setting prohibited (8.8 μs)	Setting prohibited (11.2 μs)
1	0	0	$V_{DD} \geq$ 4.5 V	$24/f_{XP}$	$72/f_{XP}$	3.0 μs	9.0 μs	2.4 μs	7.2 μs
1	0	1	$V_{DD} \geq$ 2.85 V	$48/f_{XP}$	$96/f_{XP}$	6.0 μs	12.0 μs	4.8 μs	9.6 μs
1	1	0	$V_{DD} \geq$ 2.7 V	$96/f_{XP}$	$144/f_{XP}$	12.0 μs	18.0 μs	Setting prohibited (9.6 μs)	Setting prohibited (14.4 μs)
1	1	1	$V_{DD} \geq$ 2.7 V	$176/f_{XP}$	$224/f_{XP}$	22.0 μs	28.0 μs	17.2 μs	22.4 μs

ADCE	Comparator operation control Note 5
0 Note 1	Stops operation of comparator
1	Enables operation of comparator

Remarks 1. f_{XP}: Oscillation frequency of clock to peripheral hardware

★ **2.** The conversion time refers to the total of the sampling time and the time from successively comparing with the sampling value until the conversion result is output.

★ **Notes 1.** Even when the ADCE = 0 (comparator operation stopped), the A/D conversion operation starts if the ADCS is set to 1. However, the data of the first conversion is out of the guaranteed-value range, so ignore it.

★ **2.** Be sure to set the FR2, FR1, and FR0 in accordance with the reference voltage range and satisfy **Notes 3** and **4** below.

Example When $V_{DD} \geq$ 2.7 V

- Set FR2, FR1, and FR0 = 0, 1, 1 or 1, 1, 1.
- The sampling time is 11.0 μs or more and the A/D conversion time is 14.0 μs or more and less than 100 μs.

Notes 3. Set the sampling time as follows.

- $V_{DD} \geq 4.5$ V: 1.0 μs or more
- $V_{DD} \geq 4.0$ V: 2.4 μs or more
- $V_{DD} \geq 2.85$ V: 3.0 μs or more
- $V_{DD} \geq 2.7$ V: 11.0 μs or more

4. Set the A/D conversion time as follows.

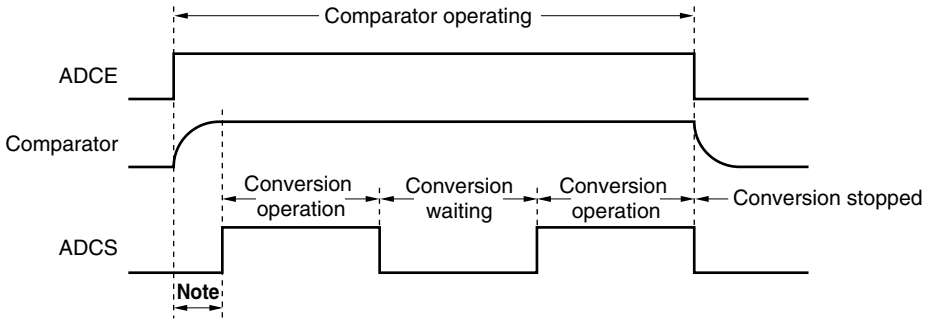
- $V_{DD} \geq 4.5$ V: 3.0 μs or more and less than 100 μs
- $V_{DD} \geq 4.0$ V: 4.8 μs or more and less than 100 μs
- $V_{DD} \geq 2.85$ V: 6.0 μs or more and less than 100 μs
- $V_{DD} \geq 2.7$ V: 14.0 μs or more and less than 100 μs

★ **5.** The operation of the comparator is controlled by ADCS and ADCE, and it takes 1 μs from operation start to operation stabilization. Therefore, when ADCS is set to 1 after 1 μs or more has elapsed from the time ADCE is set to 1, the conversion result at that time has priority over the first conversion result. If the ADCS is set to 1 without waiting for 1 μs or longer, ignore the data of the first conversion.

Table 9-3. Settings of ADCS and ADCE

ADCS	ADCE	A/D Conversion Operation
0	0	Stop status (DC power consumption path does not exist)
0	1	Conversion waiting mode (only comparator consumes power)
1	×	Conversion mode

Figure 9-4. Timing Chart When Comparator Is Used



★ **Note** The time from the rising of the ADCE bit to the rising of the ADCS bit must be 1 μs or longer to stabilize the internal circuit.

Cautions 1. The above sampling time and conversion time do not include the clock frequency error. Select the conversion time taking the clock frequency error into consideration.

2. If a bit other than ADCS of ADM is manipulated while A/D conversion is stopped (ADCS = 0) and then A/D conversion is started, execute two NOP instructions or an instruction equivalent to two machine cycles, and set ADCS to 1.

3. A/D conversion must be stopped (ADCS = 0) before rewriting bits FR0 to FR2.

4. Be sure to clear bits 6, 2, and 1 to 0.

(2) Analog input channel specification register (ADS)

This register specifies the input port of the analog voltage to be A/D converted.

ADS can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset input clears this register to 00H.

Figure 9-5. Format of Analog Input Channel Specification Register (ADS)

Address: FF81H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	0	0	0	0	0	0	ADS1	ADS0

ADS1	ADS0	Analog input channel specification
0	0	ANI0
0	1	ANI1
1	0	ANI2
1	1	ANI3

Caution Be sure to clear bits 2 to 7 of ADS to 0.

(3) 10-bit A/D conversion result register (ADCR)

This register is a 16-bit register that stores the A/D conversion result. The higher six bits are fixed to 0. Each time A/D conversion ends, the conversion result is loaded from the successive approximation register, and is stored in ADCR in order starting from bit 1 of FF19H. FF19H indicates the higher 2 bits of the conversion result, and FF18H indicates the lower 8 bits of the conversion result.

ADCR can be read by a 16-bit memory manipulation instruction.

Reset input makes ADCR undefined.

Figure 9-6. Format of 10-Bit A/D Conversion Result Register (ADCR)

Address: FF18H, FF19H After reset: Undefined R

Symbol	FF19H								FF18H							
ADCR	0	0	0	0	0	0										

Caution When writing to the A/D converter mode register (ADM) and analog input channel specification register (ADS), the contents of ADCR may become undefined. Read the conversion result following conversion completion before writing to ADM and ADS. Using timing other than the above may cause an incorrect conversion result to be read.

(4) 8-bit A/D conversion result register (ADCRH)

This register is an 8-bit register that stores the A/D conversion result. It stores the higher 8 bits of a 10-bit resolution result.

ADCRH can be read by an 8-bit memory manipulation instruction.

Reset input makes ADCRH undefined.

Figure 9-7. Format of 8-Bit A/D Conversion Result Register (ADCRH)

Address: FF1AH After reset: Undefined R

Symbol	7	6	5	4	3	2	1	0
ADCRH								

(5) Port mode register 2 (PM2) and port mode control register 2 (PMC2)

When using the when the P20/ANI0/TI000/TOH1, P21/ANI1/TI010/TO00/INTP0, P22/ANI2, and P23/ANI3 pins for analog input, set PM20 to PM23 and PMC20 to PMC23 to 1. At this time, the output latches of P20 to P23 may be 0 or 1.

PM2 and PMC2 are set by a 1-bit or 8-bit memory manipulation instruction.

Reset input sets PM2 to FFH and clears PMC2 to 00H.

Figure 9-8. Format of Port Mode Register 2 (PM2)

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	1	1	PM23	PM22	PM21	PM20

PM2n	Pmn pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 9-9. Format of Port Mode Control Register 2 (PMC2)

Address: FF84H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PMC2	0	0	0	0	PMC23	PMC22	PMC21	PMC20

PMC2n	Operation mode specification (n = 0 to 3)
0	Port/Alternate-function (except A/D converter) mode
1	A/D converter mode

Caution If PMC20 to PMC23 are set to 1, the P20/ANI0/TI000/TOH1, P21/ANI1/TIO10/TO00/INTP0, P22/ANI2, and P23/ANI3 pins cannot be used for any purpose other than the A/D converter function.

9.4 A/D Converter Operations

9.4.1 Basic operations of A/D converter

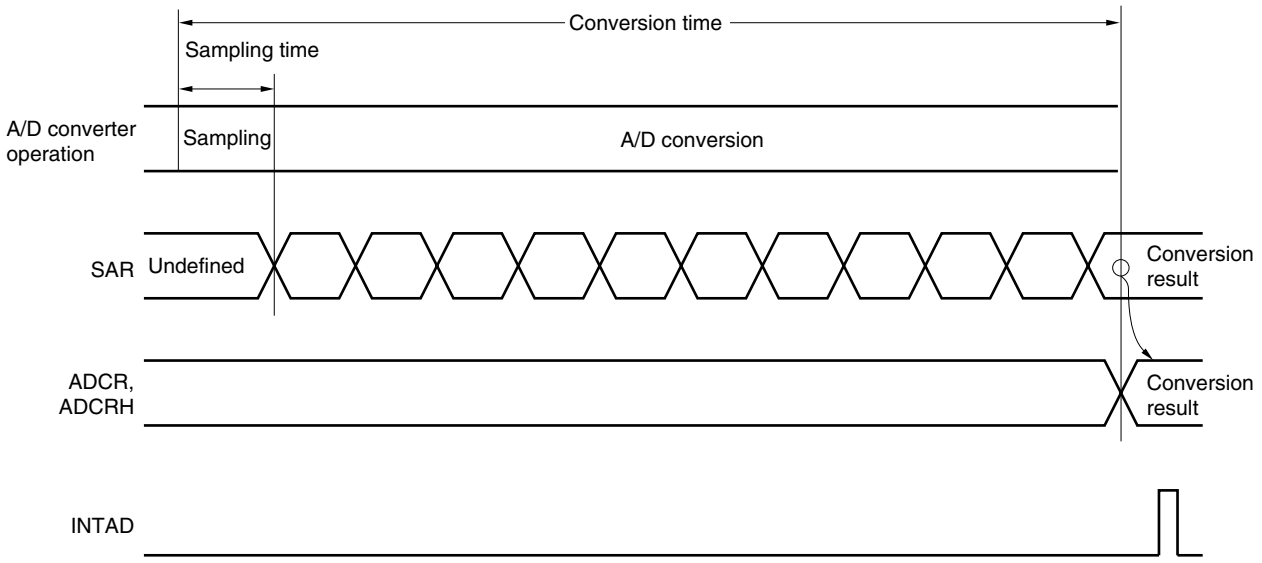
<1> Select one channel for A/D conversion using the analog input channel specification register (ADS).
<2> Set ADCE to 1 and wait for 1 μs or longer.
<3> Execute two NOP instructions or an instruction equivalent to two machine cycles.
<4> Set ADCS to 1 and start the conversion operation.
(<5> to <11> are operations performed by hardware.)
<5> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.
<6> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the input analog voltage is held until the A/D conversion operation has ended.
<7> Bit 9 of the successive approximation register (SAR) is set. The D/A converter voltage tap is set to (1/2) V_{DD} by the tap selector.
<8> The voltage difference between the D/A converter voltage tap and analog input is compared by the voltage comparator. If the analog input is greater than (1/2) AV_{DD}, the MSB of SAR remains set to 1. If the analog input is smaller than (1/2) V_{DD}, the MSB is reset to 0.
<9> Next, bit 8 of SAR is automatically set to 1, and the operation proceeds to the next comparison. The D/A converter voltage tap is selected according to the preset value of bit 9, as described below.
- Bit 9 = 1: (3/4) V_{DD}
- Bit 9 = 0: (1/4) V_{DD}

The voltage tap and analog input voltage are compared and bit 8 of SAR is manipulated as follows.
- Analog input voltage ≥ Voltage tap: Bit 8 = 1
- Analog input voltage < Voltage tap: Bit 8 = 0

<10> Comparison is continued in this way up to bit 0 of SAR.
<11> Upon completion of the comparison of 10 bits, an effective digital result value remains in SAR, and the result value is transferred to the A/D conversion result register (ADCR, ADCRH) and then latched.
At the same time, the A/D conversion end interrupt request (INTAD) can also be generated.
<12> Repeat steps <5> to <11>, until ADCS is cleared to 0.
To stop the A/D converter, clear ADCS to 0.
To restart A/D conversion from the status of ADCE = 1, start from <3>. To restart A/D conversion from the status of ADCE = 0, start from <2>.

Remark The following two types of A/D conversion result registers can be used.
<1> ADCR (16 bits): Stores a 10-bit A/D conversion value.
<2> ADCRH (8 bits): Stores an 8-bit A/D conversion value.

Figure 9-10. Basic Operation of A/D Converter



A/D conversion operations are performed continuously until bit 7 (ADCS) of the A/D converter mode register (ADM) is reset (0) by software.

If a write operation is performed to ADM or the analog input channel specification register (ADS) during an A/D conversion operation, the conversion operation is initialized, and if the ADCS bit is set (1), conversion starts again from the beginning.

Reset input makes the A/D conversion result register (ADCR, ADCRH) undefined.

9.4.2 Input voltage and conversion results

The relationship between the analog input voltage input to the analog input pins (ANI0 to ANI3) and the theoretical A/D conversion result (stored in the 10-bit A/D conversion result register (ADCR)) is shown by the following expression.

$$SAR = INT\left(\frac{V_{AIN}}{V_{DD}} \times 1024 + 0.5\right)$$

$$ADCR = SAR \times 64$$

or

$$(ADCR - 0.5) \times \frac{V_{DD}}{1024} \leq V_{AIN} < (ADCR + 0.5) \times \frac{V_{DD}}{1024}$$

where, INT( ): Function which returns integer part of value in parentheses

V_{AIN}: Analog input voltage

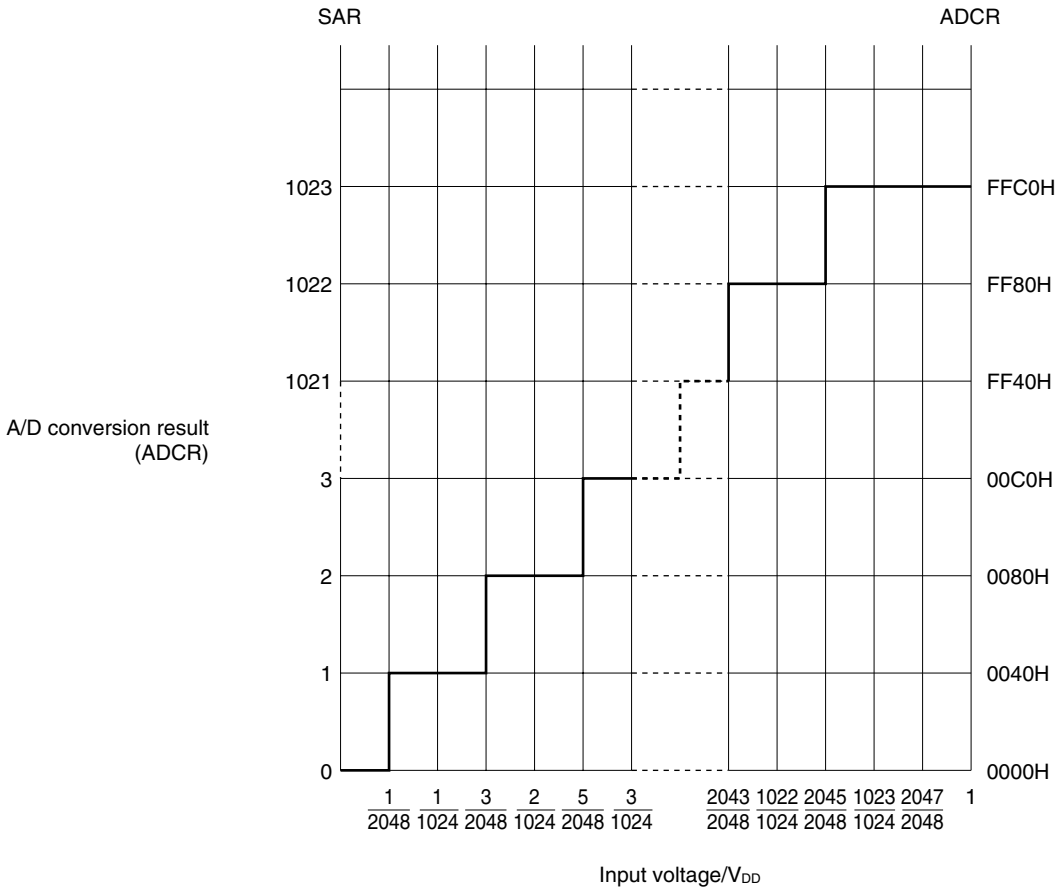
V_{DD}: V_{DD} pin voltage

ADCR: 10-bit A/D conversion result register (ADCR) value

SAR: Successive approximation register

Figure 9-11 shows the relationship between the analog input voltage and the A/D conversion result.

★ **Figure 9-11. Relationship Between Analog Input Voltage and A/D Conversion Result**



9.4.3 A/D converter operation mode

The operation mode of the A/D converter is the select mode. One channel of analog input is selected from ANI0 to ANI3 by the analog input channel specification register (ADS) and A/D conversion is executed.

(1) A/D conversion operation

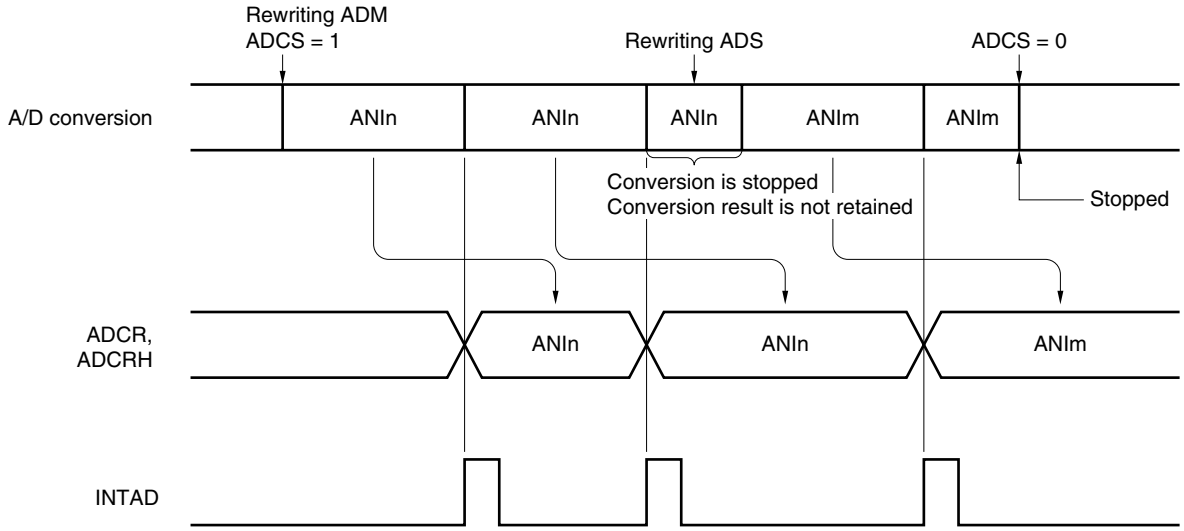
By setting bit 7 (ADCS) of the A/D converter mode register (ADM) to 1, the A/D conversion operation of the voltage, which is applied to the analog input pin specified by the analog input channel specification register (ADS), is started.

When A/D conversion has been completed, the result of the A/D conversion is stored in the A/D conversion result register (ADCR, ADCRH), and an interrupt request signal (INTAD) is generated. Once the A/D conversion has started and when one A/D conversion has been completed, the next A/D conversion operation is immediately started. The A/D conversion operations are repeated until new data is written to ADS.

If ADM or ADS is written during A/D conversion, the A/D conversion operation under execution is stopped and restarted from the beginning.

If 0 is written to ADCS during A/D conversion, A/D conversion is immediately stopped. At this time, the conversion result is undefined.

Figure 9-12. A/D Conversion Operation



Remarks 1. n = 0 to 3

2. m = 0 to 3

The setting method is described below.

<1> Set bit 0 (ADCE) of the A/D converter mode register (ADM) to 1.
<2> Select the channel and conversion time using bits 1 and 0 (ADS1, ADS0) of the analog input channel specification register (ADS) and bits 5 to 3 (FR2 to FR0) of ADM.
<3> Execute two NOP instructions or an instruction equivalent to two machine cycles.
<4> Set bit 7 (ADCS) of ADM to 1 to start A/D conversion.
<5> An interrupt request signal (INTAD) is generated.
<6> Transfer the A/D conversion data to the A/D conversion result register (ADCR, ADCRH).

<Change the channel>

<7> Change the channel using bits 1 and 0 (ADS1, ADS0) of ADS to start A/D conversion.
<8> An interrupt request signal (INTAD) is generated.
<9> Transfer the A/D conversion data to the A/D conversion result register (ADCR, ADCRH).

<Complete A/D conversion>

<10> Clear ADCS to 0.
<11> Clear ADCE to 0.

Cautions 1. Make sure the period of <1> to <4> is 1 μs or more.
2. It is no problem if the order of <1> and <2> is reversed.
3. <1> can be omitted. However, ignore the data resulting from the first conversion after <4> in this case.
4. The period from <5> to <8> differs from the conversion time set using bits 5 to 3 (FR2 to FR0) of ADM. The period from <7> to <8> is the conversion time set using FR2 to FR0.

9.5 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 10 bits.

$1LSB = 1/2^{10} = 1/1024$
$= 0.098\%FSR$

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.
Zero-scale error, full-scale error, integral linearity error, and differential linearity errors that are combinations of these express the overall error.
Note that the quantization error is not included in the overall error in the characteristics table.

(3) Quantization error

When analog values are converted to digital values, a ±1/2LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of ±1/2LSB is converted to the same digital code, so a quantization error cannot be avoided.
Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

Figure 9-13. Overall Error

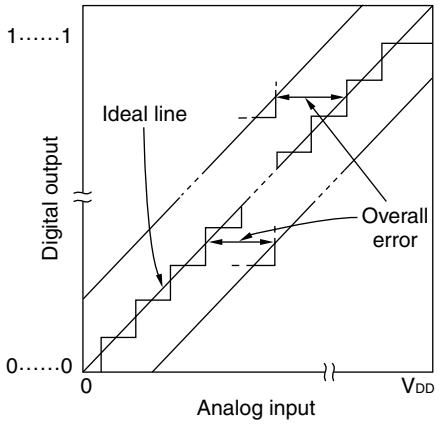
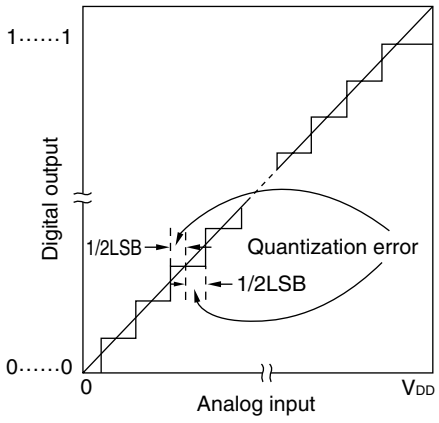


Figure 9-14. Quantization Error



(4) Zero-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (1/2LSB) when the digital output changes from 0.....000 to 0.....001.
If the actual measurement value is greater than the theoretical value, it shows the difference between the actual measurement value of the analog input voltage and the theoretical value (3/2LSB) when the digital output changes from 0……001 to 0……010.

(5) Full-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (Full-scale – 3/2LSB) when the digital output changes from 1.....110 to 1.....111.

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

(7) Differential linearity error

While the ideal width of code output is 1LSB, this indicates the difference between the actual measurement value and the ideal value.

Figure 9-15. Zero-Scale Error

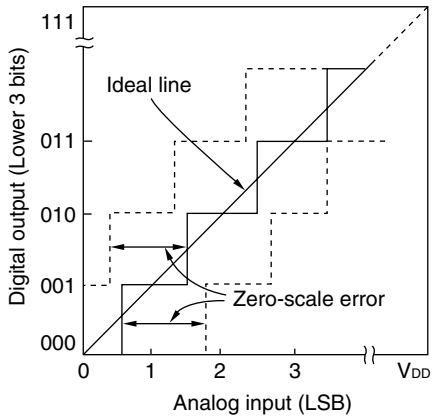


Figure 9-16. Full-Scale Error

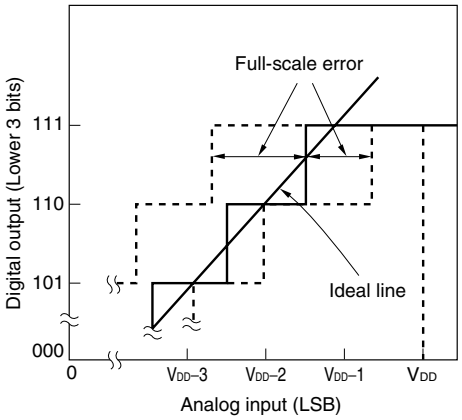


Figure 9-17. Integral Linearity Error

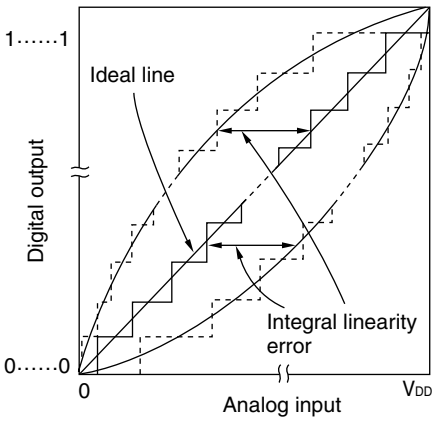
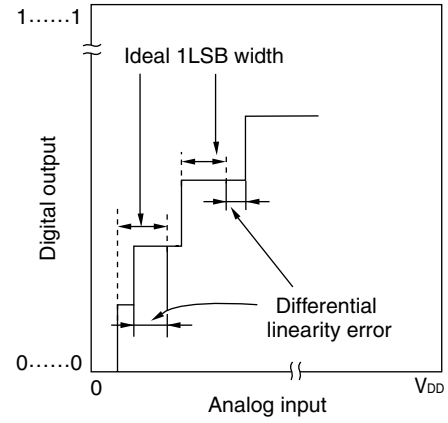


Figure 9-18. Differential Linearity Error



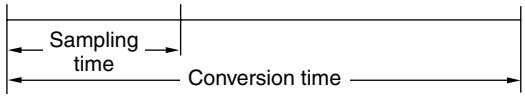
(8) Conversion time

This expresses the time from the start of sampling to when the digital output is obtained.

The sampling time is included in the conversion time in the characteristics table.

(9) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.



9.6 Cautions for A/D Converter

★ **(1) Operating current in STOP mode**

The A/D converter stops operating in the STOP mode. At this time, the operating current can be reduced by clearing bit 7 (ADCS) of the A/D converter mode register (ADM) to 0.

(2) Input range of ANI0 to ANI3

Observe the rated range of the ANI0 to ANI3 input voltage. If a voltage of V_{DD} or higher and V_{SS} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

(3) Conflicting operations

<1> Conflict between A/D conversion result register (ADCR, ADCRH) write and ADCR, ADCRH read by instruction upon the end of conversion

ADCR, ADCRH read has priority. After the read operation, the new conversion result is written to ADCR, ADCRH.

<2> Conflict between ADCR, ADCRH write and A/D converter mode register (ADM) write or analog input channel specification register (ADS) write upon the end of conversion

ADM or ADS write has priority. ADCR, ADCRH write is not performed, nor is the conversion end interrupt signal (INTAD) generated.

★ **(4) Noise countermeasures**

To maintain the 10-bit resolution, attention must be paid to noise input to the V_{DD} pin and ANI0 to ANI3 pins.

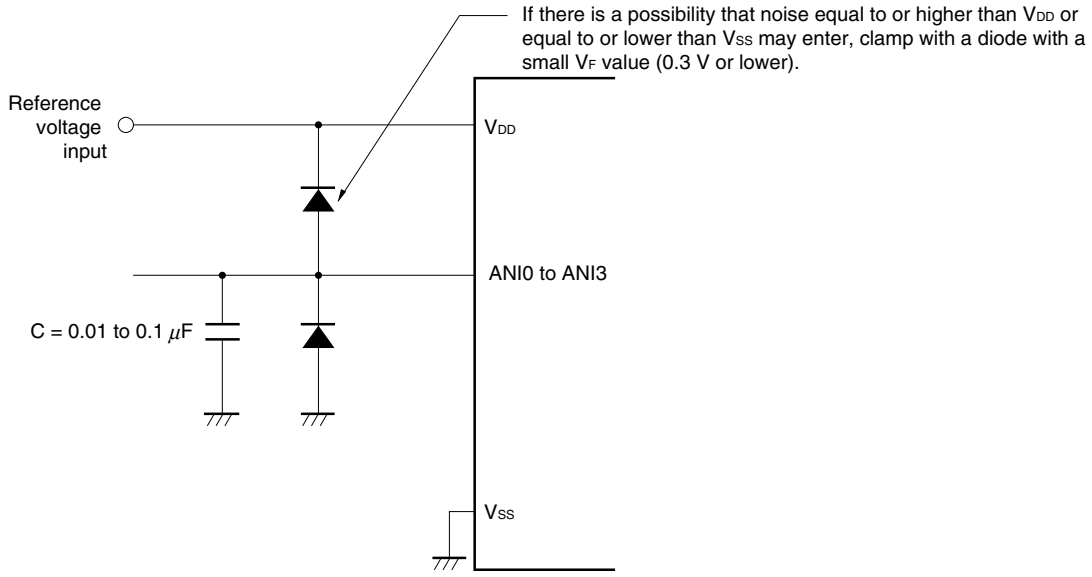
<1> Connect a capacitor with a low equivalent resistance and a high frequency response to the power supply.

<2> Because the effect increases in proportion to the output impedance of the analog input source, it is recommended that a capacitor be connected externally, as shown in Figure 9-19, to reduce noise.

<3> Do not switch the A/D conversion function of the ANI0 to ANI3 pins to their alternate functions during conversion.

<4> The conversion accuracy can be improved by setting HALT mode immediately after the conversion starts.

Figure 9-19. Analog Input Pin Connection



(5) ANI0/P20 to ANI3/P23

<1> The analog input pins (ANI0 to ANI3) are also used as input port pins (P20 to P23).
When A/D conversion is performed with any of ANI0 to ANI3 selected, do not access port 2 while conversion is in progress; otherwise the conversion resolution may be degraded.

<2> If a digital pulse is applied to the pins adjacent to the pins currently used for A/D conversion, the expected value of the A/D conversion may not be obtained due to coupling noise. Therefore, do not apply a pulse to the pins adjacent to the pin undergoing A/D conversion.

(6) Input impedance of ANI0 to ANI3 pins

In this A/D converter, the internal sampling capacitor is charged and sampling is performed for approx. one sixth of the conversion time.

Since only the leakage current flows other than during sampling and the current for charging the capacitor also flows during sampling, the input impedance fluctuates and has no meaning.

★ If the shortest conversion time of the reference voltage is used, to perform sufficient sampling, it is recommended to make the output impedance of the analog input source 1 kΩ or lower, or attach a capacitor of around 0.01 μF to 0.1 μF to the ANI0 to ANI3 pins (see **Figure 9-19**).

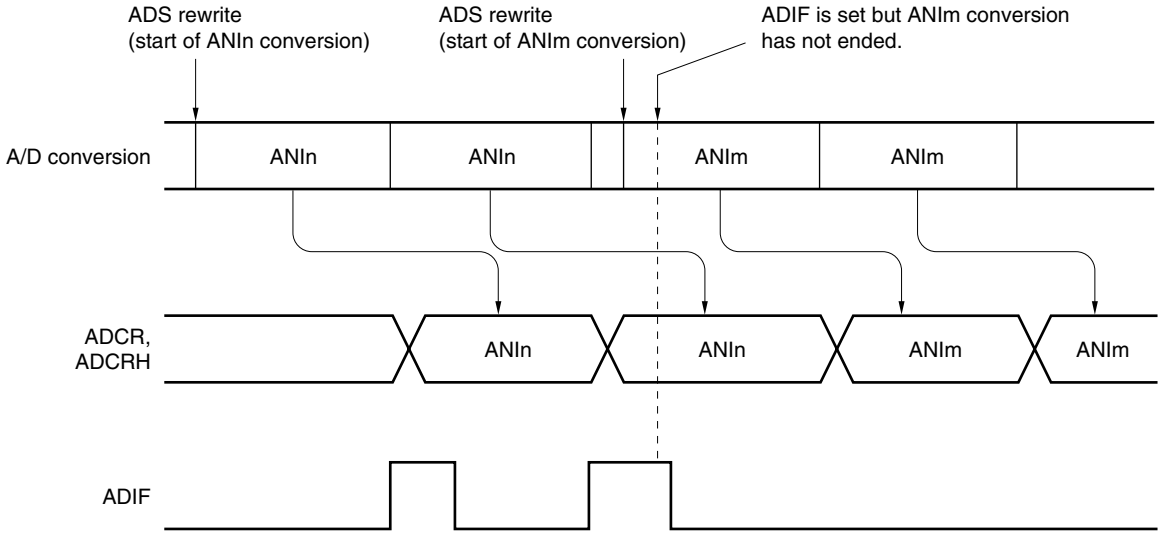
(7) Interrupt request flag (ADIF)

The interrupt request flag (ADIF) is not cleared even if the analog input channel specification register (ADS) is changed.

Therefore, if an analog input pin is changed during A/D conversion, the A/D conversion result and ADIF for the pre-change analog input may be set just before the ADS rewrite. Caution is therefore required since, at this time, when ADIF is read immediately after the ADS rewrite, ADIF is set despite the fact A/D conversion for the post-change analog input has not ended.

When A/D conversion is stopped and then resumed, clear ADIF before the A/D conversion operation is resumed.

Figure 9-20. Timing of A/D Conversion End Interrupt Request Generation



Remarks 1. n = 0 to 3

2. m = 0 to 3

(8) Conversion results just after A/D conversion start

The first A/D conversion value immediately after A/D conversion starts may not fall within the rating range if the ADCS bit is set to 1 within 1 μs after the ADCE bit was set to 1, or if the ADCS bit is set to 1 with the ADCE bit = 0. Take measures such as polling the A/D conversion end interrupt request (INTAD) and removing the first conversion result.

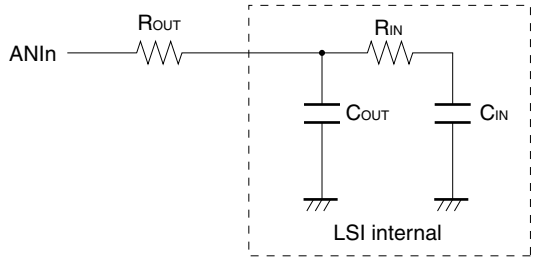
(9) A/D conversion result register (ADCR, ADCRH) read operation

When a write operation is performed to the A/D converter mode register (ADM) and analog input channel specification register (ADS), the contents of ADCR and ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM and ADS. Using a timing other than the above may cause an incorrect conversion result to be read.

(10) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

★ **Figure 9-21. Internal Equivalent Circuit of ANIn Pin**



★ **Table 9-4. Resistance and Capacitance Values (Reference Values) of Equivalent Circuit**

V_{DD}	R_{OUT}	R_{IN}	C_{OUT}	C_{IN}
4.5 V ≤ V_{DD} ≤ 5.5 V	1 kΩ	3 kΩ	8 pF	15 pF
2.7 V ≤ V_{DD} < 4.5 V	1 kΩ	60 kΩ	8 pF	15 pF

Remarks 1. The resistance and capacitance values shown in Table 9-4 are not guaranteed values.

2. n = 0 to 3

3. R_{OUT}: Allowable signal source impedance
R_{IN}: Analog input equivalent resistance
C_{OUT}: Internal pin capacitance
C_{IN}: Analog Input equivalent capacitance

CHAPTER 10 INTERRUPT FUNCTIONS

10.1 Interrupt Function Types

All interrupts are controlled as maskable interrupts.

- **Maskable interrupts**
  These interrupts undergo mask control. If two or more interrupt requests are simultaneously generated, each interrupt has a predetermined priority as shown in Table 10-1.
  A standby release signal is generated.
  There are five internal sources and two external sources of maskable interrupts.

10.2 Interrupt Sources and Configuration

There are a total of seven interrupt sources, and up to four reset sources (see **Table 10-1**).

Table 10-1. Interrupt Sources

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	1	INTLVI	Low-voltage detection[Note 3]	Internal	0006H	(A)
	2	INTP0	Pin input edge detection	External	0008H	(B)
	3	INTP1			000AH	
	4	INTTMH1	Match between TMH1 and CMP01 (when compare register is specified)	Internal	000CH	(A)
	5	INTTM000	Match between TM00 and CR000 (when compare register is specified), TI010 pin valid edge detection (when capture register is specified)		000EH	
	6	INTTM010	Match between TM00 and CR010 (when compare register is specified), TI000 pin valid edge detection (when capture register is specified)		0010H	
	7	INTAD	End of A/D conversion		0012H	
Reset	–	RESET	Reset input	–	0000H	–
		POC	Power-on-clear			
		LVI	Low-voltage detection[Note 4]			
		WDT	WDT overflow			

Notes 1. Priority is the priority order when several maskable interrupt requests are generated at the same time. 1 is the highest and 7 is the lowest.

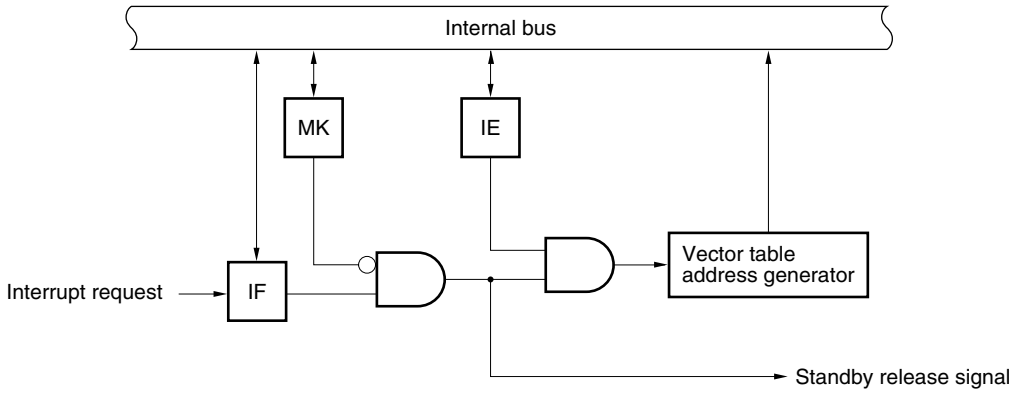
2. Basic configuration types (A) and (B) correspond to (A) and (B) in Figure 10-1.

3. When bit 1 (LVIMD) of low-voltage detection register (LVIM) = 0 is selected.

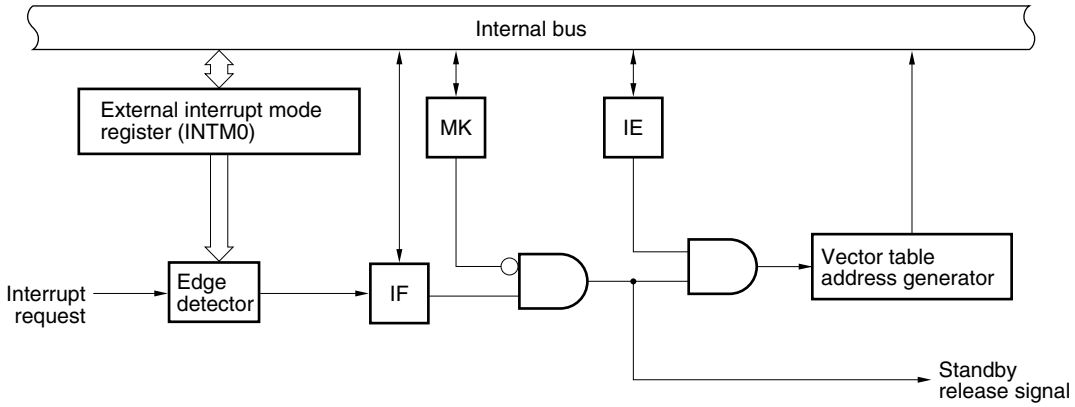
4. When bit 1 (LVIMD) of low-voltage detection register (LVIM) = 1 is selected.

Figure 10-1. Basic Configuration of Interrupt Function

(A) Internal maskable interrupt



(B) External maskable interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

10.3 Interrupt Function Control Registers

The interrupt functions are controlled by the following four types of registers.

- Interrupt request flag register 0 (IF0)
- Interrupt mask flag register 0 (MK0)
- External interrupt mode register 0 (INTM0)
- Program status word (PSW)

Table 10-2 lists interrupt requests, the corresponding interrupt request flags, and interrupt mask flags.

Table 10-2. Interrupt Request Signals and Corresponding Flags

Interrupt Request Signal	Interrupt Request Flag	Interrupt Mask Flag
INTLVI	LVIIF	LVIMK
INTP0	PIF0	PMK0
INTP1	PIF1	PMK1
INTTMH1	TMIFH1	TMMKH1
INTTM000	TMIF000	TMMK000
INTTM010	TMIF010	TMMK010
INTAD	ADIF	ADMK

(1) Interrupt request flag register 0 (IF0)

An interrupt request flag is set to 1 when the corresponding interrupt request is issued, or when the instruction is executed. It is cleared to 0 by executing an instruction when the interrupt request is acknowledged or when a reset signal is input.

IF0 is set with a 1-bit or 8-bit memory manipulation instruction.

Reset input clears IF0 to 00H.

Figure 10-2. Format of Interrupt Request Flag Register 0 (IF0)

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	0
IF0	ADIF	TMIF010	TMIF000	TMIFH1	PIF1	PIF0	LVIIF	0

××IF×	Interrupt request flag
0	No interrupt request signal has been issued.
1	An interrupt request signal has been issued; an interrupt request status.

Caution Because P21 and P32 have an alternate function as external interrupt inputs, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, the interrupt mask flag should be set to 1 before using the output mode.

(2) Interrupt mask flag register 0 (MK0)

The interrupt mask flag is used to enable and disable the corresponding maskable interrupts.

MK0 is set with a 1-bit or 8-bit memory manipulation instruction.

Reset input sets MK0 to FFH.

Figure 10-3. Format of Interrupt Mask Flag Register 0 (MK0)

Address: FFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	0
MK0	ADMK	TMMK010	TMMK000	TMMKH1	PMK1	PMK0	LVIMK	1

××MK×	Interrupt servicing control
0	Enables interrupt servicing.
1	Disables interrupt servicing.

Caution Because P21 and P32 have an alternate function as external interrupt inputs, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, the interrupt mask flag should be set to 1 before using the output mode.

(3) External interrupt mode register 0 (INTM0)

This register is used to set the valid edge of INTP0 and INTP1.

INTM0 is set with an 8-bit memory manipulation instruction.

Reset input clears INTM0 to 00H.

Figure 10-4. Format of External Interrupt Mode Register 0 (INTM0)

Address: FFECH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
INTM0	0	0	ES11	ES10	ES01	ES00	0	0

ES11	ES10	INTP1 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES01	ES00	INTP0 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Cautions 1. Be sure to clear bits 0, 1, 6, and 7 to 0.

Cautions 2. Before setting the INTM0 register, be sure to set the corresponding interrupt mask flag (××MK× = 1) to disable interrupts. After setting the INTM0 register, clear the interrupt request flag (××IF× = 0), then clear the interrupt mask flag (××MK× = 0), which will enable interrupts.

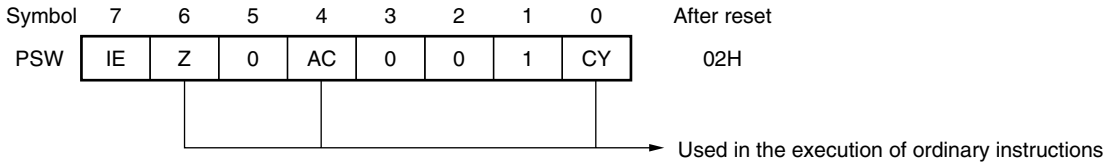
(4) Program status word (PSW)

The program status word is used to hold the instruction execution result and the current status of the interrupt requests. The IE flag, used to enable and disable maskable interrupts, is mapped to PSW.

PSW can be read- and write-accessed in 8-bit units, as well as using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt is acknowledged, the PSW is automatically saved to a stack, and the IE flag is reset to 0.

Reset input sets PSW to 02H.

Figure 10-5. Program Status Word (PSW) Configuration



IE	Whether to enable/disable interrupt acknowledgment
0	Disabled
1	Enabled

10.4 Interrupt Servicing Operation

10.4.1 Maskable interrupt request acknowledgment operation

A maskable interrupt request can be acknowledged when the interrupt request flag is set to 1 and the corresponding interrupt mask flag is cleared to 0. A vectored interrupt request is acknowledged in the interrupt enabled status (when the IE flag is set to 1).

The time required to start the interrupt servicing after a maskable interrupt request has been generated is shown in Table 10-3.

See Figures 10-7 and 10-8 for the interrupt request acknowledgment timing.

Table 10-3. Time from Generation of Maskable Interrupt Request to Servicing

Minimum Time	Maximum Time[Note]
9 clocks	19 clocks

Note The wait time is maximum when an interrupt request is generated immediately before BT and BF instructions.

Remark 1 clock: $\frac{1}{f_{CPU}}$ (f_{CPU}: CPU clock)

When two or more maskable interrupt requests are generated at the same time, they are acknowledged starting from the interrupt request assigned the highest priority.

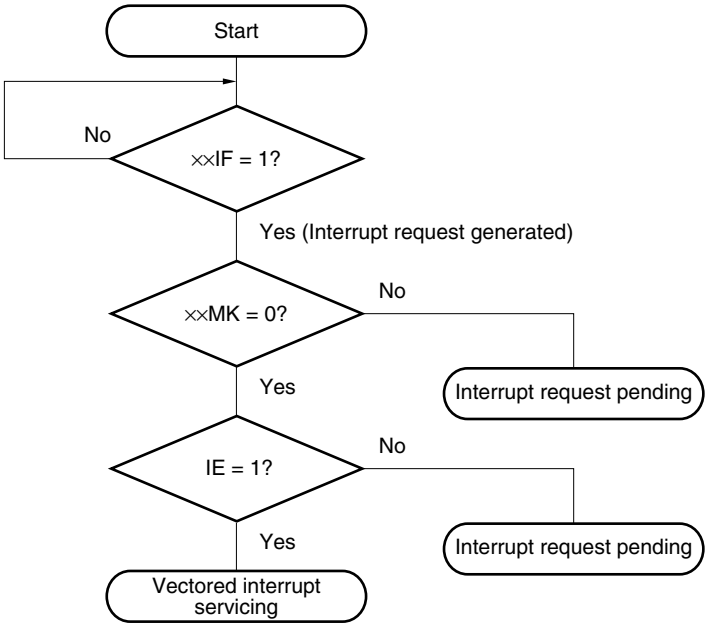
A pending interrupt is acknowledged when a status in which it can be acknowledged is set.

Figure 10-6 shows the algorithm of interrupt request acknowledgment.

When a maskable interrupt request is acknowledged, the contents of the PSW and PC are saved to the stack in that order, the IE flag is reset to 0, and the data in the vector table determined for each interrupt request is loaded to the PC, and execution branches.

To return from interrupt servicing, use the RETI instruction.

Figure 10-6. Interrupt Request Acknowledgment Processing Algorithm

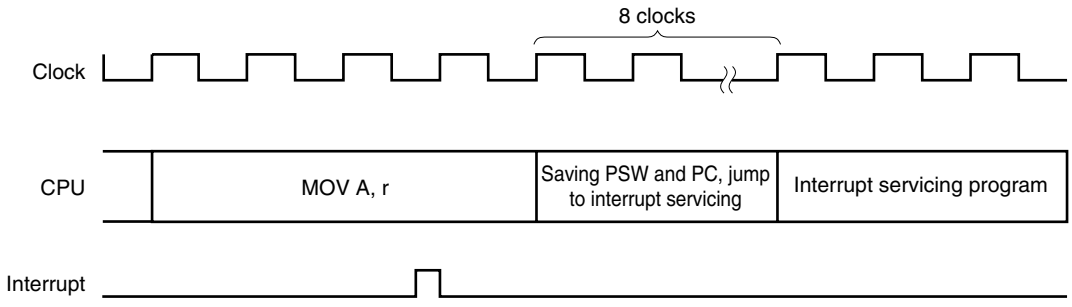


××IF: Interrupt request flag

××MK: Interrupt mask flag

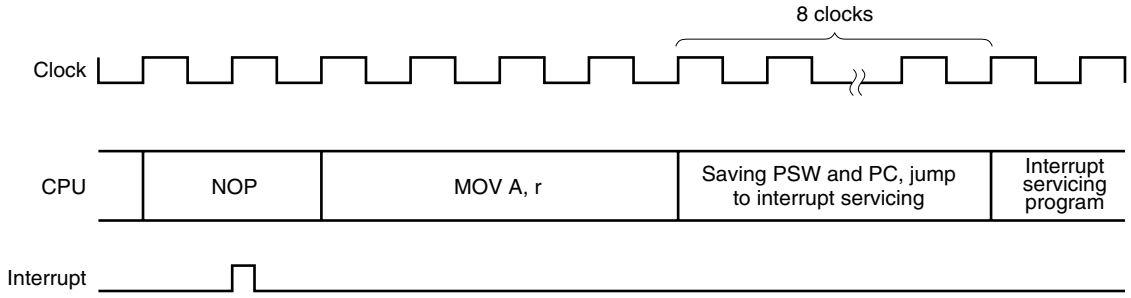
IE: Flag to control maskable interrupt request acknowledgment (1 = enable, 0 = disable)

Figure 10-7. Interrupt Request Acknowledgment Timing (Example of MOV A, r)



If an interrupt request flag (××IF) is set before an instruction clock n (n = 4 to 10) under execution becomes n – 1, the interrupt is acknowledged after the instruction under execution is complete. Figure 10-7 shows an example of the interrupt request acknowledgment timing for an 8-bit data transfer instruction MOV A, r. Since this instruction is executed for 4 clocks, if an interrupt occurs for 3 clocks after the execution starts, the interrupt acknowledgment processing is performed after the MOV A, r instruction is executed.

Figure 10-8. Interrupt Request Acknowledgment Timing (When Interrupt Request Flag Is Set at Last Clock During Instruction Execution)



If an interrupt request flag (××IF) is set at the last clock of the instruction, the interrupt acknowledgment processing starts after the next instruction is executed.

Figure 10-8 shows an example of the interrupt request acknowledgment timing for an interrupt request flag that is set at the second clock of NOP (2-clock instruction). In this case, the MOV A, r instruction after the NOP instruction is executed, and then the interrupt acknowledgment processing is performed.

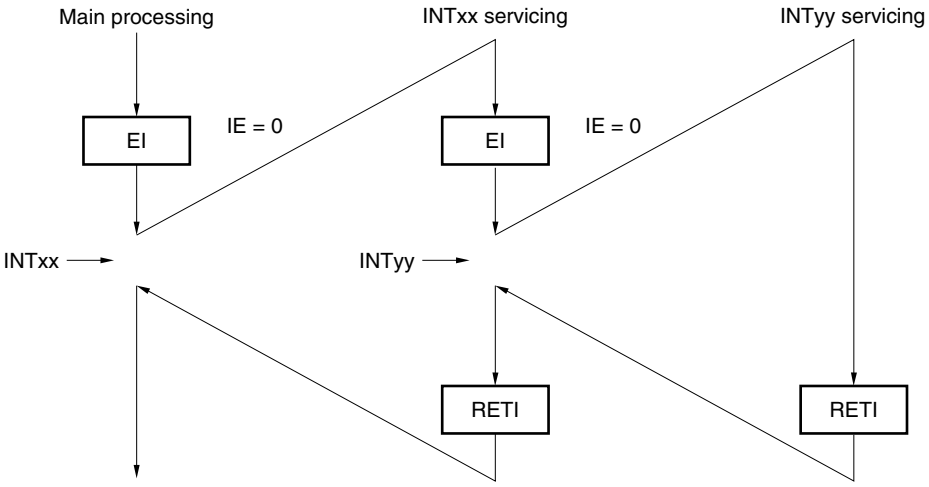
Caution Interrupt requests will be held pending while the interrupt request flag register 0 (IF0) or interrupt mask flag register 0 (MK0) are being accessed.

10.4.2 Multiple interrupt servicing

Multiple interrupt servicing in which another interrupt is acknowledged while an interrupt is being serviced can be performed using a priority order system. When two or more interrupts are generated at once, interrupt servicing is performed according to the priority assigned to each interrupt request in advance (see **Table 10-1**).

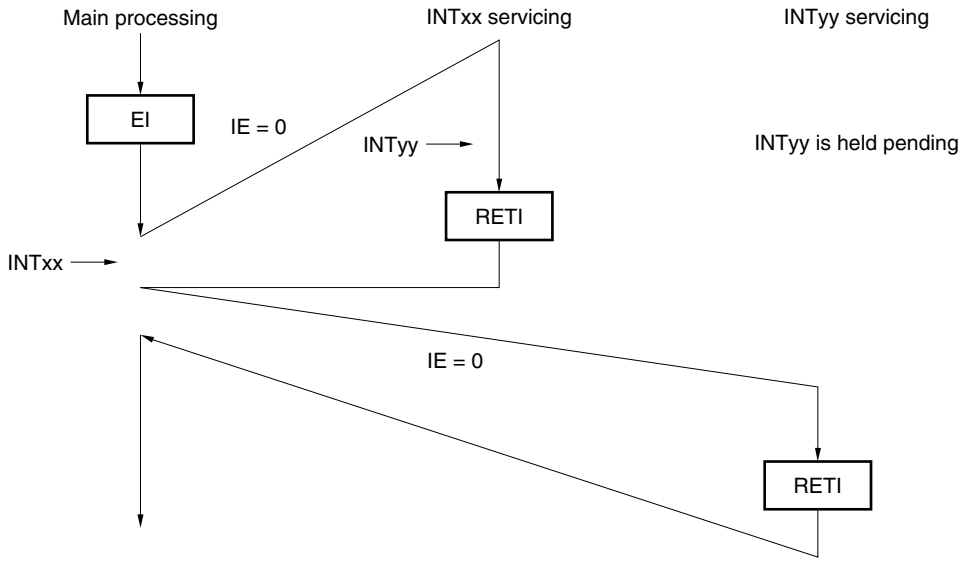
Figure 10-9. Example of Multiple Interrupts

Example 1. Multiple interrupts are acknowledged



During interrupt INTxx servicing, interrupt request INTyy is acknowledged, and multiple interrupts are generated. The EI instruction is issued before each interrupt request acknowledgment, and the interrupt request acknowledgment enable state is set.

Example 2. Multiple interrupts are not generated because interrupts are not enabled



Because interrupts are not enabled in interrupt INTxx servicing (the EI instruction is not issued), interrupt request INTyy is not acknowledged, and multiple interrupts are not generated. The INTyy request is held pending and acknowledged after the INTxx servicing is performed.

IE = 0: Interrupt request acknowledgment disabled

10.4.3 Interrupt request pending

Some instructions may keep pending the acknowledgment of an instruction request until the completion of the execution of the next instruction even if the interrupt request (maskable interrupt and external interrupt) is generated during the execution. The following shows such instructions (interrupt request pending instruction).

- Manipulation instruction for interrupt request flag register 0 (IF0)
- Manipulation instruction for interrupt mask flag register 0 (MK0)

CHAPTER 11 STANDBY FUNCTION

11.1 Standby Function and Configuration

11.1.1 Standby function

Table 11-1. Relationship Between Operation Clocks in Each Operation Status

Status / Operation Mode	Low-Speed Ring-OSC Oscillator			System Clock	Clock Supplied to Peripheral Hardware
	Note 1	**Note 2**			
		LSRSTOP = 0	LSRSTOP = 1		
Reset	Stopped			Stopped	Stopped
STOP	Oscillating	Oscillating[Note 3]	Stopped		
HALT				Oscillating	Oscillating

Notes 1. When “Cannot be stopped” is selected for low-speed Ring-OSC by the option byte.

2. When it is selected that the low-speed Ring-OSC oscillator “can be stopped by software”, oscillation of the low-speed Ring-OSC oscillator can be stopped by LSRSTOP.

3. If the operating clock of the watchdog timer is the low-speed Ring-OSC clock, the watchdog timer is stopped.

Caution The LSRSTOP setting is valid only when “Can be stopped by software” is set for the low-speed Ring-OSC oscillator by the option byte.

Remark LSRSTOP: Bit 0 of the low-speed Ring-OSC mode register (LSRCM)

The standby function is designed to reduce the operating current of the system. The following two modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. Oscillation of the system clock oscillator continues. If the low-speed Ring-OSC oscillator is operating before the HALT mode is set, oscillation of the clock of the low-speed Ring-OSC oscillator continues (refer to **Table 11-1**. Oscillation of the low-speed Ring-OSC clock (whether it cannot be stopped or can be stopped by software) is set by the option byte). In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the system clock oscillator stops, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out.

★ However, select the HALT mode if processing must be immediately started by an interrupt request when the operation stop time[Note] is generated after the STOP mode is released (because an additional wait time for stabilizing oscillation elapses when crystal/ceramic oscillation is used).

★ **Note** The operation stop time is 17 μs (MIN.), 34 μs (TYP.), and 67 μs (MAX.).

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

Cautions 1. When shifting to the STOP mode, be sure to stop the peripheral hardware operation before executing STOP instruction (except the peripheral hardware that operates on the low-speed Ring-OSC clock).

2. The following sequence is recommended for operating current reduction of the A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0 to stop the A/D conversion operation, and then execute the HALT or STOP instruction.

3. If the low-speed Ring-OSC oscillator is operating before the STOP mode is set, oscillation of the low-speed Ring-OSC clock cannot be stopped in the STOP mode (refer to Table 11-1).

11.1.2 Registers used during standby

The oscillation stabilization time after the standby mode is released is controlled by the oscillation stabilization time select register (OSTS).

Remark For the registers that start, stop, or select the clock, see **CHAPTER 5 CLOCK GENERATORS**.

(1) Oscillation stabilization time select register (OSTS)

This register is used to select oscillation stabilization time of the clock supplied from the oscillator when the STOP mode is released. The wait time set by OSTS is valid only when the crystal/ceramic oscillation clock is selected as the system clock and after the STOP mode is released. If the high-speed Ring-OSC oscillator or external clock input is selected as the system clock source, no wait time elapses.

The system clock oscillator and the oscillation stabilization time that elapses after power application or release of reset are selected by the option byte. For details, refer to **CHAPTER 15 OPTION BYTE**.

OSTS is set by using the 8-bit memory manipulation instruction.

Figure 11-1. Format of Oscillation Stabilization Time Select Register (OSTS)

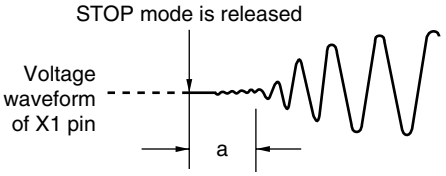
Address: FFF4H, After reset: Undefined, R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	0	OSTS1	OSTS0

OSTS1	OSTS0	Selection of oscillation stabilization time
0	0	2^{10}/fx (102.4 μs)
0	1	2^{12}/fx (409.6 μs)
1	0	2^{15}/fx (3.27 ms)
1	1	2^{17}/fx (13.1 ms)

Cautions 1. To set and then release the STOP mode, set the oscillation stabilization time as follows. Expected oscillation stabilization time of resonator ≤ Oscillation stabilization time set by OSTS

2. The wait time after the STOP mode is released does not include the time from the release of the STOP mode to the start of clock oscillation ("a" in the figure below), regardless of whether STOP mode was released by reset input or interrupt generation.



3. The oscillation stabilization time that elapses on power application or after release of reset is selected by the option byte. For details, refer to CHAPTER 15 OPTION BYTE.

Remarks 1. ( ): fx = 10 MHz

2. Determine the oscillation stabilization time of the resonator by checking the characteristics of the resonator to be used.

11.2 Standby Function Operation

11.2.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction.

The operating statuses in the HALT mode are shown below.

Caution Because an interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set.

Table 11-2. Operating Statuses in HALT Mode

Setting of HALT Mode / Item		Low-speed Ring-OSC cannot be stopped[Note].	Low-speed Ring-OSC can be stopped[Note].	
			When Low-speed Ring-OSC Oscillation Continues	When Low-speed Ring-OSC Oscillation Stops
System clock		Clock supply to CPU is stopped.		
CPU		Operation stops.		
Port (latch)		Holds status before HALT mode was set.		
16-bit timer/event counter 00		Operable		
8-bit timer H1	Sets count clock to f_{XP} to $f_{XP}/2^{12}$	Operable		
	Sets count clock to $f_{RL}/2^{7}$	Operable	Operable	Operation stops.
Watchdog timer	"System clock" selected as operating clock	Setting disabled.	Operation stops.	
	"Low-speed Ring-OSC clock" selected as operating clock	Operable (Operation continues)	Operation stops.	
A/D converter		Operable		
Power-on-clear circuit		Always operates.		
Low-voltage detector		Operable		
External interrupt		Operable		

Note "Low-speed Ring-OSC cannot be stopped" or "low-speed Ring-OSC can be stopped by software" can be selected by the option byte (for the option byte, see **CHAPTER 15 OPTION BYTE**).

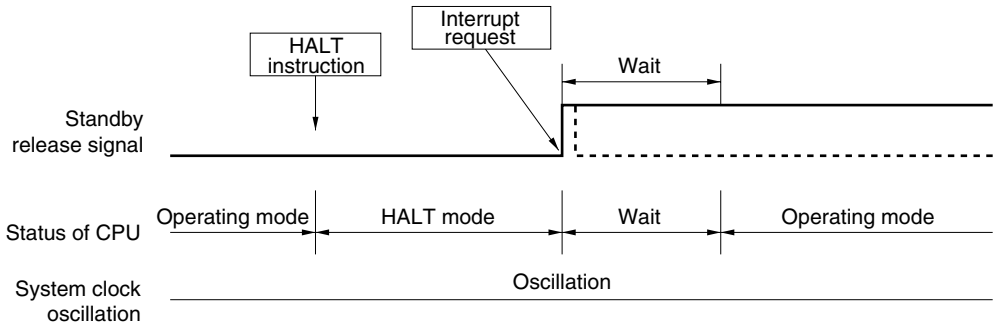
(2) HALT mode release

The HALT mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgement is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgement is disabled, the next address instruction is executed.

Figure 11-2. HALT Mode Release by Interrupt Request Generation



Remarks 1. The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

2. The wait time is as follows:

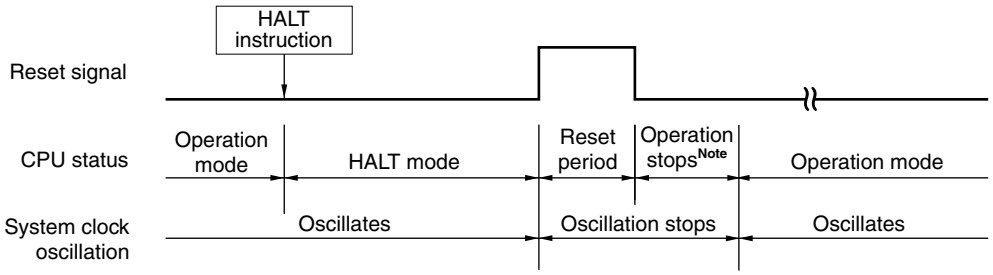
- When vectored interrupt servicing is carried out: 11 to 13 clocks
- When vectored interrupt servicing is not carried out: 3 to 5 clocks

(b) Release by reset input

When the reset signal is input, HALT mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

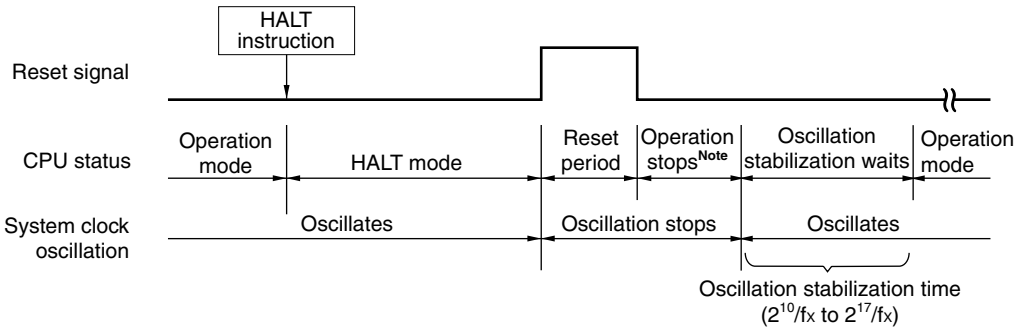
Figure 11-3. HALT Mode Release by Reset Input

(1) When CPU clock is high-speed Ring-OSC clock or external input clock



★ **Note** Operation is stopped (277 μs (MIN.), 544 μs (TYP.), and 1.075 ms (MAX.)) because the option byte is referenced.

(2) When CPU clock is crystal/ceramic oscillation clock



★ **Note** Operation is stopped (276 μs (MIN.), 544 μs (TYP.), and 1.074 ms (MAX.)) because the option byte is referenced.

Remark fx: System clock oscillation frequency

Table 11-3. Operation in Response to Interrupt Request in HALT Mode

Release Source	MK××	IE	Operation
Maskable interrupt request	0	0	Next address instruction execution
	0	1	Interrupt servicing execution
	1	×	HALT mode held
Reset input	–	×	Reset processing

×: don't care

11.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction.

Caution Because an interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, in the STOP mode, the normal operation mode is restored after the STOP instruction is executed and then the operation is stopped for the duration of 34 μs (TYP.) (after an additional wait time for stabilizing oscillation set by the oscillation stabilization time select register (OSTS) has elapsed when crystal/ceramic oscillation is used).

The operating statuses in the STOP mode are shown below.

Table 11-4. Operating Statuses in STOP Mode

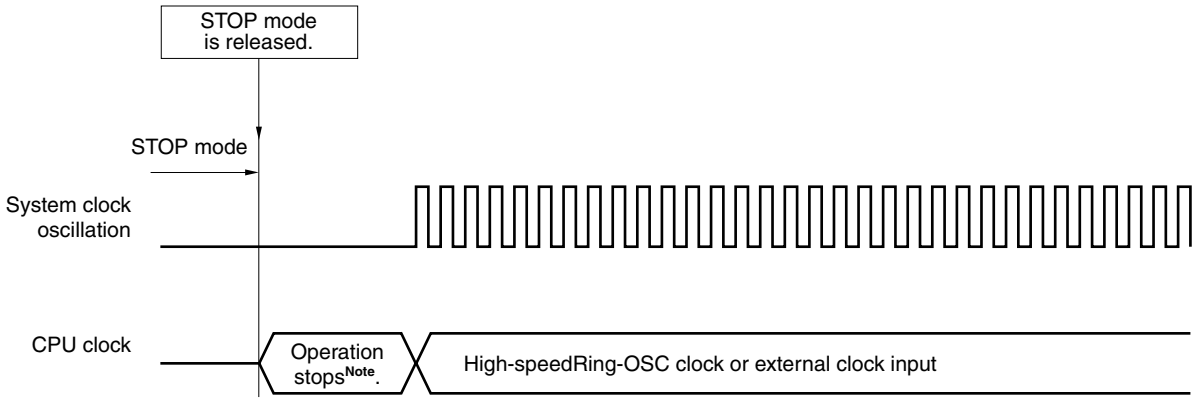
Setting of STOP Mode / Item		Low-speed Ring-OSC cannot be stopped[Note].	Low-speed Ring-OSC can be stopped[Note].	
			When Low-speed Ring-OSC Oscillation Continues	When Low-speed Ring-OSC Oscillation Stops
System clock		Oscillation stops.		
CPU		Operation stops.		
Port (latch)		Holds status before STOP mode was set.		
16-bit timer/event counter 00		Operation stops.		
8-bit timer H1	Sets count clock to f_{XP} to $f_{XP}/2^{12}$	Operation stops.		
	Sets count clock to $f_{RL}/2^{7}$	Operable	Operable	Operation stops.
Watchdog timer	"System clock" selected as operating clock	Setting disabled.	Operation stops.	
	"Low-speed Ring-OSC clock" selected as operating clock	Operable (Operation continues)	Operation stops.	
A/D converter		Operation stops.		
Power-on-clear circuit		Always operates.		
Low-voltage detector		Operable		
External interrupt		Operable		

Note "Low-speed Ring-OSC cannot be stopped" or "low-speed Ring-OSC can be stopped by software" can be selected by the option byte (for the option byte, see **CHAPTER 15 OPTION BYTE**).

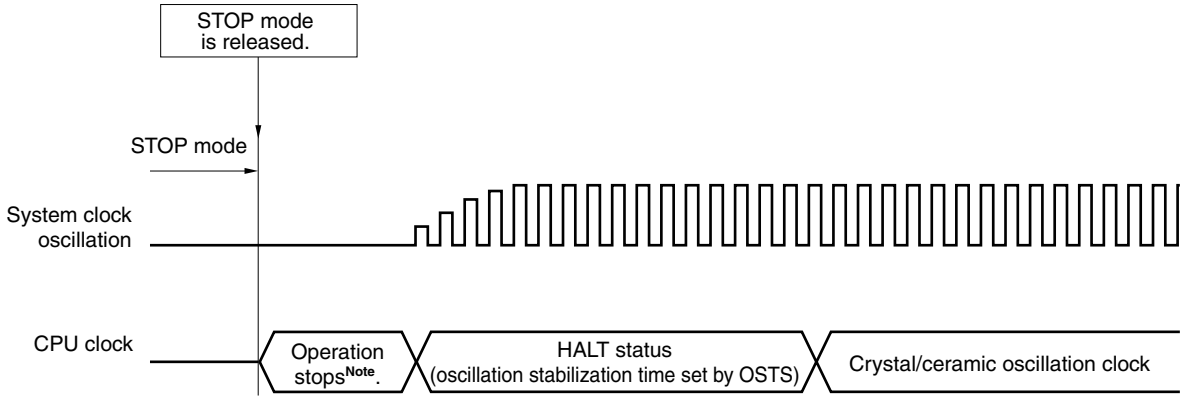
(2) STOP mode release

Figure 11-4. Operation Timing When STOP Mode Is Released

<1> If high-speed Ring-OSC clock or external input clock is selected as system clock to be supplied



<2> If crystal/ceramic oscillation clock is selected as system clock to be supplied



★ **Note** The operation stop time is 17 μs (MIN.), 34 μs (TYP.), and 67 μs (MAX.).

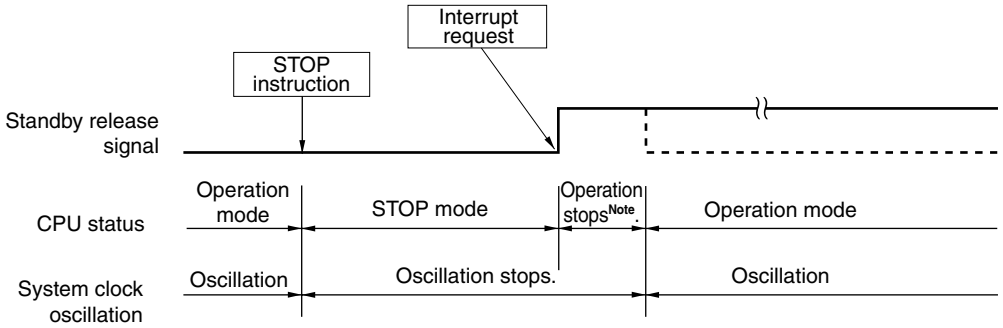
The STOP mode can be released by the following two sources.

(a) Release by unmasked interrupt request

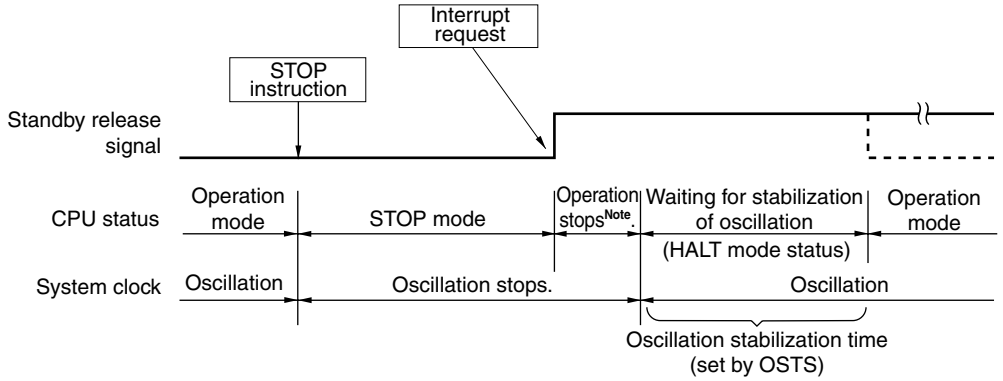
When an unmasked interrupt request is generated, the STOP mode is released. After the oscillation stabilization time has elapsed, if interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 11-5. STOP Mode Release by Interrupt Request Generation

(1) If CPU clock is high-speed Ring-OSC clock or external input clock



(2) If CPU clock is crystal/ceramic oscillation clock



★ **Note** The operation stop time is 17 μs (MIN.), 34 μs (TYP.), and 67 μs (MAX.).

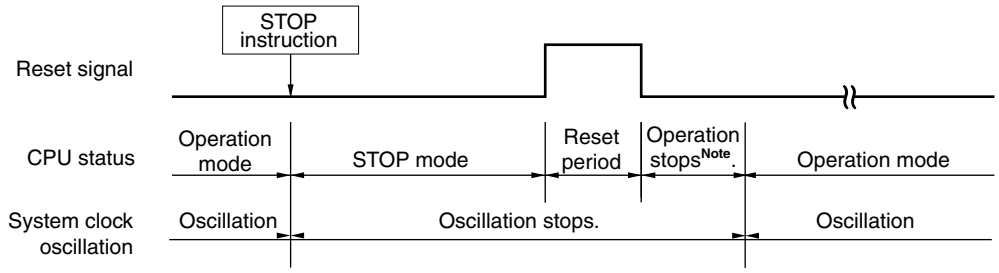
Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

(b) Release by reset input

When the reset signal is input, STOP mode is released and a reset operation is performed after the oscillation stabilization time has elapsed.

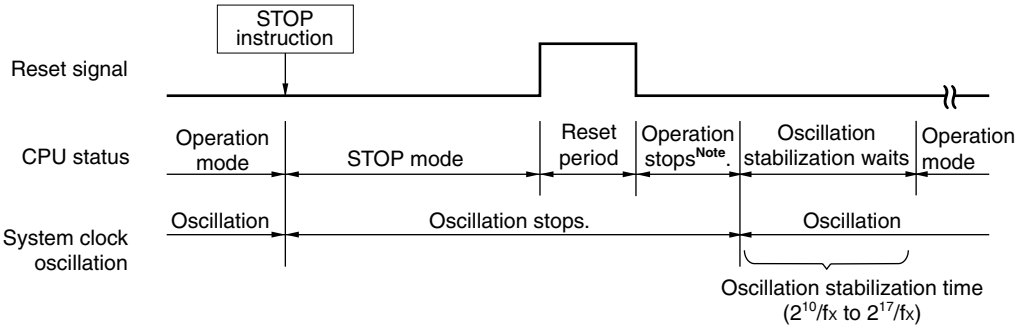
Figure 11-6. STOP Mode Release by Reset Input

(1) If CPU clock is high-speed Ring-OSC clock or external input clock



★ **Note** Operation is stopped (277 μs (MIN.), 544 μs (TYP.), and 1.075 ms (MAX.)) because the option byte is referenced.

(2) If CPU clock is crystal/ceramic oscillation clock



★ **Note** Operation is stopped (276 μs (MIN.), 544 μs (TYP.), and 1.074 ms (MAX.)) because the option byte is referenced.

Remark fx: System clock oscillation frequency

Table 11-5. Operation in Response to Interrupt Request in STOP Mode

Release Source	MK××	IE	Operation
Maskable interrupt request	0	0	Next address instruction execution
	0	1	Interrupt servicing execution
	1	×	STOP mode held
Reset input	–	×	Reset processing

×: don't care

CHAPTER 12 RESET FUNCTION

The following four operations are available to generate a reset signal.

(1) External reset input via $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer program loop detection
(3) Internal reset by comparison of supply voltage and detection voltage of power-on-clear (POC) circuit
(4) Internal reset by comparison of supply voltage and detection voltage of low-power-supply detector (LVI)

External and internal resets have no functional differences. In both cases, program execution starts at the address at 0000H and 0001H when the reset signal is input.

A reset is applied when a low level is input to the $\overline{\text{RESET}}$ pin, the watchdog timer overflows, or by POC and LVI circuit voltage detection, and each item of hardware is set to the status shown in Table 12-1. Each pin is high impedance during reset input or during the oscillation stabilization time just after reset release.

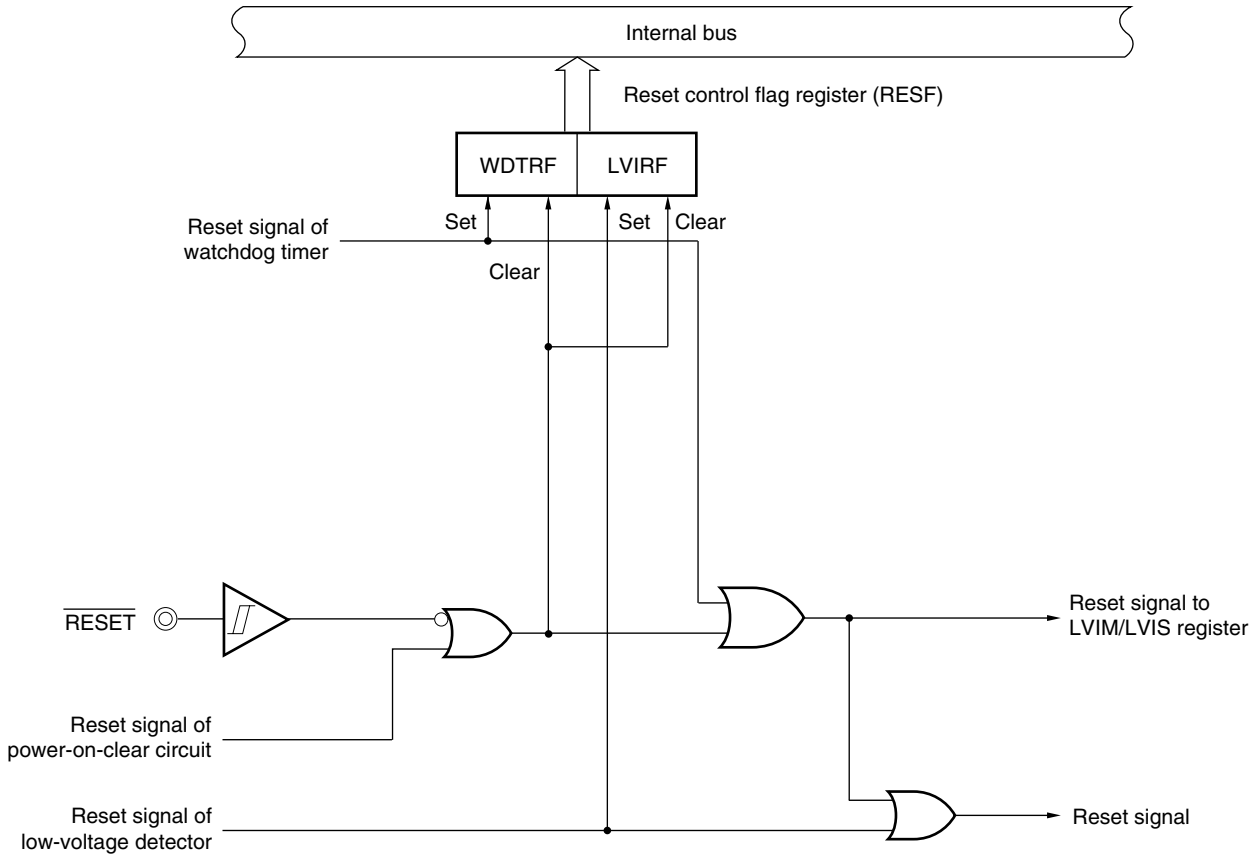
When a high level is input to the $\overline{\text{RESET}}$ pin, the reset is released and program execution starts using the CPU clock after referencing the option byte (after the option byte is referenced and the clock oscillation stabilization time elapses if crystal/ceramic oscillation is selected). A reset generated by the watchdog timer source is automatically released after the reset, and program execution starts using the CPU clock after referencing the option byte (after the option byte is referenced and the clock oscillation stabilization time elapses if crystal/ceramic oscillation is selected). (see **Figures 12-2** to **12-4**). Reset by POC and LVI circuit power supply detection is automatically released when $V_{DD} > V_{POC}$ or $V_{DD} > V_{LVI}$ after the reset, and program execution starts using the CPU clock after referencing the option byte (after the option byte is referenced and the clock oscillation stabilization time elapses if crystal/ceramic oscillation is selected) (see **CHAPTER 13 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 14 LOW-VOLTAGE DETECTOR**).

★ **Cautions 1. For an external reset, input a low level for 2 μs or more to the $\overline{\text{RESET}}$ pin.**

2. During reset input, the system clock and low-speed Ring-OSC clock stop oscillating.

3. When the $\overline{\text{RESET}}$ pin is used as an input-only port pin (P34), the 78K0S/KU1+ and 78K0S/KY1+ are reset if a low level is input to the $\overline{\text{RESET}}$ pin after reset is released by the POC circuit and before the option byte is referenced again. The reset status is retained until a high level is input to the $\overline{\text{RESET}}$ pin.

★ **Figure 12-1. Block Diagram of Reset Function**



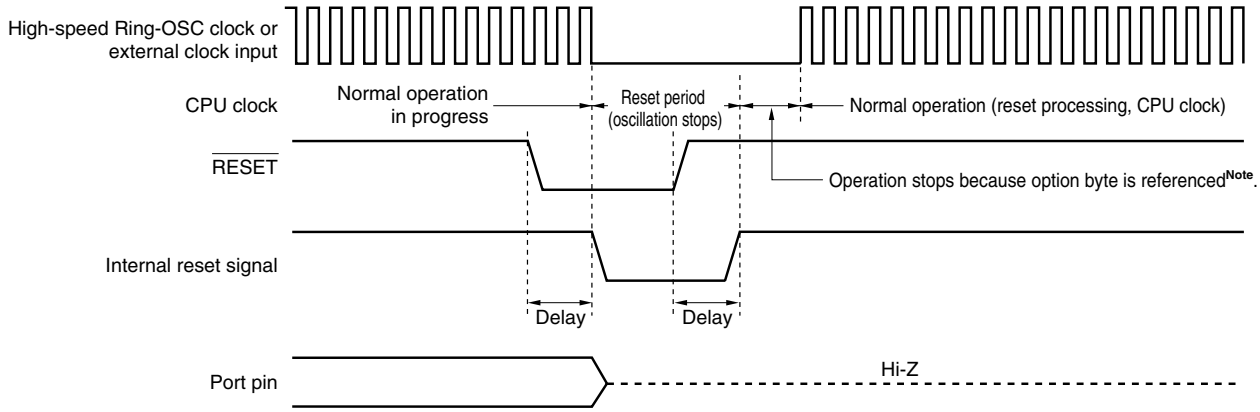
Caution The LVI circuit is not reset by the internal reset signal of the LVI circuit.

Remarks 1. LVIM: Low-voltage detect register

2. LVIS: Low-voltage detection level select register

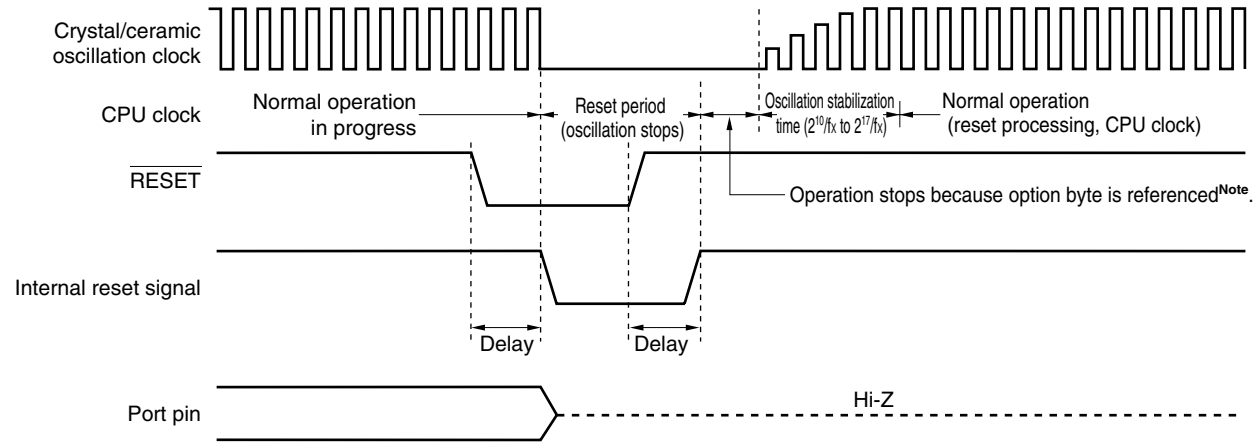
★ **Figure 12-2. Timing of Reset by $\overline{\text{RESET}}$ Input**

<1> With high-speed Ring-OSC clock or external clock input



Note The operation stop time is 277 μs (MIN.), 544 μs (TYP.), and 1.075 ms (MAX.).

<2> With crystal/ceramic oscillation clock

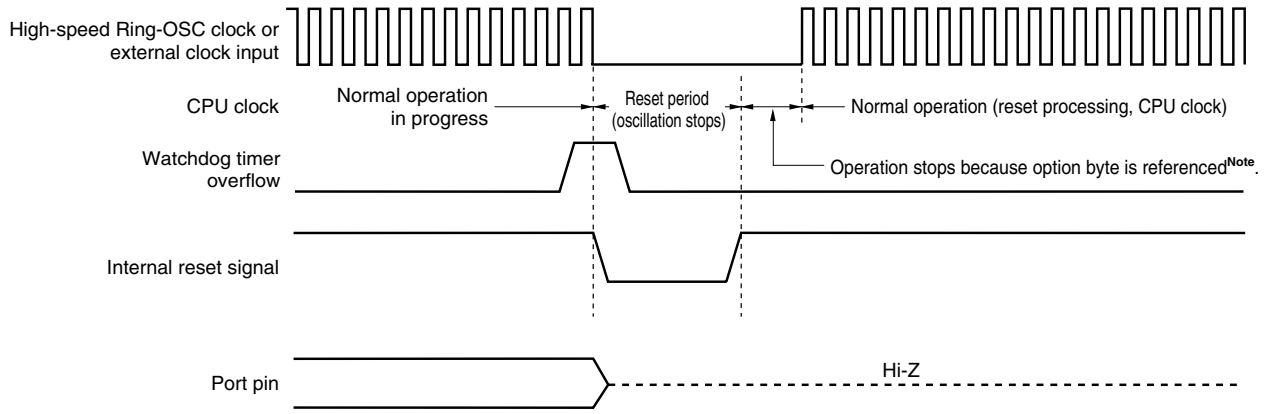


Note The operation stop time is 276 μs (MIN.), 544 μs (TYP.), and 1.074 ms (MAX.).

Remark fx: System clock oscillation frequency

★ **Figure 12-3. Timing of Reset by Overflow of Watchdog Timer**

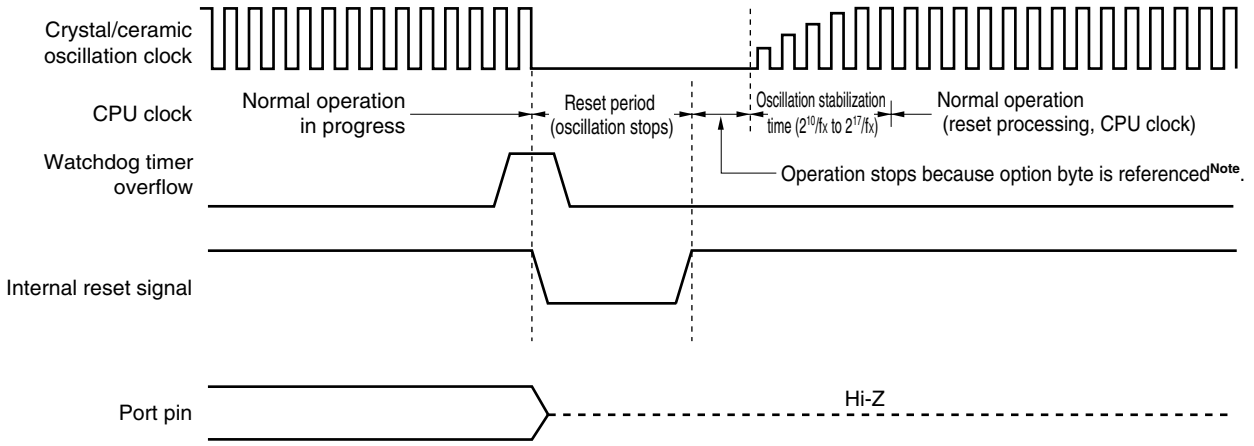
<1> With high-speed Ring-OSC clock or external clock input



Note The operation stop time is 277 μs (MIN.), 544 μs (TYP.), and 1.075 ms (MAX.).

Caution The watchdog timer is also reset in the case of an internal reset of the watchdog timer.

<2> With crystal/ceramic oscillation clock



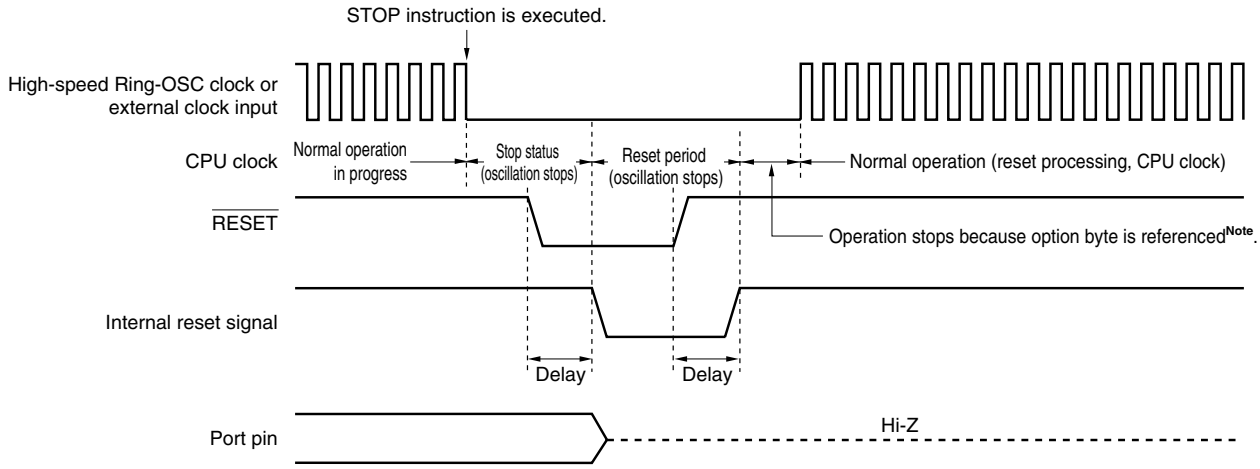
Note The operation stop time is 276 μs (MIN.), 544 μs (TYP.), and 1.074 ms (MAX.).

Caution The watchdog timer is also reset in the case of an internal reset of the watchdog timer.

Remark fx: System clock oscillation frequency

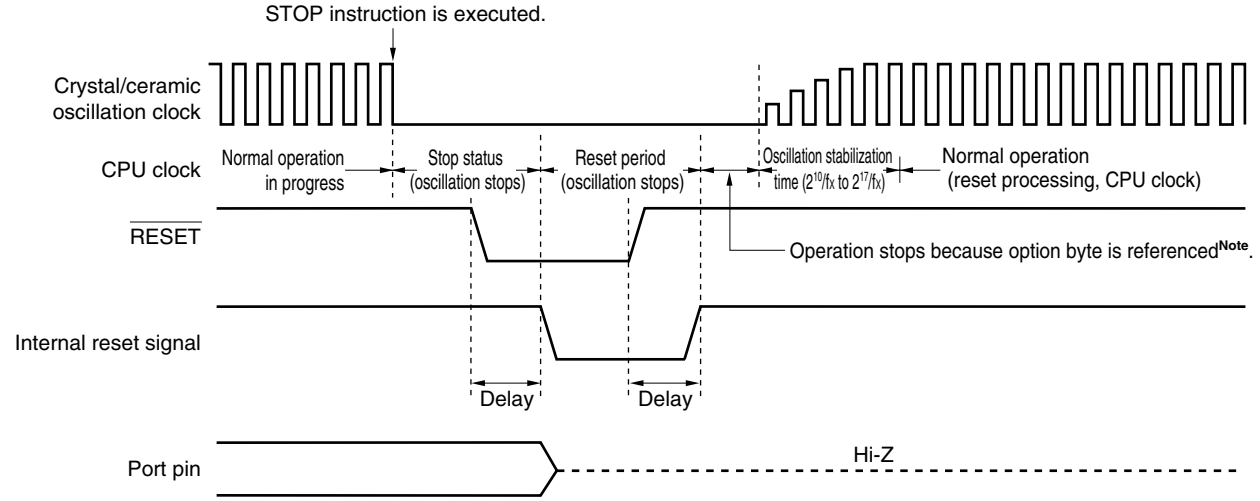
★ **Figure 12-4. Reset Timing by $\overline{\text{RESET}}$ Input in STOP Mode**

<1> With high-speed Ring-OSC clock or external clock input



★ **Note** The operation stop time is 277 μs (MIN.), 544 μs (TYP.), and 1.075 ms (MAX.).

<2> With crystal/ceramic oscillation clock



★ **Note** The operation stop time is 276 μs (MIN.), 544 μs (TYP.), and 1.074 ms (MAX.).

Remarks 1. For the reset timing of the power-on-clear circuit and low-voltage detector, refer to **CHAPTER 13 POWER-ON-CLEAR CIRCUIT and CHAPTER 14 LOW-VOLTAGE DETECTOR**.

2. fx: System clock oscillation frequency

Table 12-1. Hardware Statuses After Reset Acknowledgment (1/2)

Hardware		Status After Reset
Program counter (PC) Note 1		Contents of reset vector table (0000H and 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined Note 2
	General-purpose registers	Undefined Note 2
Ports (P2 to P4) (output latches)		00H
Port mode registers (PM2 to PM4 Note 3)		FFH
Port mode control register (PMC2)		00H
Pull-up resistor option registers (PU2 to PU4)		00H
Processor clock control register (PCC)		02H
Preprocessor clock control register (PPCC)		02H
Low-speed Ring-OSC mode register (LSRCM)		00H
Oscillation stabilization time select register (OSTS)		Undefined
16-bit timer 00	Timer counter 00 (TM00)	0000H
	Capture/compare registers 000, 010 (CR000, CR010)	0000H
	Mode control register 00 (TMC00)	00H
	Prescaler mode register 00 (PRM00)	00H
	Capture/compare control register 00 (CRC00)	00H
	Timer output control register 00 (TOC00)	00H
8-bit timer H1	Compare registers (CMP01, CMP11)	00H
	Mode register 1 (TMHMD1)	00H
Watchdog timer	Mode register (WDTM)	67H
	Enable register (WDTE)	9AH
A/D converter	Conversion result registers (ADCR, ADCRH)	Undefined
	Mode register (ADM)	00H
	Analog input channel specification register (ADS)	00H

Notes 1. Only the contents of PC are undefined while reset is being input and while the oscillation stabilization time elapses. The statuses of the other hardware units remain unchanged.

2. The status after reset is held in the standby mode.

★ **3.** When using the 78K0S/KU1+, set port mode register 4 (PM4) to 00H when initially setting the program.

Table 12-1. Hardware Statuses After Reset Acknowledgment (2/2)

Hardware		Status After Reset
Reset function	Reset control flag register (RESF)	00H[Note]
Low-voltage detector	Low-voltage detection register (LVIM)	00H[Note]
	Low-voltage detection level select register (LVIS)	00H[Note]
Interrupt	Request flag registers (IF0)	00H
	Mask flag registers (MK0)	FFH
	External interrupt mode registers (INTM0)	00H
Flash memory	Flash protect command register (PFCMD)	Undefined
	Flash status register (PFS)	00H
	Flash programming mode control register (FLPMC)	Undefined
	Flash programming command register (FLCMD)	00H
★	Flash address pointer L (FLAPL)	Undefined
	Flash address pointer H (FLAPH)	
	Flash address pointer H compare register (FLAPHC)	00H
	Flash address pointer L compare register (FLAPLC)	00H
	Flash write buffer register (FLW)	00H

Note These values change as follows depending on the reset source.

Register \ Reset Source	$\overline{\text{RESET}}$ Input	Reset by POC	Reset by WDT	Reset by LVI
RESF	See **Table 12-2**.			
LVIM	Cleared (00H)	Cleared (00H)	Cleared (00H)	Held
LVIS				

12.1 Register for Confirming Reset Source

Many internal reset generation sources exist in the 78K0S/KU1+ and 78K0S/KY1+. The reset control flag register (RESF) is used to store which source has generated the reset request.

RESF can be read by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input, reset input by power-on-clear (POC) circuit, and reading RESF clear RESF to 00H.

Figure 12-5. Format of Reset Control Flag Register (RESF)

Address: FF54H After reset: 00H[Note] R

Symbol	7	6	5	4	3	2	1	0
RESF	0	0	0	WDTRF	0	0	0	LVIRF

WDTRF	Internal reset request by watchdog timer (WDT)
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

LVIRF	Internal reset request by low-voltage detector (LVI)
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

Note The value after reset varies depending on the reset source.

Caution Do not read data by a 1-bit memory manipulation instruction.

The status of RESF when a reset request is generated is shown in Table 12-2.

Table 12-2. RESF Status When Reset Request Is Generated

Reset Source / Flag	$\overline{\text{RESET}}$ Input	Reset by POC	Reset by WDT	Reset by LVI
WDTRF	Cleared (0)	Cleared (0)	Set (1)	Held
LVIRF			Held	Set (1)

CHAPTER 13 POWER-ON-CLEAR CIRCUIT

13.1 Functions of Power-on-Clear Circuit

The power-on-clear circuit (POC) has the following functions.

- Generates internal reset signal at power on.
- Compares supply voltage (V_{DD}) and detection voltage (V_{POC} = 2.1 V ±0.1 V), and generates internal reset signal when $V_{DD} < V_{POC}$.
- Compares supply voltage (V_{DD}) and detection voltage (V_{POC} = 2.1 V ±0.1 V), and releases internal reset signal when $V_{DD} \geq V_{POC}$.

Cautions 1. If an internal reset signal is generated in the POC circuit, the reset control flag register (RESF) is cleared to 00H.

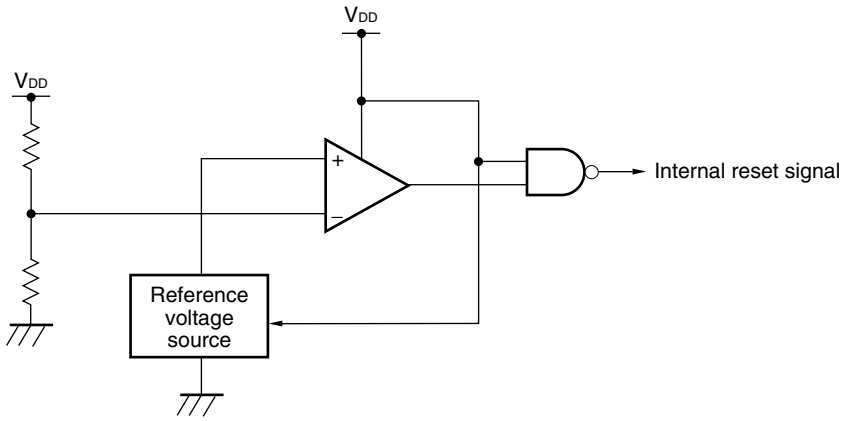
2. Because the detection voltage (V_{POC}) of the POC circuit is in a range of 2.1 V ±0.1 V, use a voltage in the range of 2.2 to 5.5 V.

Remark This product incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset cause is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT) or low-voltage-detection (LVI) circuit. RESF is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by WDT or LVI.
For details of RESF, see **CHAPTER 12 RESET FUNCTION**.

13.2 Configuration of Power-on-Clear Circuit

The block diagram of the power-on-clear circuit is shown in Figure 13-1.

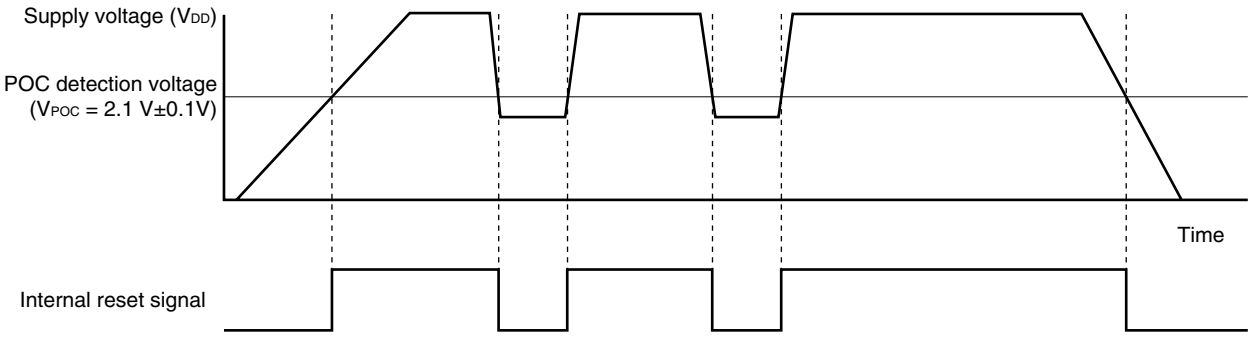
Figure 13-1. Block Diagram of Power-on-Clear Circuit



13.3 Operation of Power-on-Clear Circuit

In the power-on-clear circuit, the supply voltage (V_{DD}) and detection voltage (V_{POC} = 2.1 V ±0.1 V) are compared, and an internal reset signal is generated when $V_{DD} < V_{POC}$, and an internal reset is released when $V_{DD} \geq V_{POC}$.

Figure 13-2. Timing of Internal Reset Signal Generation in Power-on-Clear Circuit



Remark The internal reset signal is active-low.

13.4 Cautions for Power-on-Clear Circuit

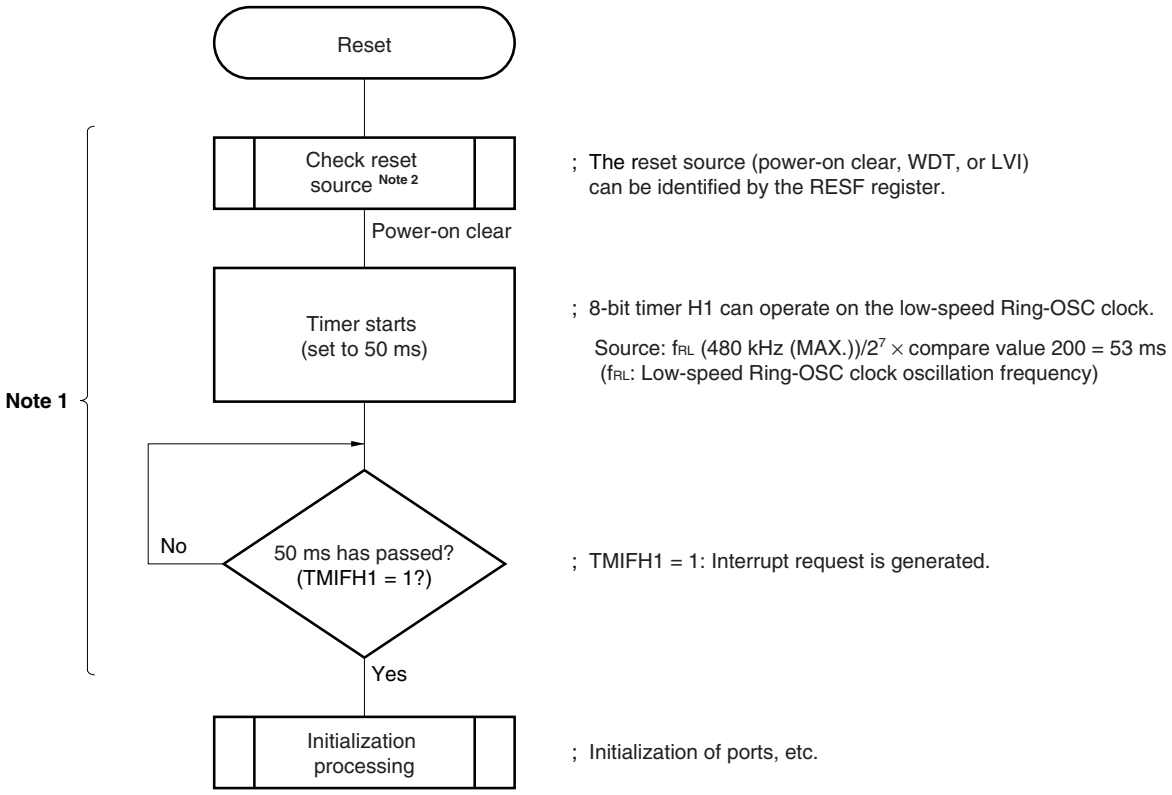
In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the POC detection voltage (V_{POC}), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.

<Action>

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports.

Figure 13-3. Example of Software Processing After Release of Reset (1/2)

• If supply voltage fluctuation is 50 ms or less in vicinity of POC detection voltage

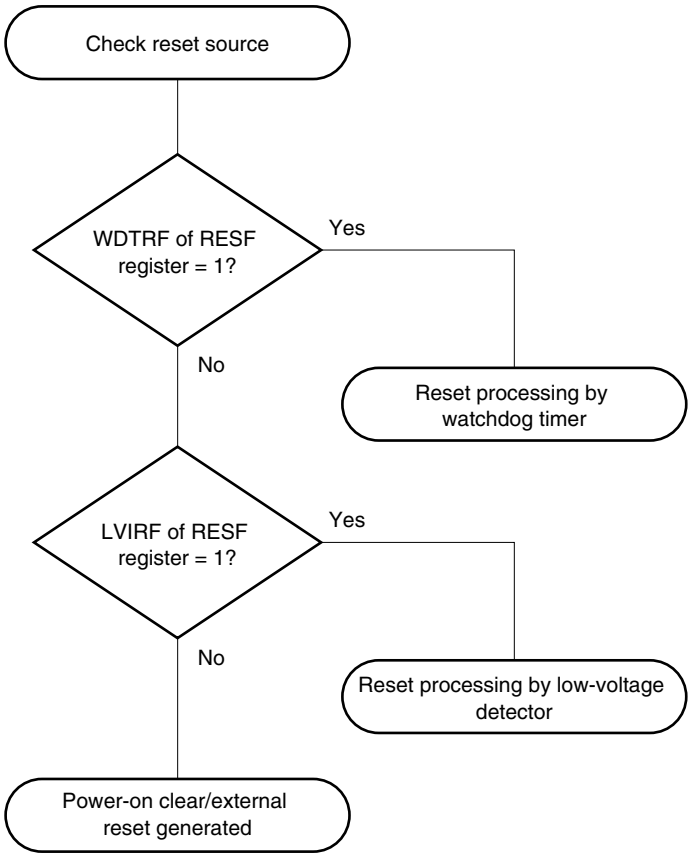


Notes 1. If reset is generated again during this period, initialization processing is not started.

2. A flowchart is shown on the next page.

Figure 13-3. Example of Software Processing After Release of Reset (2/2)

• Checking reset cause



CHAPTER 14 LOW-VOLTAGE DETECTOR

14.1 Functions of Low-Voltage Detector

The low-voltage detector (LVI) has following functions.

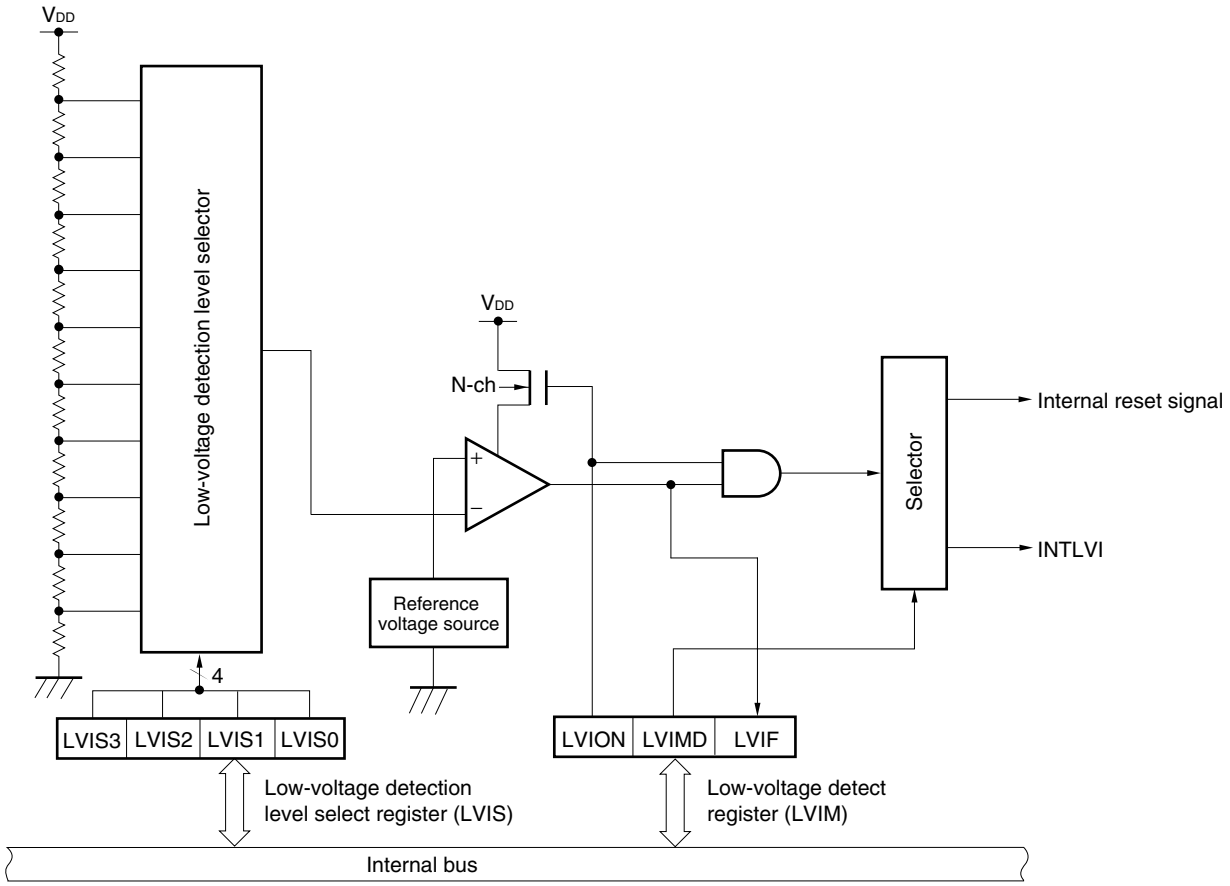
- Compares supply voltage (V_{DD}) and detection voltage (V_{LVI}), and generates an internal interrupt signal or internal reset signal when $V_{DD} < V_{LVI}$.
- Detection levels (ten levels) of supply voltage can be changed by software.
- Interrupt or reset function can be selected by software.
- Operable in STOP mode.

When the low-voltage detector is used to reset, bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of RESF, refer to **CHAPTER 12 RESET FUNCTION**.

14.2 Configuration of Low-Voltage Detector

The block diagram of the low-voltage detector is shown in Figure 14-1.

Figure 14-1. Block Diagram of Low-Voltage Detector



14.3 Registers Controlling Low-Voltage Detector

The low-voltage detector is controlled by the following registers.

- Low-voltage detect register (LVIM)
- Low-voltage detection level select register (LVIS)

(1) Low-voltage detect register (LVIM)

This register sets low-voltage detection and the operation mode.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset input clears this register to 00H[Note 1].

Figure 14-2. Format of Low-Voltage Detect Register (LVIM)

Address: FF50H After reset: 00H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	2	<1>	<0>
LVIM	LVION	0	0	0	0	0	LVIMD	LVIF

LVION[Note 3]	Enabling low-voltage detection operation
0	Disable operation
1	Enable operation

LVIMD	Low-voltage detection operation mode selection
0	Generate interrupt signal when supply voltage (V_{DD}) < detection voltage (V_{LVI})
1	Generate internal reset signal when supply voltage (V_{DD}) < detection voltage (V_{LVI})

LVIF[Note 4]	Low-voltage detection flag
0	Supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}), or when operation is disabled
1	Supply voltage (V_{DD}) < detection voltage (V_{LVI})

★ **Notes 1.** The value of LVIM is not initialized after a reset by LVI.

2. Bit 0 is a read-only bit.

3. When LVION is set to 1, operation of the comparator in the LVI circuit is started. Use software to instigate a wait of at least 0.2 ms from when LVION is set to 1 until the voltage is confirmed at LVIF.

4. The value of LVIF is output as the interrupt request signal INTLVI when LVION = 1 and LVIMD = 0.

Cautions 1. To stop LVI, follow either of the procedures below.

- **When using 8-bit manipulation instruction: Write 00H to LVIM.**
- **When using 1-bit memory manipulation instruction: Clear LVION to 0.**

2. Be sure to set bits 2 to 6 to 0.

(2) Low-voltage detection level select register (LVIS)

This register selects the low-voltage detection level.

This register can be set by an 8-bit memory manipulation instruction.

Reset input clears this register to 00H[Note].

Figure 14-3. Format of Low-Voltage Detection Level Select Register (LVIS)

Address: FF51H, After reset: 00H[Note] R/W

Symbol	7	6	5	4	3	2	1	0
LVIS	0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	0	0	0	V_{LVI0} (4.3 V ±0.2 V)
0	0	0	1	V_{LVI1} (4.1 V ±0.2 V)
0	0	1	0	V_{LVI2} (3.9 V ±0.2 V)
0	0	1	1	V_{LVI3} (3.7 V ±0.2 V)
0	1	0	0	V_{LVI4} (3.5 V ±0.2 V)
0	1	0	1	V_{LVI5} (3.3 V ±0.15 V)
0	1	1	0	V_{LVI6} (3.1 V ±0.15 V)
0	1	1	1	V_{LVI7} (2.85 V ±0.15 V)
1	0	0	0	V_{LVI8} (2.6 V ±0.15 V)
1	0	0	1	V_{LVI9} (2.35 V ±0.15 V)
Other than above				Setting prohibited

★ **Note** The value of LVIS is not initialized after a reset by LVI.

Caution Bits 4 to 7 must be set to 0.

14.4 Operation of Low-Voltage Detector

The low-voltage detector can be used in the following two modes.

- Used as reset
  Compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}), and generates an internal reset signal when $V_{DD} < V_{LVI}$, and releases internal reset when $V_{DD} \geq V_{LVI}$.

- Used as interrupt
  Compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}), and generates an interrupt signal (INTLVI) when $V_{DD} < V_{LVI}$.

The operation is set as follows.

(1) When used as reset

- When starting operation

<1> Mask the LVI interrupt (LVIMK = 1).

<2> Set the detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level select register (LVIS).

<3> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).

<4> Use software to instigate a wait of at least 0.2 ms.

<5> Wait until "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" at bit 0 (LVIF) of LVIM is confirmed.

<6> Set bit 1 (LVIMD) of LVIM to 1 (generates internal reset signal when supply voltage (V_{DD}) < detection voltage (V_{LVI})).

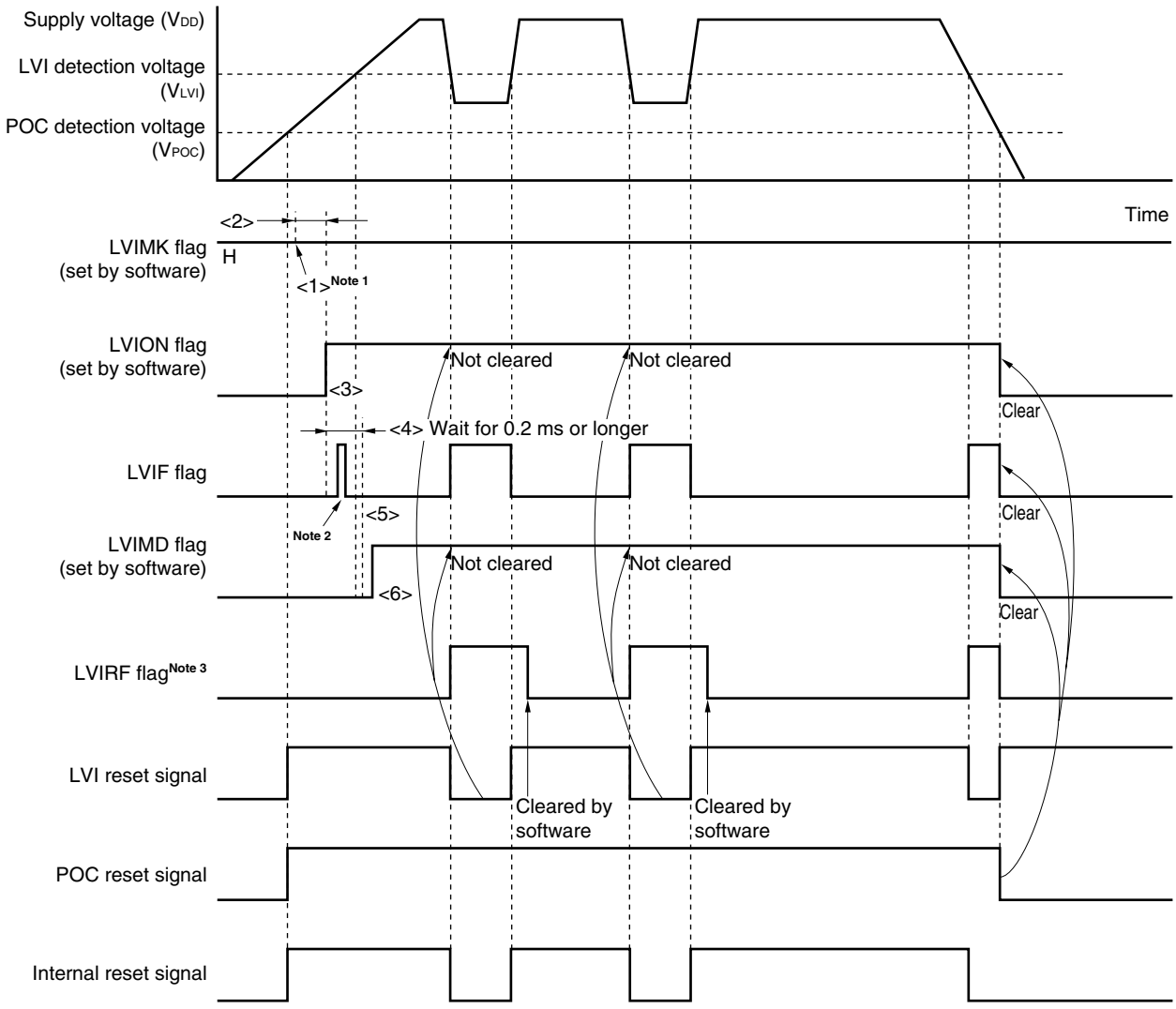
Figure 14-4 shows the timing of generating the internal reset signal of the low-voltage detector. Numbers <1> to <6> in this figure correspond to <1> to <6> above.

Cautions 1. <1> must always be executed. When LVIMK = 0, an interrupt may occur immediately after the processing in <3>.

2. If supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}) when LVIMD is set to 1, an internal reset signal is not generated.

- When stopping operation
  Either of the following procedures must be executed.
  - When using 8-bit memory manipulation instruction: Write 00H to LVIM.
  - When using 1-bit memory manipulation instruction: Clear LVIMD to 0 and LVION to 0 in that order.

Figure 14-4. Timing of Low-Voltage Detector Internal Reset Signal Generation



Notes 1. The LVIMK flag is set to “1” by reset input.

2. The LVIF flag may be set (1).

3. LVIRF is bit 0 of the reset control flag register (RESF). For details of RESF, refer to **CHAPTER 12 RESET FUNCTION**.

Remark <1> to <6> in Figure 14-4 above correspond to <1> to <6> in the description of “when starting operation” in **14.4 (1) When used as reset**.

(2) When used as interrupt

- When starting operation

<1> Mask the LVI interrupt (LVIMK = 1).

<2> Set the detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level select register (LVIS).

<3> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).

<4> Use software to instigate a wait of at least 0.2 ms.

<5> Wait until "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" at bit 0 (LVIF) of LVIM is confirmed.

<6> Clear the interrupt request flag of LVI (LVIIF) to 0.

<7> Release the interrupt mask flag of LVI (LVIMK).

<8> Execute the EI instruction (when vector interrupts are used).

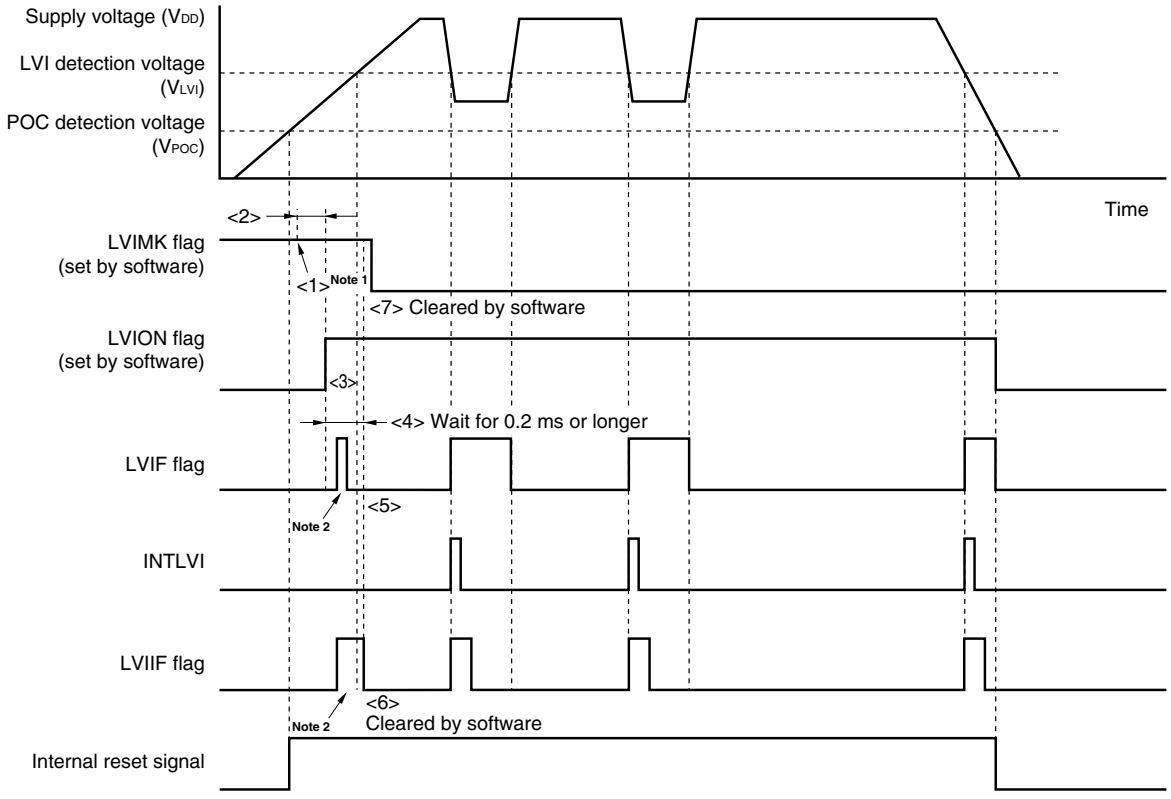
Figure 14-5 shows the timing of generating the interrupt signal of the low-voltage detector. Numbers <1> to <7> in this figure correspond to <1> to <7> above.

- When stopping operation

  Either of the following procedures must be executed.

  - When using 8-bit memory manipulation instruction: Write 00H to LVIM.
  - When using 1-bit memory manipulation instruction: Clear LVION to 0.

Figure 14-5. Timing of Low-Voltage Detector Interrupt Signal Generation



Notes 1. The LVIMK flag is set to "1" by reset input.

2. The LVIF and LVIIF flags may be set (1).

Remark <1> to <7> in Figure 14-5 above correspond to <1> to <7> in the description of "when starting operation" in **14.4 (2) When used as interrupt**.

14.5 Cautions for Low-Voltage Detector

In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the LVI detection voltage (V_{LVI}), the operation is as follows depending on how the low-voltage detector is used.

<1> When used as reset

The system may be repeatedly reset and released from the reset status.

In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking action (1) below.

<2> When used as interrupt

Interrupt requests may be frequently generated. Take action (2) below.

In this system, take the following actions.

<Action>

(1) When used as reset

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports (see **Figure 14-6**).

(2) When used as interrupt

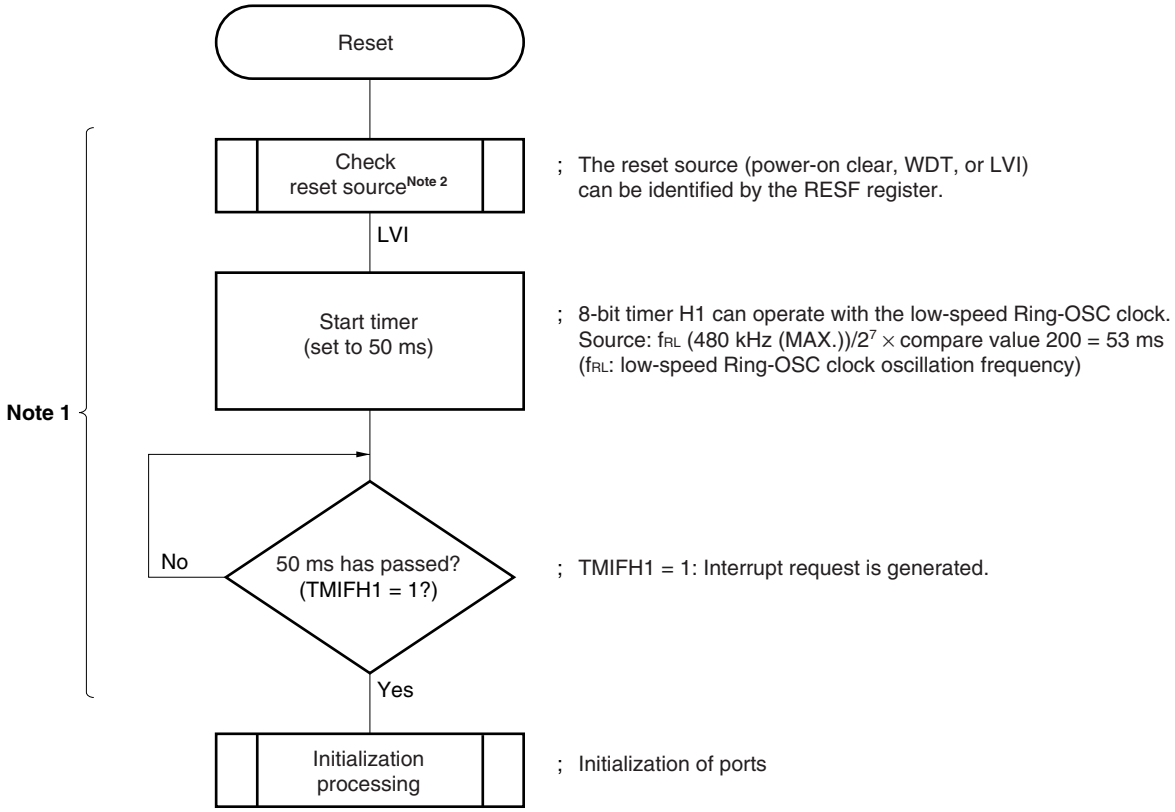
★ Perform the processing[Note] for low voltage detection. Check that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" in the servicing routine of the LVI interrupt by using bit 0 (LVIF) of the low-voltage detection register (LVIM). Clear bit 1 (LVIIF) of interrupt request flag register 0 (IF0) to 0 and enable interrupts (EI).

In a system where the supply voltage fluctuation period is long in the vicinity of the LVI detection voltage, wait for the supply voltage fluctuation period, check that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" using the LVIF flag, and then enable interrupts (EI).

★ **Note** For low voltage detection processing, the CPU clock speed is switched to slow speed and the A/D converter is stopped, etc.

Figure 14-6. Example of Software Processing After Release of Reset (1/2)

• If supply voltage fluctuation is 50 ms or less in vicinity of LVI detection voltage

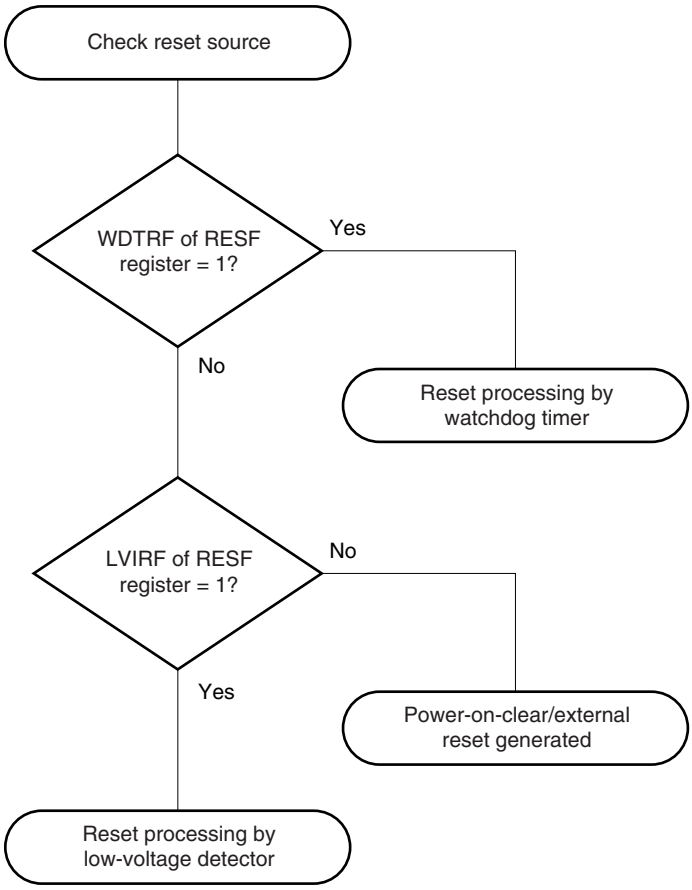


Notes 1. If reset is generated again during this period, initialization processing is not started.

2. A flowchart is shown on the next page.

Figure 14-6. Example of Software Processing After Release of Reset (2/2)

• Checking reset source



CHAPTER 15 OPTION BYTE

The 78K0S/KU1+ and 78K0S/KY1+ have an area called an option byte at address 0080H of the flash memory. When using the product, be sure to set the following functions by using the option byte.

1. **Selection of system clock source**
   - High-speed Ring-OSC clock
   - Crystal/ceramic oscillation clock
   - External clock input

2. **Low-speed Ring-OSC clock oscillation**
   - Cannot be stopped.
   - Can be stopped by software.

3. **Control of $\overline{\text{RESET}}$ pin**
   - Used as $\overline{\text{RESET}}$ pin
   - $\overline{\text{RESET}}$ pin is used as an input port pin (P34).

4. **Oscillation stabilization time on power application or after reset release**
   - 2^{10}/fx
   - 2^{12}/fx
   - 2^{15}/fx
   - 2^{17}/fx

Figure 15-1. Positioning of Option Byte

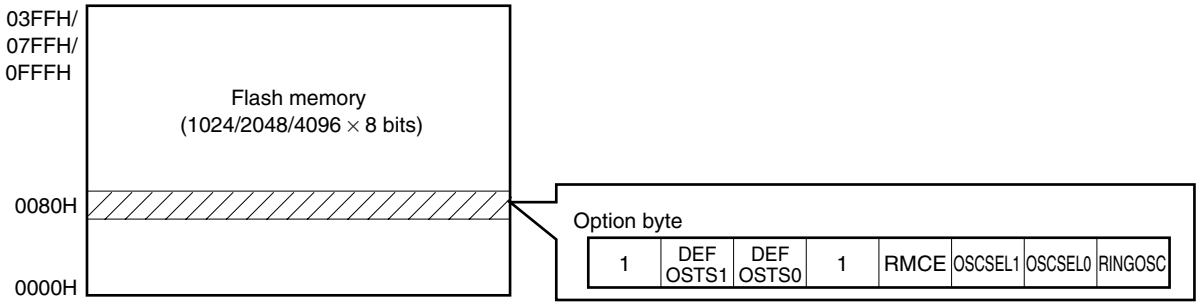


Figure 15-2. Format of Option Byte (1/2)

Address: 0080H

7	6	5	4	3	2	1	0
1	DEFOSTS1	DEFOSTS0	1	RMCE	OSCSEL1	OSCSEL0	RINGOSC

RINGOSC	Low-speed Ring-OSC clock oscillation
1	Cannot be stopped (oscillation does not stop even if 1 is written to the LSRSTOP bit)
0	Can be stopped by software (oscillation stops when 1 is written to the LSRSTOP bit)

Cautions 1. If it is selected that low-speed Ring-OSC clock oscillation cannot be stopped, the count clock to the watchdog timer (WDT) is fixed to low-speed Ring-OSC.

2. If it is selected that low-speed Ring-OSC can be stopped by software, supply of the count clock to WDT is stopped in the HALT/STOP mode, regardless of the setting of bit 0 (LSRSTOP) of the low-speed Ring-OSC mode register (LSRCM). Similarly, clock supply is also stopped when a clock other than the low-speed Ring-OSC is selected as a count clock to WDT. If low-speed Ring-OSC is selected as the count clock to 8-bit timer H1, however, the count clock is supplied in the HALT/STOP mode while low-speed Ring-OSC operates (LSRSTOP = 0).

★

OSCSEL1	OSCSEL0	Selection of system clock source
0	0	Crystal/ceramic oscillation clock
0	1	External clock input
1	×	High-speed Ring-OSC clock

Caution Because the X1 and X2 pins are also used as the P23/ANI3 and P22/ANI2 pins, the conditions under which the X1 and X2 pins can be used differ depending on the selected system clock source.

(1) High-speed Ring-OSC clock

P23/ANI3 and P22/ANI2 pins can be used as I/O port pins or analog input pins of A/D converter.

(2) Crystal/ceramic oscillation clock

The X1 and X2 pins cannot be used as I/O port pins or analog input pins of A/D converter because they are used as clock input pins.

(3) External clock input

Because the X1 pin is used as an external clock input pin, P23/ANI3 cannot be used as an I/O port pin or an analog input pin of A/D converter.

Remark × : don't care

RMCE	Control of $\overline{\text{RESET}}$ pin
1	$\overline{\text{RESET}}$ pin is used as is.
0	$\overline{\text{RESET}}$ pin is used as input port pin (P34).

Caution If a low level is input to the $\overline{\text{RESET}}$ pin after reset is released by the power-on clear function and before the option byte is referenced again, the 78K0S/KU1+ and 78K0S/KY1+ are reset, and the status is held until a high level is input to the $\overline{\text{RESET}}$ pin.

Figure 15-2. Format of Option Byte (2/2)

DEFOSTS1	DEFOSTS0	Oscillation stabilization time on power application or after reset release
0	0	2^{10}/fx (102.4 μs)
0	1	2^{12}/fx (409.6 μs)
1	0	2^{15}/fx (3.27 ms)
1	1	2^{17}/fx (13.1 ms)

Caution The setting of this option is valid only when the crystal/ceramic oscillation clock is selected as the system clock source. No wait time elapses if the high-speed Ring-OSC or external clock input is selected as the system clock source.

Remarks 1. ( ): fx = 10 MHz

2. For the oscillation stabilization time of the resonator, refer to the characteristics of the resonator to be used.

★

CHAPTER 16 FLASH MEMORY

16.1 Features

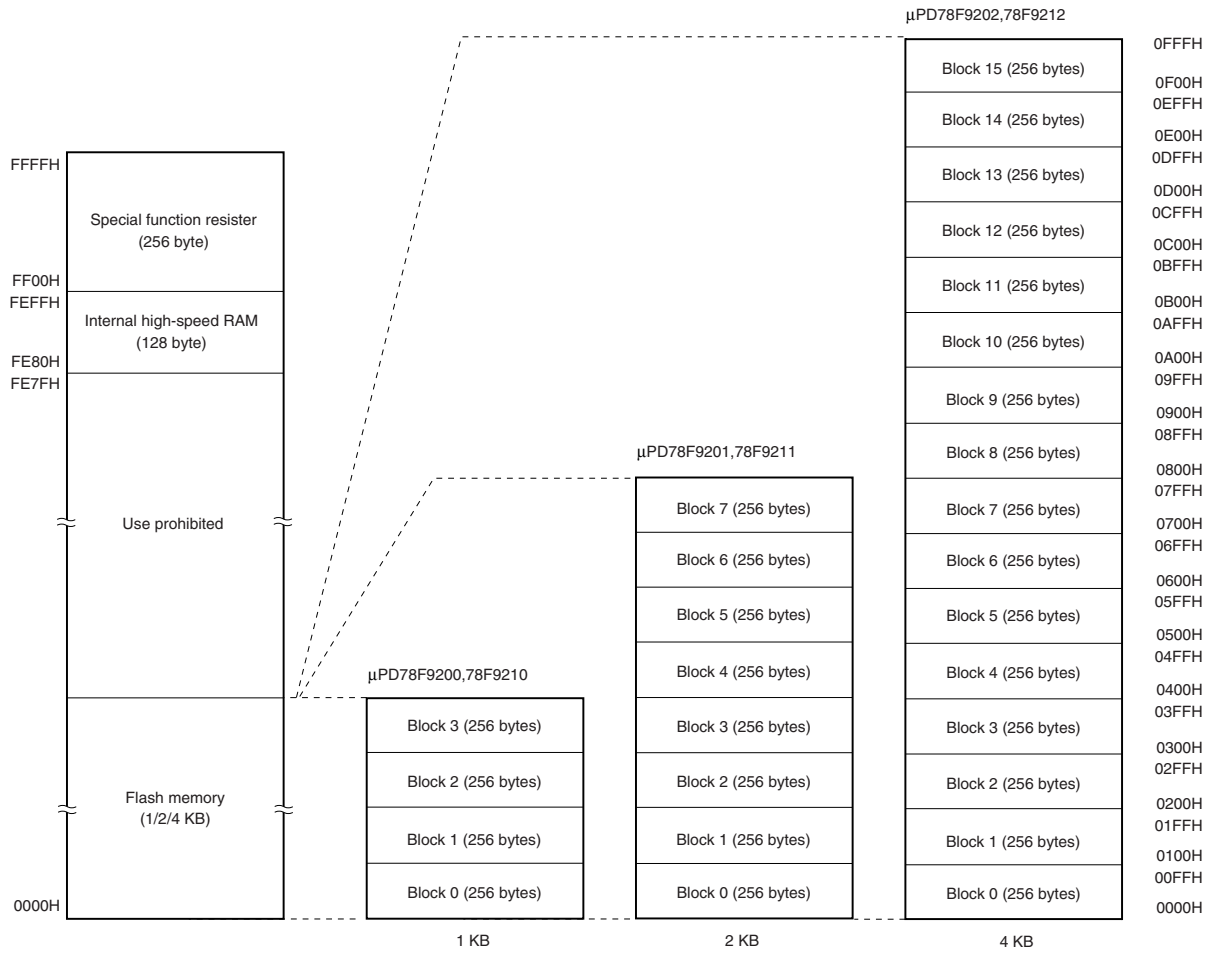
The internal flash memory of the 78K0S/KU1+ and 78K0S/KY1+ has the following features.

- ○ Erase/write with a single power supply
- ○ Capacity: 1/2/4 KB
  - Erase unit: 1 block (256 bytes)
  - Write unit: 1 byte
- ○ Rewriting method
  - Rewriting by communication with dedicated flash programmer (on-board/off-board programming)
  - Rewriting flash memory by user program (self programming)
- ○ Flash memory write prohibit function supported (security function)

16.2 Memory Configuration

The 1/2/4 KB internal flash memory area is divided into 4/8/16 blocks and can be programmed/erased in block units. All the blocks can also be erased at once.

Figure 16-1. Flash Memory Mapping



16.3 Functional Outline

The internal flash memory of the 78K0S/KU1+ and 78K0S/KY1+ can be rewritten by using the rewrite function of the dedicated flash programmer, regardless of whether the 78K0S/KU1+ and 78K0S/KY1+ have already been mounted on the target system or not (on-board/off-board programming).

The function for rewriting a program with the user program (self programming), which is ideal for an application when it is assumed that the program is changed after production/shipment of the target system, is provided.

In addition, a security function that prohibits rewriting the user program written to the internal flash memory is also supported, so that the program cannot be changed by an unauthorized person.

Refer to **16.7.4 Security settings** for details on the security function.

Table 16-1. Rewrite Method

Rewrite Method	Functional Outline	Operation Mode
On-board programming	Flash memory can be rewritten after the device is mounted on the target system, by using a dedicated flash programmer.	Flash memory programming mode
Off-board programming	Flash memory can be rewritten before the device is mounted on the target system, by using a dedicated flash programmer and a dedicated program adapter board (FA series).	
Self programming	Flash memory can be rewritten by executing a user program that has been written to the flash memory in advance by means of on-board/off-board programming.	Self programming mode

Remarks 1. The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

2. Refer to the following sections for details on the flash memory writing control function.

- **16.7 On-Board and Off-Board Flash Memory Programming**
- **16.8 Flash Memory Programming by Self Writing**

16.4 Writing with Flash Programmer

The following two types of dedicated flash programmers can be used for writing data to the internal flash memory of the 78K0S/KU1+ and 78K0S/KY1+.

- FlashPro4 (PG-FP4, FL-PR4)
- PG-FPL2

Data can be written to the flash memory on-board or off-board, by using a dedicated flash programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the 78K0S/KU1+ and 78K0S/KY1+ have been mounted on the target system. The connectors that connect the dedicated flash programmer and the test pad must be mounted on the target system. The test pad is required only when writing data with the crystal/ceramic resonator mounted (refer to Figure 16-7 for mounting of the test pad).

(2) Off-board programming

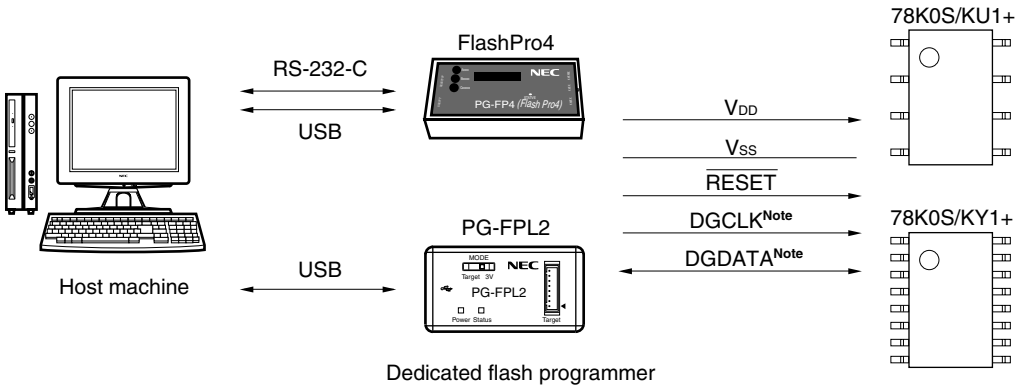
Data can be written to the flash memory with a dedicated program adapter (FA series) before the 78K0S/KU1+ and 78K0S/KY1+ are mounted on the target system.

Remark The FL-PR4 and FA series are products of Naito Densei Machida Mfg. Co., Ltd.

16.5 Programming Environment

The environment required for writing a program to the flash memory is illustrated below.

Figure 16-2. Environment for Writing Program to Flash Memory



Note DGCLK and DGDATA are single-wire bidirectional communication interfaces. They use UART as the communication mode.

A host machine that controls the dedicated flash programmer is necessary. When using the PG-FP4 or FL-PR4, data can be written with just the dedicated flash programmer after downloading the program from the host machine.

UART is used for manipulation such as writing and erasing when interfacing between the dedicated flash programmer and the 78K0S/KU1+, 78K0S/KY1+. To write the flash memory off-board, a dedicated program adapter (FA series) is necessary.

Download the latest programmer firmware, GUI, and parameter file from the download site for development tools (http://www.necel.com/micro/ods/eng/index.html).

Table 16-2. Wiring Between 78K0S/KU1+ and FlashPro4

FlashPro4 Connection Pin			78K0S/KU1+ Connection Pin	
Pin Name	I/O	Pin Function	Pin Name	Pin No.
CLK[Note]	Output	Clock to 78K0S/KU1+	X1/P23/ANI3	2
FLMD0[Note]	Output	On-board mode signal		
SI/RxD[Note]	Input	Receive signal	X2/P22/ANI2	3
SO/TxD[Note]	Output	Receive signal/on-board mode signal		
/RESET	Output	Reset signal	$\overline{\text{RESET}}$/P34	4
V_{DD}	–	V_{DD} voltage generation/voltage monitor	V_{DD}	1
GND	–	Ground	V_{SS}	8

Note In the 78K0S/KU1+, the CLK and FLMD0 signals are connected to the X1 pin and the SI/RxD and SO/TxD signals to the X2 signal; therefore, these signals need to be directly connected.

Figure 16-3. Communication with FlashPro4 (78K0S/KU1+)

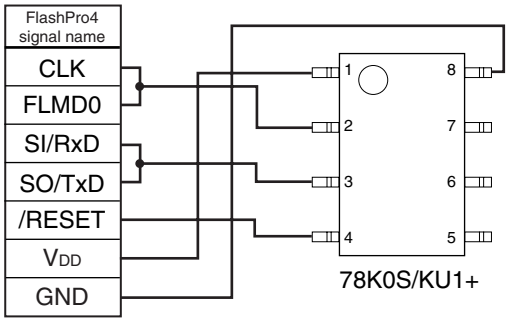


Table 16-3. Wiring Between 78K0S/KU1+ and PG-FPL2

PG-FPL2 Connection Pin			78K0S/KU1+ Connection Pin	
Pin Name	I/O	Pin Function	Pin Name	Pin No.
DGCLK	Output	Clock to 78K0S/KU1+	X1/P23/ANI3	2
DGDATA	I/O	Transmit/receive signal, on-board mode signal	X2/P22/ANI2	3
/RESET	Output	Reset signal	$\overline{\text{RESET}}$/P34	4
V_{DD}	I/O	V_{DD} voltage generation	V_{DD}	1
GND	–	Ground	V_{SS}	8

Figure 16-4. Communication with PG-FPL2 (78K0S/KU1+)

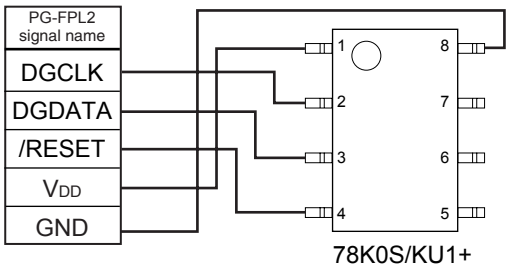


Table 16-4. Wiring Between 78K0S/KY1+ and FlashPro4

FlashPro4 Connection Pin			78K0S/KY1+ Connection Pin	
Pin Name	I/O	Pin Function	Pin Name	Pin No.
CLK[Note]	Output	Clock to 78K0S/KY1+	X1/P23/ANI3	8
FLMD0[Note]	Output	On-board mode signal		
SI/RxD[Note]	Input	Receive signal	X2/P22/ANI2	9
SO/TxD[Note]	Output	Receive signal/on-board mode signal		
/RESET	Output	Reset signal	$\overline{\text{RESET}}$/P34	12
V_{DD}	–	V_{DD} voltage generation/voltage monitor	V_{DD}	5
GND	–	Ground	V_{SS}	4

Note In the 78K0S/KY1+, the CLK and FLMD0 signals are connected to the X1 pin and the SI/RxD and SO/TxD signals to the X2 signal; therefore, these signals need to be directly connected.

Figure 16-5. Communication with FlashPro4 (78K0S/KY1+)

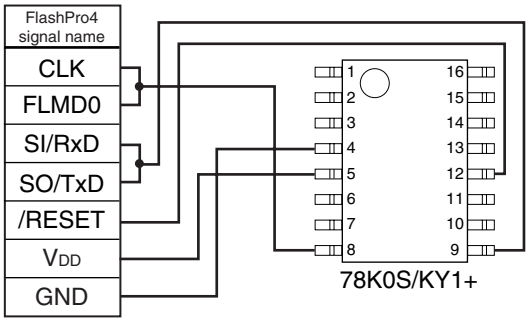
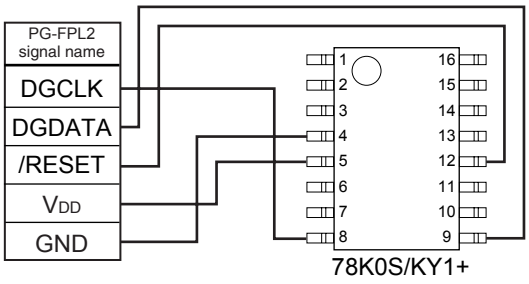


Table 16-5. Wiring Between 78K0S/KY1+ and PG-FPL2

PG-FPL2 Connection Pin			78K0S/KU1+ Connection Pin	
Pin Name	I/O	Pin Function	Pin Name	Pin No.
DGCLK	Output	Clock to 78K0S/KY1+	X1/P21	8
DGDATA	I/O	Transmit/receive signal, on-board mode signal	X2/P22	9
/RESET	Output	Reset signal	$\overline{\text{RESET}}$/P34	12
V_{DD}	I/O	V_{DD} voltage generation	V_{DD}	5
GND	–	Ground	V_{SS}	4

Figure 16-6. Communication with PG-FPL2 (78K0S/KY1+)



16.6 Processing of Pins on Board

To write the flash memory on-board, connectors that connect the dedicated flash programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be processed as described below.

The state of the pins in the self programming mode is the same as that in the HALT mode.

16.6.1 X1 and X2 pins

The X1 and X2 pins are used as the serial interface of flash memory programming. Therefore, if the X1 and X2 pins are connected to an external device, a signal conflict occurs. To prevent the conflict of signals, isolate the connection with the external device.

Perform the following processing (1) and (2) when on-board writing is performed with the resonator mounted, when it is difficult to isolate the resonator, while a crystal or ceramic resonator is selected as the system clock.

(1) Mount the minimum-possible test pads between the device and the resonator, and connect the flash programmer via the test pad. Keep the wiring as short as possible (refer to Figure 16-7 and Table 16-6).

(2) Set the oscillation frequency of the communication clock for writing using the GUI software of the dedicated flash programmer. Research the series/parallel resonant and antiresonant frequencies of the resonator used, and set the oscillation frequency so that it is outside the range of the resonant frequency ±10% (refer to Figure 16-8 and Table 16-7).

Figure 16-7. Example of Mounting Test Pads

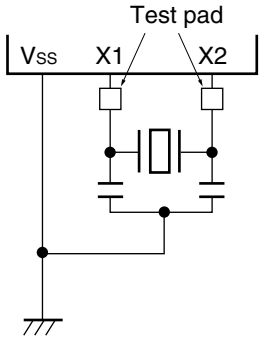
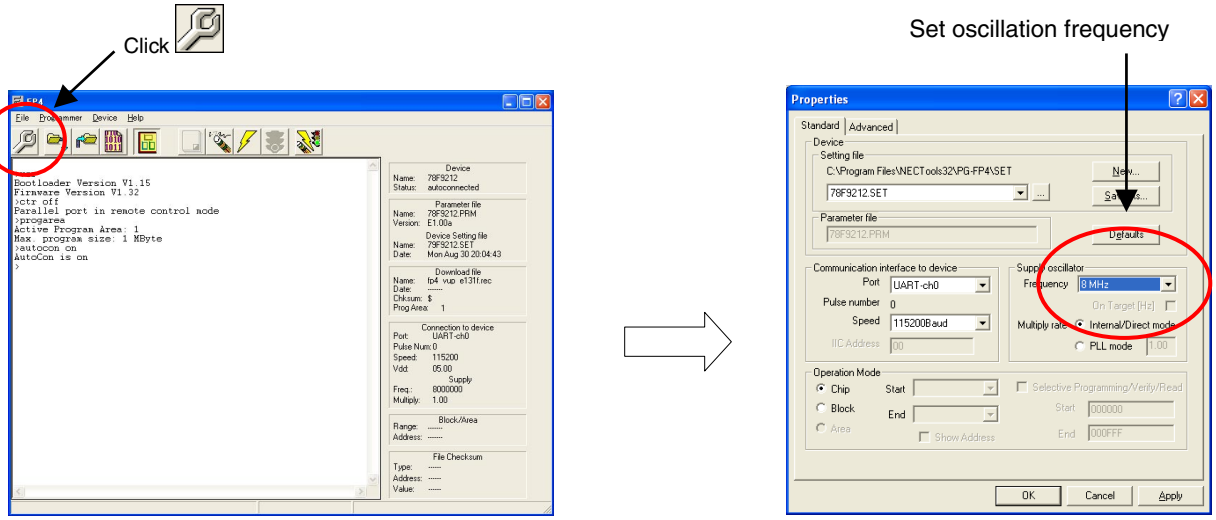


Table 16-6. Clock to Be Used and Mounting of Test Pads

Clock to Be Used		Mounting of Test Pads
High-speed Ring-OSC clock		Not required
External clock		
Crystal/ceramic oscillation clock	Before resonator is mounted	
	After resonator is mounted	Required

Figure 16-8. PG-FP4 GUI Software Setting Example



(Main window)

(Standard tab in Device setup window)

Table 16-7. Oscillation Frequency and PG-FP4 GUI Software Setting Value Example

Oscillation Frequency	PG-FP4 GUI Software Setting Value Example (Communication Frequency)
1 MHz ≤ fx < 4 MHz	8 MHz
4 MHz ≤ fx < 8 MHz	9 MHz
8 MHz ≤ fx < 9 MHz	10 MHz
9 MHz ≤ fx ≤ 10 MHz	8 MHz

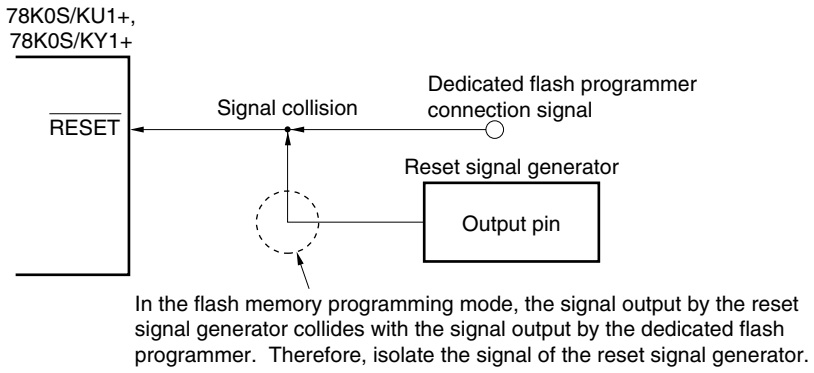
Caution The above setting values are under development, so they may be changed in the future.

16.6.2 $\overline{\text{RESET}}$ pin

If the reset signal of the dedicated flash programmer is connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board, signal collision takes place. To prevent this collision, isolate the connection with the reset signal generator.

If the reset signal is input from the user system while the flash memory programming mode is set, the flash memory will not be correctly programmed. Do not input any signal other than the reset signal of the dedicated flash programmer.

Figure 16-9. Signal Collision ($\overline{\text{RESET}}$ Pin)



16.6.3 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to V_{DD} or V_{SS} via a resistor.

The state of the pins in the self programming mode is the same as that in the HALT mode.

16.6.4 Power supply

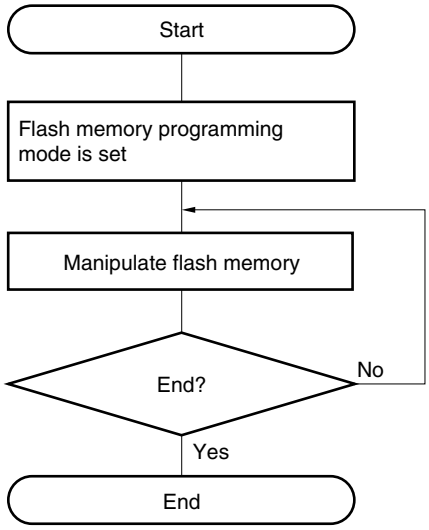
Connect the V_{DD} pin to V_{DD} of the flash programmer, and the V_{SS} pin to V_{SS} of the flash programmer.

16.7 On-Board and Off-Board Flash Memory Programming

16.7.1 Controlling flash memory

The following figure illustrates the procedure to manipulate the flash memory.

Figure 16-10. Flash Memory Manipulation Procedure



16.7.2 Flash memory programming mode

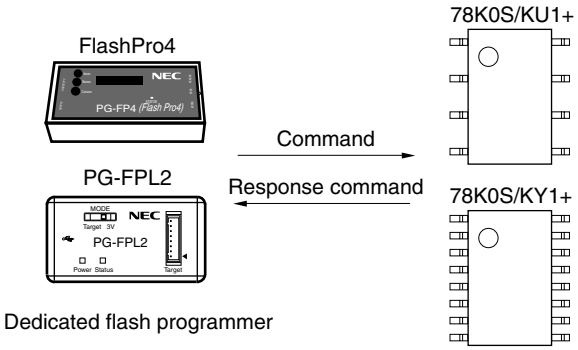
To rewrite the contents of the flash memory by using the dedicated flash programmer, set the 78K0S/KU1+ and 78K0S/KY1+ in the flash memory programming mode. When the 78K0S/KU1+ and 78K0S/KY1+ are connected to the flash programmer and a communication command is transmitted to the microcontroller, the microcontroller is set in the flash memory programming mode.

Change the mode by using a jumper when writing the flash memory on-board.

16.7.3 Communication commands

The 78K0S/KU1+ and 78K0S/KY1+ communicate with the dedicated flash programmer by using commands. The signals sent from the flash programmer to the 78K0S/KU1+ and 78K0S/KY1+ are called commands, and the commands sent from the 78K0S/KU1+ and 78K0S/KY1+ to the dedicated flash programmer are called response commands.

Figure 16-11. Communication Commands



The flash memory control commands of the 78K0S/KU1+ and 78K0S/KY1+ are listed in the table below. All these commands are issued from the programmer, 78K0S/KU1+, and 78K0S/KY1+ perform processing corresponding to the respective commands.

Table 16-8. Flash Memory Control Commands

Classification	Command Name	Function
Erase	Batch erase (chip erase) command	Erases the contents of the entire memory
	Block erase command	Erases the contents of the memory of the specified block
Write	Write command	Writes to the specified address range and executes a verify check of the contents.
Checksum	Checksum command	Reads the checksum of the specified address range and compares with the written data.
Blank check	Blank check command	Confirms the erasure status of the entire memory.
Security	Security set command	Prohibits batch erase (chip erase) command, block erase command, and write command to prevent operation by third parties.

The 78K0S/KU1+ and 78K0S/KY1+ return a response command for the command issued by the dedicated flash programmer. The response commands sent from the 78K0S/KU1+ and 78K0S/KY1+ are listed below.

Table 16-6. Response Commands

Command Name	Function
ACK	Acknowledges command/data.
NAK	Acknowledges illegal command/data.

16.7.4 Security settings

The operations shown below can be prohibited using the security setting command.

Caution The security setting is valid when the programming mode is set next time. Therefore, when the security setting command is executed, exit from the programming mode, then set the programming mode again.

- Batch erase (chip erase)
  Execution of the block erase and batch erase (chip erase) commands for entire blocks in the flash memory is prohibited. Once execution of the batch erase (chip erase) command is prohibited, all the prohibition settings can no longer be cancelled.

  Caution After the security setting of the batch erase is set, erasure cannot be performed for the device. In addition, even if a write command is executed, data different from that which has already been written to the flash memory cannot be written because the erase command is disabled.

- Block erase
  Execution of the block erase command for a specific block in the flash memory is prohibited. This prohibition setting can be cancelled using the batch erase (chip erase) command.

- Write
  Execution of the write and block erase commands for entire blocks in the flash memory is prohibited. This prohibition setting can be cancelled using the batch erase (chip erase) command.

The batch erase (chip erase), block erase, and write commands are enabled by the default setting when the flash memory is shipped. The above security settings are possible only for on-board/off-board programming. Each security setting can be used in combination.

Table 16-10 shows the relationship between the erase and write commands when the 78K0S/KU1+ and 78K0S/KY1+ security function is enabled.

Table 16-10. Relationship Between Commands When Security Function Is Enabled

Security \ Command	Batch Erase (Chip Erase) Command	Block Erase Command	Write Command
When batch erase (chip erase) security operation is enabled	Disabled	Disabled	Enabled[Note]
When block erase security operation is enabled	Enabled		Enabled
When write security operation is enabled			Disabled

Note Since the erase command is disabled, data different from that which has already been written to the flash memory cannot be written.

Table 16-11 shows the relationship between the security setting and the operation in each programming mode.

Table 16-11. Relationship Between Security Setting and Operation In Each Programming Mode

Programming Mode / Security Setting	On-Board/Off-Board Programming		Self Programming	
	Security Setting	Security Operation	Security Setting	Security Operation
Batch erase (chip erase)	Possible	Valid[Note 1]	Impossible	Invalid[Note 2]
Block erase				
Write				

Notes 1. Execution of each command is prohibited by the security setting.

2. Execution of self programming command is possible regardless of the security setting.

16.8 Flash Memory Programming by Self Writing

The 78K0S/KU1+ and 78K0S/KY1+ support a self programming function that can be used to rewrite the flash memory via a user program, making it possible to upgrade programs in the field.

Caution Self programming processing must be included in the program before performing self writing.

Remark To use the internal flash memory of the 78K0S/KU1+ and 78K0S/KY1+ as the external EEPROM for storing data, refer to “78K0S/Kx1+ EEPROM Emulation AN” (release schedule is undefined).

16.8.1 Outline of self programming

To execute self programming, shift the mode from the normal operation of the user program (normal mode) to the self programming mode. Write/erase processing for the flash memory, which has been set to the register in advance, is performed by executing the HALT instruction during self programming mode. The HALT state is automatically released when processing is completed.

To shift to the self programming mode, execute a specific sequence for a specific register. Refer to **16.8.4 Example of shifting normal mode to self programming** for details.

Remark Data written by self programming can be referenced with the MOV instruction.

Table 16-12. Self Programming Mode

Mode	User Program Execution	Execution of Write/erase for Flash Memory with HALT Instruction
Normal mode	Enabled	–
Self programming mode	Enabled[Note]	Enabled

Note Maskable interrupt servicing is disabled during self programming mode.

Figure 16-12 shows a block diagram for self programming, Figure 16-13 shows the self programming state transition diagram, Table 16-13 lists the commands for controlling self programming.

Figure 16-12. Block Diagram of Self Programming

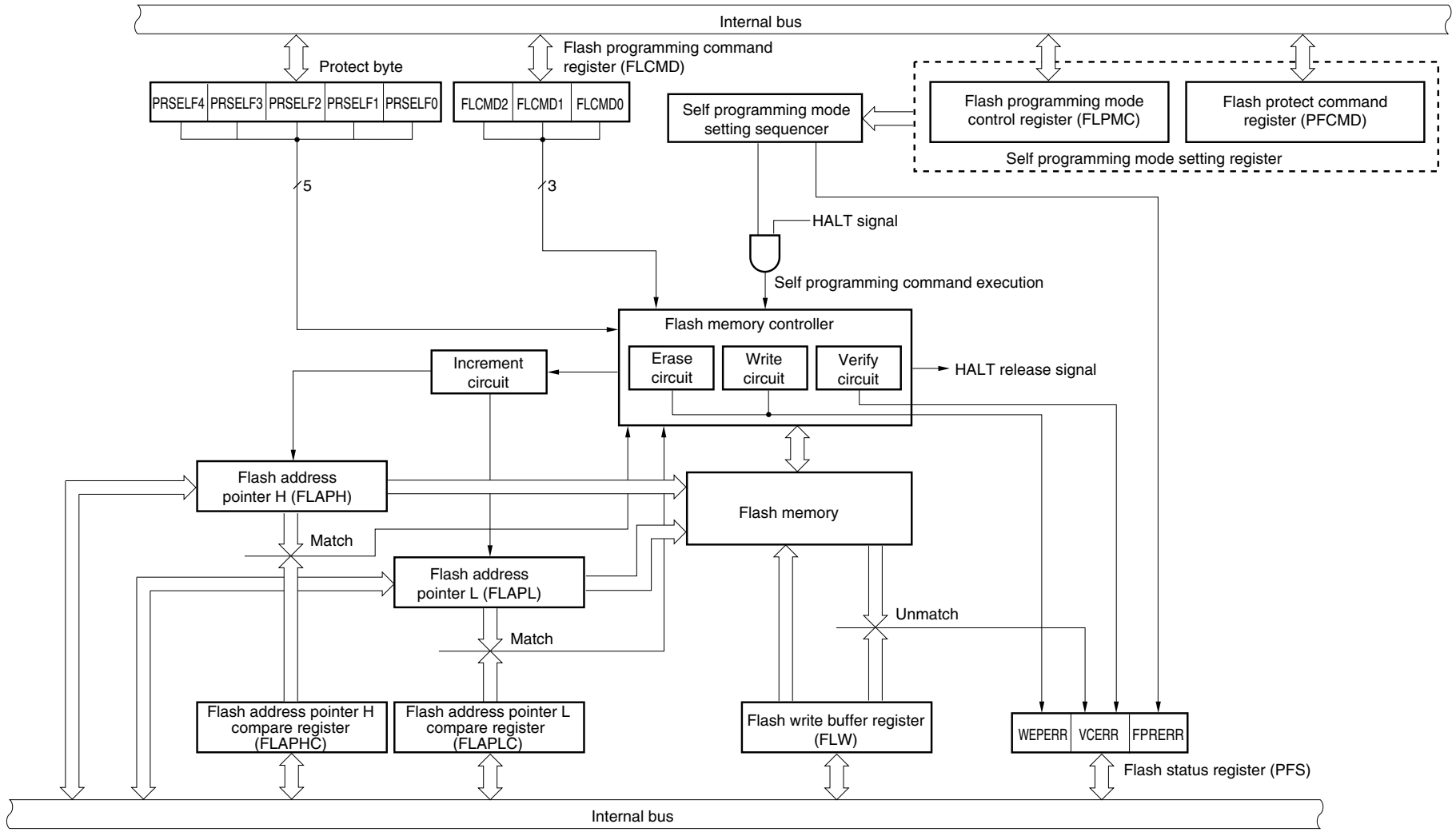


Figure 16-13. Self Programming State Transition Diagram

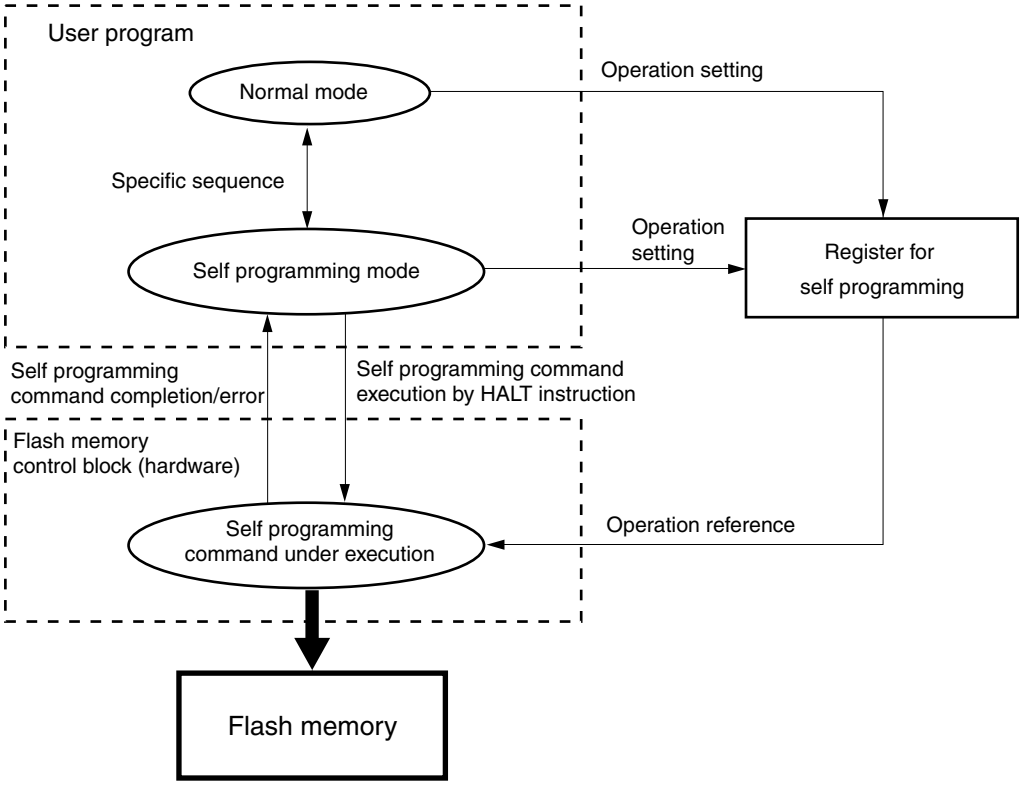


Table 16-13. Self Programming Controlling Commands

Command Name	Function	Time Taken from HALT Instruction Execution to Command Execution End
Internal verify	This command is used to check if data has been correctly written to the flash memory. After data has been written to the memory, specify the block number, the start address, and the end address, then execute this command.	Internal verify for 1 block (internal verify command executed once): 6.8 ms Internal verify for 1 byte: 27 μs
Block erasure	This command is used to erase a specified block. Specify the block number before execution.	8.5 ms
Block blank check	This command is used to check if data in a specified block has been erased. Specify the block number, then execute this command.	480 μs
Byte write	This command is used to write 1-byte data to the specified address in the flash memory. Specify the write address and write data, then execute this command.	150 μs

16.8.2 Cautions on self programming function

- If an interrupt occurs during self programming, the interrupt request flag is set (1), and interrupt servicing is performed after the self programming mode is released. To avoid this operation, disable interrupt servicing (by setting MK0 and MK1 to FFH, and executing the DI instruction) during self programming or before a mode is shifted from the normal mode to the self programming mode with a specific sequence.

- No instructions can be executed while a self programming command is being executed. Therefore, clear and restart the watchdog timer counter in advance so that the watchdog timer does not overflow during self programming. Refer to Table 16-13 for the time taken for the execution of self programming.
- RAM is not used while a self programming command is being executed.
- If the supply voltage drops or the reset signal is input while the flash memory is being written or erased, writing/erasing is not guaranteed.
- The value of the blank data set during block erasure is FFH.
- When the oscillator or the external clock is selected as the main clock, a wait time of 16 μs is required starting from the setting of the self programming mode to the execution of the HALT instruction.
- The state of the pins in self programming mode is the same as that in HALT mode.
- Since the security function set via on-board/off-board programming is disabled in self programming mode, the self programming command can be executed regardless of the security function setting. To disable write or erase processing during self programming, set the protect byte.
- Be sure to clear bits 4 to 7 of flash address pointer H (FLAPH) and flash address pointer H compare register (FLAPHC) to 0 before executing the self programming command. If the value of these bits is 1 when executing the self programming command.

16.8.3 Registers used for self-programming function

The following registers are used for the self-programming function.

- Flash programming mode control register (FLPMC)
- Flash protect command register (PFCMD)
- Flash status register (PFS)
- Flash programming command register (FLCMD)
- Flash address pointers H and L (FLAPH and FLAPL)
- Flash address pointer H compare register and flash address pointer L compare register (FLAPHC and FLAPLC)
- Flash write buffer register (FLW)

The 78K0S/KU1+ and 78K0S/KY1+ have an area called a protect byte at address 0081H of the flash memory.

(1) Flash programming mode control register (FLPMC)

This register is used to set the operation mode when data is written to the flash memory in the self-programming mode, and to read the set value of the protect byte.

Data can be written to FLPMC only in a specific sequence (refer to **16.8.3 (2) Flash protect command register (PFCMD)**) so that the application system does not stop by accident because of malfunction due to noise or program hang-up.

This register is set with an 8-bit memory manipulation instruction.

Reset input makes the contents of this register undefined.

Figure 16-14. Format of Flash Programming Mode Control Register (FLPMC)

Address: FFA2H After reset: Undefined[Note 1] R/W[Note 2]

Symbol	7	6	5	4	3	2	1	0
FLPMC	0	PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	0	FLSPM

FLSPM	Selection of operation mode during self-programming mode
0	Normal mode Flash memory instructions can be fetched from all addresses.
1	Self-programming mode Before executing the HALT instruction, set the command, address offset, write data, and set FLSPM to 1. After setting these items, execute the HALT instruction; the flash memory mode is then shifted from the normal mode to the flash memory programming mode.

PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	The set value of the protect byte is read to these bits.

Notes 1. Bit 0 (FLSPM) is cleared to 0 when reset is released. The set value of the protect byte is read to bits 2 to 6 (PRSELF0 to PRSELF4) after reset is released.

2. Bits 2 to 6 (PRSELF0 to PRSELF4) are read-only.

Cautions 1. Note the following when setting the self programming mode.

- **If an interrupt occurs during self programming, the interrupt request flag is set (1), and interrupt servicing is performed after the self programming mode is released. To avoid this operation, disable interrupt servicing (by setting MK0 to FFH, and executing the DI instruction) during self programming or before a mode is shifted from the normal mode to the self programming mode with a specific sequence.**
- **No instructions can be executed while a self programming command is being executed. Therefore, clear and restart the watchdog timer counter in advance so that the watchdog timer does not overflow during self programming. Refer to Table 16-13 for the time taken for the execution of self programming.**
- **If the supply voltage drops or the reset signal is input while the flash memory is being written or erased, writing/erasing is not guaranteed.**

2. When the oscillator or the external clock is selected as the main clock, a wait time of 16 μs is required from setting FLSPM to 1 to execution of the HALT instruction.

(2) Flash protect command register (PFCMD)

If the application system stops inadvertently due to malfunction caused by noise or program hang-up, an operation to write the flash programming mode control register (FLPMC) may have a serious effect on the system. PFCMD is used to protect FLPMC from being written, so that the application system does not stop inadvertently.

Writing FLPMC is enabled only when a write operation is performed in the following specific sequence.

<1> Write a specific value to PFCMD (PFCMD = A5H)
<2> Write the value to be set to FLPMC (writing in this step is invalid)
<3> Write the inverted value of the value to be set to FLPMC (writing in this step is invalid)
<4> Write the value to be set to FLPMC (writing in this step is valid)

This rewrites the value of the register, so that the register cannot be written illegally.
Occurrence of an illegal store operation can be checked by bit 0 (FPRERR) of the flash status register (PFS).
A5H must be written to PFCMD each time the value of FLPMC is changed.
PFCMD can be set by an 8-bit memory manipulation instruction.
Reset input makes PFCMD undefined.

Figure 16-15. Format of Flash Protect Command Register (PFCMD)

Address: FFA0H After reset: Undefined W

Symbol	7	6	5	4	3	2	1	0
PFCMD	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0

Caution Disable interrupt servicing (by setting MK0 to FFH and executing the DI instruction) while the specific sequence is under execution.

(3) Flash status register (PFS)

If data is not written to the flash programming mode control register (FLPMC), which is protected, in the correct sequence (writing the flash protect command register (PFCMD)), FLPMC is not written and a protection error occurs. If this happens, bit 0 of PFS (FPRERR) is set to 1.
When FPRERR is 1, it can be cleared to 0 by writing 0 to it.
Errors that may occur during self-programming are reflected in bit 1 (VCERR) and bit 2 (WEPRERR) of PFS.
VCERR or WEPRERR can be cleared by writing 0 to them.
All the flags of the PFS register must be pre-cleared to 0 to check if the operation is performed correctly.
PFS can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset input clears PFS to 00H.

Figure 16-16. Format of Flash Status Register (PFS)

Address: FFA1H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PFS	0	0	0	0	0	WEPRERR	VCERR	FPRERR

1. Operating conditions of FPRERR flag

<Setting conditions>

- If PFCMD is written when the store instruction operation recently performed on a peripheral register is not to write a specific value (A5H) to PFCMD
- If the first store instruction operation after <1> is on a peripheral register other than FLPMC
- If the first store instruction operation after <2> is on a peripheral register other than FLPMC
- If a value other than the inverted value of the value to be set to FLPMC is written by the first store instruction after <2>
- If the first store instruction operation after <3> is on a peripheral register other than FLPMC
- If a value other than the value to be set to FLPMC (value written in <2>) is written by the first store instruction after <3>

Remark The numbers in angle brackets above correspond to the those in **(2) Flash protect command register (PFCMD)**.

<Reset conditions>

- If 0 is written to the FPRERR flag
- If the reset signal is input

2. Operating conditions of VCERR flag

<Setting conditions>

- Erasure verification error
- Internal writing verification error

If VCERR is set, it means that the flash memory has not been erased or written correctly. Erase or write the memory again in the specified procedure.

Remark The VCERR flag may also be set if an erase or write protect error occurs.

<Reset conditions>

- When 0 is written to the VCERR flag
- When the reset signal is input

3. Operating conditions of WEPRERR flag

<Setting conditions>

- If the area specified by the protect byte to be protected from erasing or writing is specified by the flash address pointer H (FLAPH) and a command is executed to this area

<Reset conditions>

- When 0 is written to the WEPRERR flag
- When the reset signal is input

(4) Flash programming command register (FLCMD)

This register is used to specify whether the flash memory is erased, written, or verified in the self-programming mode.

This register is set by using a 1-bit or 8-bit memory manipulation instruction.

Reset input clears this register to 00H.

Figure 16-17. Format of Flash Programming Command Register (FLCMD)

Address: FFA3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
FLCMD	0	0	0	0	0	FLCMD2	FLCMD1	FLCMD0

FLCMD2	FLCMD1	FLCMD0	Command Name	Function
0	0	1	Internal verify	This command is used to check if data has been correctly written to the flash memory. After data has been written to the memory, execute this command by specifying a block number, start address, and end address. If an error occurs, bit 1 (VCERR) or bit 2 (WEPRERR) of the flash status register (PFS) is set to 1.
0	1	1	Block erase	This command is used to erase specified block. It is used both in the on-board mode and self-programming mode.
1	0	0	Block blank check	This command is used to check if the specified block has been erased.
1	0	1	Byte write	This command is used to write 1-byte data to the specified address in the flash memory. Specify the write address and write data, then execute this command.
Other than above[Note]			Setting prohibited	

Note If a value other than the above is set and the self programming mode is set, the self programming mode is canceled immediately and no execution occurs. At this time, the flag of the PFS register is not set.

(5) Flash address pointers H and L (FLAPH and FLAPL)

These registers are used to specify the start address of the flash memory when the memory is erased, written, or verified in the self-programming mode.

FLAPH and FLAPL consist of counters, and they are incremented until the values match with those of FLAPHC and FLAPLC when the programming command is not executed. When the programming command is executed, therefore, set the value again.

These registers are set with a 1-bit or 8-bit memory manipulation instruction.

Reset input makes these registers undefined.

Figure 16-18. Format of Flash Address Pointer H/L (FLAPH/FLAPL)

Address: FFA4H, FFA5H After reset: 00H R/W

FLAPH (FFA5H)								FLAPL (FFA4H)							
0	0	0	0	FLAP11	FLAP10	FLAP9	FLAP8	FLAP7	FLAP6	FLAP5	FLAP4	FLAP3	FLAP2	FLAP1	FLAP0

Caution Be sure to clear bits 4 to 7 of FLAPH and FLAPHC to 0 before executing the self programming command. If the value of these bits is 1 when executing the self programming command.

(6) Flash address pointer H compare register and flash address pointer L compare register (FLAPHC and FLAPLC)

These registers are used to specify the address range in which the internal sequencer operates when the flash memory is verified in the self-programming mode.

Set FLAPHC to the same value as that of FLAPH. Set the last address of the range in which verification is to be executed to FLAPLC.

These registers are set by a 1-bit or 8-bit memory manipulation instruction.

Reset input clears these registers to 00H.

Figure 16-19. Format of Flash Address Pointer H/L Compare Registers (FLAPHC/FLAPLC)

Address: FFA6H, FFA7H After reset: 00H R/W

FLAPHC (FFA7H)								FLAPLC (FFA6H)							
0	0	0	0	FLAPC11	FLAPC10	FLAPC9	FLAPC8	FLAPC7	FLAPC6	FLAPC5	FLAPC4	FLAPC3	FLAPC2	FLAPC1	FLAPC0

Cautions 1. Be sure to clear bits 4 to 7 of FLAPH and FLAPHC to 0 before executing the self programming command. If the value of these bits is 1 when executing the self programming command.

2. Set the number of the block subject to a block erase, write, verify, or blank check (same value as FLAPH) to FLAPHC.

3. Clear FLAPLC to 00H when a block erase is performed, and set this register to FFH when a blank check is performed.

(7) Flash write buffer register (FLW)

This register is used to store the data to be written to the flash memory.

This register is set with an 8-bit memory manipulation instruction.

Reset input clears these registers to 00H.

Figure 16-20. Format of Flash Write Buffer Register (FLW)

Address: FFA8H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
FLW	FLW7	FLW6	FLW5	FLW4	FLW3	FLW2	FLW1	FLW0

(8) Protect byte

This protect byte is used to specify the area that is to be protected from writing or erasing. The specified area is valid only in the self-programming mode. Because self-programming of the protected area is invalid, the data written to the protected area is guaranteed.

Figure 16-21. Format of Protect Byte (1/2)

Address: 0081H

7	6	5	4	3	2	1	0
1	PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	1	1

• μPD78F9200, 78F9210

PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	Status
0	1	1	1	0	Blocks 3 to 0 are protected.
0	1	1	1	1	Blocks 1 and 0 are protected. Blocks 2 and 3 can be written or erased.
1	1	1	1	1	All blocks can be written or erased.
Other than above					Setting prohibited

• μPD78F9201, 78F9211

PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	Status
0	1	1	0	0	Blocks 7 to 0 are protected.
0	1	1	0	1	Blocks 5 to 0 are protected. Blocks 6 and 7 can be written or erased.
0	1	1	1	0	Blocks 3 to 0 are protected. Blocks 4 to 7 can be written or erased.
0	1	1	1	1	Blocks 1 and 0 are protected. Blocks 2 to 7 can be written or erased.
1	1	1	1	1	All blocks can be written or erased.
Other than above					Setting prohibited

Figure 16-21. Format of Protect Byte (2/2)

• μPD78F9202, 78F9212

PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	Status
0	1	0	0	0	Blocks 15 to 0 are protected.
0	1	0	0	1	Blocks 13 to 0 are protected. Blocks 14 and 15 can be written or erased.
0	1	0	1	0	Blocks 11 to 0 are protected. Blocks 12 to 15 can be written or erased.
0	1	0	1	1	Blocks 9 to 0 are protected. Blocks 10 to 15 can be written or erased.
0	1	1	0	0	Blocks 7 to 0 are protected. Blocks 8 to 15 can be written or erased.
0	1	1	0	1	Blocks 5 to 0 are protected. Blocks 6 to 15 can be written or erased.
0	1	1	1	0	Blocks 3 to 0 are protected. Blocks 4 to 15 can be written or erased.
0	1	1	1	1	Blocks 1 and 0 are protected. Blocks 2 to 15 can be written or erased.
1	1	1	1	1	All blocks can be written or erased.
Other than above					Setting prohibited

16.8.4 Example of shifting normal mode to self programming mode

The operating mode must be shifted from normal mode to self programming mode before performing self programming.

An example of shifting to self programming mode is explained below.

<1> Disable interrupts if the interrupt function is used (by setting the interrupt mask flag registers (MK0) to FFH and executing the DI instruction).

<2> Clear the flash status register (PFS).

<3> Set self programming mode using a specific sequence.

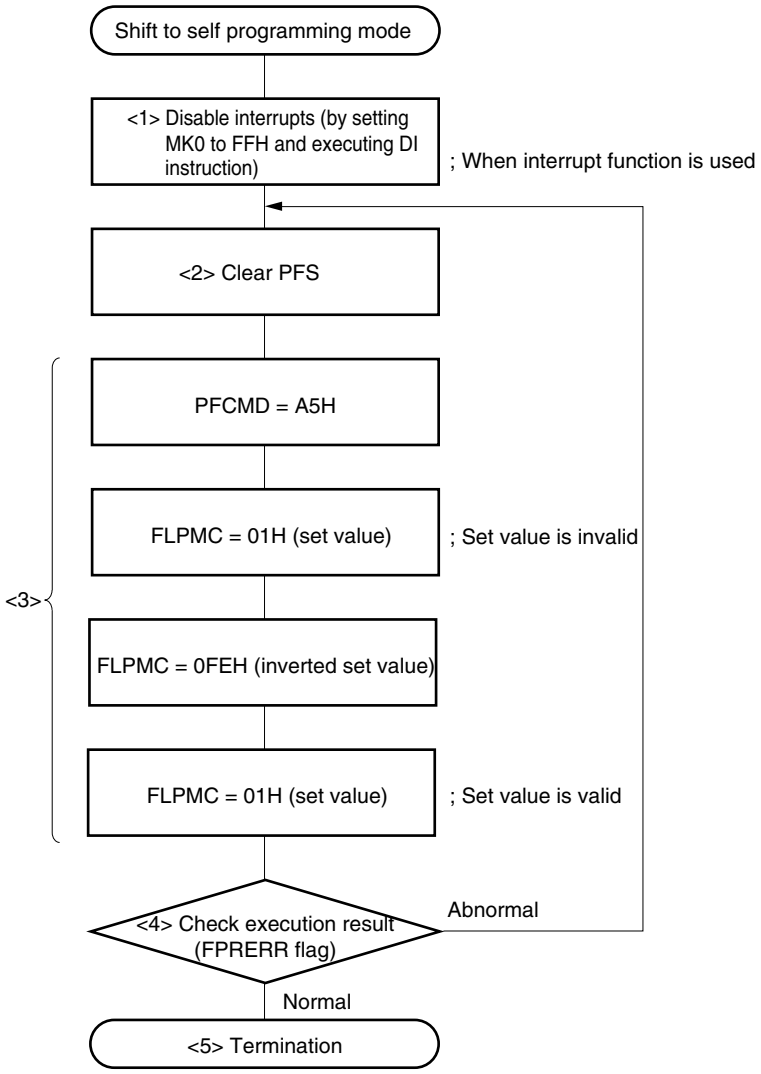
- Write a specific value (A5H) to PFCMD.
- Write 01H to FLPMC (writing in this step is invalid).
- Write 0FEH (inverted value of 01H) to FLPMC (writing in this step is invalid).
- Write 01H to FLPMC (writing in this step is valid).

<4> Check the execution result of the specific sequence using bit 0 (FPRERR) of PFS.
Abnormal → <2>, normal → <5>

<5> Mode shift is completed.

Caution Be sure to perform the series of operations described above using the user program at an address where data is not erased nor written.

Figure 16-22. Example of Shifting to Self Programming Mode



Caution Be sure to perform the series of operations described above using the user program at an address where data is not erased nor written.

Remark <1> to <5> in Figure 16-22 correspond to <1> to <5> in **16.8.4** (previous page).

An example of the program list that shifts the mode to self programming mode is shown below.

```
;----------------------------
;START
;----------------------------
       MOV      MK0,#11111111B     ; Masks all interrupts

       DI

ModeOnLoop:
       MOV      PFS,#00H
       MOV      PFCMD,#0A5H        ; PFCMD register control
       MOV      FLPMC,#01H         ; FLPMC register control (sets value)
       MOV      FLPMC,#0FEH        ; FLPMC register control (inverts set value)
       MOV      FLPMC,#01H         ; Sets self programming mode with FLPMC register
                                   ; control (sets value)

       MOV      A,PFS
       CMP      A,#00H
       BNZ      $ModeOnLoop        ; Checks completion of write to specific registers
                                   ; Repeats the same processing when an error occurs.

;----------------------------
;END
;----------------------------
```

16.8.5 Example of shifting self programming mode to normal mode

The operating mode must be returned from self programming mode to normal mode after performing self programming.

An example of shifting to normal mode is explained below.

<1> Clear the flash status register (PFS).

<2> Set normal mode using a specific sequence.

- Write the specific value (A5H) to PFCMD.
- Write 00H to FLPMC (writing in this step is invalid)
- Write 0FFH (inverted value of 00H) to FLPMC (writing in this step is invalid)
- Write 00H to FLPMC (writing in this step is valid)

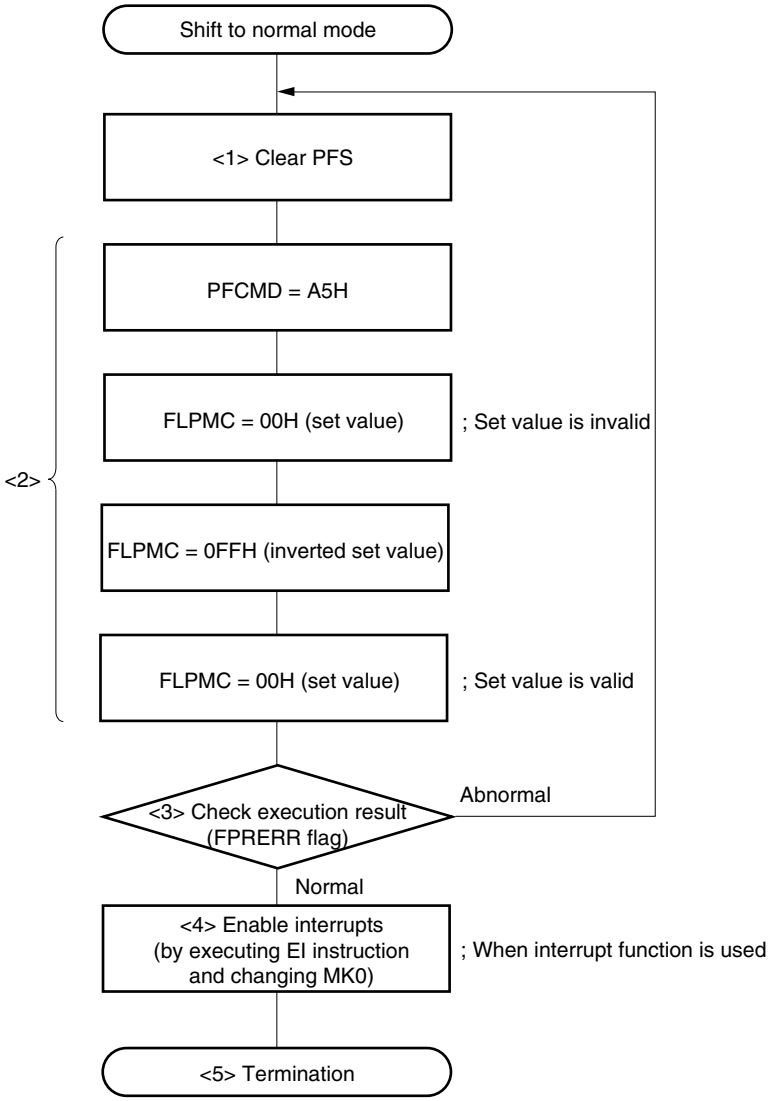
<3> Check the execution result of the specific sequence using bit 0 (FPRERR) of PFS.
Abnormal → <1>, normal → <4>

<4> Enable interrupt servicing (by executing the EI instruction and changing MK0) to restore the original state.

<5> Mode shift is completed

Caution Be sure to perform the series of operations described above using the user program at an address where data is not erased nor written.

Figure 16-23. Example of Shifting to Normal Mode



Caution Be sure to perform the series of operations described above using the user program at an address where data is not erased nor written.

Remark <1> to <5> in Figure 16-23 correspond to <1> to <5> in **16.8.5** (previous page).

An example of a program list that shifts the mode to normal mode is shown below.

```
;----------------------------
;START
;----------------------------

ModeOffLoop:
       MOV      PFS,#00H
       MOV      PFCMD,#0A5H       ; PFCMD register control
       MOV      FLPMC,#00H        ; FLPMC register control (sets value)
       MOV      FLPMC,#0FFH       ; FLPMC register control (inverts set value)
       MOV      FLPMC,#00H        ; Sets normal mode via FLPMC register control (sets value)

       MOV      A,PFS
       CMP      A,#00H
       BNZ      $ModeOffLoop      ; Checks completion of write to specific registers
                                  ; Repeats the same processing when an error occurs

       MOV      MK0,#INT_MK0      ; Restores interrupt mask flag

       EI

;----------------------------
;END
;----------------------------
```

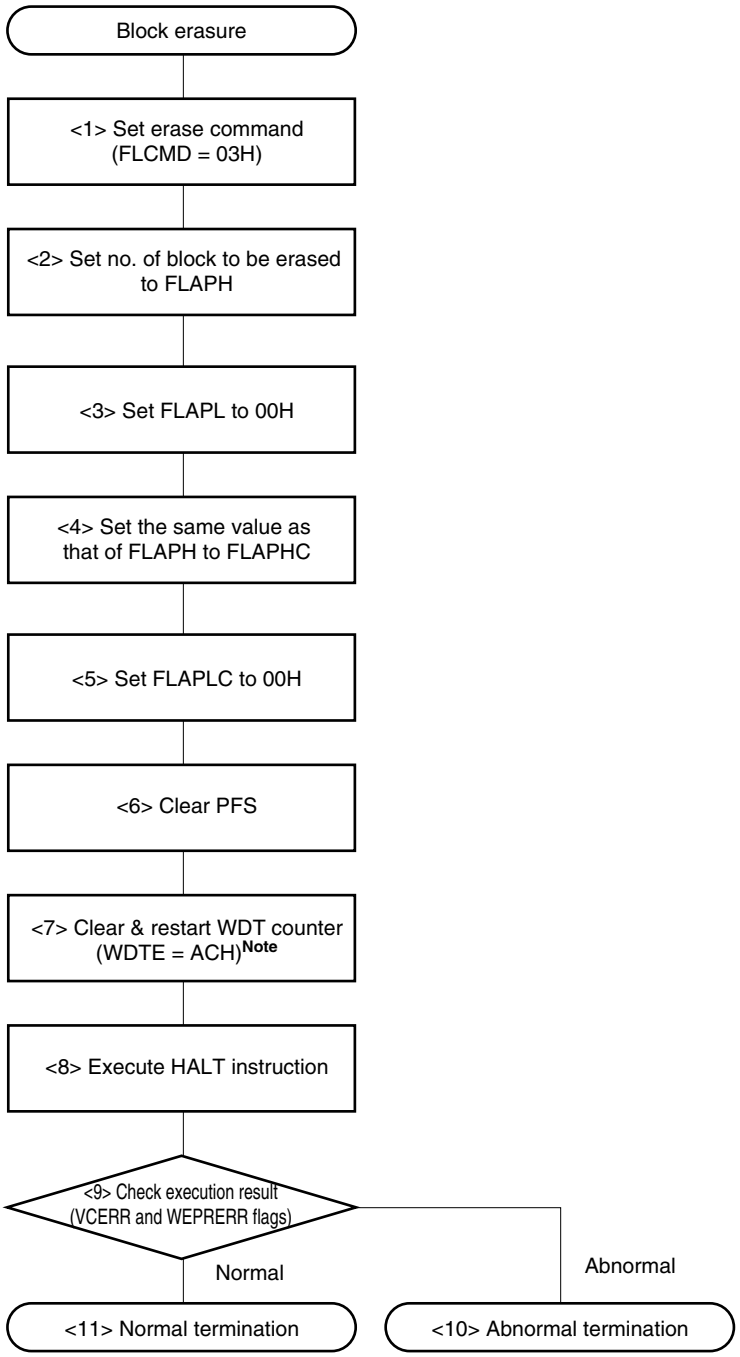
16.8.6 Example of block erase operation in self programming mode

An example of the block erase operation in self programming mode is explained below.

<1> Set 03H (block erase) to the flash program command register (FLCMD).
<2> Set the block number to be erased, to flash address pointer H (FLAPH).
<3> Set flash address pointer L (FLAPL) to 00H.
<4> Write the same value as FLAPH to the flash address pointer H compare register (FLAPHC).
<5> Set the flash address pointer L compare register (FLAPLC) to 00H.
<6> Clear the flash status register (PFS).
<7> Write ACH to the watchdog timer enable register (WDTE) (clear and restart the watchdog timer counter)[Note].
<8> Execute the HALT instruction then start self programming. (Execute an instruction immediately after the HALT instruction if self programming has been executed.)
<9> Check if a self programming error has occurred using bit 1 (VCERR) and bit 2 (WEPRERR) of PFS.
Abnormal → <10>
Normal → <11>
<10> Block erase processing is abnormally terminated.
<11> Block erase processing is normally terminated.

Note This setting is not required when the watchdog timer is not used.

Figure 16-24. Example of Block Erase Operation in Self Programming Mode



Note This setting is not required when the watchdog timer is not used.

Remark <1> to <11> in Figure 16-24 correspond to <1> to <11> in **16.8.6** (previous page).

An example of a program list that performs a block erase in self programming mode is shown below.

```
;----------------------------
;START
;----------------------------

FlashBlockErase:
       MOV      FLCMD,#03H     ; Sets flash control command (block erase)
       MOV      FLAPH,#07H     ; Sets number of block to be erased (block 7 is specified here)
       MOV      FLAPL,#00H     ; Fixes FLAPL to "00H"
       MOV      FLAPHC,#07H    ; Sets erase block compare number (same value as that of FLAPH)
       MOV      FLAPLC,#00H    ; Fixes FLAPLC to "00H"

       MOV      PFS,#00H       ; Clears flash status register
       MOV      WDTE,#0ACH     ; Clears & restarts WDT
       HALT                    ; Self programming is started
       MOV      A,PFS
       MOV      CmdStatus,A    ; Execution result is stored in variable
                               ; (CmdStatus = 0: normal termination, other than 0: abnormal
                               ; termination)

;----------------------------
;END
;----------------------------
```

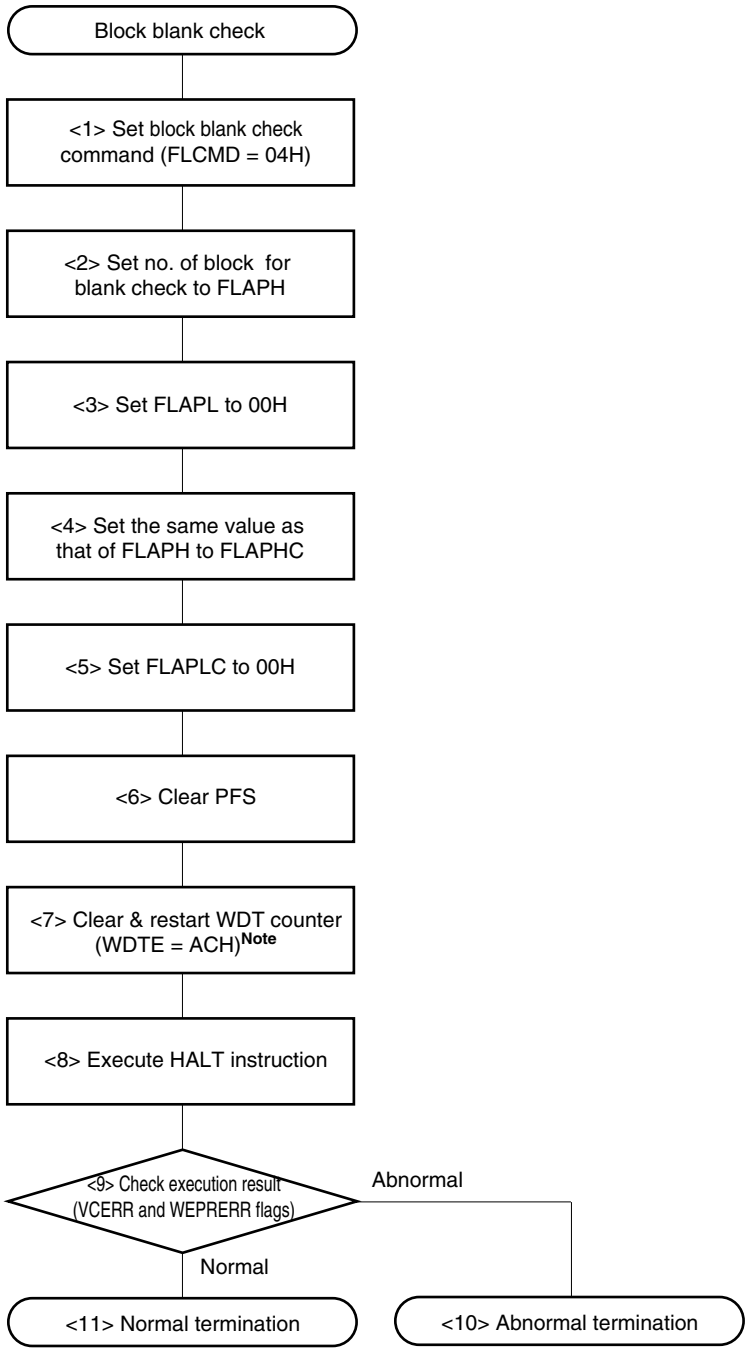
16.8.7 Example of block blank check operation in self programming mode

An example of the block blank check operation in self programming mode is explained below.

<1> Set 04H (block blank check) to the flash program command register (FLCMD).
<2> Set the number of block for which a blank check is performed, to flash address pointer H (FLAPH).
<3> Set flash address pointer L (FLAPL) to 00H.
<4> Write the same value as FLAPH to the flash address pointer H compare register (FLAPHC).
<5> Set the flash address pointer L compare register (FLAPLC) to FFH.
<6> Clear the flash status register (PFS).
<7> Write ACH to the watchdog timer enable register (WDTE) (clear and restart the watchdog timer counter)[Note].
<8> Execute the HALT instruction then start self programming. (Execute an instruction immediately after the HALT instruction if self programming has been executed.)
<9> Check if a self programming error has occurred using bit 1 (VCERR) and bit 2 (WEPRERR) of PFS.
Abnormal → <10>
Normal → <11>
<10> Block blank check is abnormally terminated.
<11> Block blank check is normally terminated.

Note This setting is not required when the watchdog timer is not used.

Figure 16-25. Example of Block Blank Check Operation in Self Programming Mode



Note This setting is not required when the watchdog timer is not used.

Remark <1> to <11>in Figure 16-25 correspond to <1> to <11> in **16.8.7** (previous page).

An example of a program list that performs a block blank check in self programming mode is shown below.

```
;----------------------------
;START
;----------------------------

FlashBlockBlankCheck:
       MOV      FLCMD,#04H      ; Sets flash control command (block blank check)
       MOV      FLAPH,#07H      ; Sets number of block for blank check (block 7 is specified
                                ; here)
       MOV      FLAPL,#00H      ; Fixes FLAPL to "00H"
       MOV      FLAPHC,#07H     ; Sets blank check block compare number (same value as that of
                                ; FLAPH)
       MOV      FLAPLC,#0FFH    ; Fixes FLAPLC to "FFH"

       MOV      PFS,#00H        ; Clears flash status register
       MOV      WDTE,#0ACH      ; Clears & restarts WDT
       HALT                     ; Self programming is started
       MOV      A,PFS
       MOV      CmdStatus,A     ; Execution result is stored in variable
                                ; (CmdStatus = 0: normal termination, other than 0: abnormal
                                ; termination)

;----------------------------
;END
;----------------------------
```

16.8.8 Example of byte write operation in self programming mode

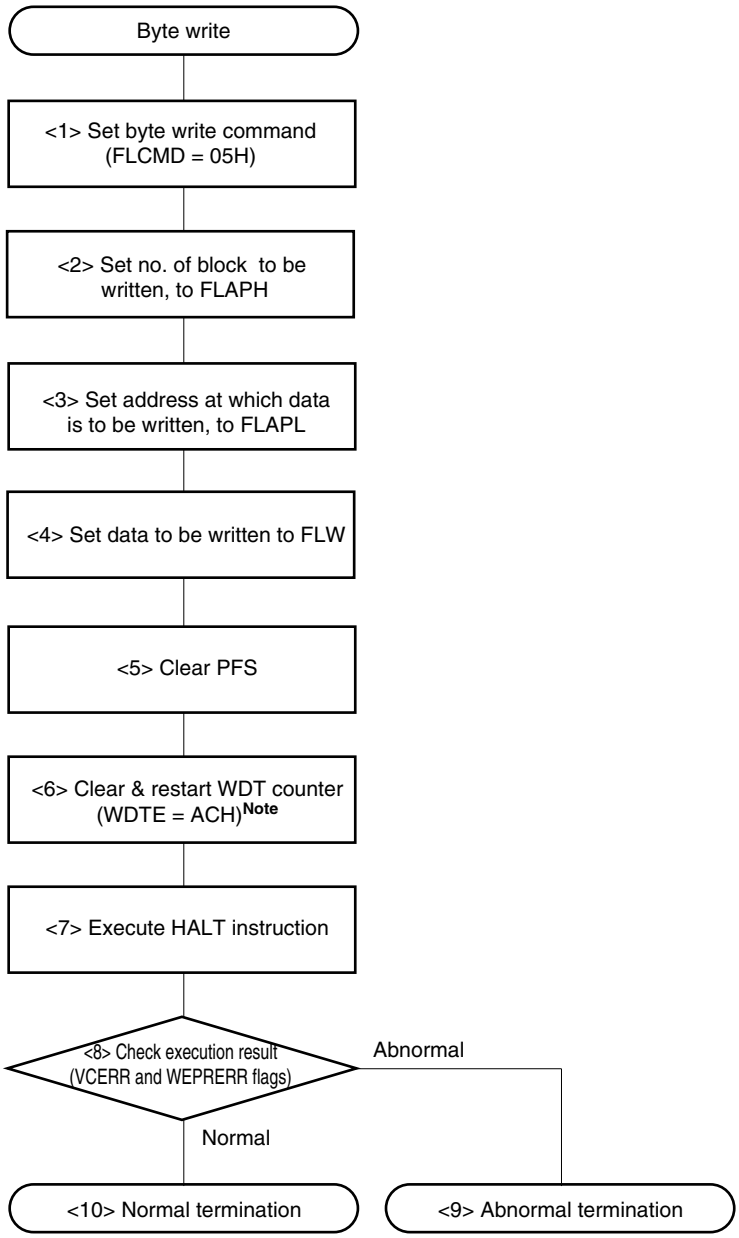
An example of the byte write operation in self programming mode is explained below.

<1> Set 05H (byte write) to the flash program command register (FLCMD).
<2> Set the number of block to which data is to be written, to flash address pointer H (FLAPH).
<3> Set the address at which data is to be written, to flash address pointer L (FLAPL).
<4> Set the data to be written, to the flash write buffer register (FLW).
<5> Clear the flash status register (PFS).
<6> Write ACH to the watchdog timer enable register (WDTE) (clear and restart the watchdog timer counter)[Note].
<7> Execute the HALT instruction then start self programming. (Execute an instruction immediately after the HALT instruction if self programming has been executed.)
<8> Check if a self programming error has occurred using bit 1 (VCERR) and bit 2 (WEPRERR) of PFS.
Abnormal → <9>
Normal → <10>
<9> Byte write processing is abnormally terminated.
<10> Byte write processing is normally terminated.

Note This setting is not required when the watchdog timer is not used.

Caution If a write results in failure, erase the block once and write to it again.

Figure 16-26. Example of Byte Write Operation in Self Programming Mode



Note This setting is not required when the watchdog timer is not used.

Remark <1> to <10> in Figure 16-26 correspond to <1> to <10> in **16.8.8** (previous page).

An example of a program list that performs a byte write in self programming mode is shown below.

```
;----------------------------
;START
;----------------------------
FlashWrite:
       MOV      FLCMD,#05H      ; Sets flash control command (byte write)
       MOV      FLAPH,#07H      ; Sets address to which data is to be written, with
                                ; FLAPH (block 7 is specified here)
       MOV      FLAPL,#20H      ; Sets address to which data is to be written, with
                                ; FLAPL (address 20H is specified here)
       MOV      FLW,#10H        ; Sets data to be written (10H is specified here)

       MOV      PFS,#00H        ; Clears flash status register
       MOV      WDTE,#0ACH      ; Clears & restarts WDT
       HALT                     ; Self programming is started
       MOV      A,PFS
       MOV      CmdStatus,A     ; Execution result is stored in variable
                                ; (CmdStatus = 0: normal termination, other than 0: abnormal
                                ; termination)

;----------------------------
;END
;----------------------------
```

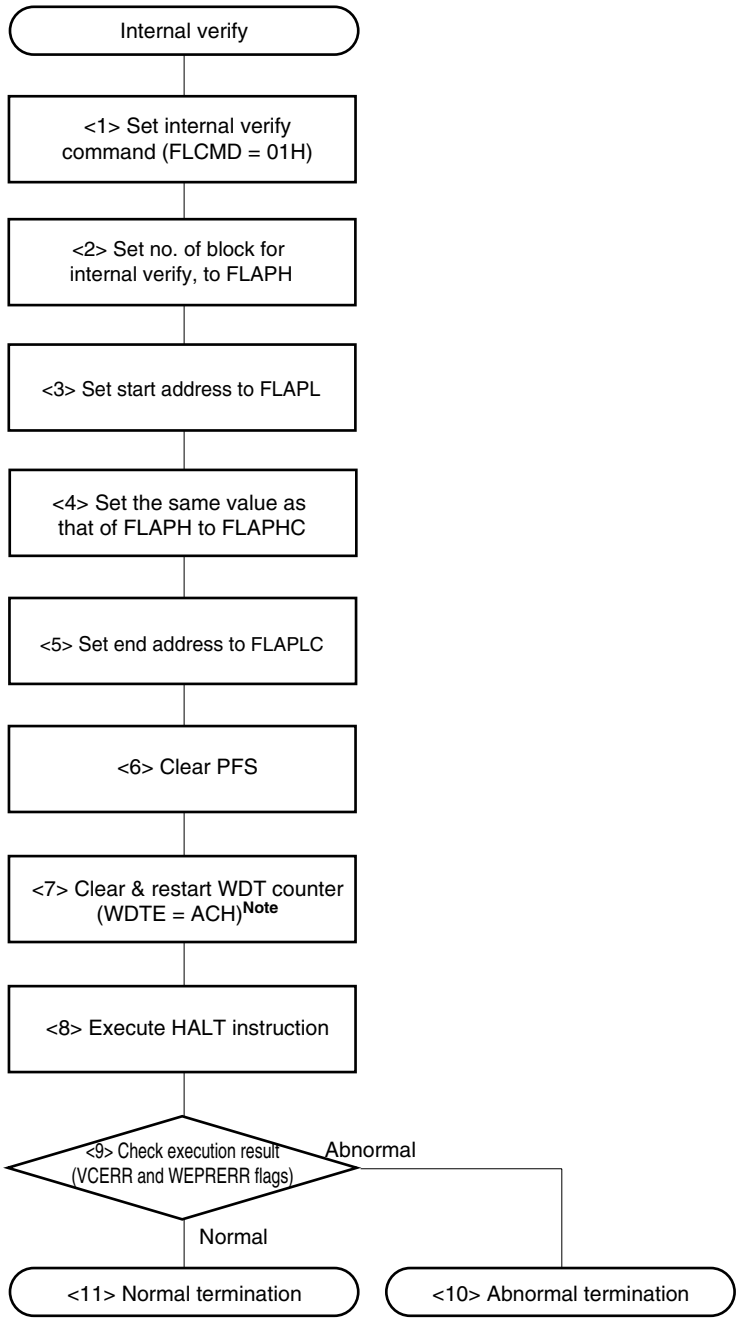
16.8.9 Example of internal verify operation in self programming mode

An example of the internal verify operation in self programming mode is explained below.

<1> Set 01H (internal verify) to the flash program command register (FLCMD).
<2> Set the number of block for which internal verify is performed, to flash address pointer H (FLAPH).
<3> Sets the verify start address to flash address pointer L (FLAPL).
<4> Write the same value as that of FLAPH to the flash address pointer H compare register (FLAPHC).
<5> Sets the verify end address to the flash address pointer L compare register (FLAPLC).
<6> Clear the flash status register (PFS).
<7> Write ACH to the watchdog timer enable register (WDTE) (clear and restart the watchdog timer counter)[Note].
<8> Execute the HALT instruction then start self programming. (Execute an instruction immediately after the HALT instruction if self programming has been executed.)
<9> Check if a self programming error has occurred using bit 1 (VCERR) and bit 2 (WEPRERR) of PFS.
Abnormal → <10>
Normal → <11>
<10> Internal verify processing is abnormally terminated.
<11> Internal verify processing is normally terminated.

Note This setting is not required when the watchdog timer is not used.

Figure 16-27. Example of Internal Verify Operation in Self Programming Mode



Note This setting is not required when the watchdog timer is not used.

Remark <1> to <11> in Figure 16-27 correspond to <1> to <11> in **16.8.9** (previous page).

An example of a program list that performs an internal verify in self programming mode is shown below.

```
;----------------------------
;START
;----------------------------
FlashVerify:
       MOV      FLCMD,#01H      ; Sets flash control command (internal verify)
       MOV      FLAPH,#07H      ; Sets verify start address with FLAPH (block 7 is specified
                                ; here)
       MOV      FLAPL,#00H      ; Sets verify start address with FLAPL (Address 00H is
                                ; specified here)
       MOV      FLAPHC,#07H
       MOV      FLAPLC,#20H     ; Sets verify end address

       MOV      PFS,#00H        ; Clears flash status register
       MOV      WDTE,#0ACH      ; Clears & restarts WDT
       HALT                     ; Self programming is started
       MOV      A,PFS
       MOV      CmdStatus,A     ; Execution result is stored in variable
                                ; (CmdStatus = 0: normal termination, other than 0: abnormal
                                ; termination)

;----------------------------
;END
;----------------------------
```

16.8.10 Examples of operation when command execution time should be minimized in self programming mode

Examples of operation when the command execution time should be minimized in self programming mode are explained below.

(1) Erasure to blank check

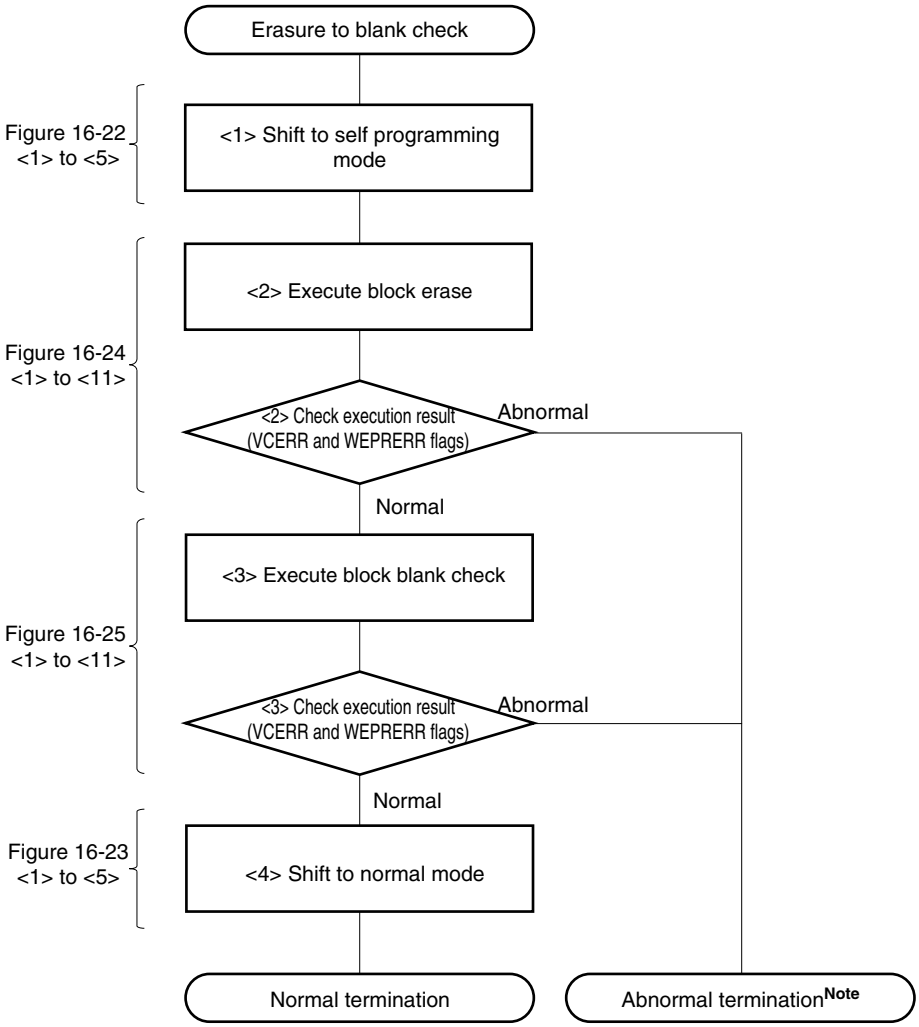
<1> Mode is shifted from normal mode to self programming mode (<1> to <5> in **16.8.4**)

<2> Execution of block erase → Error check (<1> to <11> in **16.8.6**)

<3> Execution of block blank check → Error check (<1> to <11> in **16.8.7**)

<4> Mode is shifted from self programming mode to normal mode (<1> to <5> in **16.8.5**)

Figure 16-28. Example of Operation When Command Execution Time Should Be Minimized (from Erasure to Blank Check)



Note Perform processing to shift to normal mode in order to return to normal processing.

Remark <1> to <4> in Figure 16-28 correspond to <1> to <4> in **16.8.10 (1)** above.

An example of a program list when the command execution time (from erasure to black check) should be minimized in self programming mode is shown below.

```
;---------------------------------------------------------------------
;START
;---------------------------------------------------------------------
       MOV      MK0,#11111111B   ; Masks all interrupts

       DI

ModeOnLoop:
       MOV      PFS,#00H
       MOV      PFCMD,#0A5H      ; PFCMD register control
       MOV      FLPMC,#01H       ; FLPMC register control (sets value)
       MOV      FLPMC,#0FEH      ; FLPMC register control (inverts set value)
       MOV      FLPMC,#01H       ; Sets self programming mode with FLPMC register control (sets
                                 ; value)

       MOV      A,PFS
       CMP      A,#00H
       BNZ      $ModeOnLoop      ; Checks completion of write to specific registers
                                 ; Repeats the same processing when an error occurs

FlashBlockErase:
       MOV      FLCMD,#03H       ; Sets flash control command (block erase)
       MOV      FLAPH,#07H       ; Sets number of block to be erased (block 7 is specified
                                 ; here)
       MOV      FLAPL,#00H       ; Fixes FLAPL to "00H"
       MOV      FLAPHC,#07H      ; Sets erase block compare number (same value as that of
                                 ; FLAPH)
       MOV      FLAPLC,#00H      ; Fixes FLAPLC to "00H"

       MOV      PFS,#00H         ; Clears flash status register
       MOV      WDTE,#0ACH       ; Clears & restarts WDT
       HALT                      ; Self programming is started
       MOV      A,PFS
       CMP      A,#00H
       BNZ      $StatusError     ; Checks erase error
                                 ; Performs abnormal termination processing when an error
                                 ; occurs.

FlashBlockBlankCheck:
       MOV      FLCMD,#04H       ; Sets flash control command (block blank check)
       MOV      FLAPH,#07H       ; Sets number of block for blank check (block 7 is specified
                                 ; here)
       MOV      FLAPL,#00H       ; Fixes FLAPL to "00H"
```

```
        MOV     FLAPHC,#07H     ; Sets blank check block compare number (same value as of
                                ; FLAPH)
        MOV     FLAPLC,#0FFH    ; Fixes FLAPLC to "FFH"
        MOV     PFS,#00H        ; Clears flash status register
        MOV     WDTE,#0ACH      ; Clears & restarts WDT
        HALT                    ; Self programming is started
        MOV     A,PFS
        CMP     A,#00H
        BNZ     $StatusError    ; Checks blank check error
                                ; Performs abnormal termination processing when an error
                                ; occurs.

ModeOffLoop:
        MOV     PFS,#00H
        MOV     PFCMD,#0A5H     ; PFCMD register control
        MOV     FLPMC,#00H      ; FLPMC register control (sets value)
        MOV     FLPMC,#0FFH     ; FLPMC register control (inverts set value)
        MOV     FLPMC,#00H      ; Sets normal mode via FLPMC register control (sets value)

        MOV     A,PFS
        CMP     A,#00H
        BNZ     $ModeOffLoop    ; Checks completion of write to specific registers
                                ; Repeats the same processing when an error occurs

        MOV     MK0,#INT_MK0    ; Restores interrupt mask flag

        EI

        BR      StatusNormal

;-------------------------------------------------------------------------
;END (abnormal termination processing); Perform processing to shift to
      normal mode in order to return to normal processing
;-------------------------------------------------------------------------
StatusError:

;-------------------------------------------------------------------------
;END (normal termination processing)
;-------------------------------------------------------------------------
StatusNormal:
```

(2) Write to internal verify

<1> Mode is shifted from normal mode to self programming mode (<1> to <5> in **16.8.4**)

<2> Specification of source data for write

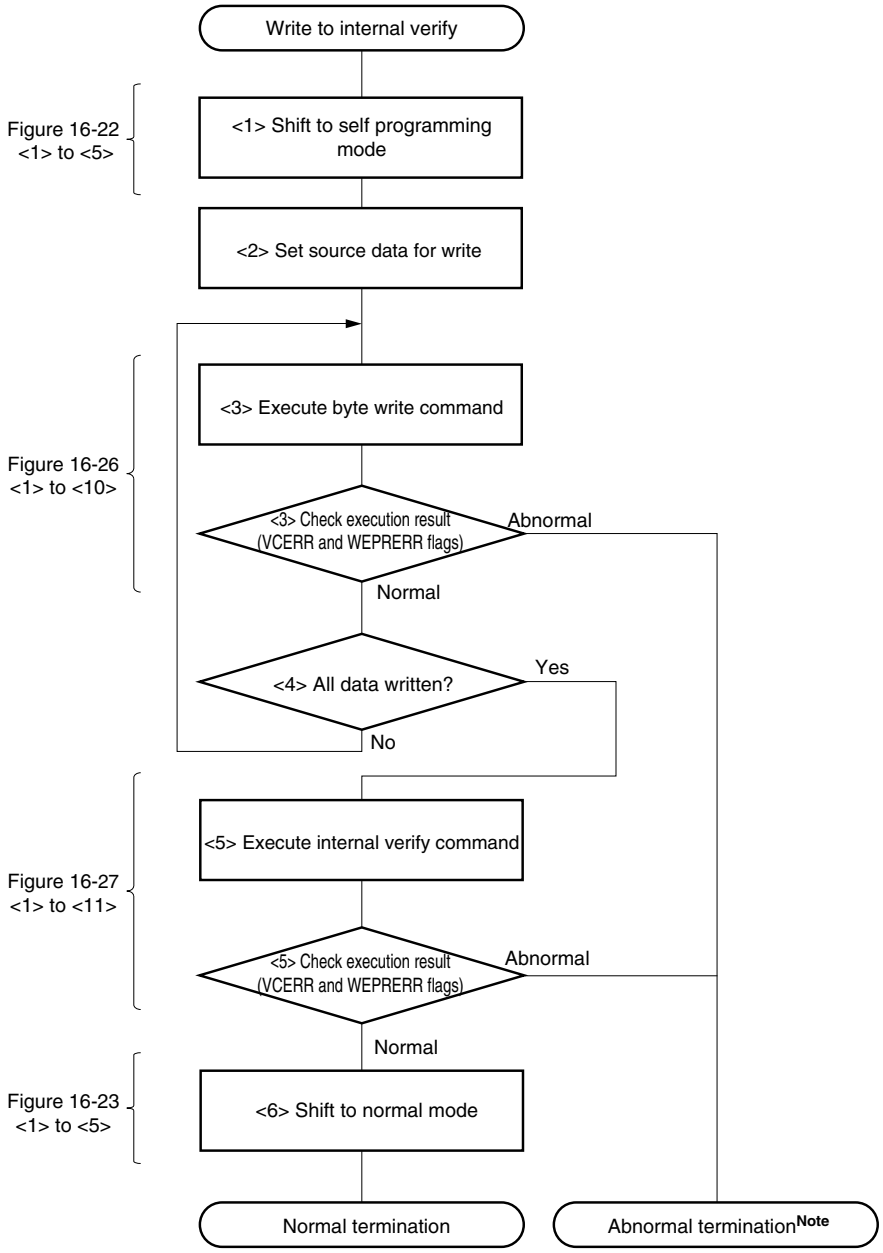
<3> Execution of byte write → Error check (<1> to <10> in **16.8.8**)

<4> <3> is repeated until all data are written.

<5> Execution of internal verify → Error check (<1> to <11> in **16.8.9**)

<6> Mode is shifted from self programming mode to normal mode (<1> to <5> in **16.8.5**)

Figure 16-29. Example of Operation When Command Execution Time Should Be Minimized (from Write to Internal Verify)



Note Perform processing to shift to normal mode in order to return to normal processing.

Remark <1> to <6> in Figure 16-29 correspond to <1> to <6> in **16.8.10 (2)** above.

An example of a program list when the command execution time (from write to internal verify) should be minimized in self programming mode is shown below.

```
;---------------------------------------------------------------------
;START
;---------------------------------------------------------------------
       MOV     MK0,#11111111B   ; Masks all interrupts

       DI

ModeOnLoop:
       MOV     PFS,#00H
       MOV     PFCMD,#0A5H      ; PFCMD register control
       MOV     FLPMC,#01H       ; FLPMC register control (sets value)
       MOV     FLPMC,#0FEH      ; FLPMC register control (inverts set value)
       MOV     FLPMC,#01H       ; Sets self programming mode with FLPMC register control
                                ; (sets value)

       MOV     A,PFS
       CMP     A,#00H
       BNZ     $ModeOnLoop      ; Checks completion of write to specific registers
                                ; Repeats the same processing when an error occurs

FlashWrite:
       MOVW    HL,#DataAdrTop   ; Sets address at which data to be written is located
       MOVW    DE,#WriteAdr     ; Sets address at which data is to be written
FlashWriteLoop:
       MOV     FLCMD,#05H       ; Sets flash control command (byte write)
       MOV     A,D
       MOV     FLAPH,A          ; Sets address at which data is to be written
       MOV     A,E
       MOV     FLAPL,A          ; Sets address at which data is to be written
       MOV     A,[HL]
       MOV     FLW,A            ; Sets data to be written

       MOV     PFS,#00H         ; Clears flash status register
       MOV     WDTE,#0ACH       ; Clears & restarts WDT
       HALT                     ; Self programming is started
       MOV     A,PFS
       CMP     A,#00H
       BNZ     $StatusError     ; Checks write error
                                ; Performs abnormal termination processing when an error
                                ; occurs.

       INCW    HL               ; address at which data to be written is located + 1
       MOVW    AX,HL
       CMPW    AX,#DataAdrBtm   ; Performs internal verify processing
       BNC     $FlashVerify     ; if write of all data is completed
```

```
        INCW    DE              ; Address at which data is to be written + 1
        BR      FlashWriteLoop

FlashVerify:
        MOVW    HL,#WriteAdr    ; Sets verify address

        MOV     FLCMD,#01H      ; Sets flash control command (internal verify)
        MOV     A,H
        MOV     FLAPH,A         ; Sets verify start address
        MOV     A,L
        MOV     FLAPL,A         ; Sets verify start address
        MOV     A,D
        MOV     FLAPHC,A        ; Sets verify end address
        MOV     A,E
        MOV     FLAPLC,A        ; Sets verify end address

        MOV     PFS,#00H        ; Clears flash status register
        MOV     WDTE,#0ACH      ; Clears & restarts WDT
        HALT                    ; Self programming is started
        MOV     A,PFS
        CMP     A,#00H
        BNZ     $StatusError    ; Checks internal verify error
                                ; Performs abnormal termination processing when an error
                                ; occurs.

ModeOffLoop:
        MOV     PFS,#00H
        MOV     PFCMD,#0A5H     ; PFCMD register control
        MOV     FLPMC,#00H      ; FLPMC register control (sets value)
        MOV     FLPMC,#0FFH     ; FLPMC register control (inverts set value)
        MOV     FLPMC,#00H      ; Sets normal mode via FLPMC register control (sets value)

        MOV     A,PFS
        CMP     A,#00H
        BNZ     $ModeOffLoop    ; Checks completion of write to specific registers
                                ; Repeats the same processing when an error occurs

        MOV     MK0,#INT_MK0    ; Restores interrupt mask flag

        EI

        BR      StatusNormal

;-------------------------------------------------------------------------
;END (abnormal termination processing); Perform processing to shift to
      normal mode in order to return to normal processing
;-------------------------------------------------------------------------
```

```
StatusError:


;---------------------------------------------------------------------
;END (normal termination processing)
;---------------------------------------------------------------------
StatusNormal:


;---------------------------------------------------------------------
; Data to be written
;---------------------------------------------------------------------
DataAdrTop:
        DB      XXH
        DB      XXH
        DB      XXH
        DB      XXH

         :
         :

        DB      XXH
DataAdrBtm:
;---------------------------------------------------------------------
```

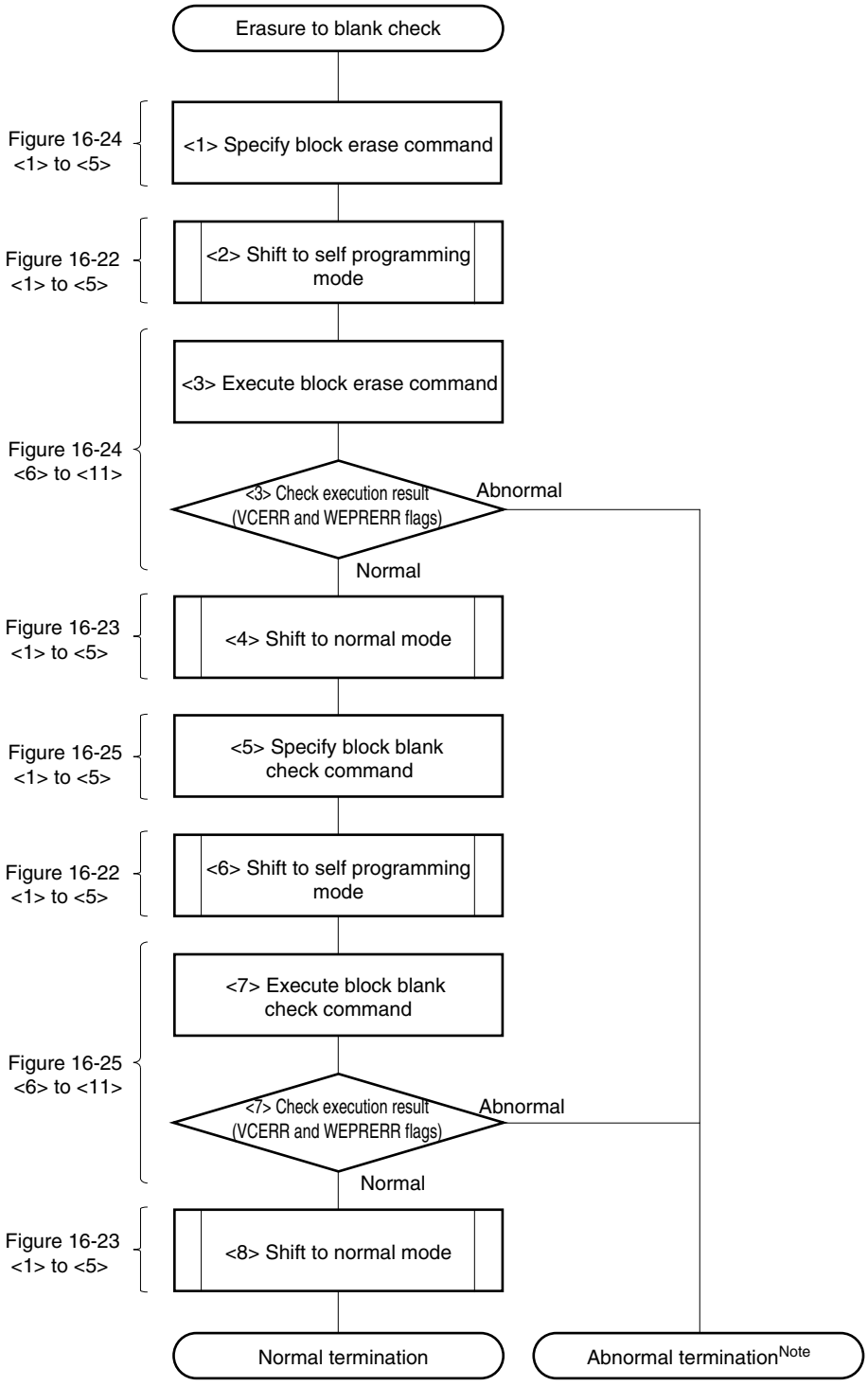
16.8.11 Examples of operation when interrupt-disabled time should be minimized in self programming mode

Examples of operation when the interrupt-disabled time should be minimized in self programming mode are explained below.

(1) Erasure to blank check

<1> Specification of block erase command (<1> to <5> in **16.8.6**)
<2> Mode is shifted from normal mode to self programming mode (<1> to <5> in **16.8.4**)
<3> Execution of block erase command → Error check (<6> to <11> in **16.8.6**)
<4> Mode is shifted from self programming mode to normal mode (<1> to <5> in **16.8.5**)
<5> Specification of block blank check command (<1> to <5> in **16.8.7**)
<6> Mode is shifted from normal mode to self programming mode (<1> to <5> in **16.8.4**)
<7> Execution of block blank check command → Error check (<6> to <11> in **16.8.7**)
<8> Mode is shifted from self programming mode to normal mode (<1> to <5> in **16.8.5**)

Figure 16-30. Example of Operation When Interrupt-Disabled Time Should Be Minimized (from Erasure to Blank Check)



Note Perform processing to shift to normal mode in order to return to normal processing.

Remark <1> to <8> in Figure 16-30 correspond to <1> to <8> in **16.8.11 (1)** (previous page).

An example of a program list when the interrupt-disabled time (from erasure to blank check) should be minimized in self programming mode is shown below.

```
;---------------------------------------------------------------------
;START
;---------------------------------------------------------------------
FlashBlockErase:
       ; Sets erase command
       MOV      FLCMD,#03H      ; Sets flash control command (block erase)
       MOV      FLAPH,#07H      ; Sets number of block to be erased (block 7 is specified here)
       MOV      FLAPL,#00H      ; Fixes FLAPL to "00H"
       MOV      FLAPHC,#07H     ; Sets erase block compare number (same value as that of FLAPH)
       MOV      FLAPLC,#00H     ; Fixes FLAPLC to "00H"

       CALL     !ModeOn         ; Shift to self programming mode

       ; Execution of erase command
       MOV      PFS,#00H        ; Clears flash status register
       MOV      WDTE,#0ACH      ; Clears & restarts WDT
       HALT                     ; Self programming is started
       MOV      A,PFS
       CMP      A,#00H
       BNZ      $StatusError    ; Checks erase error
                                ; Performs abnormal termination processing when an error
                                ; occurs.

       CALL     !ModeOff        ; Shift to normal mode


       ; Sets blank check command
       MOV      FLCMD,#04H      ; Sets flash control command (block blank check)
       MOV      FLAPH,#07H      ; Sets block number for blank check (block 7 is specified here)
       MOV      FLAPL,#00H      ; Fixes FLAPL to "00H"
       MOV      FLAPHC,#07H     ; Sets blank check block compare number (same value as that of
                                ; FLAPH)
       MOV      FLAPLC,#0FFH    ; Fixes FLAPLC to "FFH"

       CALL     !ModeOn         ; Shift to self programming mode

       ; Execution of blank check command
       MOV      PFS,#00H        ; Clears flash status register
       MOV      WDTE,#0ACH      ; Clears & restarts WDT
       HALT                     ; Self programming is started
       MOV      A,PFS
       CMP      A,#00H
       BNZ      $StatusError    ; Checks blank check error
                                ; Performs abnormal termination processing when an error occurs
```

```
        CALL    !ModeOff        ; Shift to normal mode

        BR      StatusNormal

;---------------------------------------------------------------------
;END (abnormal termination processing); Perform processing to shift to
      normal mode in order to return to normal processing
;---------------------------------------------------------------------
StatusError:


;---------------------------------------------------------------------
;END (normal termination processing)
;---------------------------------------------------------------------
StatusNormal:


;---------------------------------------------------------------------
;Processing to shift to self programming mode
;---------------------------------------------------------------------
ModeOn:
        MOV     MK0,#11111111B   ; Masks all interrupts

        DI

ModeOnLoop:
        MOV     PFS,#00H
        MOV     PFCMD,#0A5H     ; PFCMD register control
        MOV     FLPMC,#01H      ; FLPMC register control (sets value)
        MOV     FLPMC,#0FEH     ; FLPMC register control (inverts set value)
        MOV     FLPMC,#01H      ; Sets self programming mode via FLPMC register control (sets
                                ; value)

        MOV     A,PFS
        CMP     A,#00H
        BNZ     $ModeOnLoop     ; Checks completion of write to specific registers
                                ; Repeats the same processing when an error occurs

        RET

;---------------------------------------------------------------------
; Processing to shift to normal mode
;---------------------------------------------------------------------
ModeOff:
        MOV     PFS,#00H
        MOV     PFCMD,#0A5H     ; PFCMD register control
        MOV     FLPMC,#00H      ; FLPMC register control (sets value)
        MOV     FLPMC,#0FFH     ; FLPMC register control (inverts set value)
```

```
MOV     FLPMC,#00H      ; Sets normal mode via FLPMC register control (sets value)

MOV     A,PFS
CMP     A,#00H
BNZ     $ModeOff        ; Checks completion of write to specific registers
                        ; Repeats the same processing when an error occurs

MOV     MK0,#INT_MK0    ; Restores interrupt mask flag

EI

RET
```

(2) Write to internal verify

<1> Specification of source data for write

<2> Specification of byte write command (<1> to <4> in **16.8.8**)

<3> Mode is shifted from normal mode to self programming mode (<1> to <5> in **16.8.4**)

<4> Execution of byte write command → Error check (<5> to <10> in **16.8.8**)

<5> Mode is shifted from self programming mode to normal mode (<1> to <5> in **16.8.5**)

<6> <2> to <5> is repeated until all data are written.

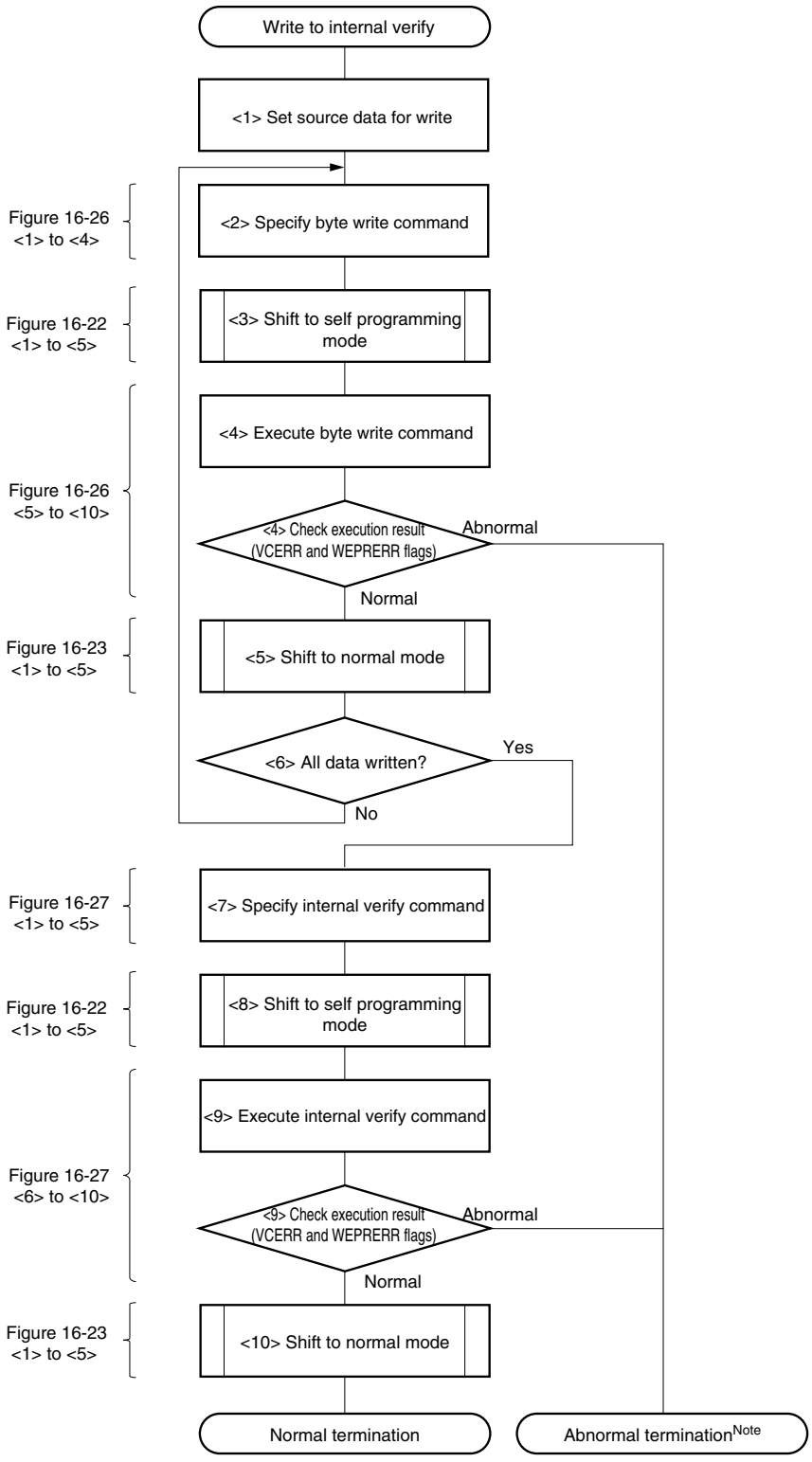
<7> The internal verify command is specified (<1> to <5> in **16.8.9**)

<8> Mode is shifted from normal mode to self programming mode (<1> to <5> in **16.8.4**)

<9> Execution of internal verify command → Error check (<6> to <11> in **16.8.9**)

<10> Mode is shifted from self programming mode to normal mode (<1> to <5> in **16.8.5**)

Figure 16-31. Example of Operation When Interrupt-Disabled Time Should Be Minimized (from Write to Internal Verify)



Note Perform processing to shift to normal mode in order to return to normal processing.

Remark <1> to <10> in Figure 16-31 correspond to <1> to <10> in **16.8.11 (2)** (previous page).

An example of a program list when the interrupt-disabled time (from write to internal verify) should be minimized in self programming mode is shown below.

```
;---------------------------------------------------------------------
;START
;---------------------------------------------------------------------
       ; Sets write command
FlashWrite:
       MOVW     HL,#DataAdrTop  ; Sets address at which data to be written is located
       MOVW     DE,#WriteAdr    ; Sets address at which data is to be written

FlashWriteLoop:
       MOV      FLCMD,#05H      ; Sets flash control command (byte write)
       MOV      A,D
       MOV      FLAPH,A         ; Sets address at which data is to be written
       MOV      A,E
       MOV      FLAPL,A         ; Sets address at which data is to be written
       MOV      A,[HL]
       MOV      FLW,A           ; Sets data to be written

       CALL     !ModeOn         ; Shift to self programming mode

       ; Execution of write command
       MOV      PFS,#00H        ; Clears flash status register
       MOV      WDTE,#0ACH      ; Clears & restarts WDT
       HALT                     ; Self programming is started
       MOV      A,PFS
       CMP      A,#00H
       BNZ      $StatusError    ; Checks write error
                                ; Performs abnormal termination processing when an error
                                ; occurs.

       CALL     !ModeOff        ; Shift to normal mode

       MOV      MK0,#INT_MK0    ; Restores interrupt mask flag

       EI

       ; Judgment of writing all data
       INCW     HL              ; Address at which data to be written is located + 1
       MOVW     AX,HL
       CMPW     AX,#DataAdrBtm  ; Performs internal verify processing
       BNC      $FlashVerify    ; if write of all data is completed

       INCW     DE              ; Address at which data is to be written + 1
       BR       FlashWriteLoop

       ; Setting internal verify command
```

```
FlashVerify:
       MOVW     HL,#WriteAdr    ; Sets verify address

       MOV      FLCMD,#01H      ; Sets flash control command (internal verify)
       MOV      A,H
       MOV      FLAPH,A         ; Sets verify start address
       MOV      A,L
       MOV      FLAPL,A         ; Sets verify start address
       MOV      A,D
       MOV      FLAPHC,A        ; Sets verify end address
       MOV      A,E
       MOV      FLAPLC,A        ; Sets verify end address

       CALL     !ModeOn         ; Shift to self programming mode

       ; Execution of internal verify command
       MOV      PFS,#00H        ; Clears flash status register
       MOV      WDTE,#0ACH      ; Clears & restarts WDT
       HALT                     ; Self programming is started
       MOV      A,PFS
       CMP      A,#00H
       BNZ      $StatusError    ; Checks internal verify error
                                ; Performs abnormal termination processing when an error occurs

       CALL     !ModeOff        ; Shift to normal mode

       BR       StatusNormal

;---------------------------------------------------------------------
;END (abnormal termination processing); Perform processing to shift to
      normal mode in order to return to normal processing
;---------------------------------------------------------------------
StatusError:


;---------------------------------------------------------------------
;END (normal termination processing)
;---------------------------------------------------------------------
StatusNormal:


;---------------------------------------------------------------------
;Processing to shift to self programming mode
;---------------------------------------------------------------------
ModeOn:
       MOV      MK0,#11111111B  ; Masks all interrupts

       DI
```

```
ModeOnLoop:
        MOV     PFS,#00H
        MOV     PFCMD,#0A5H     ; PFCMD register control
        MOV     FLPMC,#01H      ; FLPMC register control (sets value)
        MOV     FLPMC,#0FEH     ; FLPMC register control (inverts set value)
        MOV     FLPMC,#01H      ; Sets self programming mode via FLPMC register control (sets
                                ; value)

        MOV     A,PFS
        CMP     A,#00H
        BNZ     $ModeOnLoop     ; Checks completion of write to specific registers
                                ; Repeats the same processing when an error occurs

        RET


;---------------------------------------------------------------------
; Processing to shift to normal mode
;---------------------------------------------------------------------
ModeOff:
        MOV     PFS,#00H
        MOV     PFCMD,#0A5H     ; PFCMD register control
        MOV     FLPMC,#00H      ; FLPMC register control (sets value)
        MOV     FLPMC,#0FFH     ; FLPMC register control (inverts set value)
        MOV     FLPMC,#00H      ; Sets normal mode via FLPMC register control (sets value)

        MOV     A,PFS
        CMP     A,#00H
        BNZ     $ModeOff        ; Checks completion of write to specific registers
                                ; Repeats the same processing when an error occurs

        MOV     MK0,#INT_MK0    ; Restores interrupt mask flag

        EI

        RET


;---------------------------------------------------------------------
;Data to be written
;---------------------------------------------------------------------
DataAdrTop:
        DB      XXH
        DB      XXH
        DB      XXH
        DB      XXH
```

```
        :
        :

        DB      XXH
DataAdrBtm:
;-------------------------------------------------------------------------
```

CHAPTER 17 INSTRUCTION SET OVERVIEW

This chapter lists the instruction set of the 78K0S/KU1+ and 78K0S/KY1+. For details of the operation and machine language (instruction code) of each instruction, refer to **78K/0S Series Instructions User's Manual (U11047E)**.

17.1 Operation

17.1.1 Operand identifiers and description methods

Operands are described in "Operand" column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Uppercase letters and the symbols #, !, $, and [ ] are key words and are described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, $ and [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 17-1. Operand Identifiers and Description Methods

Identifier	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH Immediate data or labels FE20H to FF1FH Immediate data or labels (even addresses only)
addr16 addr5	0000H to FFFFH Immediate data or labels (only even addresses for 16-bit data transfer instructions) 0040H to 007FH Immediate data or labels (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

Remark For symbols of special function registers, see **Table 3-3 Special Function Registers**.

17.1.2 Description of “Operation” column

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
( ):	Memory contents indicated by address or register contents in parentheses
×H, ×L:	Higher 8 bits and lower 8 bits of 16-bit register
∧:	Logical product (AND)
∨:	Logical sum (OR)
∀:	Exclusive logical sum (exclusive OR)
¯:	Inverted data
addr16:	16-bit immediate data or label
jdisp8:	Signed 8-bit data (displacement value)

17.1.3 Description of “Flag” column

(Blank):	Unchanged
0:	Cleared to 0
1:	Set to 1
×:	Set/cleared according to the result
R:	Previously saved value is stored

17.2 Operation List

Mnemonic	Operand	Bytes	Clocks	Operation	Flag
					Z AC CY
MOV	r, #byte	3	6	r ← byte	
	saddr, #byte	3	6	(saddr) ← byte	
	sfr, #byte	3	6	sfr ← byte	
	A, r Note 1	2	4	A ← r	
	r, A Note 1	2	4	r ← A	
	A, saddr	2	4	A ← (saddr)	
	saddr, A	2	4	(saddr) ← A	
	A, sfr	2	4	A ← sfr	
	sfr, A	2	4	sfr ← A	
	A, !addr16	3	8	A ← (addr16)	
	!addr16, A	3	8	(addr16) ← A	
	PSW, #byte	3	6	PSW ← byte	× × ×
	A, PSW	2	4	A ← PSW	
	PSW, A	2	4	PSW ← A	× × ×
	A, [DE]	1	6	A ← (DE)	
	[DE], A	1	6	(DE) ← A	
	A, [HL]	1	6	A ← (HL)	
	[HL], A	1	6	(HL) ← A	
	A, [HL + byte]	2	6	A ← (HL + byte)	
	[HL + byte], A	2	6	(HL + byte) ← A	
XCH	A, X	1	4	A ↔ X	
	A, r Note 2	2	6	A ↔ r	
	A, saddr	2	6	A ↔ (saddr)	
	A, sfr	2	6	A ↔ sfr	
	A, [DE]	1	8	A ↔ (DE)	
	A, [HL]	1	8	A ↔ (HL)	
	A, [HL, byte]	2	8	A ↔ (HL + byte)	

Notes 1. Except r = A.

2. Except r = A, X.

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note	1	4	AX ← rp			
	rp, AX Note	1	4	rp ← AX			
XCHW	AX, rp Note	1	8	AX ↔ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×

Note Only when rp = BC, DE, or HL.

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ∨̄ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨̄ byte	×		
	A, r	2	4	A ← A ∨̄ r	×		
	A, saddr	2	4	A ← A ∨̄ (saddr)	×		
	A, !addr16	3	8	A ← A ∨̄ (addr16)	×		
	A, [HL]	1	6	A ← A ∨̄ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨̄ (HL + byte)	×		

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, $A_7 \leftarrow A_0$, $A_{m-1} \leftarrow A_m$) × 1			×
ROL	A, 1	1	2	(CY, $A_0 \leftarrow A_7$, $A_{m+1} \leftarrow A_m$) × 1			×
RORC	A, 1	1	2	(CY ← A_0, $A_7 \leftarrow$ CY, $A_{m-1} \leftarrow A_m$) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, $A_0 \leftarrow$ CY, $A_{m+1} \leftarrow A_m$) × 1			×
SET1	saddr.bit	3	6	(saddr.bit) ← 1			
	sfr.bit	3	6	sfr.bit ← 1			
	A.bit	2	4	A.bit ← 1			
	PSW.bit	3	6	PSW.bit ← 1	×	×	×
	[HL].bit	2	10	(HL).bit ← 1			
CLR1	saddr.bit	3	6	(saddr.bit) ← 0			
	sfr.bit	3	6	sfr.bit ← 0			
	A.bit	2	4	A.bit ← 0			
	PSW.bit	3	6	PSW.bit ← 0	×	×	×
	[HL].bit	2	10	(HL).bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
CALL	!addr16	3	6	$(SP - 1) \leftarrow (PC + 3)_H$, $(SP - 2) \leftarrow (PC + 3)_L$, $PC \leftarrow$ addr16, $SP \leftarrow SP - 2$			
CALLT	[addr5]	1	8	$(SP - 1) \leftarrow (PC + 1)_H$, $(SP - 2) \leftarrow (PC + 1)_L$, $PC_H \leftarrow$ (00000000, addr5 + 1), $PC_L \leftarrow$ (00000000, addr5), $SP \leftarrow SP - 2$			
RET		1	6	$PC_H \leftarrow (SP + 1)$, $PC_L \leftarrow (SP)$, $SP \leftarrow SP + 2$			
RETI		1	8	$PC_H \leftarrow (SP + 1)$, $PC_L \leftarrow (SP)$, $PSW \leftarrow (SP + 2)$, $SP \leftarrow SP + 3$, NMIS $\leftarrow 0$	R	R	R
PUSH	PSW	1	2	$(SP - 1) \leftarrow PSW$, $SP \leftarrow SP - 1$			
	rp	1	4	$(SP - 1) \leftarrow rp_H$, $(SP - 2) \leftarrow rp_L$, $SP \leftarrow SP - 2$			
POP	PSW	1	4	$PSW \leftarrow (SP)$, $SP \leftarrow SP + 1$	R	R	R
	rp	1	6	$rp_H \leftarrow (SP + 1)$, $rp_L \leftarrow (SP)$, $SP \leftarrow SP + 2$			
MOVW	SP, AX	2	8	$SP \leftarrow AX$			
	AX, SP	2	6	$AX \leftarrow SP$			
BR	!addr16	3	6	$PC \leftarrow$ addr16			
	$addr16	2	6	$PC \leftarrow PC + 2 +$ jdisp8			
	AX	1	6	$PC_H \leftarrow A$, $PC_L \leftarrow X$			
BC	$saddr16	2	6	$PC \leftarrow PC + 2 +$ jdisp8 if CY = 1			
BNC	$saddr16	2	6	$PC \leftarrow PC + 2 +$ jdisp8 if CY = 0			
BZ	$saddr16	2	6	$PC \leftarrow PC + 2 +$ jdisp8 if Z = 1			
BNZ	$saddr16	2	6	$PC \leftarrow PC + 2 +$ jdisp8 if Z = 0			
BT	saddr.bit, $addr16	4	10	$PC \leftarrow PC + 4 +$ jdisp8 if (saddr.bit) = 1			
	sfr.bit, $addr16	4	10	$PC \leftarrow PC + 4 +$ jdisp8 if sfr.bit = 1			
	A.bit, $addr16	3	8	$PC \leftarrow PC + 3 +$ jdisp8 if A.bit = 1			
	PSW.bit, $addr16	4	10	$PC \leftarrow PC + 4 +$ jdisp8 if PSW.bit = 1			
BF	saddr.bit, $addr16	4	10	$PC \leftarrow PC + 4 +$ jdisp8 if (saddr.bit) = 0			
	sfr.bit, $addr16	4	10	$PC \leftarrow PC + 4 +$ jdisp8 if sfr.bit = 0			
	A.bit, $addr16	3	8	$PC \leftarrow PC + 3 +$ jdisp8 if A.bit = 0			
	PSW.bit, $addr16	4	10	$PC \leftarrow PC + 4 +$ jdisp8 if PSW.bit = 0			
DBNZ	B, $addr16	2	6	$B \leftarrow B - 1$, then $PC \leftarrow PC + 2 +$ jdisp8 if $B \neq 0$			
	C, $addr16	2	6	$C \leftarrow C - 1$, then $PC \leftarrow PC + 2 +$ jdisp8 if $C \neq 0$			
	saddr, $addr16	3	8	(saddr) $\leftarrow$ (saddr) $- 1$, then $PC \leftarrow PC + 3 +$ jdisp8 if (saddr) $\neq 0$			
NOP		1	2	No Operation			
EI		3	6	IE $\leftarrow 1$ (Enable Interrupt)			
DI		3	6	IE $\leftarrow 0$ (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

17.3 Instructions Listed by Addressing Type

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, INC, DEC, ROR, ROL, RORC, ROLC, PUSH, POP, DBNZ

1st Operand \ 2nd Operand	#byte	A	r	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV[Note] XCH[Note] ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											
[HL + byte]		MOV											

Note Except r = A.

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp[Note]	saddrp	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	
rp	MOVW	MOVW[Note]				INCW DECW PUSH POP
saddrp		MOVW				
sp		MOVW				

Note Only when rp = BC, DE, or HL.

(3) Bit manipulation instructions

SET1, CLR1, NOT1, BT, BF

1st Operand \ 2nd Operand	$addr16	None
A.bit	BT BF	SET1 CLR1
sfr.bit	BT BF	SET1 CLR1
saddr.bit	BT BF	SET1 CLR1
PSW.bit	BT BF	SET1 CLR1
[HL].bit		SET1 CLR1
CY		SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLT, BR, BC, BNC, BZ, BNZ, DBNZ

1st Operand \ 2nd Operand	AX	!addr16	[addr5]	$addr16
Basic instructions	BR	CALL BR	CALLT	BR BC BNC BZ BNZ
Compound instructions				DBNZ

(5) Other instructions

RET, RETI, NOP, EI, DI, HALT, STOP

CHAPTER 18 ELECTRICAL SPECIFICATIONS (TARGET VALUES)

These specifications are only target values, and may not be satisfied by mass-produced products.

Absolute Maximum Ratings (T_A = 25°C)

	Parameter	Symbol	Conditions		Ratings	Unit
	Supply voltage	V_{DD}			−0.3 to +6.5	V
		V_{SS}			−0.3 to +0.3	V
	Input voltage	V_I	P20 to P23, P32, P34, P40 to P47[Note 1]		−0.3 to V_{DD} + 0.3[Note 2]	V
	Output voltage	V_O			−0.3 to V_{DD} + 0.3[Note 2]	V
	Analog input voltage	V_{AN}			−0.3 to V_{DD} + 0.3[Note 2]	V
	Output current, high	I_{OH}	Per pin		−10	mA
★			Total of all pins	P20 to P23, P32, P40 to P47[Note 1]	−44	mA
	Output current, low	I_{OL}	Per pin		20	mA
★			Total of all pins	P20 to P23, P32, P40 to P47[Note 1]	44	mA
★	Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
			During flash memory programming			°C
	Storage temperature	T_{stg}			−40 to +125	°C

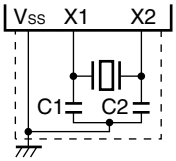
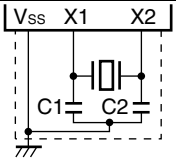
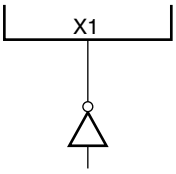
Notes 1. The P40 to P47 pins are provided only in the 78K0S/KY1+.

2. Must be 6.5 V or lower

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

★ **X1 Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note 1])**

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 2]		1		10.0	MHz
Crystal resonator		Oscillation frequency (f_X)[Note 2]		1		10.0	MHz
External clock		X1 input frequency (f_X)[Note 2]	2.7 V ≤ V_{DD} ≤ 5.5 V	1		10.0	MHz
			2.0 V ≤ V_{DD} < 2.7 V	1		5.0	
		X1 input high-/low-level width (t_{XH}, t_{XL})	2.7 V ≤ V_{DD} ≤ 5.5 V	0.045		0.5	μs
			2.0 V ≤ V_{DD} < 2.7 V	0.09		1.0	

Notes 1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

2. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Caution When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Remark For the resonator selection and oscillator constant, users are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

High-Speed Ring-OSC Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note 1])

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
On-chip high-speed Ring-OSC	Oscillation frequency (f_X)[Note 2]	2.7 V ≤ V_{DD} ≤ 5.5 V	7.60	8.00	8.40	MHz
		2.0 V ≤ V_{DD} < 2.7 V		T.B.D		MHz

Notes 1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

2. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Low-Speed Ring-OSC Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note])

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
On-chip low-speed Ring-OSC	Oscillation frequency (f_{RL})		120	240	480	kHz

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V [Note]) (1/2)

	Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
	Output current, high	I_{OH1}	Pins other than P20 to P23	Per pin	2.0 V ≤ V_{DD} ≤ 5.5 V			–5	mA
				Total	4.0 V ≤ V_{DD} ≤ 5.5 V			–25	mA
					2.0 V ≤ V_{DD} < 4.0 V			–15	mA
		I_{OH2}	P20 to P23	Per pin	2.0 V ≤ V_{DD} ≤ 5.5 V			–5	mA
				Total	2.0 V ≤ V_{DD} ≤ 5.5 V			–15	mA
	Output current, low	I_{OL}	Per pin		2.0 V ≤ V_{DD} ≤ 5.5 V			10	mA
			Total of all pins		4.0 V ≤ V_{DD} ≤ 5.5 V			30	mA
					2.0 V ≤ V_{DD} < 4.0 V			15	mA
★	Input voltage, high	V_{IH1}	P23 in external clock mode and pins other than P20 and P21			0.8V_{DD}		V_{DD}	V
		V_{IH2}	P23 in other than external clock mode, P20 and P21			0.7V_{DD}		V_{DD}	V
★	Input voltage, low	V_{IL1}	P23 in external clock mode and pins other than P20 and P21			0		0.2V_{DD}	V
		V_{IL2}	P23 in other than external clock mode, P20 and P21			0		0.3V_{DD}	V
	Output voltage, high	V_{OH1}	Total of output pins other than P20 to P23 I_{OH1} = –15 mA		4.0 V ≤ V_{DD} ≤ 5.5 V I_{OH1} = –5 mA	V_{DD} – 1.0			V
			I_{OH1} = –100 μA		2.0 V ≤ V_{DD} < 4.0 V	V_{DD} – 0.5			V
★		V_{OH2}	Total of pins P20 to P23 I_{OH2} = –10 mA		4.0 V ≤ V_{DD} ≤ 5.5 V I_{OH2} = –5 mA	V_{DD} – 1.0			V
					2.0 V ≤ V_{DD} < 4.0 V I_{OH2} = –5 mA	V_{DD} – 0.5			V
★	Output voltage, low	V_{OL}	Total of output pins I_{OL} = 30 mA		4.0 V ≤ V_{DD} ≤ 5.5 V I_{OL} = 10 mA			1.3	V
			2.0 V ≤ V_{DD} < 4.0 V I_{OL} = 400 μA					0.4	V
★	Input leakage current, high	I_{LIH}	V_I = V_{DD}	Pins other than X1				3	μA
★	Input leakage current, low	I_{LIL}	V_I = 0 V	Pins other than X1				–3	μA
★	Output leakage current, high	I_{LOH}	V_O = V_{DD}	Pins other than X2				3	μA
★	Output leakage current, low	I_{LOL}	V_O = 0 V	Pins other than X2				–3	μA
	Pull-up resistance value	R_{PU}	V_I = 0 V			10	30	100	kΩ
★	Pull-down resistance value	R_{PD}	P22, P23 reset status			10	30	100	kΩ

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

★ **DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note 1]) (2/2)**

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note 2]	I_{DD1}[Note 3]	Crystal/ceramic oscillation, external clock input oscillation operating mode[Note 6]	f_X = 10 MHz V_{DD} = 5.0 V ±10%[Note 4]	When A/D converter is stopped		6.1	12.2	mA
				When A/D converter is operating		7.6	15.2	
			f_X = 6 MHz V_{DD} = 5.0 V ±10%[Note 4]	When A/D converter is stopped		5.5	11.0	mA
				When A/D converter is operating			14.0	
			f_X = 5 MHz V_{DD} = 3.0 V ±10%[Note 5]	When A/D converter is stopped		3.0	6.0	mA
				When A/D converter is operating		4.5	9.0	
	I_{DD2}	Crystal/ceramic oscillation, external clock input HALT mode[Note 6]	f_X = 10 MHz V_{DD} = 5.0 V ±10%[Note 4]	When peripheral functions are stopped		1.7	3.8	mA
				When peripheral functions are operating			6.7	
			f_X = 6 MHz V_{DD} = 5.0 V ±10%[Note 4]	When peripheral functions are stopped		1.3	3.0	mA
				When peripheral functions are operating			6.0	
			f_X = 5 MHz V_{DD} = 3.0 V ±10%[Note 5]	When peripheral functions are stopped		0.48	1	mA
				When peripheral functions are operating			2.1	
	I_{DD3}	High-speed Ring-OSC operation mode[Note 7]	f_X = 8 MHz V_{DD} = 5.0 V ±10%[Note 4]	When A/D converter is stopped		5.5	11.0	mA
				When A/D converter is operating		7.0	14.0	
	I_{DD4}	High-speed Ring-OSC HALT mode[Note 7]	f_X = 8 MHz V_{DD} = 5.0 V ±10%[Note 4]	When peripheral functions are stopped		1.4	3.2	mA
				When peripheral functions are operating			5.9	
	I_{DD5}	STOP mode	V_{DD} = 5.0 V ±10%	When low-speed Ring-OSC is stopped		3.5	35.5	μA
				When low-speed Ring-OSC is operating		17.5	63.5	
			V_{DD} = 3.0 V ±10%	When low-speed Ring-OSC is stopped		3.5	15.5	μA
				When low-speed Ring-OSC is operating		11.0	30.5	

Notes 1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

2. Total current flowing through the internal power supply (V_{DD}). However, the current that flows through the pull-up resistors of ports is not included.

3. I_{DD1} includes peripheral operation current.

4. When the processor clock control register (PCC) is set to 00H.

5. When the processor clock control register (PCC) is set to 02H.

6. When crystal/ceramic oscillation clock, external clock input is selected as the system clock source using the option byte.

7. When high-speed Ring-OSC clock is selected as the system clock source using the option byte.

AC Characteristics

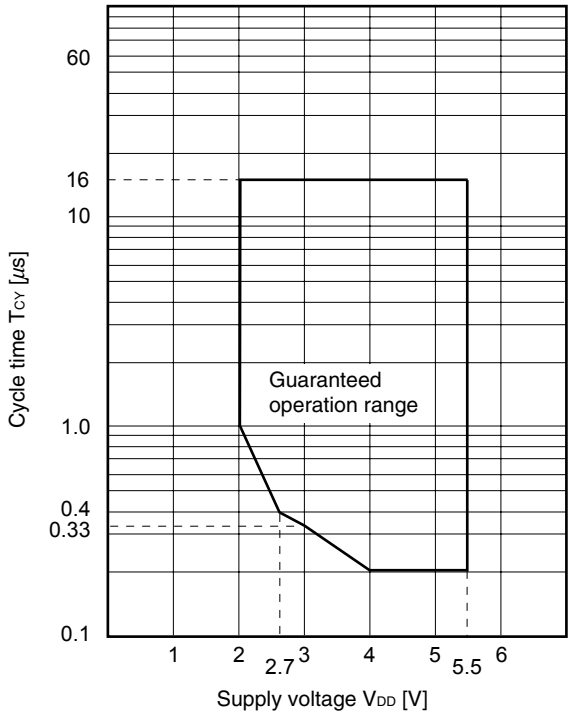
Basic operation (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note 1])

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★ Cycle time (minimum instruction execution time)	T_{CY}	Crystal/ceramic oscillation clock, external clock input	4.0 V ≤ V_{DD} ≤ 5.5 V	0.2		16	μs
			3.0 V ≤ V_{DD} < 4.0 V	0.33		16	μs
			2.7 V ≤ V_{DD} < 3.0 V	0.4		16	μs
			2.0 V ≤ V_{DD} < 2.7 V	1		16	μs
		High-speed Ring-OSC clock	4.0 V ≤ V_{DD} ≤ 5.5 V	0.23		4.22	μs
			2.7 V ≤ V_{DD} < 4.0 V	0.47		4.22	μs
			2.0 V ≤ V_{DD} < 2.7 V	0.95		4.22	μs
TI000 input high-level width, low-level width	t_{TIH}, t_{TIL}	4.0 V ≤ V_{DD} ≤ 5.5 V		2/fsam+ 0.1[Note 2]			μs
		2.0 V ≤ V_{DD} < 4.0 V		2/fsam+ 0.2[Note 2]			μs
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}			1			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}			2			μs

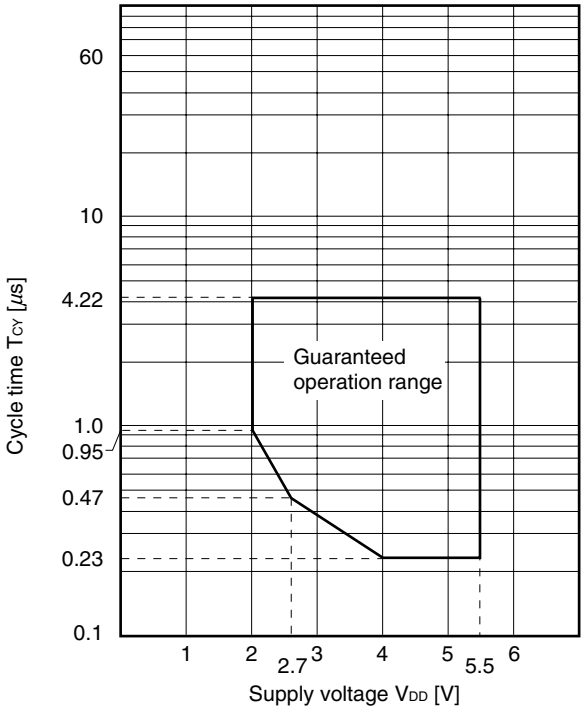
Notes1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

2. Selection of fsam = f_{XP}, f_{XP}/4, or f_{XP}/256 is possible using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00). Note that when selecting the TI000 valid edge as the count clock, fsam = f_{XP}.

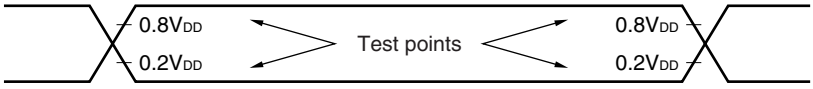
★ **T_{CY} vs. V_{DD} (Crystal/Ceramic Oscillation Clock, External Clock Input)**



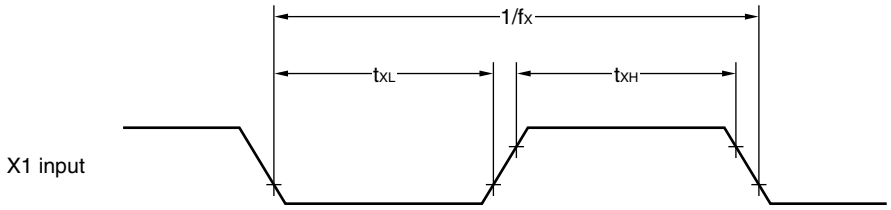
★ **T_{CY} vs. V_{DD} (High-speed Ring-OSC Clock)**



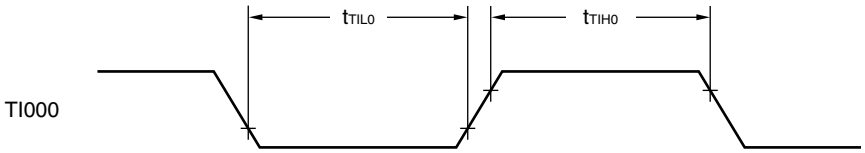
AC Timing Test Points (Excluding X1 Input)



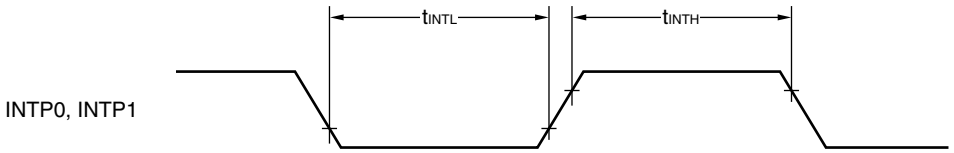
Clock Timing



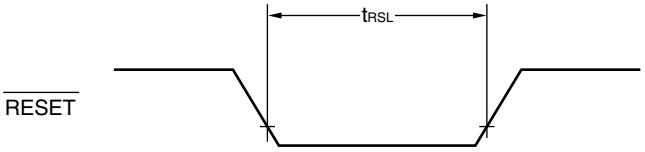
TI000 Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



★ **A/D Converter Characteristics (T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V[Note 1], V_{SS} = 0 V[Note 2])**

(1) A/D converter basic characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Conversion time	t_{CONV}	4.5 V ≤ V_{DD} ≤ 5.5 V	3.0		100	μs
		4.0 V ≤ V_{DD} < 4.5 V	4.8		100	μs
		2.85 V ≤ V_{DD} < 4.0 V	6.0		100	μs
		2.7 V ≤ V_{DD} < 2.85 V	14.0		100	μs
Analog input voltage	V_{AIN}		V_{SS}[Note 2]		V_{DD}	V

(2) A/D Converter Characteristics (High-speed Ring-OSC Clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Overall error[Notes 3, 4]	AINL			–0.1 to +0.2[Note 5]	-0.35 to +0.45	%FSR
Zero-scale error[Notes 3, 4]	Ezs			–0.1 to +0.2[Note 5]	-0.35 to +0.45	%FSR
Full-scale error[Notes 3, 4]	Efs			–0.1 to +0.2[Note 5]	-0.35 to +0.40	%FSR
Integral non-linearity error[Note 3]	ILE			±1[Note 5]	±3	LSB
Differential non-linearity error[Note 3]	DLE			±1[Note 5]	±1.5	LSB

(3) A/D Converter Characteristics (Crystal/Ceramic Oscillation Clock, External Clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Overall error[Notes 1, 2]	AINL	4.0 V ≤ V_{DD} ≤ 5.5 V		–0.15 to +0.40[Note 5]	–0.35 to +0.65	%FSR
		2.7 V ≤ V_{DD} < 4.0 V		–0.15 to +0.30[Note 5]	–0.35 to +0.55	%FSR
Zero-scale error[Notes 3, 4]	Ezs	4.0 V ≤ V_{DD} ≤ 5.5 V		–0.15 to +0.40[Note 5]	–0.35 to +0.65	%FSR
		2.7 V ≤ V_{DD} < 4.0 V		–0.15 to +0.30[Note 5]	–0.35 to +0.55	%FSR
Full-scale error[Notes 3, 4]	Efs	4.0 V ≤ V_{DD} ≤ 5.5 V		–0.15 to +0.30[Note 5]	–0.35 to +0.55	%FSR
		2.7 V ≤ V_{DD} < 4.0 V		–0.15 to +0.30[Note 5]	–0.35 to +0.50	%FSR
Integral non-linearity error[Note 3]	ILE	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.5[Note 5]	±3.0	LSB
		2.7 V ≤ V_{DD} < 4.0 V		±1.5[Note 5]	±4.0	LSB
Differential non-linearity error[Note 3]	DLE	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.0[Note 5]	±2.5	LSB
		2.7 V ≤ V_{DD} < 4.0 V		±1.0[Note 5]	±2.5	LSB

Notes 1. In the 78K0S/KU1+ and 78K0S/KY1+, V_{DD} functions alternately as the A/D converter reference voltage input. When using the A/D converter, stabilize V_{DD} at the supply voltage used (2.7 to 5.5 V).

2. In the 78K0S/KU1+ and 78K0S/KY1+, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

3. Excludes quantization error (±1/2 LSB).

4. This value is indicated as a ratio (%FSR) to the full-scale value.

5. A value when HALT mode is set by an instruction immediately after A/D conversion starts.

Caution The conversion accuracy may be degraded if the level of a port that is not used for A/D conversion is changed during A/D conversion.

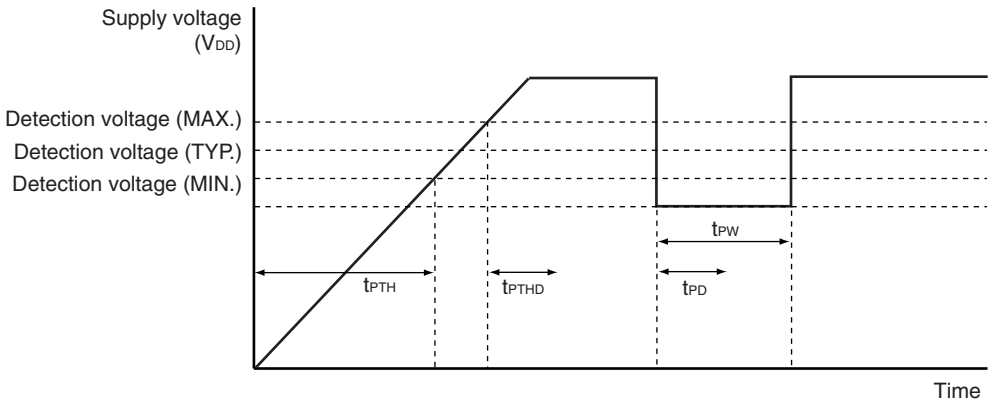
POC Circuit Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC}		2.0	2.1	2.2	V
Power supply rise time	t_{PTH}	V_{DD}: 0 V → 2.1 V	1.5			μs
Response delay time 1[Note 1]	t_{PTHD}	When power supply rises, after reaching detection voltage (MAX.)			3.0	ms
Response delay time 2[Note 2]	t_{PD}	When power supply falls			1.0	ms
Minimum pulse width	t_{PW}		0.2			ms

Note1. Time required from voltage detection to internal reset release.

2. Time required from voltage detection to internal reset signal generation.

POC Circuit Timing



LVI Circuit Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVI0}		4.1	4.3	4.5	V
	V_{LVI1}		3.9	4.1	4.3	V
	V_{LVI2}		3.7	3.9	4.1	V
	V_{LVI3}		3.5	3.7	3.9	V
	V_{LVI4}		3.3	3.5	3.7	V
	V_{LVI5}		3.15	3.3	3.45	V
	V_{LVI6}		2.95	3.1	3.25	V
	V_{LVI7}		2.7	2.85	3.0	V
	V_{LVI8}		2.5	2.6	2.7	V
	V_{LVI9}		2.25	2.35	2.45	V
Response time[Note 1]	t_{LD}			0.2	2.0	ms
Minimum pulse width	t_{LW}		0.2			ms
Operation stabilization wait time[Note 2]	t_{LWAIT}			0.1	0.2	ms

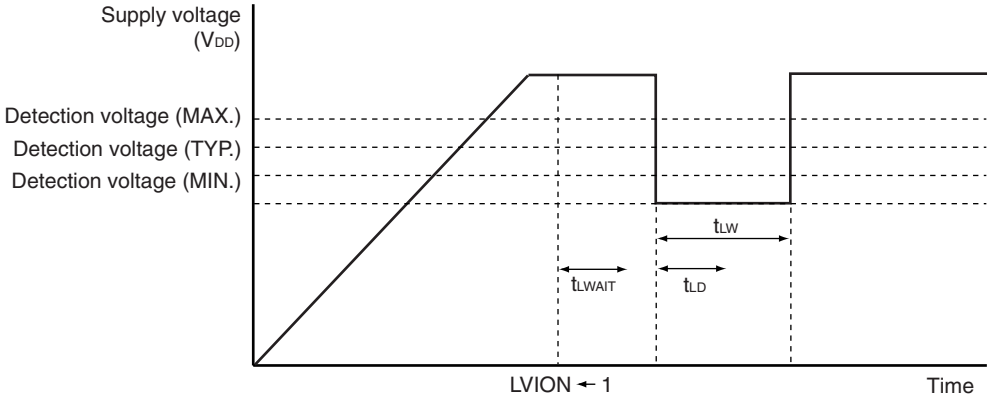
Notes 1. Time required from voltage detection to interrupt output or internal reset signal generation.

2. Time required from setting LVION to 1 to operation stabilization.

Remarks 1. $V_{LVI0} > V_{LVI1} > V_{LVI2} > V_{LVI3} > V_{LVI4} > V_{LVI5} > V_{LVI6} > V_{LVI7} > V_{LVI8} > V_{LVI9}$

2. $V_{POC} < V_{LVIm}$ (m = 0 to 9)

LVI Circuit Timing



Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Release signal set time	t_{SREL}		0			μs

★ **Flash Memory Programming Characteristics (T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

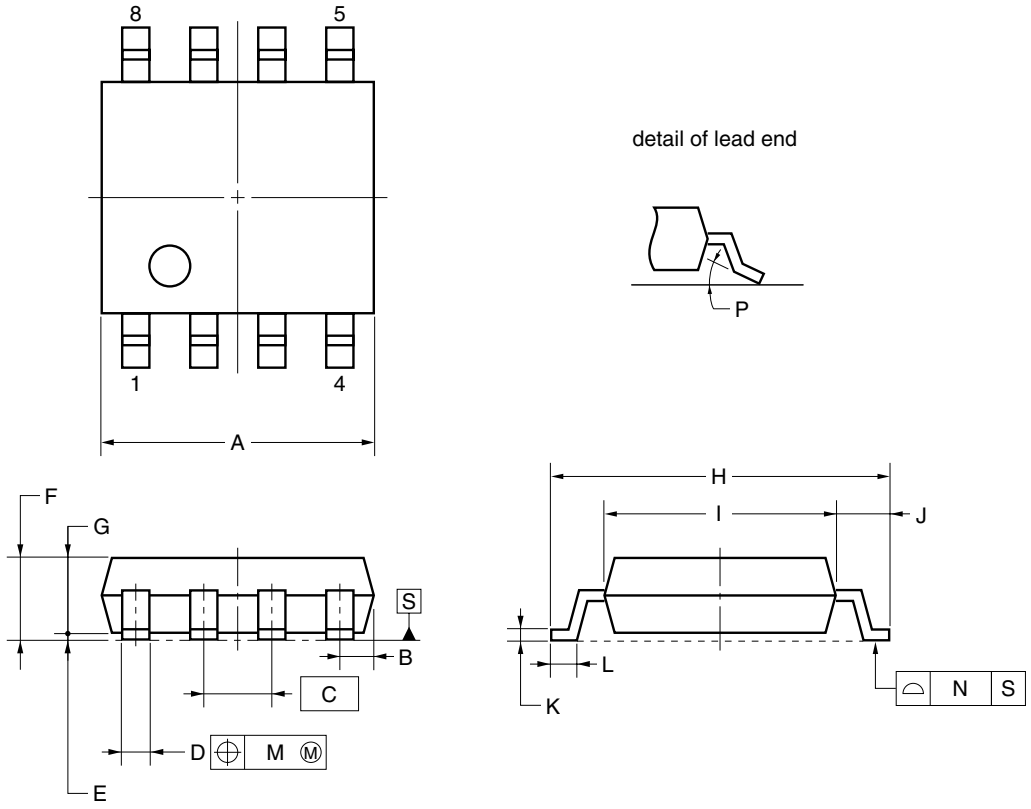
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current	I_{DD}	V_{DD} = 5.5 V				7.0	mA
Erasure count[Note] (per 1 block)	N_{ERASE}	T_A = –10 to +85°C		1000			Times
		T_A = –40 to +85°C		T.B.D.			Times
Chip erase time	T_{CERASE}	T_A = –10 to +85°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			0.90	s
			3.5 V ≤ V_{DD} < 4.5 V			1.00	s
			2.7 V ≤ V_{DD} < 3.5 V			1.20	s
		T_A = –10 to +85°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			3.52	s
			3.5 V ≤ V_{DD} < 4.5 V			3.92	s
			2.7 V ≤ V_{DD} < 3.5 V			4.69	s
		T_A = –40 to +85°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			T.B.D.	s
			3.5 V ≤ V_{DD} < 4.5 V			T.B.D.	s
			2.7 V ≤ V_{DD} < 3.5 V			T.B.D.	s
		T_A = –40 to +85°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			T.B.D.	s
			3.5 V ≤ V_{DD} < 4.5 V			T.B.D.	s
			2.7 V ≤ V_{DD} < 3.5 V			T.B.D.	s
Block erase time	T_{BERASE}	T_A = –10 to +85°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			0.48	s
			3.5 V ≤ V_{DD} < 4.5 V			0.53	s
			2.7 V ≤ V_{DD} < 3.5 V			0.63	s
		T_A = –10 to +85°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			1.86	s
			3.5 V ≤ V_{DD} < 4.5 V			2.07	s
			2.7 V ≤ V_{DD} < 3.5 V			2.48	s
		T_A = –40 to +85°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			T.B.D.	s
			3.5 V ≤ V_{DD} < 4.5 V			T.B.D.	s
			2.7 V ≤ V_{DD} < 3.5 V			T.B.D.	s
		T_A = –40 to +85°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			T.B.D.	s
			3.5 V ≤ V_{DD} < 4.5 V			T.B.D.	s
			2.7 V ≤ V_{DD} < 3.5 V			T.B.D.	s
Byte write time	T_{WRITE}	T_A = –10 to +85°C, N_{ERASE} ≤ 1000				150	μs
		T_A = –40 to +85°C, N_{ERASE} ≤ 1000				T.B.D.	μs
Internal verify	T_{VERIFY}	Per 1 block				6.8	ms
		Per 1 byte				27	μs
Blank check	T_{BLKCHK}	Per 1 block				480	μs
Retention years		T_A = –10 to +85°C, N_{ERASE} ≤ 1000		10			Years
		T_A = –40 to +85°C, N_{ERASE} ≤ 1000		T.B.D.			Years

Note Depending on the erasure count (N_{ERASE}), the erase time varies. Refer to the chip erase time and block erase time parameters.

Remark When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

19.1 Package drawing of the 78K0S/KU1+

★ 8-PIN PLASTIC SOP (5.72 mm (225))



NOTE

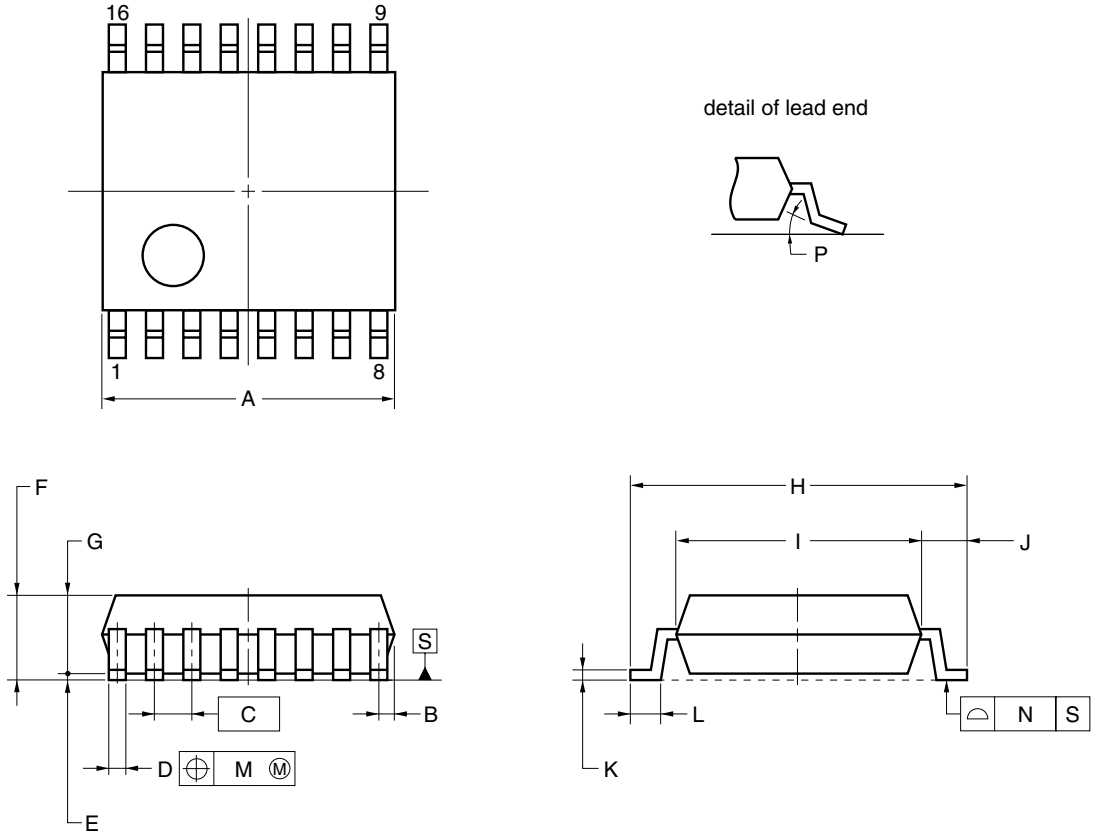
Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	$5.2^{+0.17}_{-0.20}$
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.15
J	1.1±0.2
K	$0.17^{+0.08}_{-0.07}$
L	0.6±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

S8GM-50-225B-6

19.2 Package drawing of the 78K0S/KY1+

★ 16-PIN PLASTIC SSOP (5.72 mm (225))



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2±0.3
B	0.475 MAX.
C	0.65 (T.P.)
D	0.22±0.08
E	0.125±0.075
F	1.565±0.235
G	1.44
H	6.2±0.3
I	4.4±0.2
J	0.9±0.2
K	$0.17^{+0.08}_{-0.07}$
L	0.5±0.2
M	0.10
N	0.10
P	5°±5°

P16GM-65-225B-5

APPENDIX A DEVELOPMENT TOOLS

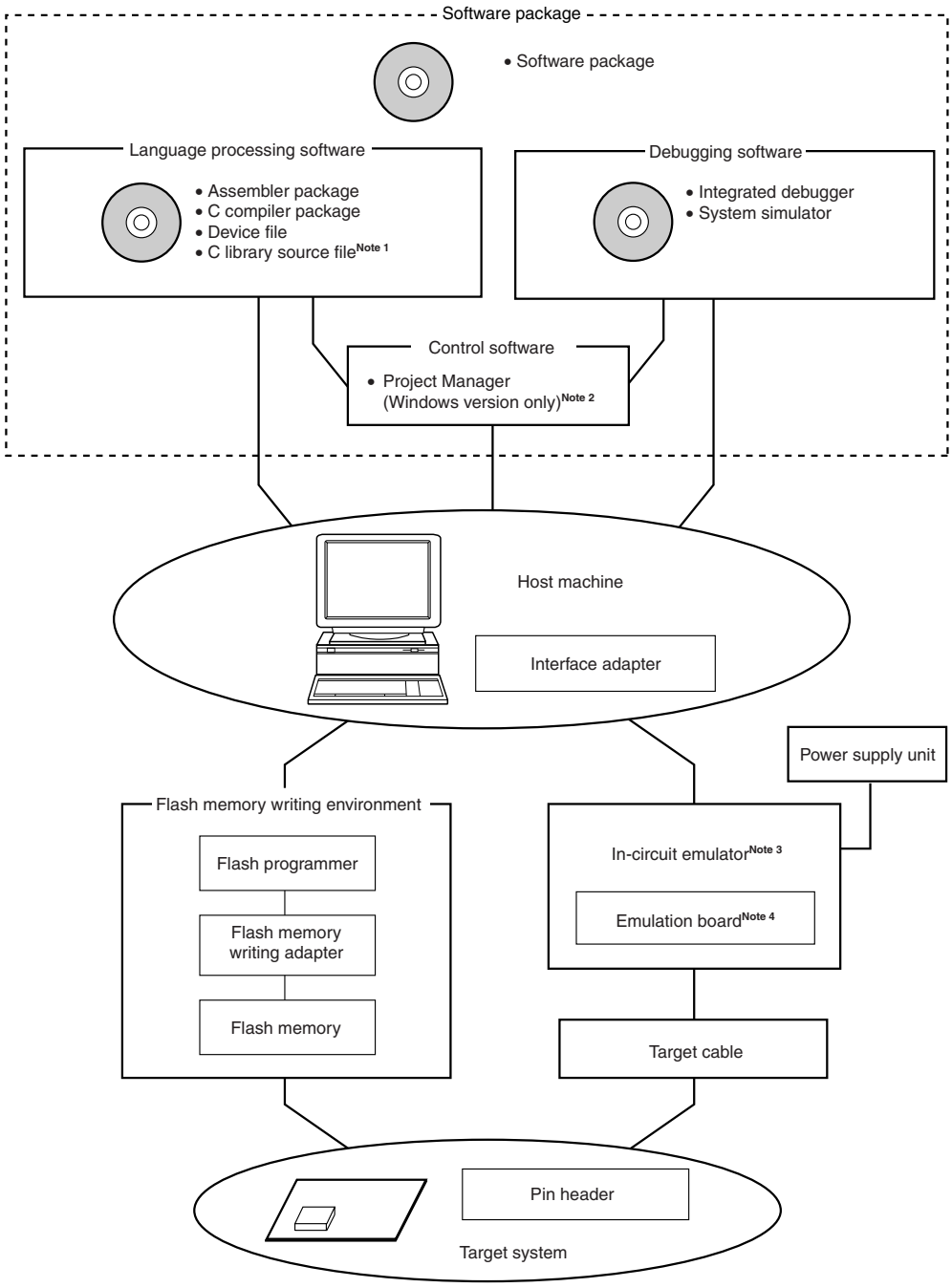
The following development tools are available for development of systems using the 78K0S/KU1+ and 78K0S/KY1+. Figure A-1 shows development tools.

- Compatibility with PC98-NX series
  Unless stated otherwise, products which are supported by IBM PC/AT™ and compatibles can also be used with the PC98-NX series. When using the PC98-NX series, therefore, refer to the explanations for IBM PC/AT and compatibles.

- Windows™
  Unless stated otherwise, “Windows” refers to the following operating systems.
  - Windows 98
  - Windows NT™ Ver. 4.0
  - Windows 2000
  - Windows XP

★ **Figure A-1. Development Tools (1/2)**

(1) When using the in-circuit emulator IE-78K0S-NS or IE-78K0S-NS-A



Notes 1. The C library source file is not included in the software package.

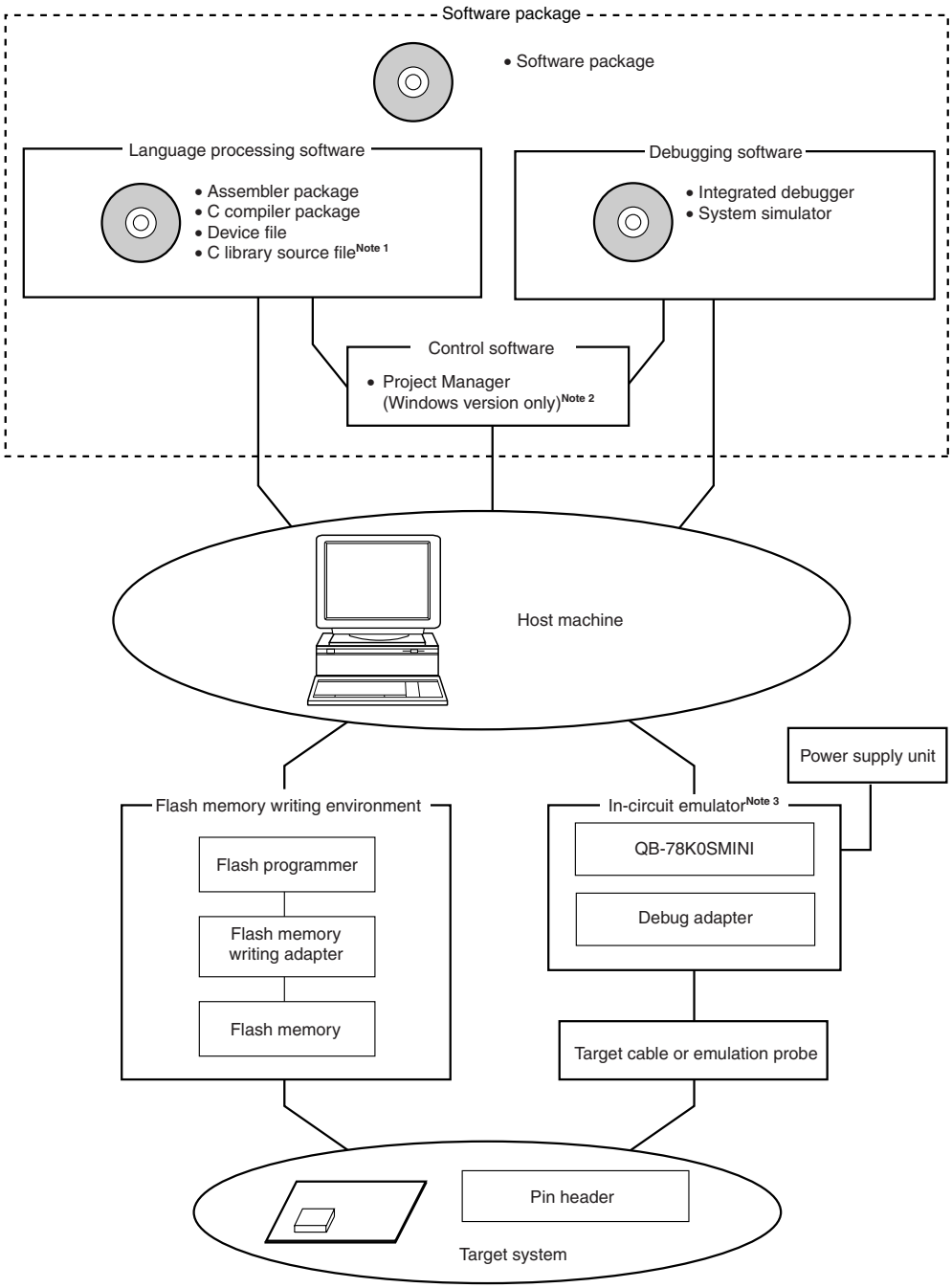
2. The Project Manager PM plus is included in the assembler package.
PM plus is used only in the Windows environment.

3. All products other than the in-circuit emulators IE-78K0S-NS and IE-78K0S-NS-A are optional.

4. The in-circuit emulator IE-789234-NS-EM1 is provided with the target cable.

★ **Figure A-1. Development Tools (2/2)**

(2) When using the in-circuit emulator QB-78K0SKX1MINI



Notes 1. The C library source file is not included in the software package.

2. The Project Manager PM plus is included in the assembler package.
PM plus is used only in the Windows environment.

3. The in-circuit emulator QB-78K0SKX1MINI is provided with the integrated debugger ID78K0S-QB, the flash memory programmer PG-FPL2, a power supply unit, and a target cable. Other products are optional.

A.1 Software Package

SP78K0S Software package	This is a package that bundles the software tools required for development of the 78K/0S Series. The following tools are included. RA78K0S, CC78K0S, ID78K0S-NS, SM+ for 78K0S[Note 1], SM78K0S[Notes 2], and device files
	Part number: μS××××SP78K0S

Notes 1. SM+ for 78K0S is not included in SP78K0S Ver. 2.00 or earlier.

2. The SM78K0S does not support the 78K0S/Kx1+.

3. The DF789234 is not included in SP78K0S Ver. 2.00 or earlier.

Remark ×××× in the part number differs depending on the operating system to be used.

μS××××SP78K0S

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT and compatibles	Japanese Windows	CD-ROM
BB17		English Windows	

A.2 Language Processing Software

RA78K0S Assembler package	Program that converts program written in mnemonic into object code that can be executed by microcontroller. In addition, automatic functions to generate symbol table and optimize branch instructions are also provided. Used in combination with device file (DF789234) (sold separately). **<Caution when used in PC environment>** The assembler package is a DOS-based application but may be used under the Windows environment by using PM plus of Windows (included in the assembler package).
	Part number: μS××××RA78K0S
CC78K0S C library package	Program that converts program written in C language into object codes that can be executed by microcontroller. Used in combination with assembler package (RA78K0S) and device file (DF789234) (both sold separately). **<Caution when used in PC environment>** The C compiler package is a DOS-based application but may be used under the Windows environment by using PM plus of Windows (included in the assembler package).
	Part number: μS××××CC78K0S
★ DF789234[Note 1] Device file	File containing the information inherent to the device. Used in combination with other tools (RA78K0S, CC78K0S, ID78K0S-NS, ID78K0S-QB, or SM+ for 78K0S) (all sold separately).
	Part number: μS××××DF789234
CC78K0S-L[Note 2] C library source file	Source file of functions constituting object library included in C compiler package. Necessary for changing object library included in C compiler package according to customer's specifications. Since this is the source file, its working environment does not depend on any particular operating system.
	Part number: μS××××CC78K0S-L

Notes 1. DF789234 is a common file that can be used with RA78K0S, CC78K0S, ID78K0S-NS, ID78K0S-QB and SM+ for 78K0S.

2. CC78K0S-L is not included in the software package (SP78K0S).

★ **Remark** ××××in the part number differs depending on the host machine and operating system to be used.

μS××××RA78K0S
μS××××CC78K0S
μS××××CC78K0S-L

××××	Host Machine	OS	Supply Media
AB17	PC-9800 series, IBM PC/AT and compatibles	Japanese Windows	CD-ROM
BB17		English Windows	
3P17	HP9000 series 700™	HP-UX™ (Rel.10.10)	
3K17	SPARCstation™	SunOS™ (Rel.4.1.4), Solaris™ (Rel.2.5.1)	

μS××××DF789234

××××	Host Machine	OS	Supply Media
AB13	PC-9800 series, IBM PC/AT and compatibles	Japanese Windows	3.5” 2HD FD
BB13		English Windows	

A.3 Control Software

★ PM plus Project manager	This is control software designed so that the user program can be efficiently developed in the Windows environment. With this software, a series of user program development operations, including starting the editor, build, and starting the debugger, can be executed on the PM plus. **<Caution>** The PM plus is included in the assembler package (RA78K0S). It can be used only in the Windows environment.

A.4 Flash Memory Writing Tools

FlashPro4 (FL-PR4, PG-FP4) Flash memory programmer	Flash programmer dedicated to the microcontrollers incorporating a flash memory
★ PG-FPL2 Flash memory programmer	Flash programmer dedicated to the microcontrollers incorporating a flash memory Provided with the in-circuit emulator QB-78K0SKX1MINI.
★ FA-78F9202GR-AND-MX[Note] ★ FA-78F9212GR-JJG-MX[Note] Flash memory writing adapter	Flash memory writing adapter. Used in connection with FlashPro4. • FA-78F9202GR-AND-MX: For 78K0S/KU1+ • FA-78F9212GR-JJG-MX: For 78K0S/KY1+

Note Under development

Remark FL-PR4, FA-78F9202GR-AND-MX, and FA-78F9212GR-JJG-MX are products of Naito Densei Machida Mfg. Co., Ltd.
For further information, contact: Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191)

A.5 Debugging Tools (Hardware)

A.5.1 When using in-circuit emulator IE-78K0S-NS or IE-78K0S-NS-A

IE-78K0S-NS In-circuit emulator	In-circuit emulator for debugging hardware and software of application system using 78K/0S Series. Supports integrated debugger (ID78K0S-NS). Used in combination with AC adapter, emulation probe, and interface adapter for connecting the host machine.
IE-78K0S-NS-A In-circuit emulator	This in-circuit emulator has a coverage function in addition to the functions of the IE-78K0S-NS, and enhanced debugging functions such as an enhanced tracer function and timer function.
IE-70000-MC-PS-B AC adapter	Adapter for supplying power from 100 to 240 VAC outlet.
IE-70000-CD-IF-A PC card interface	PC card and interface cable required when using a notebook type PC as the host machine (PCMCIA socket supported).
IE-70000-PC-IF-C Interface adapter	Adapter required when using IBM PC/AT and compatibles as the host machine (ISA bus supported).
IE-70000-PCI-IF-A Interface adapter	Adapter required when using a personal computer incorporating the PCI bus is used as the host machine.
★ IE-789234-NS-EM1 Emulation board	Emulation board for emulating the peripheral hardware inherent to the device. Used in combination with in-circuit emulator. A target cable is provided.
★ Specifications of pin header on target system	0.635 mm × 0.635 mm (height: 6 mm)

★ A.5.2 When using in-circuit emulator QB-78K0SKX1MINI

QB-78K0SKX1MINI In-circuit emulator	In-circuit emulator for debugging hardware and software of application system using 78K0S/Kx1+ Series. Supports integrated debugger (ID78K0S-QB). Used in combination with AC adapter, target cable, and USB interface cable for connecting the host machine.
Specifications of pin header on target system	0.635 mm × 0.635 mm (height: 6 mm)

A.6 Debugging Tools (Software)

ID78K0S-NS (supporting in-circuit emulator IE-78K0S-NS/ IE-78K0S-NS-A) Integrated debugger	This debugger supports the in-circuit emulators for the 78K/0S Series. ID78K0S-NS is Windows-based software. This debugger has enhanced debugging functions supporting C language. By using its window integration function that associates the source program, disassemble display, and memory display with trace results, the trace results can be displayed corresponding to the source program. It is used with a device file (DF789234) (sold separately).
	Part number: μS××××ID78K0S-NS
★ ID78K0S-QB (supporting in-circuit emulator QB-78K0SKX1MINI) Integrated debugger	This debugger supports the in-circuit emulators for the 78K0S/Kx1+ Series. ID78K0S-QB is Windows-based software. Provided with the debug function supporting C language, source programming, disassemble display, and memory display are possible. This is used with the device file (DF789234) (sold separately). It is provided with the in-circuit emulator QB-78K0SKX1MINI.
	Ordering number: μS××××ID78K0S-QB (not for sale)
★ SM+ for 78K0S[Notes 1] System simulator	This is a system simulator for the 78K/0S series. SM+ for 78K0S is Windows-based software. This simulator can execute C-source-level or assembler-level debugging while simulating the operations of the target system on the host machine. By using SM+ for 78K0S, the logic and performance of the application can be verified independently of hardware development. Therefore, the development efficiency can be enhanced and the software quality can be improved. This simulator is used with a device file (DF789234) (sold separately).
	Part number: μS××××SM789234-B
★ DF789234[Notes 2] Device file	This is a file that has device-specific information. It is used with the RA78K0S, CC78K0S, ID78K0S-NS, ID78K0S-QB, and SM+ for 78K0S (all sold separately).
	Part number: μS××××DF789234

Notes 1. Under development

★ **2.** DF789234 is a common file that can be used with the RA78K0S, CC78K0S, ID78K0S-NS, ID78K0S-QB, and SM+ for 78K0S.

Remark ××××in the part number differs depending on the operating system to be used and the supply medium.

μS××××ID78K0S-NS
μS××××ID78K0S-QB
μS××××SM789234-NS

××××	Host Machine	OS	Supply Medium
BB13	PC-9800 series, IBM PC/AT and compatibles	English Windows	3.5” 2HD FD
AB17		Japanese Windows	CD-ROM
BB17		English Windows	

μS××××DF789234

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT and compatibles	Japanese Windows	3.5” 2HD FD
BB13		English Windows	

APPENDIX B REGISTER INDEX

B.1 Register Index (Register Name)

[P]

[R]

[W]

B.2 Register Index (Symbol)

★

APPENDIX C REVISION HISTORY

C.1 Major Revisions in This Edition

(1/2)

Page	Description
Throughout	Addition of settings for port mode register 4 (PM4) when using 78K0S/KU1+
	Deletion of high-speed Ring-OSC mode register (HSRCM)
p. 15	Addition of Part Number to **1.3 Ordering Information**
p. 27	Modification of **Type36** in **Figure 2-1 Pin I/O Circuits**
p. 40	Addition of **Note 4** to **Table 3-3 Special Function Registers (1/2)**
p. 51	Addition of **Remarks 1, 2** in **Table 4-1 Port Functions**
p. 54	Addition of **Figure 4-3 Block Diagram of P22**
pp. 72, 74, 76	Modification of operation stop time in the following figures. • **Figure 5-8 Timing Chart of Default Start by High-Speed Ring-OSC Oscillator** • **Figure 5-10 Timing Chart of Default Start by Crystal/Ceramic Oscillator** • **Figure 5-12 Timing of Default Start by External Clock Input**
pp. 82-84	Addition of **Cautions** to **6.2 Configuration of 16-Bit Timer/Event Counter 00 (1) 16-bit timer counter 00 (TM00), (2) 16-bit timer capture/compare register 000 (CR000),** and **(3) 16-bit timer capture/compare register 010 (CR010)**
p. 86	Addition of **Cautions** in **Figure 6-5 Format of 16-Bit Timer Mode Control Register 00 (TMC00)**
p. 89	Addition of **Caution 6** to **Figure 6-7 Format of 16-Bit Timer Output Control Register 00 (TOC00)**
p. 90	Modification of **Caution 3** and addition of **Caution 4** in **Figure 6-8 Format of Prescaler Mode Register 00 (PRM00)**
p. 95	Addition of **(1) INTTM000 generation timing immediately after operation starts** : The setting value +2 of CR000 to 1 **Figure 6-17 External Event Counter Operation Timing (with Rising Edge Specified)**
p. 101	Modification of **Note** in **Figure 6-24 Control Register Settings for Pulse Width Measurement with Free-Running Counter and Two Capture Registers (with Rising Edge Specified)**
p. 114	Modification and addition to **6.5 Cautions Related to 16-Bit Timer/Event Counter 00**
p. 135	Modification of **Table 8-1 Loop Detection Time of Watchdog Timer**
pp. 138, 139	Addition of **Caution 4** and modification to **Figure 8-2 Format of Watchdog Timer Mode Register (WDTM)**
p. 141	Modification of **Figure 8-4 Status Transition Diagram When "Low-Speed Ring-OSC Cannot Be Stopped" Is Selected by Option Byte**
p. 143	Modification of **Figure 8-5 Status Transition Diagram When "Low-Speed Ring-OSC Can Be Stopped by Software" Is Selected by Option Byte**
pp. 144, 145	Modification of operation stop time in the following figures • **Figure 8-6 Operation in STOP Mode (WDT Operation Clock: Clock to Peripheral Hardware)** • **Figure 8-7 Operation in STOP Mode (WDT Operation Clock: Low-Speed Ring-OSC Clock)**
p. 146	Addition of **Note** to and modification of **Figure 9-1 Timing of A/D Converter Sampling and A/D Conversion**
p. 147	Addition of **Note 1** and **Remark 2** to and modification of **Table 9-1 Sampling Time and A/D Conversion Time**
p. 148	Modification of **Figure 9-2 Block Diagram of A/D Converter**
pp. 151, 152	Modification of **Note 5**, addition of **Notes 1, 2**, and **Remark 2** to, and modification of **Figure 9-3 Format of A/D Converter Mode Register (ADM)**
p. 157	Modification of **Figure 9-11 Relationship Between Analog Input Voltage and A/D Conversion Result**
pp. 162, 163	Modification of **9.6 (1) Operating current in STOP mode, (4) Noise countermeasures,** and **(6) Input impedance of ANI0 to ANI3 pins**

(2/2)

Page	Description
p. 162	Modification of capacitor value in **Figure 9-19 Analog Input Pin Connection**
p. 164	Modification of **Figure 9-21 Internal Equivalent Circuit of ANIn Pin** and **Table 9-4 Resistance and Capacitance Values (Reference Values) of Equivalent Circuit**
p. 174	Modification of description on operation stop time in **11.1.1 (2) STOP mode**
p. 178	Modification of **Note** in **Figure 11-3 HALT Mode Release by Reset Input**
pp. 180, 181	Modification of operation stop time in the following figures. • **Figure 11-4 Operation Timing When STOP Mode Is Released** • **Figure 11-5 STOP Mode Release by Interrupt Request Generation**
p. 182	Modification of **Note** in **Figure 11-6 STOP Mode Release by Reset Input**
pp. 184-187	Modification of the following figures • **Figure 12-1 Block Diagram of Reset Function** • **Figure 12-2 Timing of Reset by $\overline{\text{RESET}}$ Input** • **Figure 12-3 Timing of Reset by Overflow of Watchdog Timer** • **Figure 12-4 Reset Timing by $\overline{\text{RESET}}$ Input in STOP Mode**
p. 196	Addition of **Note 1** to **Figure 14-2 Format of Low-Voltage Detect Register (LVIM)**
p. 197	Addition of **Note** to **Figure 14-3 Format of Low-Voltage Detection Level Select Register (LVIS)**
p. 201	Addition of **Note** to **14.5 Cautions for Low-Voltage Detector <Action> (2) When used as interrupt**
p. 207	Revision of **CHAPTER 16 FLASH MEMORY**
pp. 274, 275, 277-280, 282, 285	Modification or addition of values in the following characteristics in **CHAPTER 18 ELECTRICAL SPECIFICATIONS (TARGET VALUES)** • Absolute maximum ratings Output current high, output current low, and operating ambient temperature • X1 oscillator characteristics • DC characteristics • AC characteristics Basic operation cycle time (minimum instruction execution time) • A/D Converter Characteristics • Flash memory programming characteristics
pp. 286, 287	Modification of **19.1 Package drawing of the 78K0S/KU1+** and **19.2 Package drawing of the 78K0S/KY1+**
pp. 289, 290	Modification **Figure A-1 Development Tools**
pp. 291, 292	Modification of device file names and **Remark** in **A.2 Language Processing Software**
p. 292	Addition of project manager name to **A.3 Control Software**
p. 292	Addition of PG-FPL2 to **A.4 Flash Memory Writing Tools,**
p. 293	Modification of emulation board name used when the IE-78K0S-NS or IE-78K0S-NS-A is used, and addition of **Specification of pin header on target system** to **A.5.1 When using in-circuit emulator IE-78K0S-NS or IE-78K0S-NS-A**
p. 293	Addition of **A.5.2 When using in-circuit emulator QB-78K0SKX1MINI**
pp. 294, 295	Modification of system simulator name, device file name, and **Remark** in and addition of ID78K0S-QB to **A.6 Debugging Tools (Software)**
p. 300	Addition of **APPENDIX C REVISION HISTORY**