



Integrated Device Technology, Inc.

16-BIT CMOS MICROPROCESSOR SLICE

IDT49C402
IDT49C402A
IDT49C402B

T-49-17-51

FEATURES:

- Functionally equivalent to four 2901s and one 2902
- IDT49C402B is 60% faster than four 2901Cs and one 2902A
- Expanded two-address architecture with independent, simultaneous access to two 64 x 16 register files
- Expanded destination functions with 8 new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- Clamp diodes on all inputs provide noise suppression
- Fully cascadable
- 68-pin ceramic PGA, Plastic Leaded Chip Carrier (PLCC), and Ceramic Flatpack (25 mil centers)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

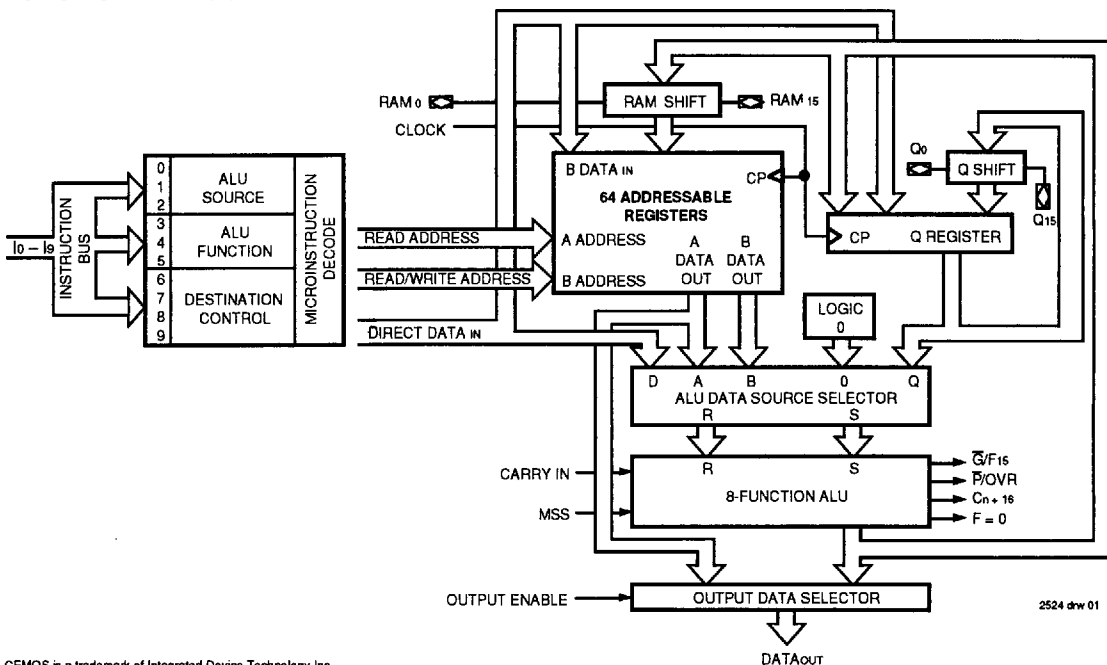
The IDT49C402s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

The IDT49C402s include all of the normal functions associated with standard 2901 bit-slice operation: a) a 3-bit instruction field (I₀, I₁, I₂) which controls the source operand selection for the ALU; b) a 3-bit microinstruction field (I₃, I₄, I₅) used to control the eight possible functions of the ALU; c) eight destination control functions which are selected by the microcode inputs (I₆, I₇, I₈); and d) a tenth microinstruction input, I₉, offering eight additional destination control functions. This I₉ input, in conjunction with I₆, I₇ and I₈, allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU, and having the RAM A data output port available at the Y output pins of the device.

Also featured is an on-chip dual-port RAM that contains 64-words-by-16 bits—four times the number of working registers in a 2901.

The IDT49C402s are fabricated using CEMOS™, a CMOS technology designed for high performance and high reliability. These performance-enhanced devices feature both bipolar speed and bipolar output drive capabilities, while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

FUNCTIONAL BLOCK DIAGRAM



2524 drw 01

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

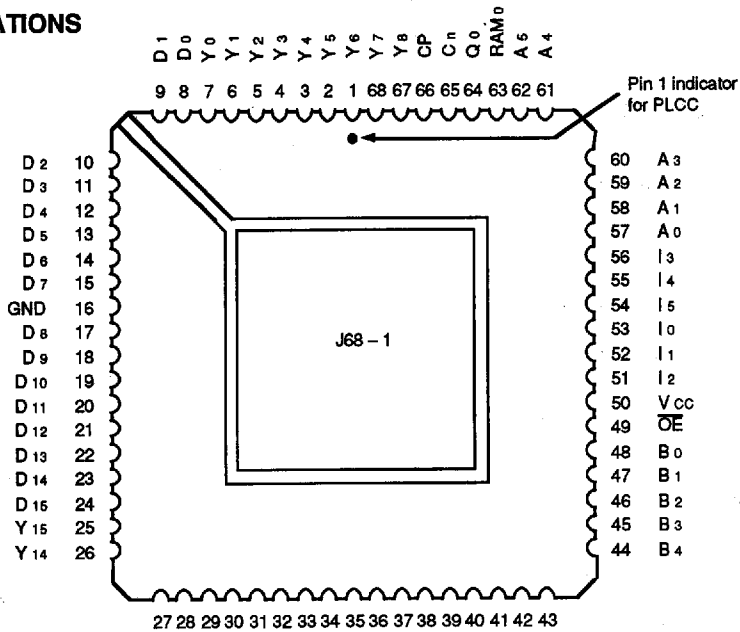
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IDT49C402/A/B
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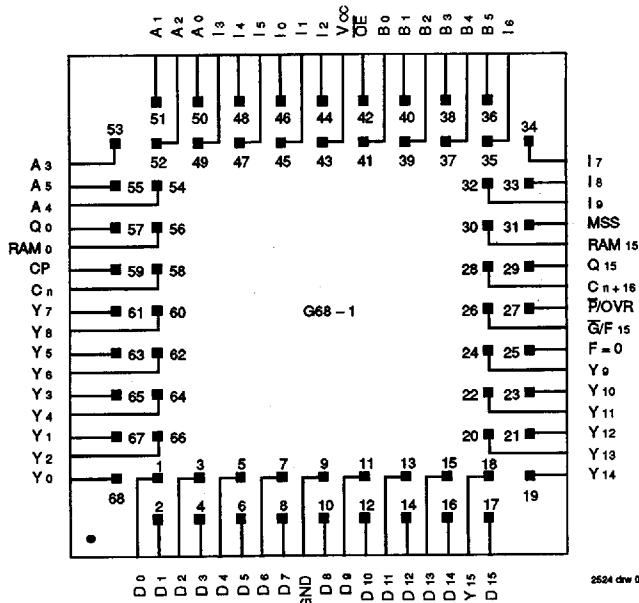
MILITARY AND COMMERCIAL TEMPERATURE RANGES

PIN CONFIGURATIONS



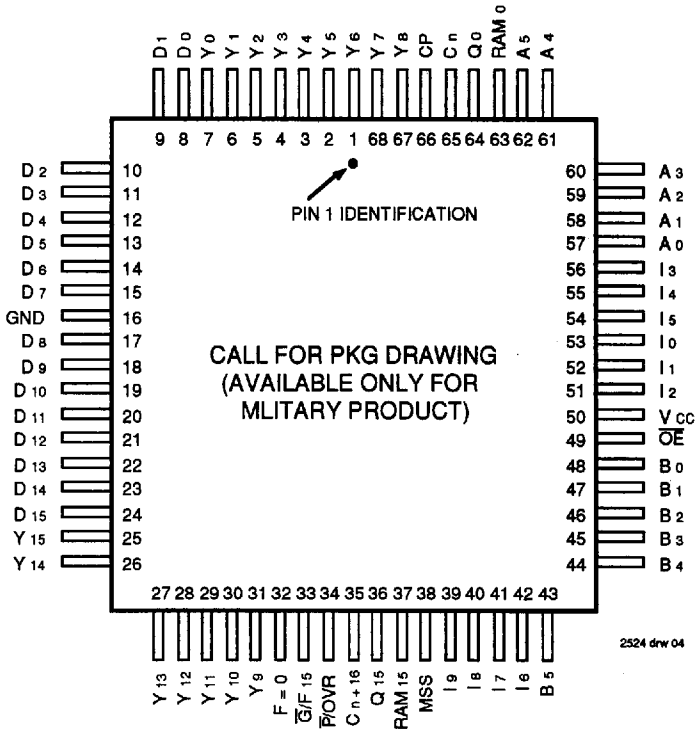
2524 drw 02

PLCC
TOP VIEW



2524 drw 03

PGA
TOP VIEW



FLATPACK
TOP VIEW

IDT49C402/A/B
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PIN DESCRIPTIONS

Pin Name	I/O	Description
A ₀ - A ₅	I	Six address inputs to the register file which selects one register and displays its contents through the A port.
B ₀ - B ₅	I	Six address inputs to the register file which selects one of the registers in the file, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the clock goes LOW.
I ₀ - I ₉	I	Ten instruction control lines which determine what data source will be applied to the ALU I ₀ (0, 1, 2), what function the ALU will perform I ₃ (3, 4, 5) and what data is to be deposited in the Q Register or the register file I ₆ (6, 7, 8, 9). Original 2901 destinations are selected if I ₉ is disconnected in this mode, proper I ₉ bias is achieved by an external pullup resistor to V _{cc} (47K ohms recommended).
D ₀ - D ₁₅	I	Sixteen-bit direct data inputs which are the data source for entering external data into the device ALU, Q Register or RAM. D ₀ is the LSB.
Y ₀ - Y ₁₅	O	Sixteen three-state output lines which, when enabled, display either the sixteen outputs of the ALU or the data on the A port of the register stack. This is determined by the destination code I ₆ (6, 7, 8, 9).
\bar{G}/F_{15}	O	A multipurpose pin which indicates the carry generate (\bar{G}) function at the least significant and intermediate slices or as F ₁₅ , the most significant ALU output (sign bit). \bar{G}/F_{15} selection is controlled by the MSS pin. If MSS = HIGH, F ₁₅ is enabled. If MSS = LOW, \bar{G} is enabled.
F = 0	O	Open drain output which goes HIGH if the F ₀ - F ₁₅ ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C _n	I	Carry-in to the internal ALU.
C _{n+16}	O	Carry-out of the ALU.
Q ₁₅ RAM ₁₅	I/O	Bidirectional lines controlled by I ₆ (6, 7, 8, 9). Both are three-state output drivers connected to the TTL-compatible inputs. When the destination code on I ₆ (6, 7, 8, 9) indicates an up shift, the three-state outputs are enabled, the MSB of the Q Register is available on the Q ₁₅ pin and the MSB of the ALU output is available on the RAM ₁₅ pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q ₀ RAM ₀	I/O	Both bidirectional lines function identically to Q ₁₅ and RAM ₁₅ lines except they are the LSB of the Q Register and RAM.
$\bar{O}E$	I	Output enable. When pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
\bar{P}/OVR	O	A multipurpose pin which indicates the carry propagate (\bar{P}) output for performing a carry lookahead operation or overflow (OVR) the Exclusive-OR of the carry-in and carry-out of the ALU MSB. OVR, at the most significant end of the word, indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. \bar{P}/OVR selection is controlled by the MSS pin. If MSS = HIGH, OVR is enabled. If MSS = LOW, \bar{P} is enabled.
CP	I	The clock input LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 64 x 16 RAM. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.
MSS	I	When HIGH, enables OVR and F ₁₅ on the \bar{P}/OVR and \bar{G}/F_{15} pins. When LOW, enables \bar{G} and \bar{P} on these pins. If left open, internal pullup resistor to V _{cc} provides declaration that the device is the most significant slice.

2524 ibi 01

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DEVICE ARCHITECTURE

The IDT49C402 CMOS bit-slice microprocessor is configured sixteen bits wide and is cascadable to any number of bits (16, 32, 48, 64). Key elements which make up this 16-bit microprocessor slice are the 1) register file (64 x 16 dual-port RAM) with shifter; 2) ALU and 3) Q Register and shifter.

REGISTER FILE — A 16-bit data word from one of the 64 RAM registers can read from the A port as selected by the 6-bit A address field. Simultaneously, the same data word, or any other word from the 64 RAM registers, can be read from the B port as selected by the 6-bit B address field. New data is written into the RAM register location selected by the B address field during the clock (CP) LOW time. Two sixteen-bit latches hold the RAM A port and B port during the clock (CP) LOW time, eliminating any data races. During clock HIGH, these latches are transparent, reading the data selected by the A and B addresses. The RAM data input field is driven from a four-input multiplexer that selects the ALU output or the D inputs. The ALU output can be shifted up one position, down one position or not shifted. Shifting data operations involves the RAM₁₅ and RAM₀ I/O pins. For a shift up operation, the RAM shifter MSB is connected to an enabled RAM₁₅ I/O output, while the RAM₀ I/O input is selected as the input to the LSB. During a shift down operation, the RAM shifter LSB is connected to an enabled RAM₀ I/O output, while the RAM₁₅ I/O input is selected as the input to the MSB.

ALU — The ALU can perform three binary arithmetic and five logic operations on the two 16-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer, with both having a zero source operand. Both multiplexers are controlled by the I(0, 1, 2) inputs. This multiplexer configuration enables the user to select the various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs I(3, 4, 5) are used to select the ALU function. This high-speed ALU cascades to any word length, providing carry-in (C_n), carry-out (C_{n+16}) and an open-drain (F = 0) output. When all bits of the

ALU are zero, the pull-down device of F = 0 is off, allowing a wire-OR of this pin over all cascaded devices. Multipurpose pins \bar{G}/F_{15} and \bar{P}/OVR are aimed at accelerating arithmetic operations. For intermediate and least significant slices, the MSS pin is programmed LOW, selecting the carry-generate (\bar{G}) and carry propagate (\bar{P}) output functions to be used by carry lookahead logic. For the most significant slice, MSS is programmed HIGH, selecting the sign-bit (F₁₅) and the two's complement overflow (OVR) output functions. The sign bit (F₁₅) allows the ALU sign bit to be monitored without enabling the three-state ALU outputs. The overflow (OVR) output is high when the two's complement arithmetic operation has overflowed into the sign bit, as logically determined from the Exclusive-OR of the carry-in and carry-out of the most significant bit of the ALU. The ALU data outputs are available at the three-state outputs Y(0-15) or as inputs to the RAM register file and Q register under control of the I(6, 7, 8, 9) instruction inputs.

Q REGISTER — The Q Register is a separate 16-bit file intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 4-input multiplexer. In the no-shift mode, the multiplexer enters the ALU F output or Direct Data into the Q Register. In either the shift up or shift down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q₀ and Q₁₅, which operate comparably to the RAM shifter. They are controlled by the I(6, 7, 8, 9) inputs.

The clock input of the IDT49C402 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and I(6, 7, 8, 9) define the RAM as the destination, new data will be written into the RAM file defined by the B address field.

ALU SOURCE OPERAND CONTROL

Mnemonic	Microcode				ALU Source Operands	
	I ₂	I ₁	I ₀	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

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ALU FUNCTION CONTROL

Mnemonic	Microcode				ALU Function	Symbol
	I ₅	I ₄	I ₃	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S - R
SUBS	L	H	L	2	R Minus S	R - S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	R AND S	R ∧ S
EXOR	H	H	L	6	R EX-OR S	R ⊕ S
EXNOR	H	H	H	7	R EX-NOR S	R ⊘ S

2524 tbl 04

ALU ARITHMETIC MODE FUNCTIONS

Octal		C _n = L		C _n = H	
I ₅ , 4, 3	I ₂ , 1, 0	Group	Function	Group	Function
0	0	ADD	A + Q	ADD plus one	A + Q + 1
0	1		A + B		A + B + 1
0	5		D + A		D + A + 1
0	6		D + Q		D + Q + 1
0	2	PASS	Q	Increment	Q + 1
0	3		B		B + 1
0	4		A		A + 1
0	7		D		D + 1
1	2	Decrement	Q - 1	PASS	Q
1	3		B - 1		B
1	4		A - 1		A
2	7		D - 1		D
2	2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2	3		-B - 1		-B
2	4		-A - 1		-A
1	7		-D - 1		-D
1	0	Subtract (1's Comp)	Q - A - 1	Subtract (2's Comp)	Q - A
1	1		B - A - 1		B - A
1	5		A - D - 1		A - D
1	6		Q - D - 1		Q - D
2	0		A - Q - 1		A - Q
2	1		A - B - 1		A - B
2	5		D - A - 1		D - A
2	6		D - Q - 1		D - Q

2524 tbl 03

ALU LOGIC MODE FUNCTIONS

Octal		Group	Function
I ₅ , 4, 3	I ₂ , 1, 0		
4	0	AND	A ∧ Q
4	1		A ∧ B
4	5		D ∧ A
4	6		D ∧ Q
3	0	OR	A ∨ Q
3	1		A ∨ B
3	5		D ∨ A
3	6		D ∨ Q
6	0	EX-OR	A ⊕ Q
6	1		A ⊕ B
6	5		D ⊕ A
6	6		D ⊕ Q
7	0	EX-NOR	A ⊘ Q
7	1		A ⊘ B
7	5		D ⊘ A
7	6		D ⊘ Q
7	2	INVERT	Q̄
7	3		B̄
7	4		Ā
7	7		D̄
6	2	PASS	Q
6	3		B
6	4		A
6	7		D
3	2	PASS	Q
3	3		B
3	4		A
3	7		D
4	2	"ZERO"	0
4	3		0
4	4		0
4	7		0
5	0	MASK	Ā ∧ Q
5	1		Ā ∧ B
5	5		D̄ ∧ A
5	6		D̄ ∧ Q

2524 tbl 05

SOURCE OPERAND AND ALU FUNCTION MATRIX (1)

Octal Is, 4, 3	ALU Function	I2, 1, 0 Octal							
		0	1	2	3	4	5	6	7
		ALU Source							
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	Cn = L R Plus S Cn = H	A + Q	A + B	Q	B	A	D + A	D + Q	D
		A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	Cn = L S Minus R Cn = H	Q - A - 1	B - A - 1	Q - 1	B - 1	A - 1	A - D - 1	Q - D - 1	-D - 1
		Q - A	B - A	Q	B	A	A - D	Q - D	-D
2	Cn = L R Minus S Cn = H	A - Q - 1	A - B - 1	-Q - 1	-B - 1	-A - 1	D - A - 1	D - Q - 1	D - 1
		A - Q	A - B	-Q	-B	-A	D - A	D - Q	D
3	R OR S	A V Q	A V B	Q	B	A	D V A	D V Q	D
4	R AND S	A ^ Q	A ^ B	0	0	0	D ^ A	D ^ Q	0
5	R AND S	A ^ Q	A ^ B	Q	B	A	D ^ A	D ^ Q	0
6	R EX-OR S	A V Q	A V B	Q	B	A	D V A	D V Q	D
7	R EX-NOR S	A V Q	A V B	Q	B	A	D V A	D V Q	D

2524 tbl 06

NOTE:

1. + = Plus; - = Minus; ^ = AND; V = EX-OR; V = OR.

ALU DESTINATION CONTROL (1)

Mnemonic	Microcode					RAM Function		Q Register Function		Y Output	RAM Shifter		Q Shifter		
	Is	Is	Ir	Is	Hex Code	Shift	Load	Shift	Load		RAM0	RAM15	Q0	Q15	
OREG	H	L	L	L	8	X	NONE	NONE	F → Q	F	X	X	X	X	Existing 2901 Functions
NOP	H	L	L	H	9	X	NONE	X	NONE	F	X	X	X	X	
RAMA	H	L	H	L	A	NONE	F → B	X	NONE	A	X	X	X	X	
RAMF	H	L	H	H	B	NONE	F → B	X	NONE	F	X	X	X	X	
RAMQD	H	H	L	L	C	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F0	IN15	Q0	IN15	
RAMD	H	H	L	H	D	DOWN	F/2 → B	X	NONE	F	F0	IN15	Q0	X	
RAMQU	H	H	H	L	E	UP	2F → B	UP	2Q → Q	F	IN0	F15	IN0	Q15	
RAMU	H	H	H	H	F	UP	2F → B	X	NONE	F	IN0	F15	X	Q15	
DFF	L	L	L	L	0	NONE	D → B	NONE	F → Q	F	X	X	X	X	New Added IDT49C402 Functions
DFA	L	L	L	H	1	NONE	D → B	NONE	F → Q	A	X	X	X	X	
FDL	L	L	H	L	2	NONE	F → B	NONE	D → Q	F	X	X	X	X	
FDA	L	L	H	H	3	NONE	F → B	NONE	D → Q	A	X	X	X	X	
XQDF	L	H	L	L	4	X	NONE	DOWN	Q/2 → Q	F	X	X	Q0	IN15	
DXF	L	H	L	H	5	NONE	D → B	X	NONE	F	X	X	Q0	X	
XQUF	L	H	H	L	6	X	NONE	UP	2Q → Q	F	X	X	IN0	Q15	
XDF	L	H	H	H	7	X	NONE	NONE	D → Q	F	X	X	X	Q15	

NOTE:

1. X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the impedance state.

B = Register Addressed by B inputs.

UP is toward MSB; DOWN is toward LSB.

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16-BIT CMOS MICROPROCESSOR SLICE

MILITARY AND COMMERCIAL TEMPERATURE RANGES

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
V _{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V _{TERM}	Terminal Voltage with Respect to Ground	-0.5 to V _{CC} + 0.5	-0.5 to V _{CC} + 0.5	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.5	1.5	W
I _{OUT}	DC Output Current	50	50	mA

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested. 2524 tbi 09

NOTE: 2524 tbi 08
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic High Level ⁽⁴⁾	2.0	-	-	V
V _{IL}	Input LOW Level	Guaranteed Logic Low Level ⁽⁴⁾	-	-	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}	-	0.1	5	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND	-	-0.1	-5	μA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. I _{OH} = -8mA MIL.	2.4	4.3	-	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -8mA COM'L.	2.4	4.3	-	
V _{OL}	Output LOW Voltage	V _{CC} = Min. I _{OL} = 8mA MIL.	-	0.3	0.5	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 10mA COM'L.	-	0.3	0.5	
I _{OZ}	Off State (High Impedance) Output Current	V _{CC} = Max. V _O = 0V	-	-0.1	-10	μA
		V _O = V _{CC} (Max.)	-	0.1	10	
I _{OS}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = 0V ⁽³⁾	-15	-30	-70	mA

NOTES: 2524 tbi 10
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS

Commercial: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
I _{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V _{CC} = Max.	MIL.	—	—	10	mA
		V _{IH} = V _{CC} , V _{IL} = 0V f _{CP} = 0, CP = H	COM'L.	—	—	10	
I _{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V _{CC} = Max.	MIL.	—	—	10	mA
		V _{IH} = V _{CC} , V _{IL} = 0V f _{CP} = 0, CP = L	COM'L.	—	—	10	
I _{CCCT}	Quiescent Input Power Supply ⁽⁶⁾ Current (per Input @ TTL High)	V _{CC} = Max., V _{IH} = 3.4V, f _{CP} = 0	MIL.	—	—	1.5	mV Input
			COM'L.	—	—	0.85	
I _{CCD}	Dynamic Power Supply Current	V _{CC} = Max.	MIL.	—	—	7.5	mV MHz
		V _{IH} = V _{CC} , V _{IL} = 0V Outputs Open, $\overline{OE} = L$	COM'L.	—	—	4.5	
I _{CC}	Total Power Supply Current ⁽⁷⁾	V _{CC} = Max., f _{CP} = 10MHz Outputs Open, $\overline{OE} = L$ CP = 50 % Duty cycle V _{IH} = V _{CC} , V _{IL} = 0V	MIL.	—	—	85	mA
			COM'L.	—	—	55	
		V _{CC} = Max., f _{CP} = 10MHz Outputs Open, $\overline{OE} = L$ CP = 50 % Duty cycle V _{IH} = 3.4V, V _{IL} = 0.4V	MIL.	—	—	130	
			COM'L.	—	—	95	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
- Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
- These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
- Guaranteed by design, not production tested.
- I_{CCCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
- Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH} (CDH) + I_{CCQL} (1 - CDH) + I_{CCCT} (NT \times DH) + I_{CCD} (f_{CP})$$

CDH = Clock duty cycle high period
DH = Data duty cycle TTL high period (V_{IN} = 3.4V)
NT = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock input frequency
I_{CCCT} = Quiescent Power Supply Current for TTL level inputs
I_{CCD} = Dynamic Power Supply Current in mA/MHz

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic testing environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

- All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
- Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should

also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.

- Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
- To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using V_{IL} ≤ 0V and V_{IH} ≥ 3V for AC tests.

IDT49C402/A/B
16-BIT CMOS MICROPROCESSOR SLICE

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS

IDT49C402

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402 over the -55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil. (6)	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	50	48	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)	20	21	MHz
Minimum Clock LOW Time	30	30	ns
Minimum Clock HIGH Time	20	20	ns
Minimum Clock Period	50	48	ns


2524 tbl 13

MAXIMUM COMBINATIONAL PROPAGATION DELAYS⁽¹⁾ CL = 50pF

From Input	To Output																Unit
	Y		(MSS = L) G, P		(MSS = H) F15 OVR				Cn + 16		F = 0		RAM0 RAM15		Q0 Q15		
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Address	52	47	47	42	52	47	47	42	38	34	52	47	44	40	-	-	ns
D	35	32	34	31	35	32	34	31	27	25	35	32	28	26	-	-	ns
Cn	29	26	-	-	29	26	27	25	20	18	29	26	23	21	-	-	ns
I0, 1, 2	41	37	30	27	41	37	38	35	29	26	41	37	30	27	-	-	ns
I3, 4, 5	40	36	28	26	40	36	37	34	27	25	40	36	28	26	-	-	ns
I6, 7, 8, 9	26	24	-	-	-	-	-	-	-	-	-	-	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ns
Clock \overline{f}	42	38	41	37	42	38	41	37	30	27	42	38	41	37	25	23	ns

2524 tbl 14

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

Input	CP: 								Unit
	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	20	18	2 ⁽³⁾	1 ⁽³⁾	50 ⁽⁴⁾	50 ⁽⁴⁾	2	1	ns
B Destination Address	20	18	Do not change ⁽²⁾				2	1	ns
D	- ⁽¹⁾	-	-	-	30/40 ⁽⁵⁾	26/36 ⁽⁵⁾	2	1	ns
Cn	-	-	-	-	35	32	0	0	ns
I0, 1, 2	-	-	-	-	45	41	0	0	ns
I3, 4, 5	-	-	-	-	45	41	0	0	ns
I6, 7, 8, 9	12	11	Do not change ⁽²⁾				0	0	ns
RAM0,15, Q0,15	-	-	-	-	12	11	0	0	ns

2524 tbl 15

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path (DATAin → RAM/Q Register). Second value is indirect path (DATAin → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

AC ELECTRICAL CHARACTERISTICS

IDT49C402A

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402A over the -55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil. ⁽⁶⁾	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle) ⁽⁶⁾	23	22	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32) ⁽⁶⁾	35	41	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period ⁽⁶⁾	36	31	ns


2524 tbl 16

MAXIMUM COMBINATIONAL PROPAGATION DELAYS⁽¹⁾ CL = 50pF

From Input	To Output																Unit
	Y		(MSS = L) G, F		(MSS = H) F15 OVR				Cn + 16		F = 0		RAM0 RAM15		Q0 Q15		
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Address	41	37	39	35	41	37	41	37	37	34	41	37	40	36	-	-	ns
D	32	29	29	26	29	26	31	28	27	25	32	29	28	26	-	-	ns
Cn	28	25	-	-	26	24	25	23	20	18	29	26	23	21	-	-	ns
l0, 1, 2	35	32	30	27	35	32	34	31	29	26	35	32	30	27	-	-	ns
l3, 4, 5	35	32	28	26	34	31	34	31	27	25	35	32	28	26	-	-	ns
l6, 7, 8, 9	25	23	-	-	-	-	-	-	-	-	-	-	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ns
Clock \checkmark	34	31	31	28	33	30	34	31	30	27	34	31	34	31	25	23	ns

2524 tbl 17

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

Input	CP: 								Unit
	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	11	10	2 ⁽³⁾	1 ⁽³⁾	25 ⁽⁴⁾	21 ⁽⁴⁾	2	1	ns
B Destination Address	11	10	Do not change ⁽²⁾				2	1	ns
D	- ⁽¹⁾	-	-	-	12/22 ⁽⁵⁾	10/20 ⁽⁵⁾	2	1	ns
Cn	-	-	-	-	17	15	0	0	ns
l0, 1, 2	-	-	-	-	28	25	0	0	ns
l3, 4, 5	-	-	-	-	28	25	0	0	ns
l6, 7, 8, 9	11	10	Do not change ⁽²⁾				0	0	ns
RAM0,15, Q0,15	-	-	-	-	12	11	0	0	ns

NOTES: 2524 tbl 18

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path (DATAin → RAM/Q Register). Second value is indirect path (DATAin → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

IDT49C402/A/B
16-BIT CMOS MICROPROCESSOR SLICE

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS
IDT49C402B

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402B over the -55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil. ⁽⁶⁾	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle) ⁽⁶⁾	22	19	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32) ⁽⁶⁾	52	60	MHz
Minimum Clock LOW Time	11	9	ns
Minimum Clock HIGH Time	11	9	ns
Minimum Clock Period ⁽⁶⁾	24	20	ns


2524 tbl 19

MAXIMUM COMBINATIONAL PROPAGATION DELAYS⁽¹⁾ CL = 50pF

From Input	To Output																Unit
	Y		(MSS = L) Q, P		(MSS = H) F15 OVR				Cn + 16		F = 0		RAM0 RAM15		Q0 Q15		
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Address	33	28	31	26	31	28	31	28	28	26	31	28	32	29	-	-	ns
D	26	23	23	21	23	21	25	22	22	20	26	23	24	23	-	-	ns
Cn	22	20	-	-	20	18	19	17	15	14	22	20	18	17	-	-	ns
I0, 1, 2	28	26	24	22	28	26	27	25	23	21	28	26	26	24	-	-	ns
I3, 4, 5	28	26	22	21	27	25	27	25	22	20	28	26	25	23	-	-	ns
I6, 7, 8, 9	20	18	-	-	-	-	-	-	-	-	-	-	16	14	16	14	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	24	22	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ns
Clock \overline{f}	27	25	25	22	26	24	27	25	-	-	27	25	27	25	-	-	ns

2524 tbl 20

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

Input	CP: 								Unit
	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	10	9	2 ⁽³⁾	1 ⁽³⁾	20 ⁽⁴⁾	18 ⁽⁴⁾	2	1	ns
B Destination Address	10	9	Do not change ⁽²⁾				2	1	ns
D	- ⁽¹⁾	-	-	-	12/22 ⁽⁵⁾	10/20 ⁽⁵⁾	2	1	ns
Cn	-	-	-	-	16	14	0	0	ns
I0, 1, 2	-	-	-	-	26	24	0	0	ns
I3, 4, 5	-	-	-	-	26	24	0	0	ns
I6, 7, 8, 9	10	9	Do not change ⁽²⁾				0	0	ns
RAM0,15, Q0,15	-	-	-	-	12	10	0	0	ns

NOTES:

2524 tbl 21

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path (DATAin → RAM/Q Register). Second value is indirect path (DATAin → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

IDT49C402/A/B
16-BIT CMOS MICROPROCESSOR SLICE

MILITARY AND COMMERCIAL TEMPERATURE RANGES

IDT49C402B
MAX. OUTPUT ENABLE/DISABLE TIMES

(CL = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)
Tested at CL = 50pF, correlated to 5pF

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
OE	Y	18	16	15	13

2524 tbl 22

IDT49C402A
MAX. OUTPUT ENABLE/DISABLE TIMES

(CL = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)
Tested at CL = 50pF, correlated to 5pF

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
OE	Y	22	20	20	18

2524 tbl 23

IDT49C402
MAX. OUTPUT ENABLE/DISABLE TIMES

(CL = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)
Tested at CL = 50pF, correlated to 5pF

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
OE	Y	25	23	25	23

2524 tbl 24

CRITICAL SPEED PATH ANALYSIS

Critical speed paths are for the IDT49C402B versus the equivalent bipolar circuit implementation using four 2901Cs and one 2902A is shown below.

The IDT49C402B operates faster than the theoretically achievable values of the discrete bipolar implementation. Actual speed values for the discrete bipolar circuit will increase due to on-chip/off-chip circuit board delays.

TIMING COMPARISON: IDT49C402B vs 2901C w/2902A

16-Bit μP System	Data Path (Com'l.)		Data Path (Mil.)		Unit
	AB ADDR → F = 0	AB ADDR → RAM _{0, 15}	AB ADDR → F = 0	AB ADDR → RAM _{0, 15}	
	Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	
IDT49C402B	28	23	31	25	ns
Speed Savings	43	48	52	55	ns

2524 tbl 26

TIMING COMPARISON: IDT49C402A vs 2901C w/2902A

16-Bit μP System	Data Path (Com'l.)		Data Path (Mil.)		Unit
	AB ADDR → F = 0	AB ADDR → RAM _{0, 15}	AB ADDR → F = 0	AB ADDR → RAM _{0, 15}	
	Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	
IDT49C402A	37	36	41	25	ns
Speed Savings	34	35	42.5	43.5	ns

2524 tbl 27

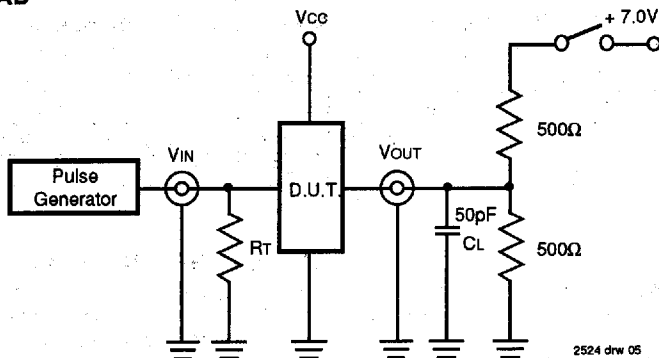
TIMING COMPARISON: IDT49C402 vs 2901C w/2902A

16-Bit μP System	Data Path (Com'l.)		Data Path (Mil.)		Unit
	AB ADDR → F = 0	AB ADDR → RAM _{0, 15}	AB ADDR → F = 0	AB ADDR → RAM _{0, 15}	
	Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	
IDT49C402A	47	40	52	44	ns
Speed Savings	24	31	31.5	39.5	ns

2524 tbl 28



TEST CIRCUIT LOAD



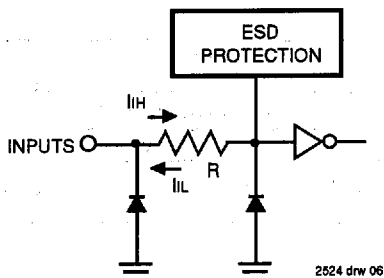
2524 drw 05

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance
 RL = Termination resistance: should be equal to ZOUT of the Pulse Generator

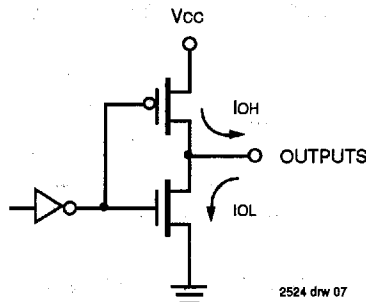
Figure 1. Switching Test Circuit (All Outputs)

INPUT/OUTPUT INTERFACE CIRCUIT



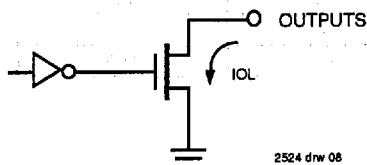
2524 drw 06

Figure 2. Input Structure (All Inputs)



2524 drw 07

Figure 3. Outputs Structure (All Outputs Except F = 0)



2524 drw 08

Figure 4. Outputs Structure (F = 0)

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2524 tbl 25

Test	Switch
Disable Low	Closed
Enable Low	Closed
All other Tests	Open

2524 tbl 28