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April 1st, 2010
Renesas Electronics Corporation

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Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

M37735EHBXXXFP
M37735EHBFS

PROM VERSION OF M37735MHBXXXFP

DESCRIPTION

The M37735EHBXXXFP is a single-chip microcomputer using the 7700 Family core. This single-chip microcomputer has a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can be an 8-bit parallel processor, and the bus interface unit enhances the memory access efficiency to execute instructions fast. This microcomputer also includes a 32 kHz oscillation circuit, in addition to the PROM, RAM, multiple-function timers, serial I/O, A-D converter, and so on.

The M37735EHBXXXFP has the same function as the M37735MHBXXXFP except that the built-in ROM is PROM. For program development, the M37735EHBFS with erasable ROM that is housed in a windowed ceramic LCC is also provided. (Refer to the basic function blocks description.)

FEATURES

- Number of basic instructions 103
- Memory size PROM .... 124 Kbytes
  RAM .... 3968 bytes
- Instruction execution time
  The fastest instruction at 25 MHz frequency .... 160 ns
- Single power supply .... 5 V ± 10%
- Low power dissipation (at 25 MHz frequency)
  ....47.5 mW (Typ.)
- Interrupts .... 19 types, 7 levels
- Multiple-function 16-bit timer .... 5 + 3
- Serial I/O (UART or clock synchronous) 3
- 10-bit A-D converter .... 8-channel inputs
- Watchdog timer
- Programmable input/output
  (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) 68
- Clock generating circuit .... 2 circuits built-in

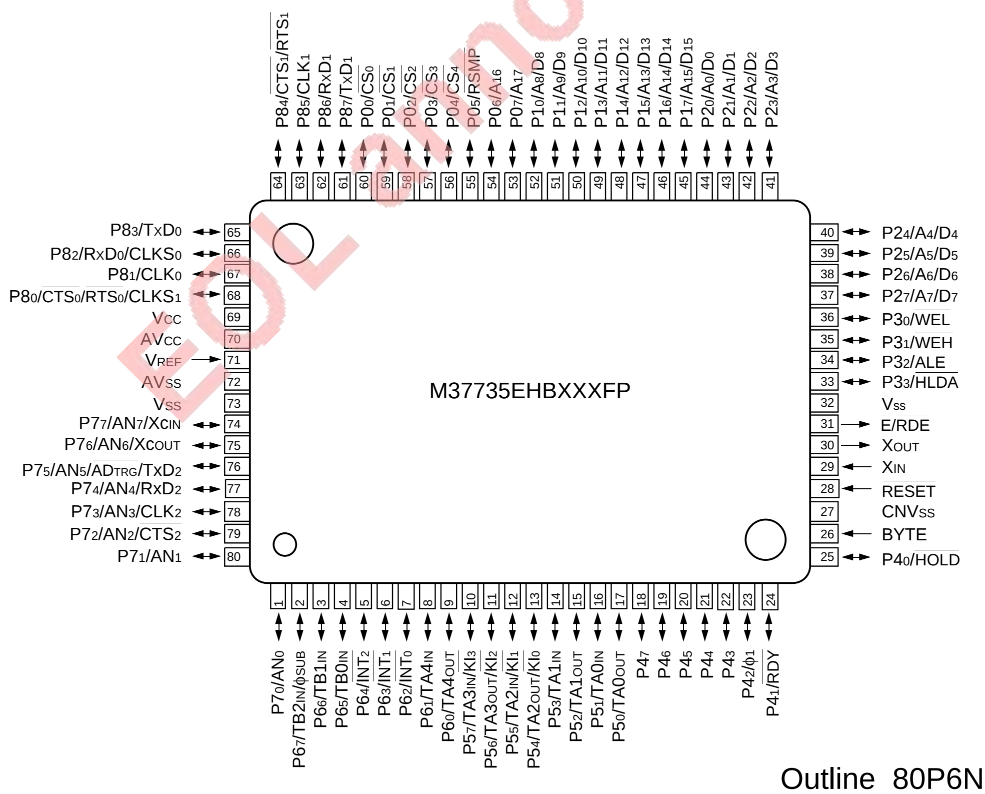
APPLICATION

Control devices for general commercial equipment such as office automation, office equipment, and so on.

Control devices for general industrial equipment such as communication equipment, and so on.

Note. Do not use the windowed EPROM version for mass production, because it is a tool for program development (for evaluation).

PIN CONFIGURATION (TOP VIEW)



Outline 80P6N-A

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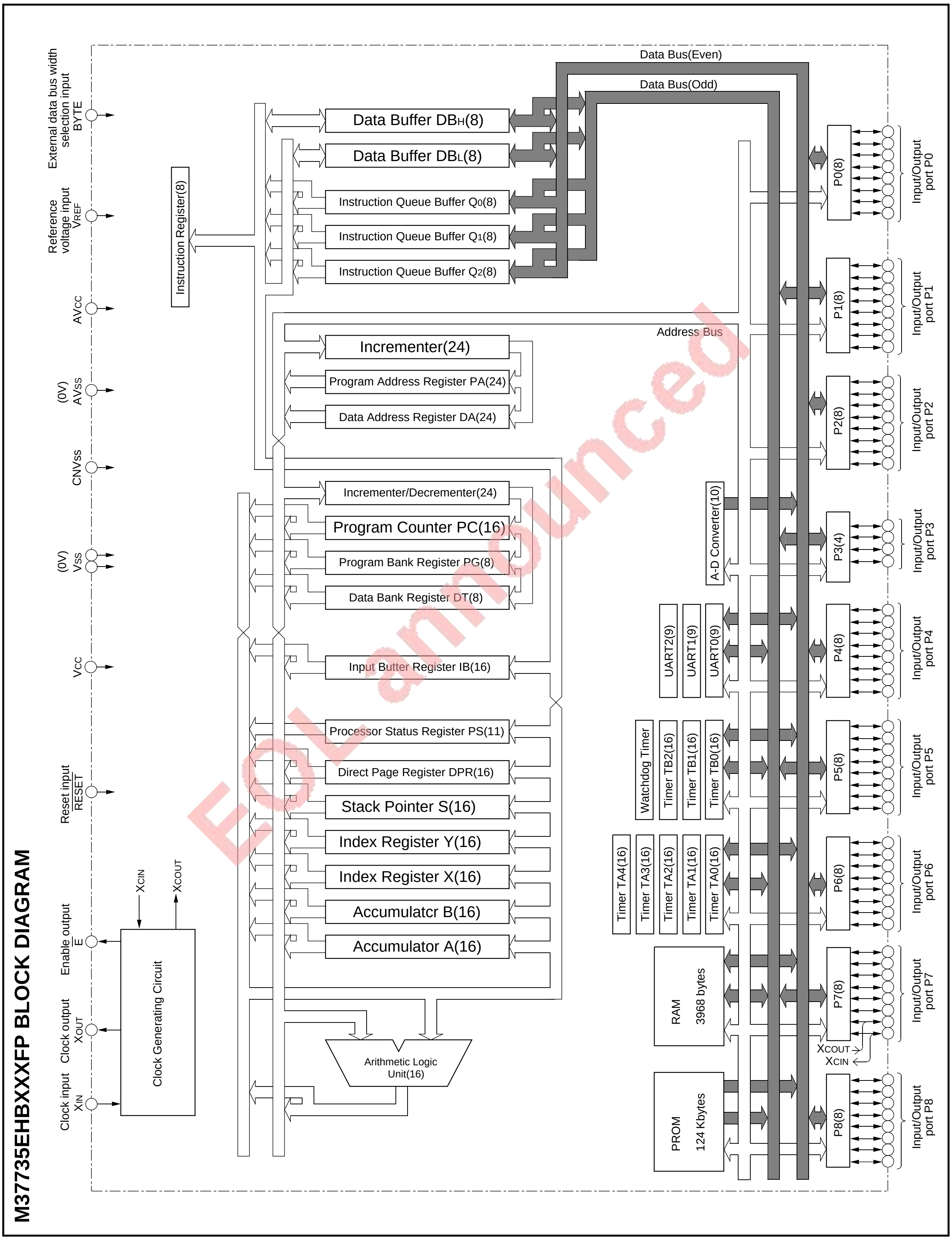
M37735EHBXXXFP BLOCK DIAGRAM



FUNCTIONS OF M37735EHBXXXFP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		160 ns (the fastest instruction at external clock 25 MHz frequency)
Memory size	PROM	124 Kbytes
	RAM	3968 bytes
Input/Output ports	P0 – P2, P4 – P8	8-bit ✕ 8
	P3	4-bit ✕ 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit ✕ 5
	TB0, TB1, TB2	16-bit ✕ 3
Serial I/O		(UART or clock synchronous serial I/O) ✕ 3
A-D converter		10-bit ✕ 1 (8 channels)
Watchdog timer		12-bit ✕ 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		5 V ± 10%
Power dissipation		47.5 mW (at external clock 25 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 1 Mbytes
Operating temperature range		–20 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package	M37735EHBXXXFP	80-pin plastic molded QFP (80P6N-A)
	M37735EHBFS	80-pin ceramic LCC (with a window) (80D0)

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 5 V ± 10% to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.
$\overline{RESET}$	Reset input	Input	When “L” level is applied to this pin, the microcomputer enters the reset state.
X_{IN}	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between X_{IN} and X_{OUT}. When an external clock is used, the clock source should be connected to the X_{IN} pin, and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	This pin functions as the enable signal output pin which indicates the access status in the internal bus. In the memory expansion mode or the microprocessor mode, this pin functions as the $\overline{RDE}$ signal output pin.
BYTE	External data bus width selection input	Input	In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when “L” signal is input and an 8-bit width when “H” signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
$P0_0$ – $P0_7$	I/O port P0	I/O	In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset. In the memory expansion mode or the microprocessor mode, these pins output $\overline{CS_0}$ – $\overline{CS_4}$, $\overline{RSMP}$ signals, and address (A_{16}, A_{17}).
$P1_0$ – $P1_7$	I/O port P1	I/O	In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to “L” in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D_8 – D_{15}) is input/output or an address (A_8 – A_{15}) is output. When the BYTE pin is “H” and an external data bus has an 8-bit width, only address (A_8 – A_{15}) is output.
$P2_0$ – $P2_7$	I/O port P2	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D_0 – D_7) is input/output or an address (A_0 – A_7) is output .
$P3_0$ – $P3_3$	I/O port P3	I/O	In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, $\overline{WEL}$, $\overline{WEH}$, ALE, and $\overline{HLDA}$ signals are output.
$P4_0$ – $P4_7$	I/O port P4	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, $P4_0$, $P4_1$, and $P4_2$ become $\overline{HOLD}$ and $\overline{RDY}$ input pins, and a clock ϕ_1 output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, $P4_2$ can be selected as an I/O port.
$P5_0$ – $P5_7$	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3 and input pins for key input interrupt input ($\overline{KI_0}$ – $\overline{KI_3}$).
$P6_0$ – $P6_7$	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input ($\overline{INT_0}$ – $\overline{INT_2}$) and input pins for timers B0 to B2. $P6_7$ also functions as a sub-clock ϕ_{SUB} output pin.
$P7_0$ – $P7_7$	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. $P7_2$ to $P7_5$ also function as I/O pins for UART2. Additionally, $P7_6$ and $P7_7$ have the function as the output pin (X_{COUT}) and the input pin (X_{CIN}) of the sub-clock (32 kHz) oscillation circuit, respectively. When $P7_6$ and $P7_7$ are used as the X_{COUT} and X_{CIN} pins, connect a resonator or an oscillator between the both.
$P8_0$ – $P8_7$	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.

PIN DESCRIPTION (EPROM MODE)

Pin	Name	Input/Output	Functions
V_{CC}, V_{SS}	Power supply		Supply 5V±10% to V_{CC} and 0V to V_{SS}.
CNV_{SS}	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
BYTE	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic resonator between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	Keep open.
AV_{CC}, AV_{SS}	Analog supply input		Connect AV_{CC} to V_{CC} and AV_{SS} to V_{SS}.
V_{REF}	Reference voltage input	Input	Connect to V_{SS}.
$P0_0$ – $P0_7$	Address input (A_0 – A_7)	Input	Port P0 functions as the lower 8 bits address input (A_0 – A_7).
$P1_0$ – $P1_7$	Address input (A_8 – A_{15})	Input	Port P1 functions as the higher 8 bits address input (A_8 – A_{15}).
$P2_0$ – $P2_7$	Data I/O (D_0 – D_7)	I/O	Port P2 functions as the 8 bits data bus(D_0 – D_7).
$P3_0$	Address input (A_{16})	Input	$P3_0$ functions as the most significant bit address input (A_{16}).
$P3_1$ – $P3_3$	Input port P3	Input	Connect to V_{SS}.
$P4_0$ – $P4_7$	Input port P4	Input	Connect to V_{SS}.
$P5_0$ – $P5_7$	Control signal input	Input	$P5_0$, $P5_1$ and $P5_2$ function as $\overline{PGM}$, $\overline{OE}$ and $\overline{CE}$ input pins respectively. Connect $P5_3$, $P5_4$, $P5_5$ and $P5_6$ to V_{CC}. Connect $P5_7$ to V_{SS}.
$P6_0$ – $P6_7$	Input port P6	Input	Connect to V_{SS}.
$P7_0$ – $P7_7$	Input port P7	Input	Connect to V_{SS}.
$P8_0$ – $P8_7$	Input port P8	Input	Connect to V_{SS}.

BASIC FUNCTION BLOCKS

The M37735EHBXXXFP has the same functions as the M37735MHBXXXFP except for the following:

(1) The built-in ROM is PROM.

(2) The status of bit 3 of the oscillation circuit control register 1 (address $6F_{16}$) at a reset is different.

(3) The usage condition of bit 3 of the oscillation circuit control register 1 is different.

(4) Part of the processor mode selection method is different.

Accordingly, refer to the basic function blocks description in the M37735MHBXXXFP except for Figure 1 (bit configuration of oscillation circuit control register 1), Figure 3 (microcomputer internal status during reset), and Table 1 (microprocessor mode selection method).

In the M37735EHBXXXFP, bit 3 of the oscillation circuit control register 1 must be “0”. (Refer to Figure 1.) Bit 3 is “1” at a reset. Accordingly, write “0” to bit 3 in the single-chip mode after reset.

Figure 2 shows how to write data in oscillation circuit control register 1.

In the M37735EHBXXXFP, the microprosessor mode cannot be selected by connecting the CNV_{SS} pin to V_{CC}. Connect the CNV_{SS} pin to V_{SS} and start the microcomputer’s operating from the single-chip mode.

Table 1. Relationship between CNV_{SS} pin input level and processor modes

CNV_{SS}	Mode	Description
V_{SS}	· Single-chip · Memory expansion · Microprocessor	Single-chip mode upon starting after reset. Each mode can be selected by changing the processor mode bits by software.

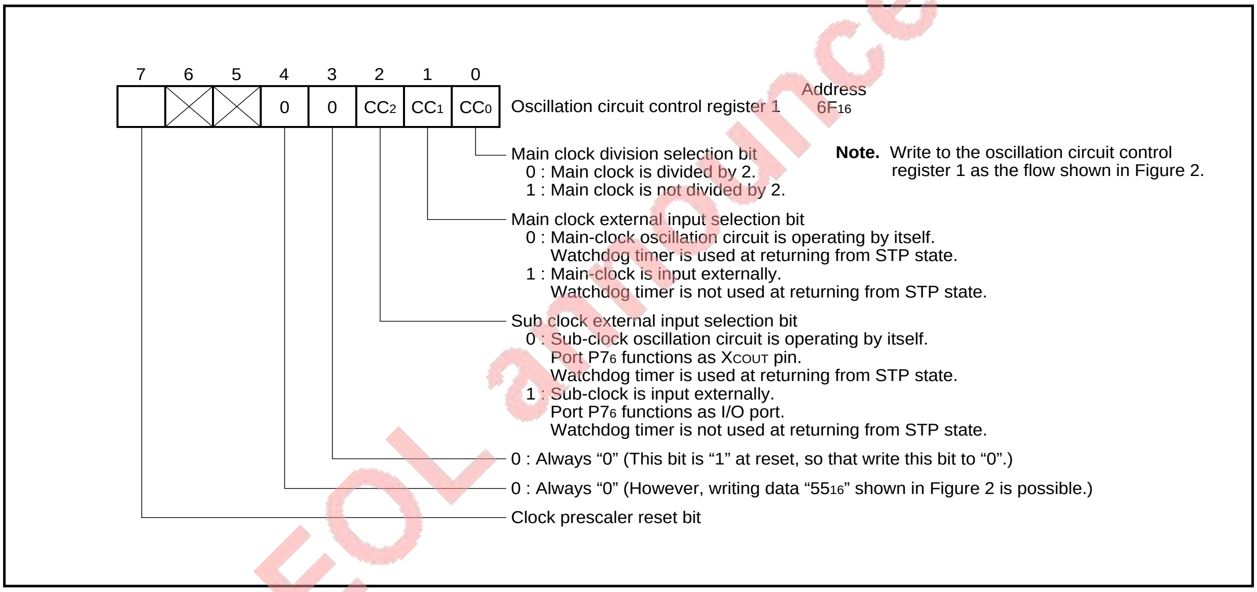


Fig. 1 Bit configuration of oscillation circuit control register 1 (corresponding to Figure 63 in data sheet “M37735MHBXXXFP”)

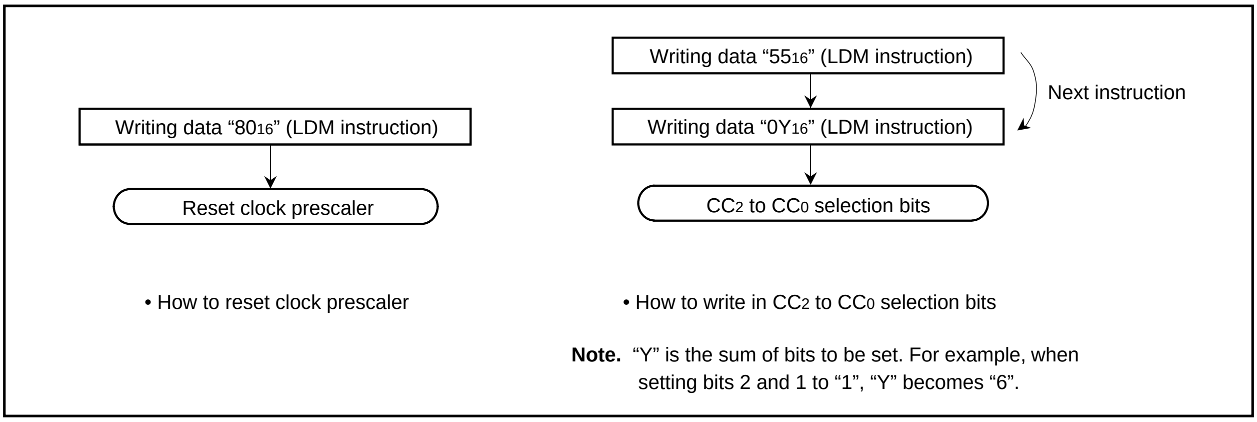


Fig. 2 How to write data in oscillation circuit control register 1 (indentical with Figure 64 in data sheet “M37735MHBXXXFP”)

	Address	
Port P0 direction register	(04₁₆)···	00₁₆
Port P1 direction register	(05₁₆)···	00₁₆
Port P2 direction register	(08₁₆)···	00₁₆
Port P3 direction register	(09₁₆)···	× × × × 0 0 0 0
Port P4 direction register	(0C₁₆)···	00₁₆
Port P5 direction register	(0D₁₆)···	00₁₆
Port P6 direction register	(10₁₆)···	00₁₆
Port P7 direction register	(11₁₆)···	00₁₆
Port P8 direction register	(14₁₆)···	00₁₆
A-D control register 0	(1E₁₆)···	0 0 0 0 0 ? ? ?
A-D control register 1	(1F₁₆)···	× × 0 0 0 × 1 1
UART 0 transmit/receive mode register	(30₁₆)···	00₁₆
UART 1 transmit/receive mode register	(38₁₆)···	00₁₆
UART 0 transmit/receive control register 0	(34₁₆)···	0 0 0 0 1 0 0 0
UART 1 transmit/receive control register 0	(3C₁₆)···	0 0 0 0 1 0 0 0
UART 0 transmit/receive control register 1	(35₁₆)···	0 0 0 0 0 0 1 0
UART 1 transmit/receive control register 1	(3D₁₆)···	0 0 0 0 0 0 1 0
Count start flag	(40₁₆)···	00₁₆
One- shot start flag	(42₁₆)···	× × × 0 0 0 0 0
Up-down flag	(44₁₆)···	00₁₆
Timer A0 mode register	(56₁₆)···	00₁₆
Timer A1 mode register	(57₁₆)···	00₁₆
Timer A2 mode register	(58₁₆)···	00₁₆
Timer A3 mode register	(59₁₆)···	00₁₆
Timer A4 mode register	(5A₁₆)···	00₁₆
Timer B0 mode register	(5B₁₆)···	0 0 1 0 0 0 0 0
Timer B1 mode register	(5C₁₆)···	0 0 1 × 0 0 0 0
Timer B2 mode register	(5D₁₆)···	0 0 1 × 0 0 0 0
Processor mode register 0	(5E₁₆)···	00₁₆
Processor mode register 1	(5F₁₆)···	× × × × × × × 0
Watchdog timer register	(60₁₆)···	FFF₁₆
Watchdog timer frequency selection flag	(61₁₆)···	× × × × × × × 0
Memory allocation control register	(63₁₆)···	× × × 0 0 0 0 0
UART2 transmit/receive mode register	(64₁₆)···	× 0 0 0 0 0 0 0
UART2 transmit/receive control register 0	(68₁₆)···	× × × × 1 0 0 0
UART2 transmit/receive control register 1	(69₁₆)···	0 0 0 0 0 0 1 0
Oscillation circuit control register 0	(6C₁₆)···	× 0 0 0 0 0 × 1
Port function control register	(6D₁₆)···	00₁₆
Serial transmit control register	(6E₁₆)···	× × 0 0 × × × ×
Oscillation circuit control register 1	(6F₁₆)···	0 × × 0 1 0 0 0
A-D/UART2 trans./rece. interrupt control register	(70₁₆)···	× × × × 0 0 0 0
UART 0 transmission interrupt control register	(71₁₆)···	× × × × 0 0 0 0
UART 0 receive interrupt control register	(72₁₆)···	× × × × 0 0 0 0
UART 1 transmission interrupt control register	(73₁₆)···	× × × × 0 0 0 0
UART 1 receive interrupt control register	(74₁₆)···	× × × × 0 0 0 0
Timer A0 interrupt control register	(75₁₆)···	× × × × 0 0 0 0
Timer A1 interrupt control register	(76₁₆)···	× × × × 0 0 0 0
Timer A2 interrupt control register	(77₁₆)···	× × × × 0 0 0 0
Timer A3 interrupt control register	(78₁₆)···	× × × × 0 0 0 0
Timer A4 interrupt control register	(79₁₆)···	× × × × 0 0 0 0
Timer B0 interrupt control register	(7A₁₆)···	× × × × 0 0 0 0
Timer B1 interrupt control register	(7B₁₆)···	× × × × 0 0 0 0
Timer B2 interrupt control register	(7C₁₆)···	× × × × 0 0 0 0
$\overline{INT_0}$ interrupt control register	(7D₁₆)···	× × 0 0 0 0 0 0
$\overline{INT_1}$ interrupt control register	(7E₁₆)···	× × 0 0 0 0 0 0
$\overline{INT_2}$/Key input interrupt control register	(7F₁₆)···	× × 0 0 0 0 0 0
Processor status register (PS)		0 0 0 ? ? 0 0 0 1 ? ?
Program bank register (PG)		00₁₆
Program counter (PCH)		Content of FFFF₁₆
Program counter (PCL)		Content of FFFE₁₆
Direct page register (DPR)		0000₁₆
Data bank register (DT)		00₁₆

Contents of other registers and RAM are undefined during reset. Initialize them by software.

Fig. 3 Microcomputer internal status during reset

EPROM MODE

The M37735EHBXXXFP features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is "L", the chip automatically enters the EPROM mode. Table 2 list the correspondence between pins and Figure 4 shows the pin connections in the EPROM mode.

The EPROM mode is the 1M mode for the EPROM that is equivalent to the M5M27C101K.

When in the EPROM mode, ports P0, P1, P2, $P3_0$, $P5_0$, $P5_1$, $P5_2$, CNV_{SS}, and BYTE are used for the EPROM (equivalent to the M5M27C101K).

When in this mode, the built-in PROM can be programmed or read from using these pins in the same way as with the M5M27C101K.

This chip does not have Device Identifier Mode, so that set the corresponding program algorithm. The program area should specify address 01000_{16} – $1FFFF_{16}$.

Connect the clock which is either ceramic resonator or external clock to X_{IN} pin and X_{OUT} pin.

Table 2 Pin function in EPROM mode

	M37735EHBXXXFP	M5M27C101K
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}, BYTE	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, P1, $P3_0$	A_0 – A_{16}
Data I/O	Port P2	D_0 – D_7
$\overline{CE}$	$P5_2$	$\overline{CE}$
$\overline{OE}$	$P5_1$	$\overline{OE}$
$\overline{PGM}$	$P5_0$	$\overline{PGM}$

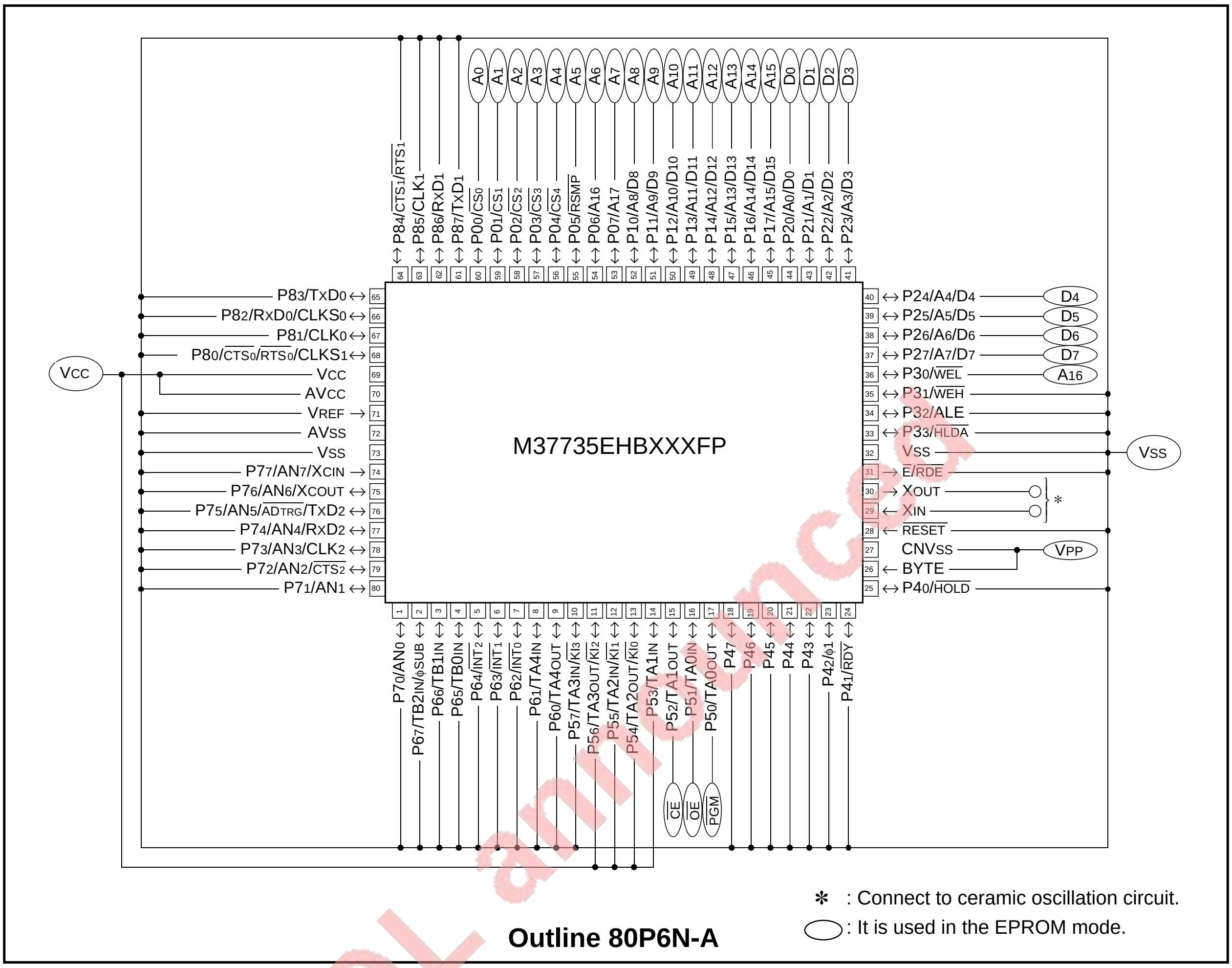


Fig. 4 Pin connection in EPROM mode

FUNCTION IN EPROM MODE
1M mode (equivalent to the M5M27C101K)

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a “L” level. Input the address of the data (A_0 – A_{16}) to be read, and the data will be output to the I/O pins D_0 – D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the “H” state.

Programming

Programming must be performed in 8 bits by a byte program. To program to the EPROM, set the $\overline{CE}$ pin to a “L” level and the $\overline{OE}$ pin to a “H” level. The CPU will enter the programming mode when 12.5 V is applied to the V_{PP} pin. The address to be programmed to is selected with pins A_0 – A_{16}, and the data to be programmed is input to pins D_0 – D_7. Set the $\overline{PGM}$ pin to a “L” level to being programming.

Erasing

To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15 J/cm^2.

Programming operation

To program the M37735EHBXXXFP, first set V_{CC} = 6 V, V_{PP} = 12.5 V, and set the address to 0100_{16}. Apply a 0.2 ms programming pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 0.2 ms programming pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further once this number of pulses (0.2 × X ms).
When this series of programming operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.
Finally, when all addresses have been programmed, read with V_{CC} = V_{PP} = 5 V (or V_{CC} = V_{PP} = 5.5 V).

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	X	5 V	5 V	Output
Output	V_{IL}	V_{IH}	X	5 V	5 V	Floating
Disable	V_{IH}	X	X	5 V	5 V	Floating
Programming	V_{IL}	V_{IH}	V_{IL}	12.5 V	6 V	Input
Programming Verify	V_{IL}	V_{IL}	V_{IH}	12.5 V	6 V	Output
Program Disable	V_{IH}	V_{IH}	V_{IH}	12.5 V	6 V	Floating

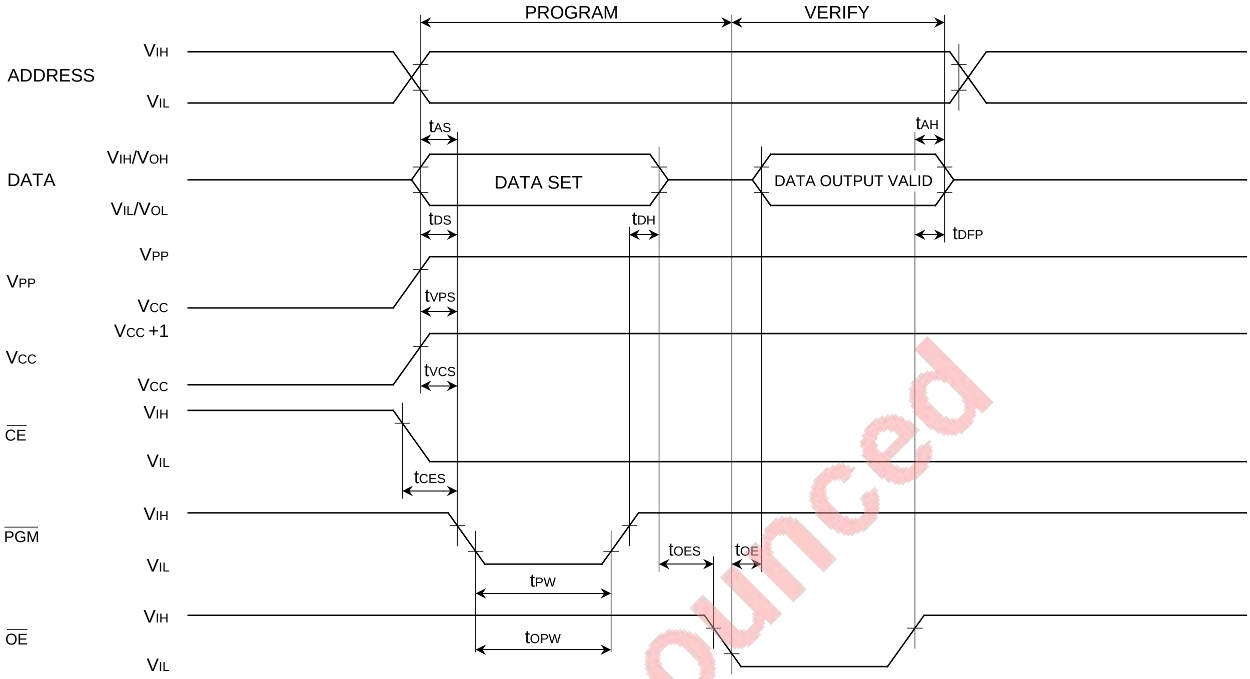
Note 1 : An X indicates either V_{IL} or V_{IH}.

Programming operation (equivalent to the M5M27C101K)

AC ELECTRICAL CHARACTERISTICS (T_a = 25 ± 5 °C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, unless otherwise noted)

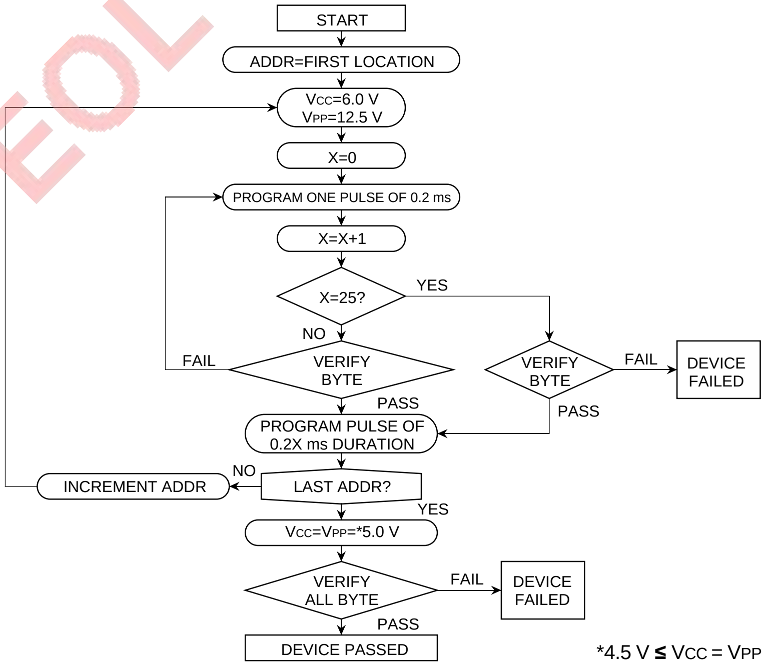
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address setup time		2			µs
t_{OES}	$\overline{OE}$ setup time		2			µs
t_{DS}	Data setup time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			µs
t_{VPS}	V_{PP} setup time		2			µs
t_{PW}	$\overline{PGM}$ pulse width		0.19	0.2	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time		2			µs
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC waveforms



Test conditions for A.C. characteristics
Input voltage : V_{IL} = 0.45 V, V_{IH} = 2.4 V
Input rise and fall times (10 % – 90 %) : ≤ 20 ns
Reference voltage at timing measurement : Input, Output
"L" = 0.8 V, "H" = 2 V

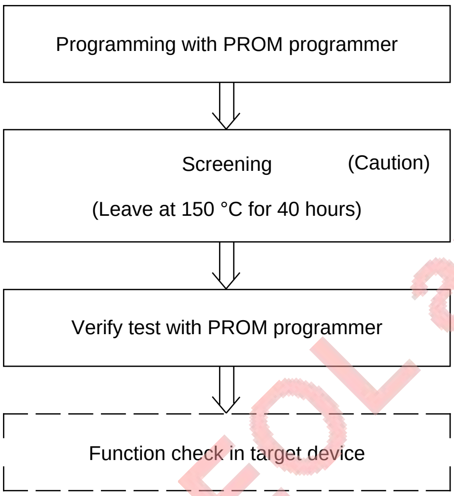
Programming algorithm flow chart



*4.5 V ≤ V_{CC} = V_{PP} ≤ 5.5 V

SAFETY INSTRUCTIONS

(1) Sunlight and fluorescent lamp contain light that can erase written information. When using in read mode, be sure to cover the transparent glass portion with a seal or other materials (ceramic package product).
(2) Mitsubishi Electric corp. provides the seal for covering the transparent glass. Take care that the seal does not touch the read pins (ceramic package product).
(3) Clean the transparent glass before erasing. Fingers' fat and paste disturb the passage of ultraviolet rays and may affect badly the erasure capability (ceramic package product).
(4) A high voltage is used for programming. Take care that over-voltage is not applied. Take care especially at power on.
(5) The programmable M37735EHBFP that is shipped in blank is also provided. For the M37735EHBFP, Mitsubishi Electric corp. does not perform PROM programming test and screening following the assembly processes. To improve reliability after programming, performing programming and test according to the flow below before use is recommended.



Caution : Never expose to 150 °C exceeding 100 hours.

ADDRESSING MODES

The M37735EHBXXXFP has 28 powerful addressing modes. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37735EHBXXXFP has 103 machine instructions. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for details.

DATA REQUIRED FOR PROM ORDERING

Please send the following data for writing to PROM.
(1) M37735EHBXXXFP writing to PROM order confirmation form
(2) 80P6N mark specification form
(3) ROM data (EPROM 3 sets)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Power source voltage		–0.3 to +7	V
AVcc	Analog power source voltage		–0.3 to +7	V
V_I	Input voltage $\overline{RESET}$, CNVss, BYTE		–0.3 to +12 (Note)	V
V_I	Input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, V_{REF}, X_{IN}		–0.3 to Vcc + 0.3	V
V_O	Output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, X_{OUT}, $\overline{E}$		–0.3 to Vcc + 0.3	V
P_d	Power dissipation	Ta = 25 °C	300	mW
T_{opr}	Operating temperature		–20 to +85	°C
T_{stg}	Storage temperature		–40 to +150	°C

Note. When the EPROM is programmed, input voltage of pins CNVss and BYTE is 13 V respectively.

RECOMMENDED OPERATING CONDITIONS (Vcc = 5 V ± 10%, Ta = –20 to +85 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
Vcc	Power source voltage	$f(X_{IN})$: Operating	4.5	5.0	5.5	V
		$f(X_{IN})$: Stopped, $f(X_{CIN})$ = 32.768 kHz	2.7		5.5	
AVcc	Analog power source voltage			Vcc		V
Vss	Power source voltage			0		V
AVss	Analog power source voltage			0		V
V_{IH}	High-level input voltage $P0_0$ – $P0_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, X_{CIN} (Note 3)		0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in single-chip mode)		0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in memory expansion mode and microprocessor mode)		0.5 Vcc		Vcc	V
V_{IL}	Low-level input voltage $P0_0$ – $P0_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, X_{CIN} (Note 3)		0		0.2Vcc	V
V_{IL}	Low-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in single-chip mode)		0		0.2Vcc	V
V_{IL}	Low-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in memory expansion mode and microprocessor mode)		0		0.16Vcc	V
$I_{OH(peak)}$	High-level peak output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$				–10	mA
$I_{OH(avg)}$	High-level average output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$				–5	mA
$I_{OL(peak)}$	Low-level peak output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_3$, $P5_4$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$				10	mA
$I_{OL(peak)}$	Low-level peak output current $P4_4$ – $P4_7$, $P5_0$ – $P5_3$				20	mA
$I_{OL(avg)}$	Low-level average output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_3$, $P5_4$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$				5	mA
$I_{OL(avg)}$	Low-level average output current $P4_4$ – $P4_7$, $P5_0$ – $P5_3$				15	mA
$f(X_{IN})$	Main-clock oscillation frequency (Note 4)				25	MHz
$f(X_{CIN})$	Sub-clock oscillation frequency			32.768	50	kHz

Notes 1. Average output current is the average value of a 100 ms interval.

2. The sum of $I_{OL(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of $I_{OH(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of $I_{OL(peak)}$ for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of $I_{OH(peak)}$ for ports P4, P5, P6, and P7 must be 80 mA or less.

3. Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = “1”.

4. The maximum value of $f(X_{IN})$ = 12.5 MHz when the main clock division selection bit = “1”.

ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	High-level output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$	I_{OH} = –10 mA	3			V
V_{OH}	High-level output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_3$	I_{OH} = –400 µA	4.7			V
V_{OH}	High-level output voltage $P3_0$ – $P3_2$	I_{OH} = –10 mA	3.1			V
		I_{CH} = –400 µA	4.8			
V_{OH}	High-level output voltage $\overline{E}$	I_{OH} = –10 mA	3.4			V
		I_{OH} = –400 µA	4.8			
V_{OL}	Low-level output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_3$, $P4_0$ – $P4_3$, $P5_4$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_5$, $P8_0$ – $P8_7$	I_{OL} = 10 mA			2	V
V_{OL}	Low-level output voltage $P4_4$ – $P4_7$, $P5_0$ – $P5_3$	I_{OL} = 20 mA			2	V
V_{OL}	Low-level output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_3$	I_{OL} = 2 mA			0.45	V
V_{OL}	Low-level output voltage $P3_0$ – $P3_2$	I_{OL} = 10 mA			1.9	V
		I_{OL} = 2 mA			0.43	
V_{OL}	Low-level output voltage $\overline{E}$	I_{OL} = 10 mA			1.6	V
		I_{OL} = 2 mA			0.4	
V_{T+} – V_{T-}	Hysteresis $\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$ – $TA4_{IN}$, $TB0_{IN}$ – $TB2_{IN}$, $\overline{INT_0}$ – $\overline{INT_2}$, $\overline{AD_{TRG}}$, $\overline{CTS_0}$, $\overline{CTS_1}$, $\overline{CTS_2}$, CLK_0, CLK_1, CLK_2, $\overline{KI_0}$ – $\overline{KI_3}$		0.4		1	V
V_{T+} – V_{T-}	Hysteresis $\overline{RESET}$		0.2		0.5	V
V_{T+} – V_{T-}	Hysteresis X_{IN}		0.1		0.4	V
V_{T+} – V_{T-}	Hysteresis X_{CIN} (When external clock is input)		0.1		0.4	V
I_{IH}	High-level input current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE	V_I = 5 V			5	µA
I_{IL}	Low-level input current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_3$, $P6_0$, $P6_1$, $P6_5$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE	V_I = 0 V			–5	µA
I_{IL}	Low-level input current $P5_4$ – $P5_7$, $P6_2$ – $P6_4$	V_I = 0 V, without a pull-up transistor			–5	µA
		V_I = 0 V, with a pull-up transistor	–0.25	–0.5	–1.0	mA
V_{RAM}	RAM hold voltage	When clock is stopped.	2			V

ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
I_{CC}	Power source current	In single-chip mode, output pins are open, and other pins are V_{SS}.	V_{CC} = 5 V, f(X_{IN}) = 25 MHz (square waveform), (f(f_2) = 12.5 MHz), f(X_{CIN}) = 32.768 kHz, in operating (Note 1)		9.5	19	mA
			V_{CC} = 5 V, f(X_{IN}) = 25 MHz (square waveform), (f(f_2) = 1.5625 MHz), f(X_{CIN}) = Stopped, in operating (Note 1)		1.3	2.6	mA
			V_{CC} = 5V, f(X_{IN}) = 25 MHz (square waveform), f(X_{CIN}) = 32.768 kHz, when a WIT instruction is executed (Note 2)		10	20	µA
			V_{CC} = 5 V, f(X_{IN}) : Stopped, f(X_{CIN}) : 32.768 kHz, in operating (Note 3)		50	100	µA
			V_{CC} = 5 V, f(X_{IN}) : Stopped, f(X_{CIN}) : 32.768 kHz, when a WIT instruction is executed (Note 4)		5	10	µA
			Ta = 25 °C, when clock is stopped			1	µA
			Ta = 85 °C, when clock is stopped			20	µA

Notes 1. This applies when the main clock external input selection bit = “1”, the main clock division selection bit = “0”, and the signal output stop bit = “1”.

2. This applies when the main clock external input selection bit = “1” and the system clock stop bit at wait state = “1”.

3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.

4. This applies when the X_{COUT} drivability selection bit = “0” and the system clock stop bit at wait state = “1”.

A–D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz (Note), unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF} = V_{CC}			10	Bits
—	Absolute accuracy	V_{REF} = V_{CC}			± 3	LSB
R_{LADDER}	Ladder resistance	V_{REF} = V_{CC}	10		25	kΩ
t_{CONV}	Conversion time		9.44			µs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

Note. This applies when the main clock division selection bit = “0” and f(f_2) = 12.5 MHz.

TIMING REQUIREMENTS (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz, unless otherwise noted (Note))

Notes 1. This applies when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2. Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits Min.	Limits Max.	Unit
t_c	External clock input cycle time (Note 3)	40		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 4)	15		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 4)	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns

Notes 3. When the main clock division selection bit = "1", the minimum value of tc = 80 ns.
4. When the main clock division selection bit = "1", values of $t_{w(H)}$ / tc and $t_{w(L)}$ / tc must be set to values from 0.45 through 0.55.

Single-chip mode

Symbol	Parameter	Limits Min.	Limits Max.	Unit
$t_{su(P0D–E)}$	Port P0 input setup time	60		ns
$t_{su(P1D–E)}$	Port P1 input setup time	60		ns
$t_{su(P2D-E)}$	Port P2 input setup time	60		ns
$t_{su(P3D–E)}$	Port P3 input setup time	60		ns
$t_{su(P4D–E)}$	Port P4 input setup time	60		ns
$t_{su(P5D–E)}$	Port P5 input setup time	60		ns
$t_{su(P6D–E)}$	Port P6 input setup time	60		ns
$t_{su(P7D–E)}$	Port P7 input setup time	60		ns
$t_{su(P8D–E)}$	Port P8 input setup time	60		ns
$t_{h(E–P0D)}$	Port P0 input hold time	0		ns
$t_{h(E–P1D)}$	Port P1 input hold time	0		ns
$t_{h(E–P2D)}$	Port P2 input hold time	0		ns
$t_{h(E–P3D)}$	Port P3 input hold time	0		ns
$t_{h(E–P4D)}$	Port P4 input hold time	0		ns
$t_{h(E–P5D)}$	Port P5 input hold time	0		ns
$t_{h(E–P6D)}$	Port P6 input hold time	0		ns
$t_{h(E–P7D)}$	Port P7 input hold time	0		ns
$t_{h(E–P8D)}$	Port P8 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits Min.	Limits Max.	Unit
$t_{su(D–RDE)}$	Data input setup time	32		ns
$t_{su(RDY–\phi1)}$	$\overline{RDY}$ input setup time	55		ns
$t_{su(HOLD–\phi1)}$	$\overline{HOLD}$ input setup time	55		ns
$t_{h(RDE–D)}$	Data input hold time	0		ns
$t_{h(\phi1–RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(\phi1–HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

Timer A input (Count input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	80		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	40		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time (Note)	320		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width (Note)	160		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width (Note)	160		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS" on page 19.

Timer A input (External trigger input in one-shot pulse mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time (Note)	320		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	80		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	80		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS" on page 19.

Timer A input (External trigger input in pulse width modulation mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	80		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	80		ns

Timer A input (Up-down input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} input cycle time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} input high-level pulse width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} input low-level pulse width	1000		ns
$t_{su(UP-T_{IN})}$	TAi_{OUT} input setup time	400		ns
$t_{h(T_{IN}-UP)}$	TAi_{OUT} input hold time	400		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAj_{IN} input cycle time	800		ns
$t_{su(TAj_{IN}-TAj_{OUT})}$	TAj_{IN} input setup time	200		ns
$t_{su(TAj_{OUT}-TAj_{IN})}$	TAj_{OUT} input setup time	200		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (one edge count)	80		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (one edge count)	40		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (one edge count)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (both edges count)	160		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (both edges count)	80		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (both edges count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (Note)	320		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (Note)	160		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (Note)	160		ns

Note. Limits change depending on f(XIN). Refer to "DATA FORMULAS" on page 19.

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (Note)	320		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (Note)	160		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (Note)	160		ns

Note. Limits change depending on f(XIN). Refer to "DATA FORMULAS" on page 19.

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ input cycle time (minimum allowable trigger)	1000		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ input low-level pulse width	125		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high-level pulse width	100		ns
$t_{w(CKL)}$	CLKi input low-level pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	30		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

External interrupt $\overline{INT_i}$ input, key input interrupt $\overline{KI_i}$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input high-level pulse width	250		ns
$t_{w(INL)}$	$\overline{INT_i}$ input low-level pulse width	250		ns
$t_{w(KIL)}$	$\overline{KI_i}$ input low-level pulse width	250		ns

DATA FORMULAS

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. $f(f_2)$ represents the clock f_2 frequency.
For the relation to the main clock and sub clock, refer to Table 10 in data sheet “M37735MHBXXXFP”.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = –20 to 85°C, f(X_{IN}) = 25 MHz (Note), unless otherwise noted)

Single-chip mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time	Fig. 5		80	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time			80	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			80	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time			80	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time			80	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time			80	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time			80	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time			80	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time			80	ns

Note. This applies when the main clock division selection bit = “0” and f(f_2) = 12.5 MHz.

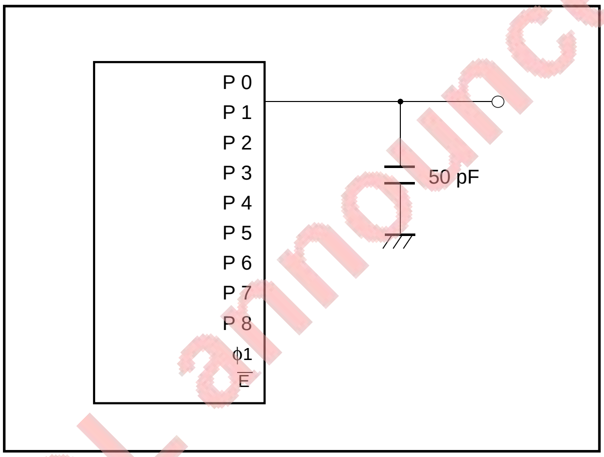


Fig. 5 Measuring circuit for ports P0 – P8 and ϕ_1

Memory expansion mode and microprocessor mode

(V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz (Note 1), unless otherwise noted)

Symbol	Parameter	Wait mode (Note 2)	Test conditions	Limits Min.	Limits Max.	Unit
$t_{d(CS-WE)}$ $t_{d(CS-RDE)}$	Chip-select output delay time	No wait Wait 1	Fig. 5	12		ns
		Wait 0		87		ns
$t_{h(WE-CS)}$ $t_{h(RDE-CS)}$	Chip-select hold time			4		ns
$t_{d(An-WE)}$ $t_{d(An-RDE)}$	Address output delay time	No wait Wait 1		12		ns
		Wait 0		87		ns
$t_{d(A-WE)}$ $t_{d(A-RDE)}$	Address output delay time	No wait Wait 1		12		ns
		Wait 0		75		ns
$t_{h(WE-An)}$ $t_{h(RDE-An)}$	Address hold time			18		ns
$t_{w(ALE)}$	ALE pulse width	No wait Wait 1		22		ns
		Wait 0		57		ns
$t_{su(A-ALE)}$	Address output setup time	No wait Wait 1		5		ns
		Wait 0		45		ns
$t_{h(ALE-A)}$	Address hold time	No wait Wait 1		9		ns
		Wait 0		15		ns
$t_{d(ALE-WE)}$ $t_{d(ALE-RDE)}$	ALE output delay time	No wait Wait 1		4		ns
		Wait 0		10		ns
$t_{d(WE-DQ)}$	Data output delay time				45	ns
$t_{h(WE-DQ)}$	Data hold time			18		ns
$t_{w(WE)}$	$\overline{WEL}$/$\overline{WEH}$ pulse width	No wait		50		ns
		Wait 1 Wait 0		130		ns
$t_{pxz(RDE-DZ)}$	Floating start delay time				5	ns
$t_{pzx(RDE-DZ)}$	Floating release delay time			20		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width	No wait		48		ns
		Wait 1 Wait 0		128		ns
$t_{d(RSMP-WE)}$ $t_{d(RSMP-RDE)}$	$\overline{RSMP}$ output delay time			10		ns
$t_{h(\phi_1-RSMP)}$	$\overline{RSMP}$ hold time			0		ns
$t_{d(WE-\phi_1)}$ $t_{d(RDE-\phi_1)}$	ϕ_1 output delay time			0	18	ns
$t_{d(\phi_1-HLDA)}$	$\overline{HLDA}$ output delay time				50	ns

Notes 1. This applies when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2. No wait : Wait bit = "1".
Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".
Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

Memory expansion mode and microprocessor mode

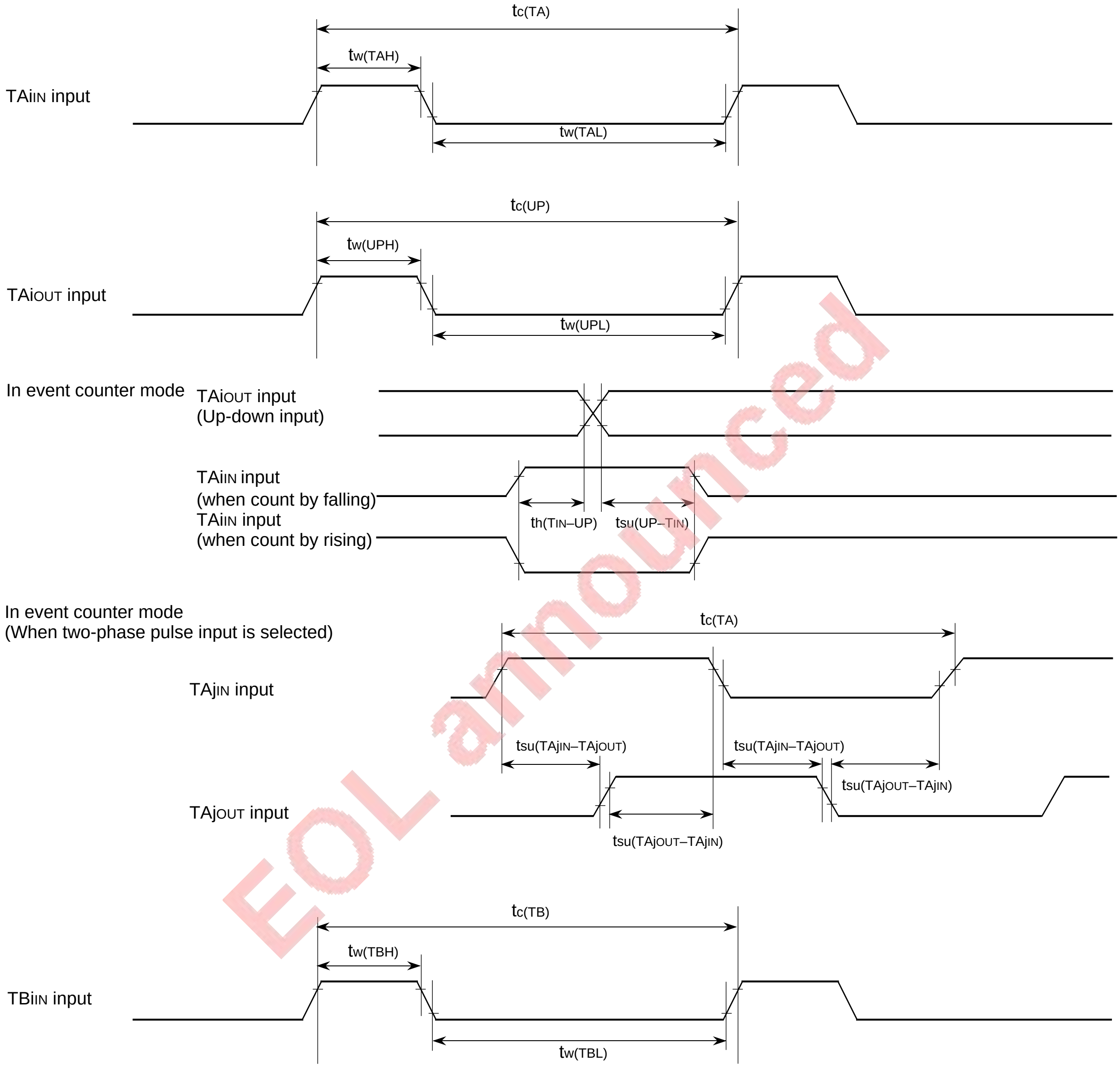
Bus timing data formulas (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = –20 to 85 °C, $f(X_{IN})$ = 25 MHz (Max., Note1), unless otherwise noted)

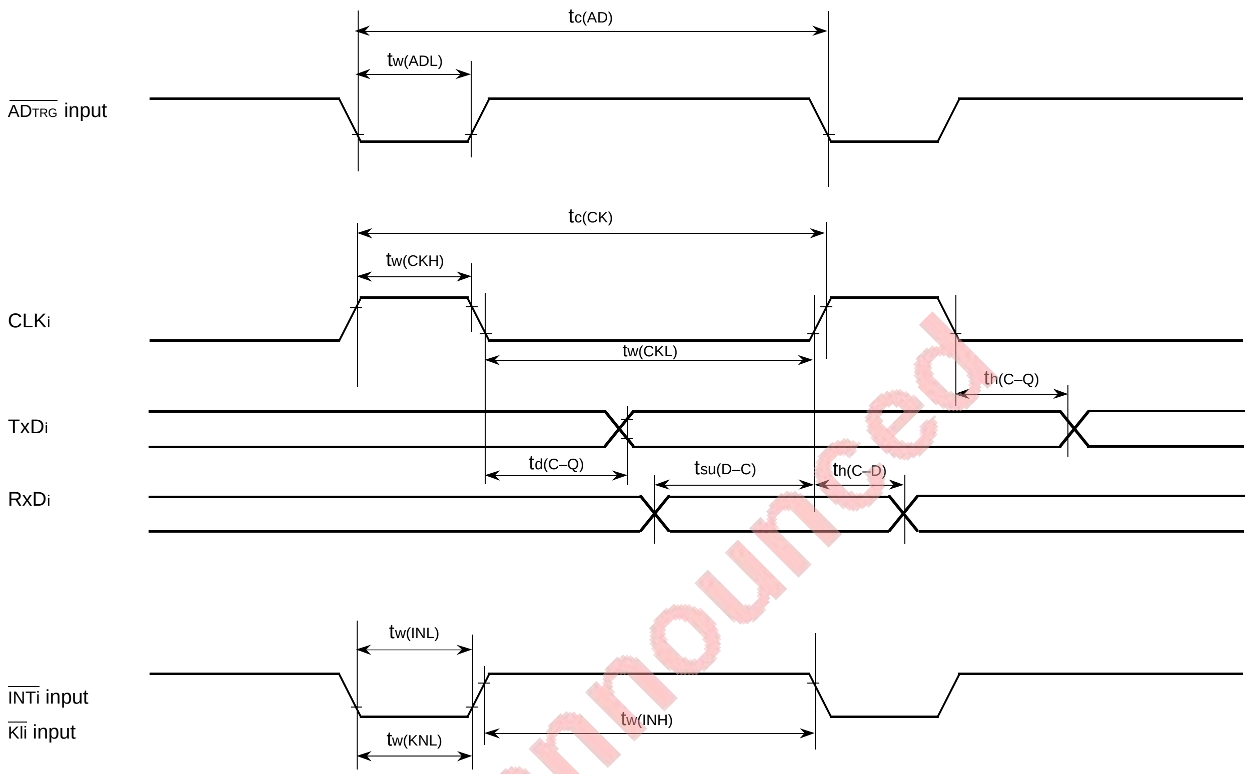
Symbol	Parameter	Wait mode	Limits Min.	Limits Max.	Unit
$t_{d(CS-WE)}$, $t_{d(CS-RDE)}$	Chip-select output delay time	No wait, Wait 1	$\frac{1\times10^9}{2\cdot f(f_2)} - 28$		ns
		Wait 0	$\frac{3\times10^9}{2\cdot f(f_2)} - 33$		ns
$t_{h(WE-CS)}$, $t_{h(RDE-CS)}$	Chip-select hold time		4		ns
$t_{d(An-WE)}$, $t_{d(An-RDE)}$	Address output delay time	No wait, Wait 1	$\frac{1\times10^9}{2\cdot f(f_2)} - 28$		ns
		Wait 0	$\frac{3\times10^9}{2\cdot f(f_2)} - 33$		ns
$t_{d(A-WE)}$, $t_{d(A-RDE)}$	Address output delay time	No wait, Wait 1	$\frac{1\times10^9}{2\cdot f(f_2)} - 28$		ns
		Wait 0	$\frac{3\times10^9}{2\cdot f(f_2)} - 45$		ns
$t_{h(WE-An)}$, $t_{h(RDE-An)}$	Address hold time		$\frac{1\times10^9}{2\cdot f(f_2)} - 22$		ns
$t_{w(ALE)}$	ALE pulse width	No wait, Wait 1	$\frac{1\times10^9}{2\cdot f(f_2)} - 18$		ns
		Wait 0	$\frac{2\times10^9}{2\cdot f(f_2)} - 23$		ns
$t_{su(A-ALE)}$	Address output setup time	No wait, Wait 1	$\frac{1\times10^9}{2\cdot f(f_2)} - 35$		ns
		Wait 0	$\frac{2\times10^9}{2\cdot f(f_2)} - 35$		ns
$t_{h(ALE-A)}$	Address hold time	No wait, Wait 1	9		ns
		Wait 0	$\frac{1\times10^9}{2\cdot f(f_2)} - 25$		ns
$t_{d(ALE-WE)}$, $t_{d(ALE-RDE)}$	ALE output delay time	No wait, Wait 1	4		ns
		Wait 0	$\frac{1\times10^9}{2\cdot f(f_2)} - 30$		ns
$t_{d(WE-DQ)}$	Data output delay time			45	ns
$t_{h(WE-DQ)}$	Data hold time		$\frac{1\times10^9}{2\cdot f(f_2)} - 22$		ns
$t_{w(WE)}$	$\overline{WEL}/\overline{WEH}$ pulse width	No wait	$\frac{2\times10^9}{2\cdot f(f_2)} - 30$		ns
		Wait 1, Wait 0	$\frac{4\times10^9}{2\cdot f(f_2)} - 30$		ns
$t_{pxz(RDE-DZ)}$	Floating start delay time			5	ns
$t_{pzx(RDE-DZ)}$	Floating release delay time		$\frac{1\times10^9}{2\cdot f(f_2)} - 20$		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width	No wait	$\frac{2\times10^9}{2\cdot f(f_2)} - 32$		ns
		Wait 1, Wait 0	$\frac{4\times10^9}{2\cdot f(f_2)} - 32$		ns
$t_{d(RSMP-WE)}$, $t_{d(RSMP-RDE)}$	$\overline{RSMP}$ output delay time		$\frac{1\times10^9}{2\cdot f(f_2)} - 30$		ns
$t_{h(\phi_1-RSMP)}$	$\overline{RSMP}$ hold time		0		ns
$t_{d(WE-\phi_1)}$, $t_{d(RDE-\phi_1)}$	ϕ_1 output delay time		0	18	ns

Notes 1. This applies when the main-clock division selection bit = "0".

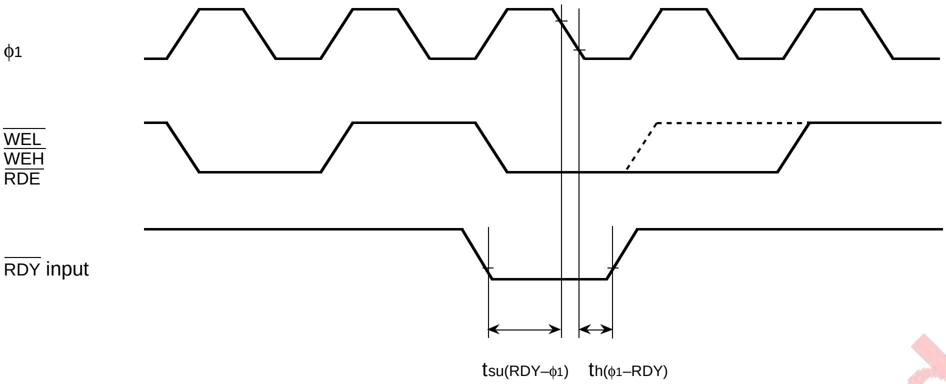
2. $f(f_2)$ represents the clock f_2 frequency.
For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37735MHBXXXFP".

TIMING DIAGRAM

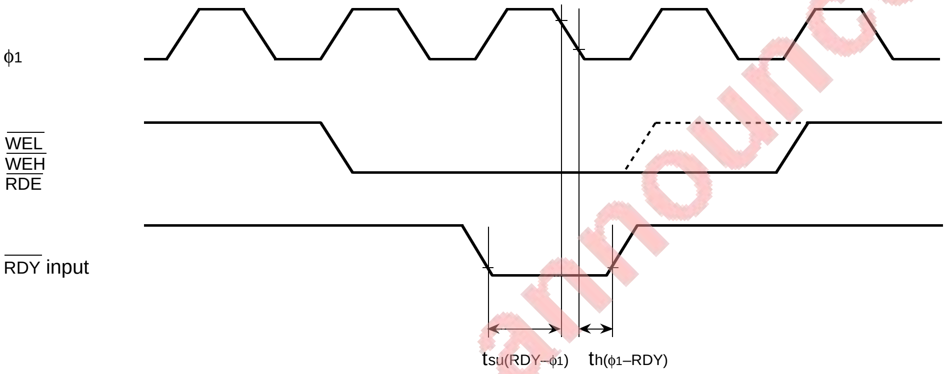

tc(TA)
tw(TAH)
TAiIN input
tw(TAL)
tc(UP)
tw(UPH)
TAiOUT input
tw(UPL)
In event counter mode
TAiOUT input
(Up-down input)
TAiIN input
(when count by falling)
TAiIN input
(when count by rising)
th(TIN–UP)
tsu(UP–TIN)
In event counter mode
(When two-phase pulse input is selected)
tc(TA)
TAjIN input
tsu(TAjIN–TAjOUT)
tsu(TAjIN–TAjOUT)
tsu(TAjOUT–TAjIN)
TAjOUT input
tsu(TAjOUT–TAjIN)
tc(TB)
tw(TBH)
TBiIN input
tw(TBL)


tc(AD)
tw(ADL)
ADTRG input
tc(CK)
tw(CKH)
CLKi
tw(CKL)
th(C–Q)
TxDi
td(C–Q)
tsu(D–C)
th(C–D)
RxDi
tw(INL)
INTi input
KIi input
tw(INH)
tw(KNL)

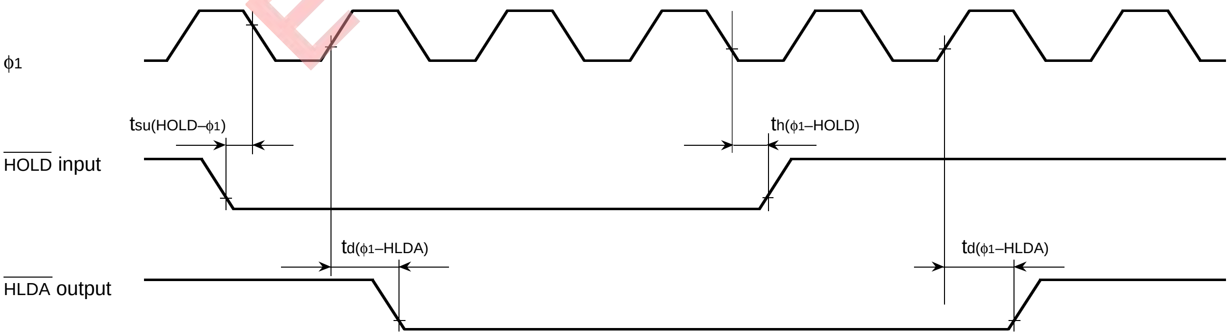
Memory expansion mode and microprocessor mode
(When wait bit = "1")



(When wait bit = "0")

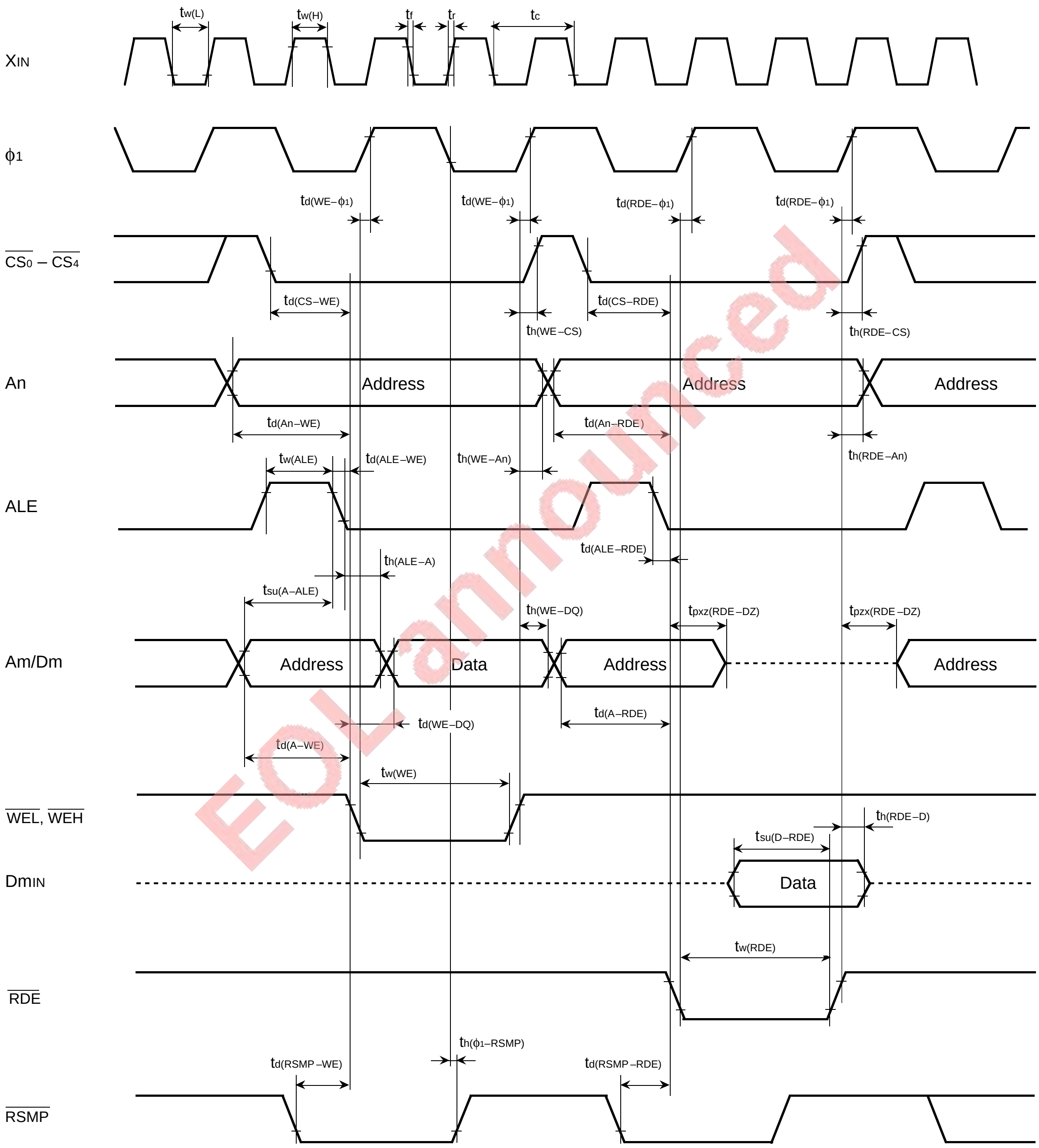


(When wait bit = "1" or "0" in common)



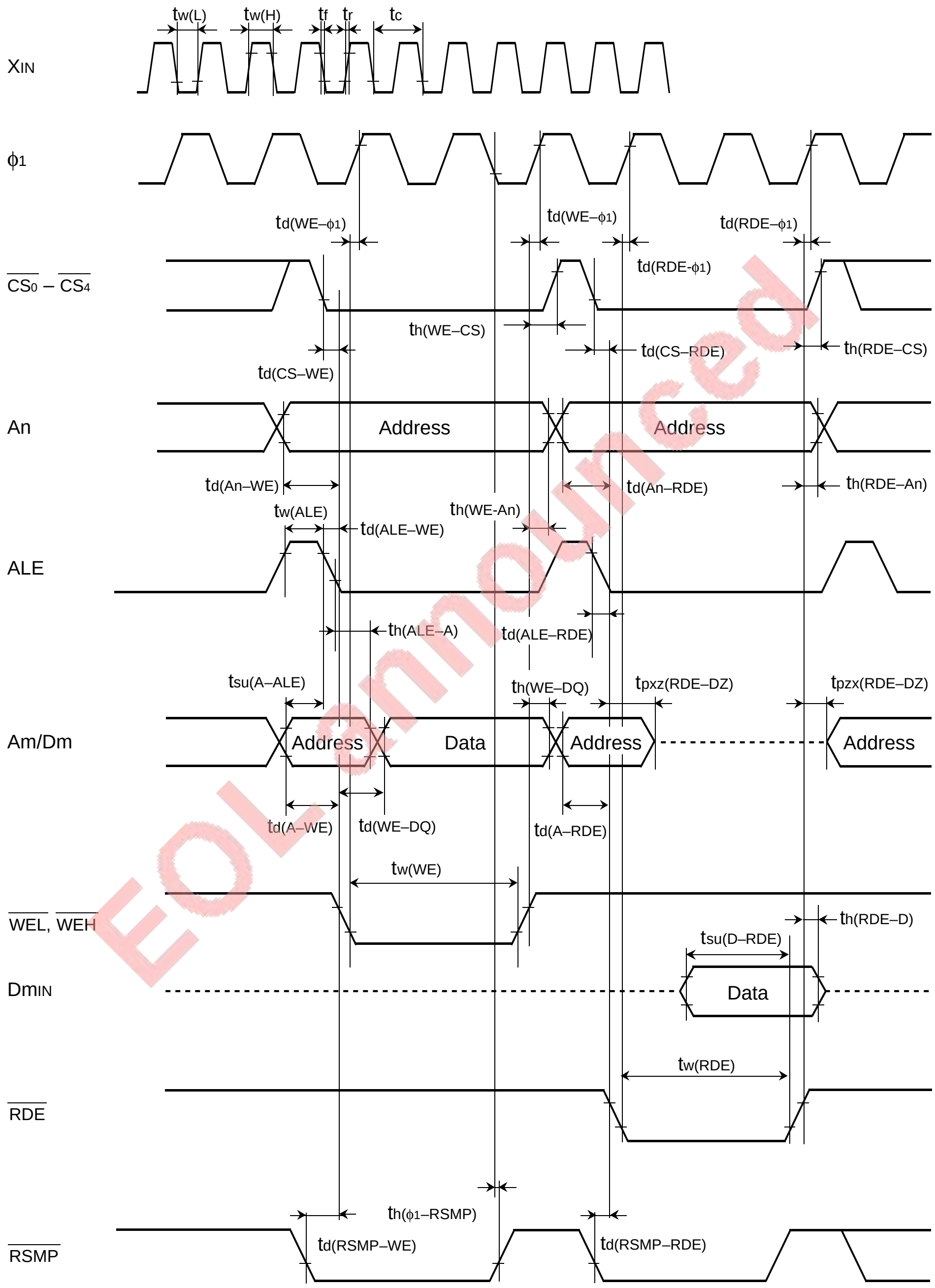
Test conditions
• V_{CC} = 5 V ± 10%
• Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
• Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

Memory expansion mode and microprocessor mode
(No wait : When wait bit = “1”)



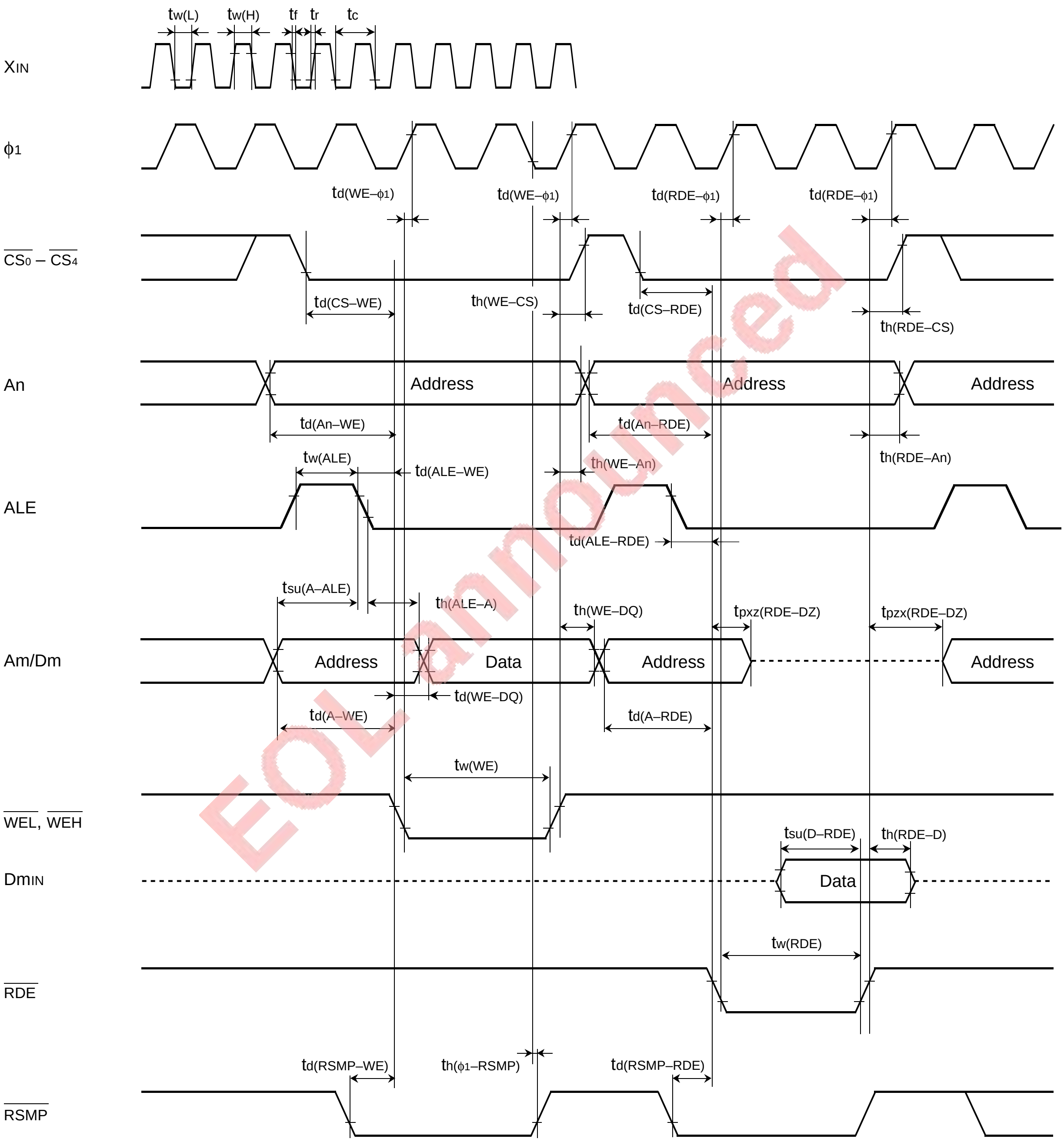
Test conditions
- V_{CC} = 5 V ± 10%
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input Dm_{IN} : V_{IL} = 0.8 V, V_{IH} = 2.5 V

Memory expansion mode and microprocessor mode
(Wait 1 : The external memory area is accessed when wait bit = “0” and wait selection bit = “1”.)



Test conditions
- Vcc = 5 V ± 10%
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input Dm_{IN} : V_{IL} = 0.8 V, V_{IH} = 2.5 V

Memory expansion mode and microprocessor mode
(Wait 0 : The external memory area is accessed when wait bit = “0” and wait selection bit = “0”.)



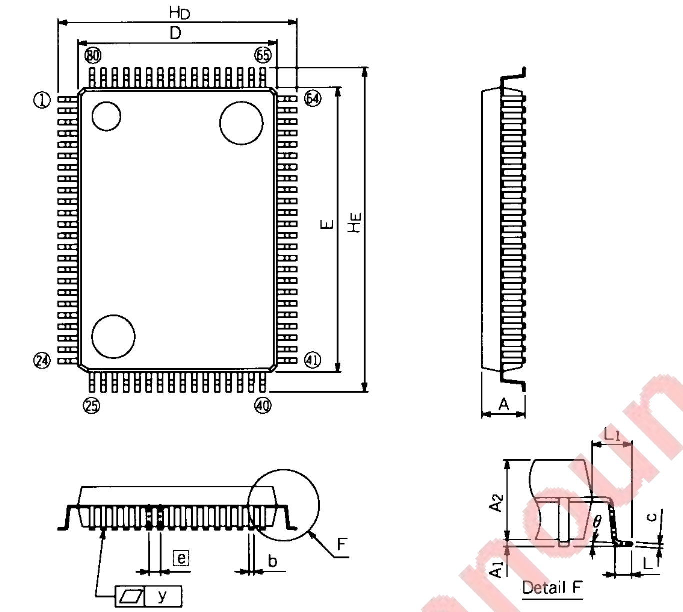
Test conditions
- V_{CC} = 5 V ± 10%
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input Dm_{IN} : V_{IL} = 0.8 V, V_{IH} = 2.5 V

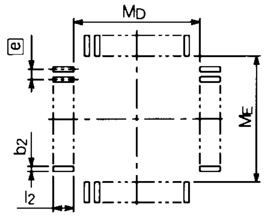
PACKAGE OUTLINE

80P6N−A Plastic 80pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1420-0.80	–	1.58	Alloy 42

Scale : 2/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.8	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	–	1.4	–
y	–	–	0.1
θ	0°	–	10°
b2	–	0.5	–
l2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

GZZ–SH00–81B<84A0>

ROM number	

Receipt	Date:	
	Section head signature	Supervisor signature

7700 FAMILY WRITING TO PROM ORDER CONFIRMATION FORM
SINGLE-CHIP 16-BIT MICROCOMPUTER
M37735EHBXXXFP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked ※

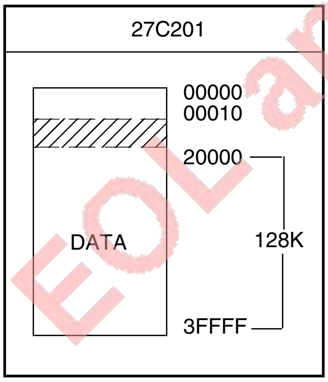
※	Customer	Company name	TEL ( )	Issuance signatures	Responsible officer	Supervisor
		Date issued	Date:			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce writing to PROM based on this data. We shall assume the responsibility for errors only if the written PROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM Type :



Note : Make sure that address 01FFFF16 of the microcomputer's internal ROM corresponds to address 3FFFF16 of EPROM.

(1) Set "FF16" in the shaded area.

(2) Address 016 to 0F16 are the area for storing the data on model designation.This area must be written with the data shown below.
Address and data are written in hexadecimal notation.

Data	Address	Data	Address
4D	0	42	8
33	1	FF	9
37	2	FF	A
37	3	FF	B
33	4	FF	C
35	5	FF	D
45	6	FF	E
48	7	FF	F

※2. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered fill out the appropriate 80P6N Mark Specification Form (for M37735EHBXXXFP) and attach to the Writing to PROM Order Confirmation Form.

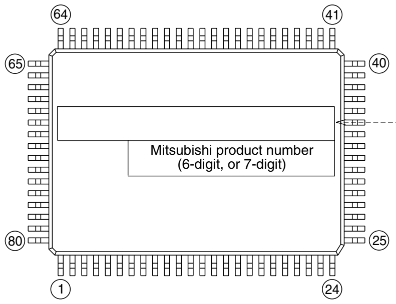
※3. Comments

80P6N (80-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

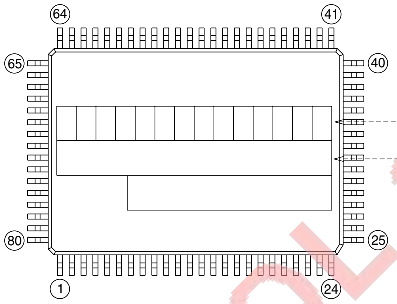
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

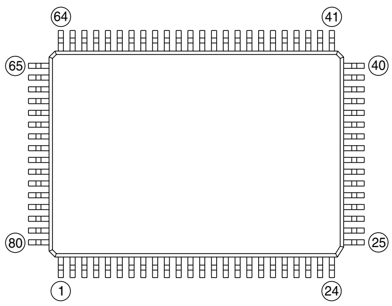
B. Customer's Parts Number + Mitsubishi IC Catalog Name



Customer's Parts Number
Note : The fonts and size of characters are standard Mitsubishi type.
Mitsubishi IC catalog name

Notes 1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 14 alphanumeric characters for capital letters, hyphens, commas, periods and so on.

C. Special Mark Required



Notes1 : If special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible.
Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.
2 : If special character fonts (e,g., customer's trade mark logo) must be used in Special Mark, check the box below.
For the new special character fonts, a clean font original (ideally logo drawing) must be submitted.

Special character fonts required

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

H-LF450-A KI-9610 Printed in Japan (ROD) Ⅱ
New publication, effective Oct. 1996.
Specifications subject to change without notice.

Renesas Technology Corp.

REVISION DESCRIPTION LIST	M37735EHBXXXFP, M37735EHBFS Datasheet

Rev. No.	Revision Description	Rev. date
1.00	First Edition	970604
1.01	The following are added: • PROM ORDER CONFIRMATION FORM • MARK SPECIFICATION FORM	980526
2.00	The following are revised:	980731

Page	Previous Version	Revised Version
P12 Right column Line 2	The M37735EHBXXXFP has 28 powerful addressing modes. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for the details of each addressing mode. **MACHINE INSTRUCTION LIST** The M37735EHBXXXFP has 103 machine instructions. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for details.	The M37735EHBXXXFP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details. **MACHINE INSTRUCTION LIST** The M37735EHBXXXFP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.