Data Sheet

32

Preliminary Document

V850E2/FG4-L

Hardware

V850E2/FG4-L

μPD70F3576
μPD70F3577
μPD70F3578
μPD70F3579
μPD70F3580

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Notes for CMOS Devices

(1) Precaution against ESD for semiconductors

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All text and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) Handling of unused input pins for CMOS

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

(3) Status before initialization of MOS devices

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Table of contents

Chapter 1 Overview

1.1 Naming

1.1.1 Alternative function pins

Peripheral	Prefix	Function name	Suffix
Short-cut of macro name	Consecutive number for same peripheral module[a]	Peripheral Macro pin naming	Consecutive number for same pin names[a]

a) This is an option that can be omitted if meaning is obvious

Example:

– TAUB0I0, TAUB1I5
– URTE0TX, URTE0RX, URTE1TX, URTE1RX
– CSIG0SO, CSIG0SI, CSIG0SC, CSIG0RY

1.1.2 Power supply pins

Function	Prefix	Kind of supply	Suffix
Symbol	Consecutive number for different functions[a]	VDD or VSS	Consecutive number for different pins with same meaning[a]

a) This is an option that can be omitted if meaning is obvious

Example:

– E0VDDn, REG0VSS

Table 1-1 Selection for Functions

Function	Explanation
REG	Internal regulator supply
OSC	Oscillator supply
I0	Flash module supply and ISO0 Internal regulator supply(mainly 5V)
E	Standard buffer supply (mainly 5V or up to 20Mhz)
A	Analog module supply (e.g. ADC)

If not mentioned otherwise this document neglects suffixes for power supply pins with same functions that can be treated as equal.

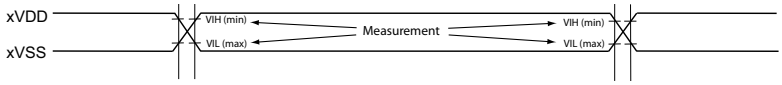
1.2 Pin Groups

Symbol	Pin group supplied by	Related pins / ports
PgE0	E0VDD / E0VSS	JP0, P0, _RESET, FLMD0,
PgE1	E1VDD / E1VSS	P1, P3, P4
PgOSC	OSCVDD / OSCVSS	X1, X2
PgA0	A0VDD / A0VSS	P10, P11

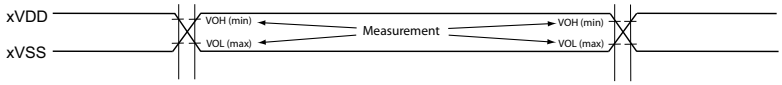
1.3 General measurement conditions

1.3.1 AC characteristic measurement condition

AC test input waveform

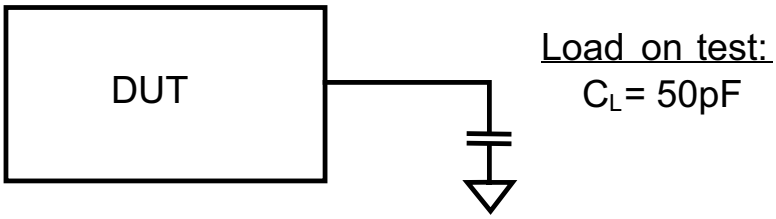


AC test output waveform



Standard AC test condition is 70%/30% of the applied IO supply voltage (XmVDD) if not otherwise stated in the according AC timing specification of an interface.

AC Test Condition: Ext. Capacitive Load



Chapter 2 Absolute maximum ratings

2.1 Supply voltages

Table 2-1 VDD Data

Parameter	Symbol	Condition	Ratings	Unit
System	I0VDD		-0.3 ~ 6.0	V
	OSCVDD		-0.3 ~ 6.0	V
	REG0VDD		-0.3 ~ 6.0	V
	REG1VDD		-0.3 ~ 6.0	V
	REG2VDD		-	V
	REG3VDD		-	V
Ports	E0VDD		-0.3 ~ 6.0	V
	E1VDD		-0.3 ~ 6.0	V
ADCA0	A0VDD		-0.3 ~ 6.0	V

2.2 Port voltages

Table 2-2 Port Input voltage

Parameter	Pin Group	Symbol[a]	Condition	Ratings	Unit
Input voltage[b]	PgE0	V_{I0}	E0VDD≤5.5	-0.3 ~ E0VDD+0.3	V
	PgE1	V_{I1}	E1VDD≤5.5	-0.3 ~ E1VDD+0.3	V
	PgOSC	V_{I5}	OSCVDD≤5.5	-0.3 ~ OSCVDD+0.3	V
	PgA0	V_{I3}		A0VDD+0.3	V

a) The symbols reflect all supplies within the device series. Therefore not every symbol is available for each product.

b) The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

2.3 Port current

Table 2-3 High level port output current

Parameter	Pin Group[a]	Symbol	Condition	Max. spec	Unit
High level output current	PgE0	IOH	1 pin of PgE0	-10	mA
			Power supply of PgE0 + PgE1	-120[b]	
	PgE1		1 pin of PgE1	-10	
	PgA0		1 pin of PgA0	-10	
			Power supply of PgA0	-25	

a) The column reflects all supplies within the device series. Therefore not each pin group is available for each product.

b) Do not exceed 30mA per each side of the device

Table 2-4 Low level port output current

Parameter	Pin Group[a]	Symbol	Condition	Max. spec	Unit
Low level output current	PgE0	IOL	1 pin of PgE0	10	mA
			Power supply of PgE0 + PgE1	120[b]	
	PgE1		1 pin of PgE1	10	
	PgA0		1 pin of PgA0	10	
			Power supply of PgA0	25	

a) The column reflects all supplies within the device series. Therefore not each pin group is available for each product.

b) Do not exceed 30mA per each side of the device

2.4 Capacitance

Parameter	Symbol	Condition	Max. spec	Unit
Input capacitance	C_I	f = 1 MHz 0V for non measurement pins	15	pF
Input/Output capacitance	C_{IO}		15	pF
Output capacitance	C_O		15	pF

2.5 Thermal characteristics

Table 2-5 Thermal characteristics

Parameter	Symbol	Condition	Ratings	Unit
Storage temperature	T_{STG}		-55 ~125	°C
Operating ambient temperature	T_a	(A) grade products	-40 ~85	
		(A1) grade products	-40 ~110	
		(A2) grade products	-40 ~125	

This section specifies the absolute maximum limitation of operating and storage temperature.

The device's functions are not guaranteed outside of the specified maximum temperature ratings.

Chapter 3 Power supply specification

3.1 Requirements for external power supply connections

The user has to ensure a low resistive connection of all VSS pins on the PCB. This specification denotes ground supply pins as:

- VSS = OSCVSS = REGnVSS = EnVSS = AnVSS = 0V

in the further text.

With

- EnVSS = E0VSS = E1VSS
- REGnVSS = REG0VSS = REG1VSS
- AnVSS = A0VSS

The user has to ensure a low resistive connection of all VDD pins to the related power supply. This specification denotes power supply pins as:

- EnVDD, I/OVDD, REGnVDD, OSCVDD, AnVDD.

in the further text.

With

- EnVDD = E0VDD = E1VDD
- REGnVDD = REG0VDD = REG1VDD.
- AnVDD = A0VDD
- I/OVDD = AnVDD, EnVDD, I0VDD, OSCVDD

3.2 Power area definitions

The device consists of the following power areas:

- AWO (Always On area)
- ISO0 (Isolated area 0)

The table below lists the related core and port voltage supply of each power area:

Table 3-1 Power areas supply voltages

Power Area	Supply voltage	Related pins
AWO	Internal regulator supply	REG0VDD, REG0VSS
	Port Supply	E0VDD, E0VSS
	Other	OSCVDD, OSCVSS I0VDD

Table 3-1 Power areas supply voltages

Power Area	Supply voltage	Related pins
ISO0	Internal regulator supply	REG1VDD, REG1VSS
	Port Supply	E1VDD, E1VSS
	Other	A0VDD, A0VSS

3.3 Power supply groups

For each of the following power supply groups the same voltage must by supplied:

Table 3-2 Power supply groups

Power supply group	Related pins
#1	REG0VDD, REG1VDD, I0VDD, OSCVDD, E0VDD, E1VDD
#5	A0VDD
#7	All VSS

3.4 Supply voltages

Table 3-3 VDD Data

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
System supply voltage	I0VDD		VPOC		5.5	V
System supply voltage	OSCVDD		VPOC		5.5	V
System supply voltage	REG0VDD	REG0VDD = REG1VDD	VPOC		5.5	V
System supply voltage	REG1VDD		VPOC		5.5	V
System supply voltage	REG2VDD		-		-	V
System supply voltage	REG3VDD		-		-	V
Port supply voltages	E0VDD		VPOC		5.5	V
Port supply voltages	E1VDD		VPOC		5.5	V
ADC supply voltages	A0VDD		VPOC		5.5	V

3.4.1 AWO Regulator characteristics

Table 3-4 AWO Regulator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Regulator Output voltage	VRO		1.35	1.50	1.65	V
System supply voltage slope	RAVS	0V to VPOC	0.5		150[a]	V/ms
Capacitance on REG0C	REG0C		2.31		6.11[a]	µF

a) Reference values

3.4.2 ISO Regulator characteristics

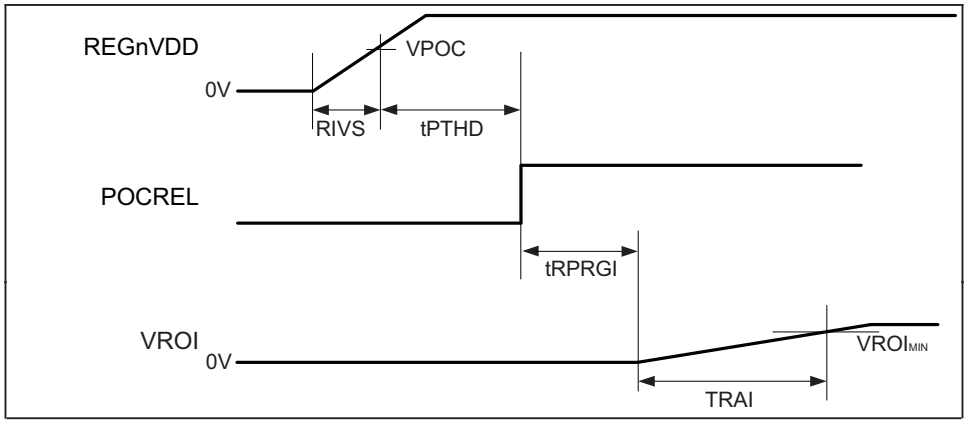
Table 3-5 ISO regulator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Output voltage	VROI		1.35	1.50	1.65	V
Capacitance on REGnC	REGnC		0.07	0.1	0.13	µF
Voltage slope	RIVS		0.18		1800	V/ms
Response time	tPTHD					a
CPU Start-up time	T_{cpusu}	Time from ISO0 wake-up to 1st CPU instruction fetch.		750		µs

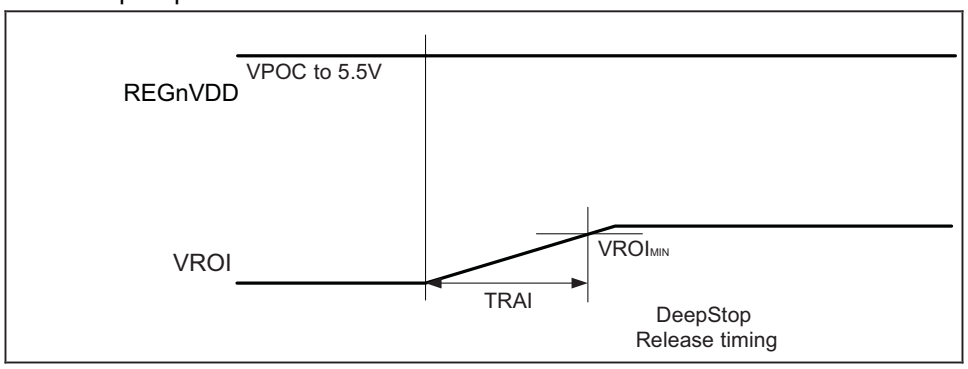
a) see chapter *3.4.3 "POC characteristics"*

Note n=1

During power-up sequence



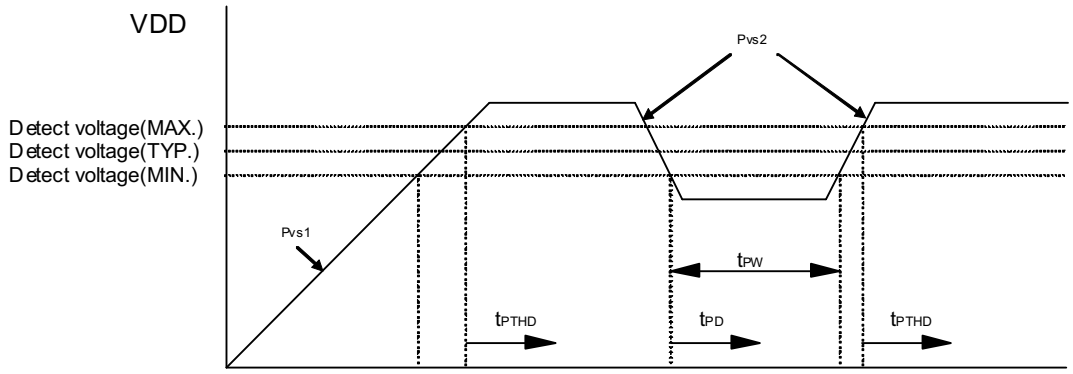
After DeepStop mode



3.4.3 POC characteristics

Table 3-6 POC characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Detection voltage	VPOC		2.8	2.9	3.0	V
Voltage slope 1	PVS1		0.18		1800	V/ms
Voltage slope 2	PVS2		0.0018		1800	V/ms
Response time 1	tPTHD	From detect voltage to release of reset signal. Voltage slope = PVS1, PVS2			2	ms
Response time 2	tPD	From detect voltage to occurence of reset signal Voltage slope = PVS2			2	ms
VDD minimum width	tPW		0.2			ms



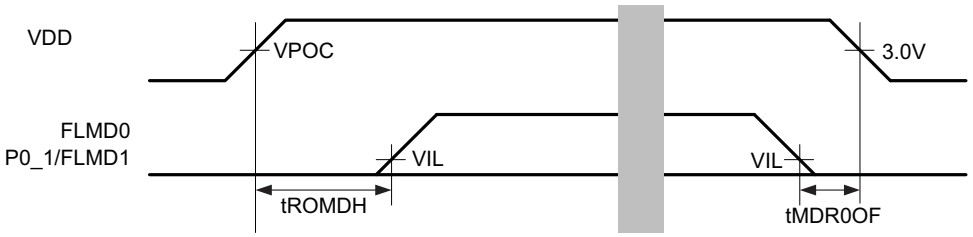
Note VDD: REG0VDD

3.5 Power-up/-down sequence of external supply voltages

3.5.1 Condition 1

RESET is not used

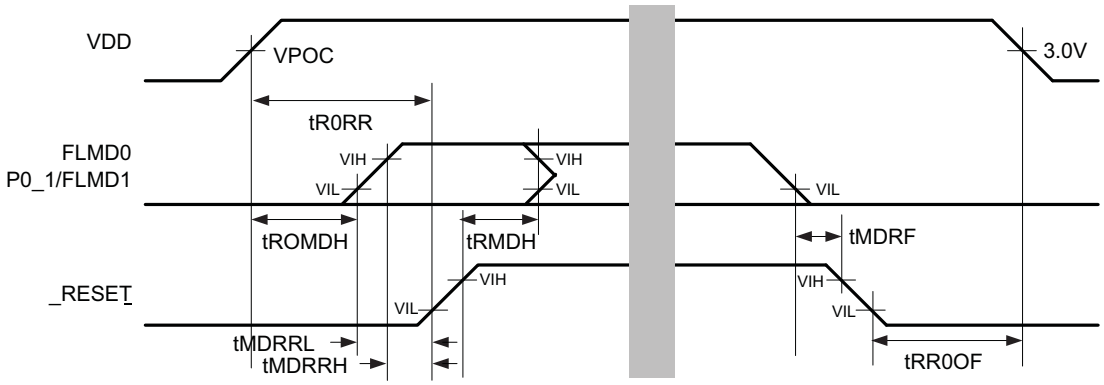
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
VDD (rise) to FLMD0,1(≤VIL) hold time	tR0MDH		2			ms
FLMD0,1 (≤VIL) to VDD (fall)	tMDR0OF		0			ms



3.5.2 Condition 2

RESET is used

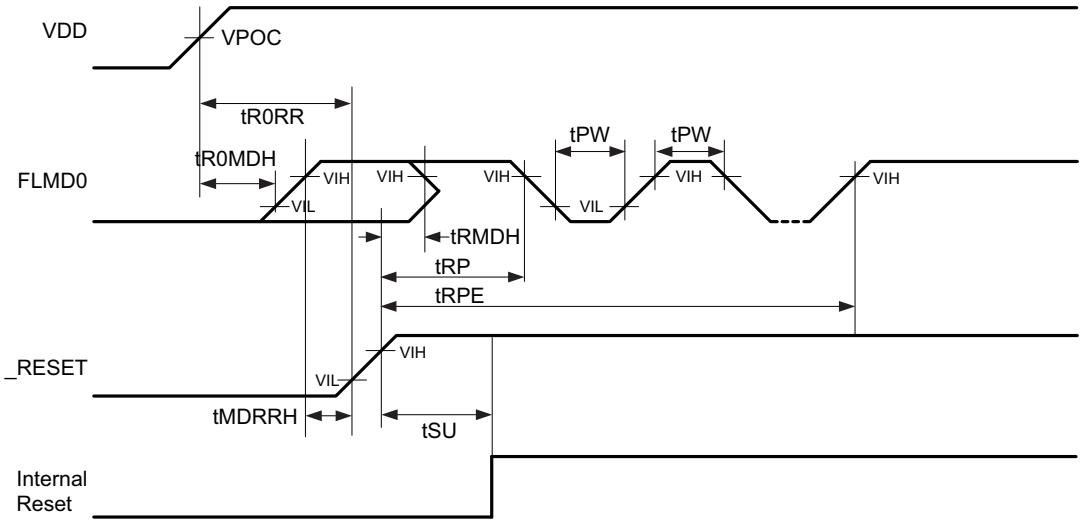
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
VDD (rise) to FLMD0,1(≤VIL) hold time	tR0MDH		1			ms
VDD (rise) to _RESET (≤VIL) hold time	tR0RR		2			ms
FLMD0,1 (≥VIH) to _RESET (rise)	tMDRRH		1			ms
FLMD0,1 (VIH or VIL1) to _RESET (rise)	tMDRRL		1			ms
_RESET (rise) to FLMD0,1(≥VIH or ≤VIL) hold time	tRMDH		1			ms
FLMD0,1(≤VIL) to _RESET (≥VIH) (fall) setup time	tMDRF		0			ms
_RESET (≤VIL) (fall) to VDD (fall) hold time	tRR0OF		0			ms



3.5.3 Condition 3

RESET is used.
Normal operating mode / Serial programming mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
VDD (rise) to FLMD0,1 (≤VIL) hold time	tR0MDH		1			ms
VDD (rise) to _RESET (≤VIL) hold time	tR0RR		2			ms
_RESET (≥VIH) to FLMD0 (≥VIH) hold time	tRMDH		1			ms
FLMD0(≥VIH) to _RESET (≤VIL) setup time	tMDRRH		1			ms
CPU start-up time (_RESET (≥VIH) to internal reset delay time)	tSU				2.5	ms
_RESET (≥VIH) to FLMD0 pulse input start time	tRP		tSU(max)+ 0.73			ms
_RESET (≥VIH) to FLMD0 pulse input end time	tRPE				tSU(max)+ 10	ms
FLMD0 low/high level width	tPW		0.8			µs



Chapter 4 Clock generators

4.1 CPU clock

Table 4-1 CPU clock frequency

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
CPU clock frequency	fCPU	≥768KB CodeFlash			64	MHz
		≤512KB CodeFlash			48	MHz

4.2 Peripheral clock

Table 4-2 Peripheral clock frequency

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Peripheral clock frequency	fPERI				48[a]	MHz

a) Some peripherals can be operated at 64MHz. Refer to the chapter ‘Clock Selection’ in the UM for details.

4.3 Oscillator characteristics

4.3.1 Main oscillator

A ceramic or crystal resonator can be connected to the main clock input pins as shown in figure *4-1 “Recommended Main Oscillator Circuit”*

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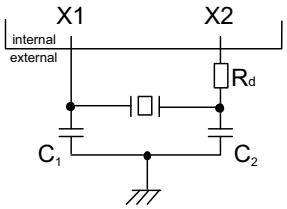


Figure 4-1 Recommended Main Oscillator Circuit

Caution Values of C_1, C_2 and R_d depend on the used ceramic or crystal resonator and must be specified in cooperation with ceramic or crystal resonator manufacturer.

(1) Main oscillator charactrisitics

Table 4-3 Main oscillator characteristics

Parameter	Symbol	Condition	Ratings	Unit
MainOSC frequency	fMOSC	Crystal / Ceramic	4, 5, 6, 8, 10, 12, 16, 20	MHz

Cautions

1. External clock input is prohibited.
2. General guidance for PCB layout:
   - Keep the wiring length as short as possible.
   - Do not cross the wiring with other signal lines.
   - Do not route this circuit close to a signal line with high fluctuating current flow.
   - Always make the ground point of the oscillator capacitor the same potential as REG0VSS and OSCVSS.
   - Do not ground the capacitor to a ground pattern with high current flow.
   - Do not tap signals from the oscillator.

4.3.2 Internal oscillator

Table 4-4 Internal oscillator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Lowspeed OSC frequency	fRL	• Other than DeepStop mode • DeepStop mode with PSC0.REGSTP = 0	220.8	240	259.2	kHz
	fRLLP	• DeepStop mode with PSC0.REGSTP = 1	172.0	240	268.0	kHz
Highspeed OSC frequency	fRH	• Other than DeepStop mode • DeepStop mode with PSC0.REGSTP = 0	7.2	8.0	8.8	MHz
		• Other than DeepStop mode • DeepStop mode with PSC0.REGSTP = 0 • ACT13M=1	8.558		17.41	MHz
	fRHLP	• DeepStop mode with PSC0.REGSTP = 1	5.3	8.0	9.0	MHz
		• DeepStop mode with PSC0.REGSTP = 1 • ACT13M=1	2.534		6.385	MHz

4.4 PLL Characteristics

Table 4-5 PLL characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Output frequency	fxxn	≥768KB CodeFlash	20		64	MHz
		≤512KB CodeFlash	20		48	MHz
Lock time	TLCKPn	PLL mode			50[a]	µs
Period jitter	TPEJTn				160[a]	ps
Long term jitter	TLTJTn	20µs			2500[a]	ps

a) Reference value, not tested in production

Chapter 5 I/O specification

5.1 Port Characteristics

5.1.1 Condition settings

Some of the conditions mentioned in this chapter can be selected by software. The related register settings are described below:

(1) Input characteristic

The input characteristics can be selected by the registers PIS and PISE with the following coding:

Table 5-1 Input characteristic selection for JP0_1, JP0_5, P0, P1, P3, P4

PISE	PIS	Reference in UserManual	Electrical characteristic
1	0	Type 3	Schmitt1
1	1	Type 4	Schmitt4[a]
0	x	Setting prohibited	

a) Default value after reset

Table 5-2 Input characteristic selection JP0_0, JP0_2, JP0_3

PISE	PIS	Reference in UserManual	Characteristic
0	1	Type 2	Schmitt2
1	1	Type 4	Schmitt4[a]
other than the above		Setting prohibited	

a) Default value after reset

Table 5-3 Input characteristic selection JP0_4

PISE	PIS	Reference in UserManual	Characteristic
1	1	Type 4	Schmitt4[a]
other than the above		Setting prohibited	

a) Default value after reset

Table 5-4 Input characteristic of RESET pin

PISE	PIS	Reference in UserManual	Characteristic
-	-	Type 2	Schmitt2[a]

a) Default value after reset (fixed)

5.1.2 PgE0

Table 5-5 PgE0 characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
High level input voltage	VIH	-	-		-	V
		Schmitt1	0.7·E0VDD		E0VDD+0.3	
		Schmitt2	0.8·E0VDD		E0VDD+0.3	
		Schmitt4 (E0VDD=VPOC~3.0)	0.84·E0VDD		E0VDD+0.3	
		Schmitt4 (E0VDD=3.0~5.5)	0.8·E0VDD		E0VDD+0.3	
Low level input voltage	VIL	-	-		-	V
		Schmitt1	-0.3		0.3·E0VDD	
		Schmitt2	-0.3		0.2·E0VDD	
		Schmitt4 (E0VDD=VPOC~3.4)	-0.3		0.4·E0VDD	
		Schmitt4 (E0VDD=3.4~5.5)	-0.3		0.5·E0VDD	
High level output voltage	VOH	IOH = -3mA	E0VDD-1.0			V
		IOH = -100µA	E0VDD-0.5			
Low level output voltage	VOL	IOL = 3mA			0.4	V
		IOL = 100µA			0.4	
Input hysteresis of Schmit	VH	Schmitt1	0.3			V
		Schmitt2	0.3			
		Schmitt4	0.1			
Internal pull-up resistor	RU		15	40	150	kΩ
Internal pull-down resistor	RD		15	40	150	kΩ
High level port output current	IOH	Power supply of PgE0 + PgE1			-120	mA
Low level port output current	IOL	Power supply of PgE0 + PgE1			120	mA
High level input leakage current	ILIH	VI = E0VDD			0.5	µA
Low level input leakage current	ILIL	VI = 0V			-0.5	µA
High level output leakage current	ILOH	VO = E0VDD			0.5	µA
Low level output leakage current	ILOL	VO = 0V			-0.5	µA
Output frequency	fO				20	MHz
Rise time (output)	tKRP				15	ns
Fall time (output)	tKFP				15	ns

5.1.3 PgE1

Table 5-6 PgE1 characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
High level input voltage	VIH	CMOS1	0.7·E1VDD		E1VDD+0.3	V
		Schmitt1	0.7·E1VDD		E1VDD+0.3	
		-	-		-	
		Schmitt4 (E1VDD=VPOC~3.0)	0.84·E1VDD		E1VDD+0.3	
		Schmitt4 (E1VDD=3.0~5.5)	0.8·E1VDD		E1VDD+0.3	
Low level input voltage	VIL	CMOS1	-0.3		0.3·E1VDD	V
		Schmitt1	-0.3		0.3·E1VDD	
		-	-		-	
		Schmitt4 (E1VDD=VPOC~3.4)	-0.3		0.4·E1VDD	
		Schmitt4 (E1VDD=3.4~5.5)	-0.3		0.5·E1VDD	
High level output voltage	VOH	IOH = -3mA	E1VDD-1.0			V
		IOH = -100µA	E1VDD-0.5			
Low level output voltage	VOL	IOL = 3mA			0.4	V
		IOL = 100µA			0.4	
Input hysteresis of Schmit	VH	Schmitt1	0.3			V
		-	-		-	
		Schmitt4	0.1			
Internal pull-up resistor	RU		15	40	150	kΩ
Internal pull-down resistor	RD		15	40	150	kΩ
High level port output current	IOH	Power supply of PgE1 + PgE0			-120	mA
Low level port output current	IOL	Power supply of PgE1 + PgE0			120	mA
High level input leakage current	ILIH	VI = E1VDD			0.5	µA
Low level input leakage current	ILIL	VI = 0V			-0.5	µA
High level output leakage current	ILOH	VO = E1VDD			0.5	µA
Low level output leakage current	ILOL	VO = 0V			-0.5	µA
Output frequency	FO				20	MHz
Rise time (output)	tKRP				15	ns
Fall time (output)	tKFP				15	ns

5.1.4 PgA0

Table 5-7 PgA0 characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
High level input voltage	VIH	CMOS1	0.7·AnVDD		AnVDD+0.3	V
Low level input voltage	VIL	CMOS1	-0.3		0.3·AnVDD	V
High level output voltage	VOH	IOH = -1mA	AnVDD-1.0			V
		IOH = -100µA	AnVDD-0.5			
Low level output voltage	VOL	IOL = 1mA			0.4	V
		IOL = 100µA			0.4	
High level port output current	IOH	Power supply of PgA0			-25	mA
Low level port output current	IOL	Power supply of PgA0			25	mA
High level input leakage current	ILIH	VI = AnVDD			0.5	µA
Low level input leakage current	ILIL	VI = 0V			-0.5	µA
High level output leakage current	ILOH	VO = AnVDD			0.5	µA
Low level output leakage current	ILOL	VO = 0V			-0.5	µA
Output frequency	fO				20	MHz
Rise time (output)	tKRP				15.5	ns
Fall time (output)	tKFP				15.5	ns

5.2 Analog noise filter

Noise filter

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Pulse width	tANFA tANFB	Except for Reset and DCUTRST	50		250	ns
	tANFC	Reset, DCUTRST	100		400	ns

Chapter 6 Supply current specification

6.1 Supply current of µPDF70F3580

Item	Power[a]	Condition[b]					Specification					Unit
	ISO	8MHz intOSC	Main OSC	PLL	CPU Freq	Peripherals	Min.	Typ.	(A)	(A1)	(A2)	
RUN mode	ON	ON	ON	ON	64	WORKING at 32MHz		18	30	33	36	mA
RUN mode (EEPROM emulation)	ON	ON	ON	ON	64	WORKING at 32MHz		35	58	61	64	mA
RUN mode	ON	ON	ON	ON	48	WORKING at 48MHz		18	30	33	36	mA
RUN mode (EEPROM emulation)	ON	ON	ON	ON	48	WORKING at 48MHz		35	58	61	64	mA
RUN mode	ON	ON	OFF	OFF	8	WORKING at 8MHz		6	18	20	22	mA
STOP mode	ON	OFF	OFF	OFF	-	STOPPED		1.3	12	13	16	mA
DEEPSTOP mode[c]	OFF	OFF	OFF	OFF	-	STOPPED[d]		0.025	0.220	0.250	0.300	mA

a) The AWO is always ON.
b) The 240kHz IntOSC is always ON.
c) With PSC0.REGSTP=1
d) Except Sequencer (SEQ) in digital input mode

Notes

1. The above currents do not include port buffer currents.
2. The currents in run mode include currents for self-programming.
3. The ‘typical’ specification is for reference only and not a guaranteed value. The ‘typical’ specification is applicable under the following conditions:
   - Ta = 25°C
   - REGnVDD=I0VDD=OSCVDD=EmVDD=AnVDD=5.0V
   - REGnVSS=OSCVSS=EmVSS=AnVSS=0V

6.2 Supply current of µPDF70F3579

Item	Power[a]	Condition[b]					Specification					Unit
	ISO	8MHz intOSC	Main OSC	PLL	CPU Freq	Peripherals	Min.	Typ.	(A)	(A1)	(A2)	
RUN mode	ON	ON	ON	ON	64	WORKING at 32MHz		18	30	33	36	mA
RUN mode (EEPROM emulation)	ON	ON	ON	ON	64	WORKING at 32MHz		35	58	61	64	mA
RUN mode	ON	ON	ON	ON	48	WORKING at 48MHz		18	30	33	36	mA
RUN mode (EEPROM emulation)	ON	ON	ON	ON	48	WORKING at 48MHz		35	58	61	64	mA

Item	Power[a]	Condition[b]					Specification					Unit
	ISO	8MHz intOSC	Main OSC	PLL	CPU Freq	Peripherals	Min.	Typ.	(A)	(A1)	(A2)	
RUN mode	ON	ON	OFF	OFF	8	WORKING at 8MHz		6	18	20	22	mA
STOP mode	ON	OFF	OFF	OFF	-	STOPPED		1.3	12	13	16	mA
DEEPSTOP mode[c]	OFF	OFF	OFF	OFF	-	STOPPED[d]		0.025	0.220	0.250	0.300	mA

a) The AWO is always ON.
b) The 240kHz IntOSC is always ON.
c) With PSC0.REGSTP=1
d) Except Sequencer (SEQ) in digital input mode

Notes
1. The above currents do not include port buffer currents.
2. The currents in run mode include currents for self-programming.
3. The 'typical' specification is for reference only and not a guaranteed value. The 'typical' specification is applicable under the following conditions:
   - Ta = 25°C
   - REGnVDD=I0VDD=OSCVDD=EmVDD=AnVDD=5.0V
   - REGnVSS=OSCVSS=EmVSS=AnVSS=0V

6.3 Supply current of µPDF70F3578

Item	Power[a]	Condition[b]					Specification					Unit
	ISO	8MHz intOSC	Main OSC	PLL	CPU Freq	Peripherals	Min.	Typ.	(A)	(A1)	(A2)	
RUN mode	ON	ON	ON	ON	64	WORKING at 32MHz		-	-	-	-	mA
RUN mode	ON	ON	ON	ON	48	WORKING at 48MHz		17	28	31	34	mA
RUN mode (EEPROM emulation)	ON	ON	ON	ON	48	WORKING at 48MHz		34	56	59	62	mA
RUN mode	ON	ON	OFF	OFF	8	WORKING at 8MHz		6	16	17	18	mA
STOP mode	ON	OFF	OFF	OFF	-	STOPPED		1.3	12	13	16	mA
DEEPSTOP mode[c]	OFF	OFF	OFF	OFF	-	STOPPED[d]		0.025	0.220	0.250	0.300	mA

a) The AWO is always ON.
b) The 240kHz IntOSC is always ON.
c) With PSC0.REGSTP=1
d) Except Sequencer (SEQ) in digital input mode

Notes
1. The above currents do not include port buffer currents.
2. The currents in run mode include currents for self-programming.
3. The 'typical' specification is for reference only and not a guaranteed value. The 'typical' specification is applicable under the following conditions:
   - Ta = 25°C
   - REGnVDD=I0VDD=OSCVDD=EmVDD=AnVDD=5.0V
   - REGnVSS=OSCVSS=EmVSS=AnVSS=0V

6.4 Supply current of µPDF70F3577

Item	Power[a]	Condition[b]					Specification					Unit
	ISO	8MHz intOSC	Main OSC	PLL	CPU Freq	Peripherals	Min.	Typ.	(A)	(A1)	(A2)	
RUN mode	ON	ON	ON	ON	64	WORKING at 32MHz		-	-	-	-	mA
RUN mode	ON	ON	ON	ON	48	WORKING at 48MHz		17	28	31	34	mA
RUN mode (EEPROM emulation)	ON	ON	ON	ON	48	WORKING at 48MHz		34	56	59	62	mA
RUN mode	ON	ON	OFF	OFF	8	WORKING		6	16	17	18	mA
STOP mode	ON	OFF	OFF	OFF	-	STOPPED		1.3	12	13	16	mA
DEEPSTOP mode[c]	OFF	OFF	OFF	OFF	-	STOPPED[d]		0.025	0.220	0.250	0.300	mA

a) The AWO is always ON.
b) The 240kHz IntOSC is always ON.
c) With PSC0.REGSTP=1
d) Except Sequencer (SEQ) in digital input mode

Notes
1. The above currents do not include port buffer currents.
2. The currents in run mode include currents for self-programming.
3. The ‘typical’ specification is for reference only and not a guaranteed value. The ‘typical’ specification is applicable under the following conditions:
   - Ta = 25°C
   - REGnVDD=I0VDD=OSCVDD=EmVDD=AnVDD=5.0V

6.5 Supply current of µPDF70F3576

Item	Power[a]	Condition[b]					Specification					Unit
	ISO	8MHz intOSC	Main OSC	PLL	CPU Freq	Peripherals	Min.	Typ.	(A)	(A1)	(A2)	
RUN mode	ON	ON	ON	ON	64	WORKING at 32MHz		-	-	-	-	mA
RUN mode	ON	ON	ON	ON	48	WORKING at 48MHz		17	28	31	34	mA
RUN mode (EEPROM emulation)	ON	ON	ON	ON	48	WORKING at 48MHz		34	56	59	62	mA
RUN mode	ON	ON	OFF	OFF	8	WORKING at 8MHz		6	16	17	18	mA
STOP mode	ON	OFF	OFF	OFF	-	STOPPED		1.3	12	13	16	mA
DEEPSTOP mode[c]	OFF	OFF	OFF	OFF	-	STOPPED[d]		0.025	0.220	0.250	0.300	mA

a) The AWO is always ON.
b) The 240kHz IntOSC is always ON.
c) With PSC0.REGSTP=1
d) Except Sequencer (SEQ) in digital input mode

Notes
1. The above currents do not include port buffer currents.

2. The currents in run mode include currents for self-programming.
3. The ‘typical’ specification is for reference only and not a guaranteed value. The ‘typical’ specification is applicable under the following conditions:
   - Ta = 25°C
   - REGnVDD=I0VDD=OSCVDD=EmVDD=AnVDD=5.0V

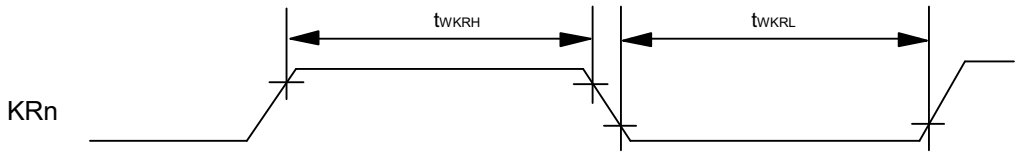
Chapter 7 Peripherals specification

7.1 Reset timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
RESET input Low level width	tWRSL		450			ns

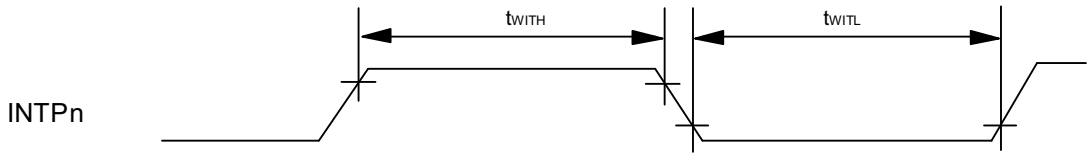
7.2 NMI timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
NMI input High level width	tWNIH		300			ns
NMI input Low level width	tWNIL		300			ns



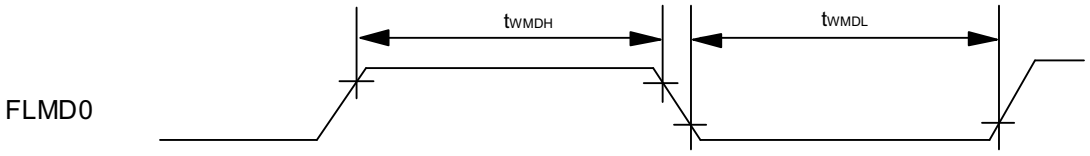
7.3 INTP timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
INTPn input High level width	tWITH		300			ns
INTPn input Low level width	tWITL		300			ns



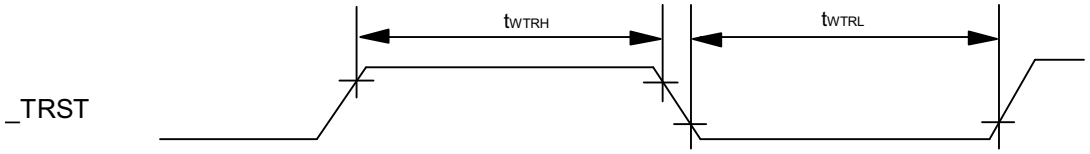
7.4 FLMD0 timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
FLMD0 input High level width	tWMDH		300			ns
FLMD0 input Low level width	tWMDL		300			ns
FLMD0 external pull down resistor	R_{FLMD0}		82k			Ohm



7.5 _DCUTRST timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
_DCUTRST input High level width	tWRH		450			ns
_DCUTRST input Low level width	tWTRL		450			ns



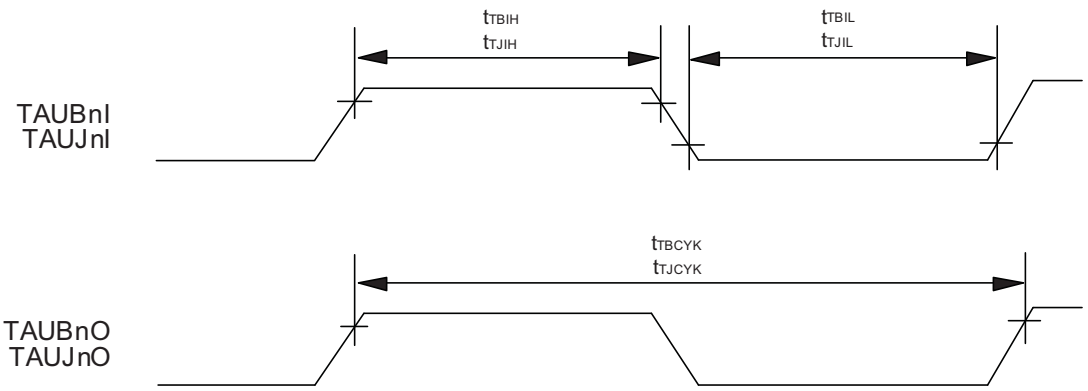
7.6 Timer timing

Table 7-1 Timer timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
TAUBnI input High level width	tTBIH	n=0	a, b			ns
TAUBnI input Low level width	tTBIL	n=0	a,b			ns
TAUJnI input High level width	tTJIH	n=0	300			ns
TAUJnI input Low level width	tTJIL	n=0	300			ns
TAUBnO output cycle	tTBCYK				20	MHz
TAUJnO output cycle	tTJCYK				20	MHz

a) With digital noise filter enabled: 2, 3, 4 or 5 x Tsamp + 20 (Tsamp shows sampling period specified in Noise filter macro. More than 1 PCLK width of Timer macro must be kept regarding DNF pass through pulse width.

b) With digital noise filter disabled: 1xtSYNC+20 (tSYNC: 1 PCLK of Timer macro)



7.7 CSI timing

7.7.1 Master modes

(1) CSIG timing

Table 7-2 CSIG timing (Master mode)

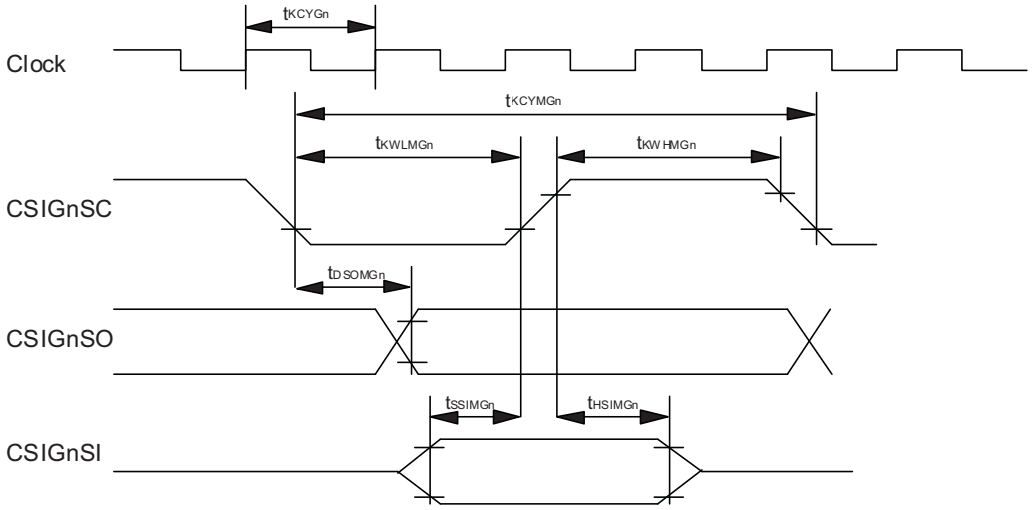
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Macro Operation clock cycle time	tKCYGn		20.83			ns
CSIGnSC cycle time	tKCYMGn		100			ns
CSIGnSC high level width	tKWHMGn		0.5 · tKCYMGn-10			ns
CSIGnSC low level width	tKWLMGn		0.5 · tKCYMGn-10			ns
CSIGnSI setup time (vs. CSIGnSC)	tSSIMGn		30			ns
CSIGnSI hold time (vs. CSIGnSC)	tHSIMGn		0			ns
CSIGnSO output delay (vs. CSIGnSC)	tDSOMGn				7	ns
CSIGnRYI setup time (vs. CSIGnSC)	tSRYIGn	CSIGnCTL1.CSIGnSIT=x CSIGnCTL1.CSIGnHSE=1	2 · tKCYGn+25			ns
CSIGnRYI High level width	tWRYIGn	CSIGnCTL1.CSIGnHSE=1	tKCYGn- 5.0			ns

Note n: Number of macro instances. Refer to the User Manual for the detailed specification.

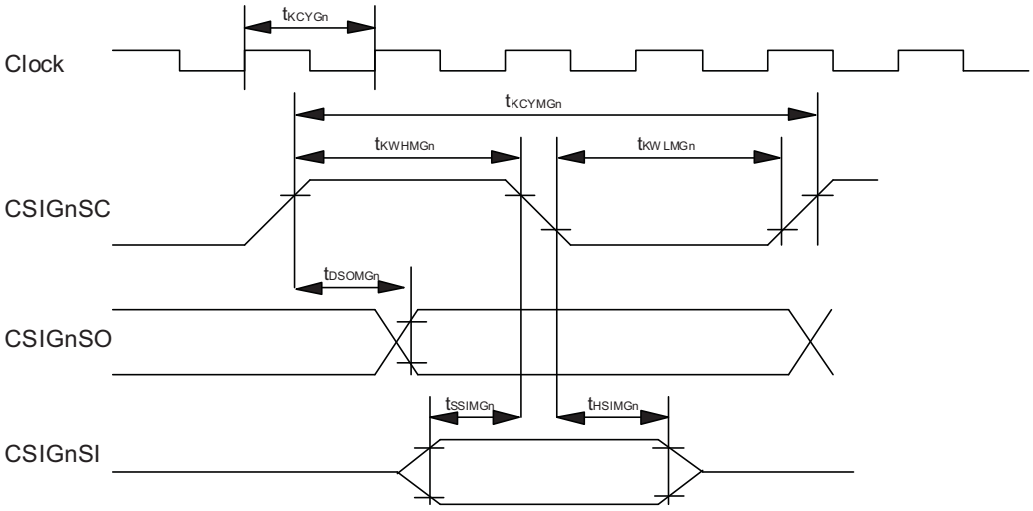
(2) Timing diagrams

SCKO / SI / SO

CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 0 / 0 or 1 / 1)



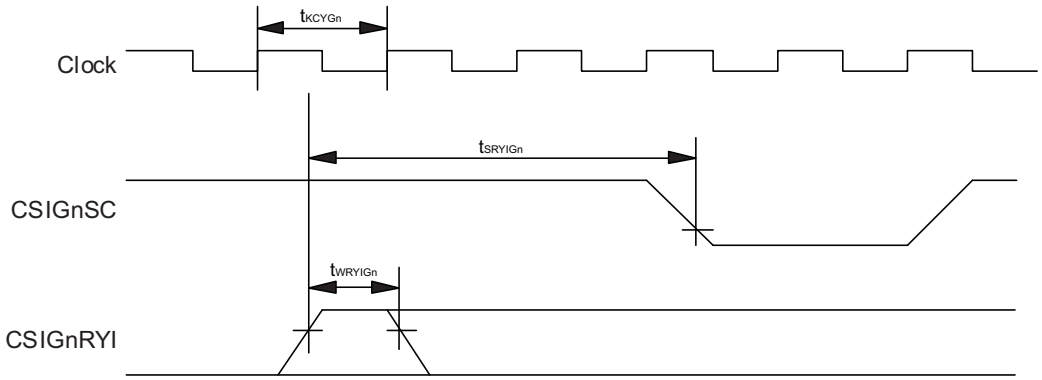
CSIG(CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 1 / 0 or 0 / 1)



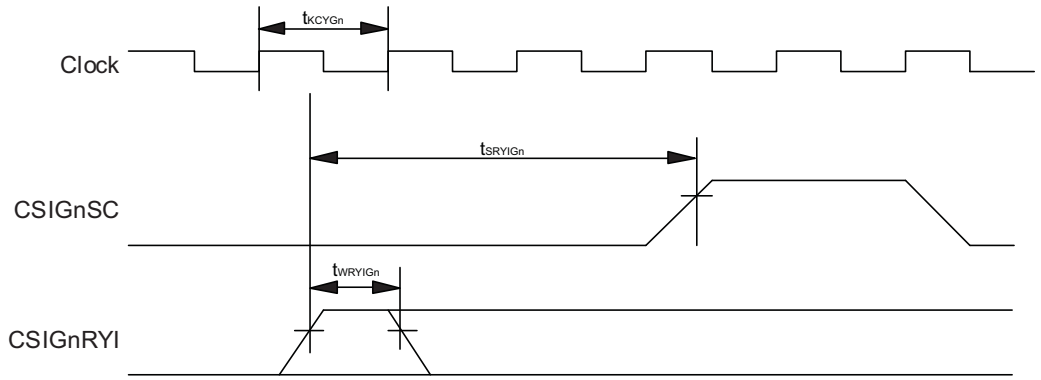
RYI

CSIGnCTL1 : CSIGnHSE=1, CSIGnCTL1 : CSIGnSIT = 0)

CSIG (CSIGnCTL1 :CSIGnCKR= 0)



CSIG (CSIGnCTL1 :CSIGnCKR= 1)



7.7.2 Slave mode

(1) CSIG timing slave mode

Table 7-3 CSIG timing (Slave mode)

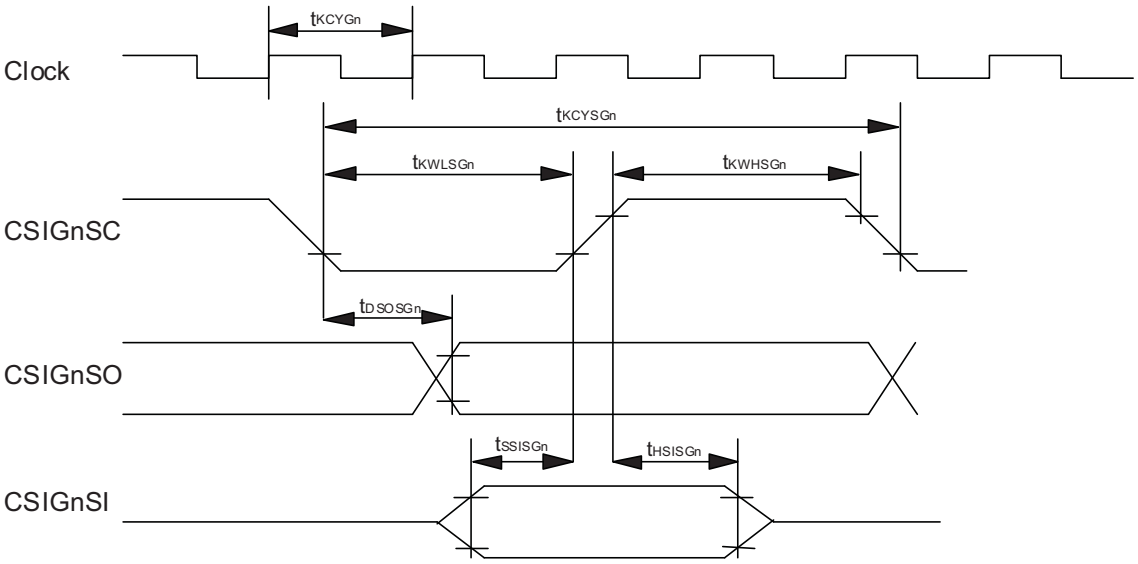
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Macro Operation clock cycle time	tKCYGn		20.83			ns
CSIGnSC cycle time	tKCYSGn		200			ns
CSIGnSC high level width	tKWHSGn		0.5 · tKCYSGn-10			ns
CSIGnSC low level width	tKWLSGn		0.5 · tKCYSGn-10			ns
CSIGnSI setup time (vs. CSIGnSC)	tSSISGn		20			ns
CSIGnSI hold time (vs. CSIGnSC)	tHSISGn		tKCYGn+5.0			ns
SO output delay (vs SCKI)	tDSOSGn				35	ns
CSIGnRYO output delay	tSRYOGn				35	ns
_CSIGnSSI setup time (vs CSIGnSC)	tSSSISGn		0.5 · tKCYSn-5.0			ns
_CSIGnSSI hold time (vs CSIGnSC)	tHSSISGn		tKCY+5.0			ns

Note n: Number of macro instances. Refer to the User Manual for the detailed specification.

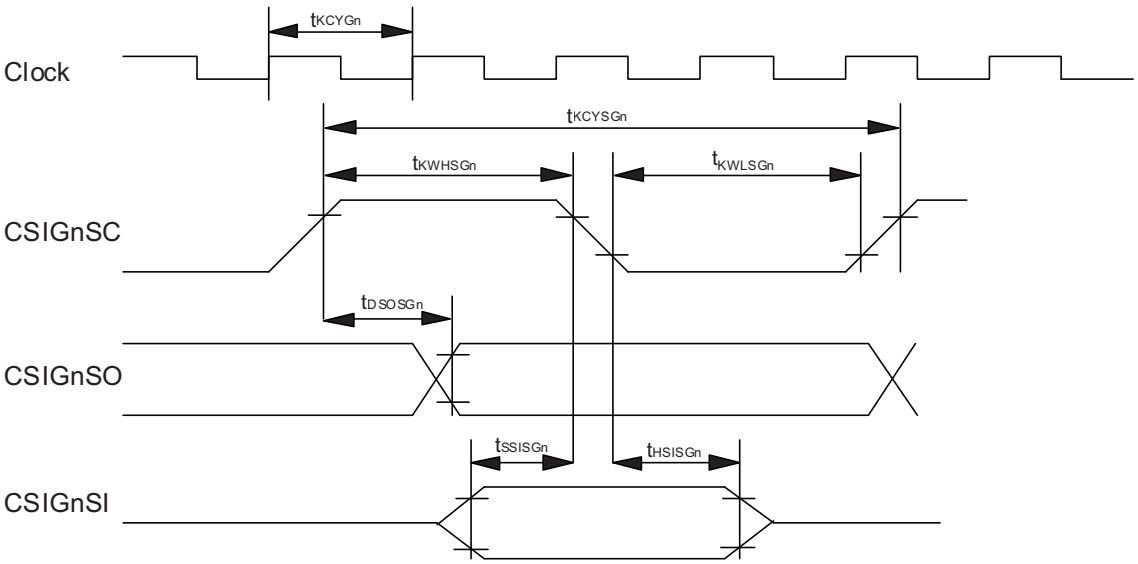
(2) Timing diagrams

SCKO / SI / SO

CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 0/0 or 1/1)

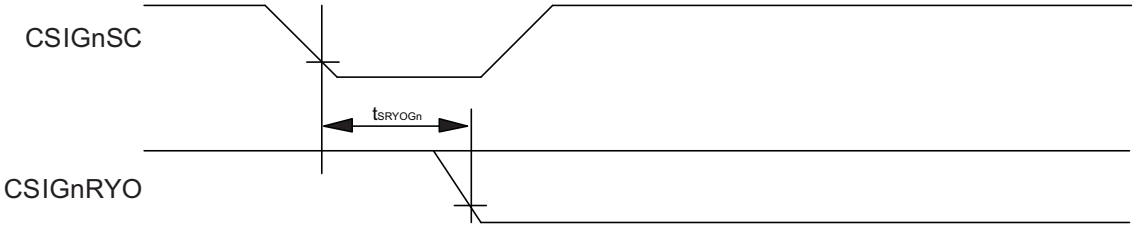


CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 1/0 or 0/1)

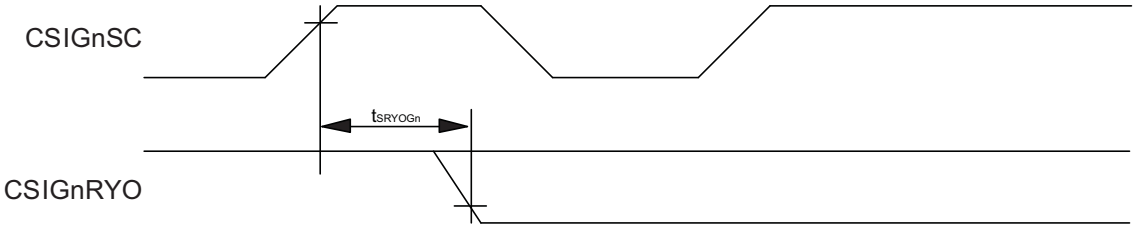


RYO

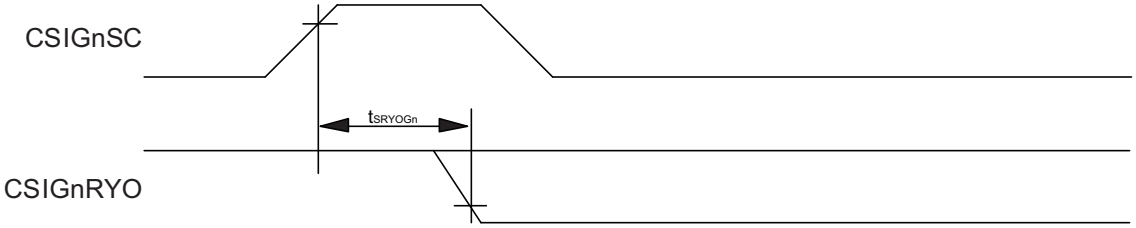
CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 0/0)



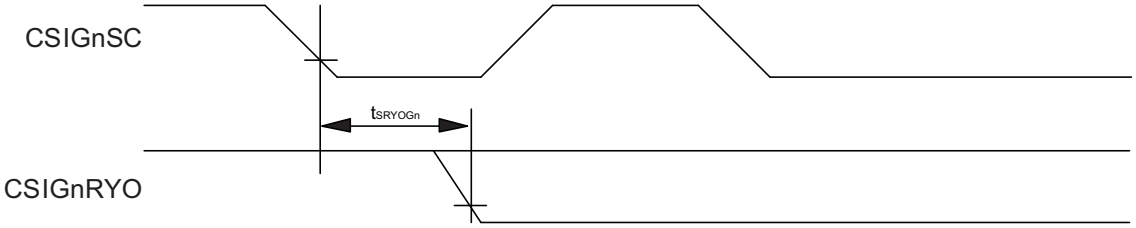
CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 0/1)



CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 1/0)

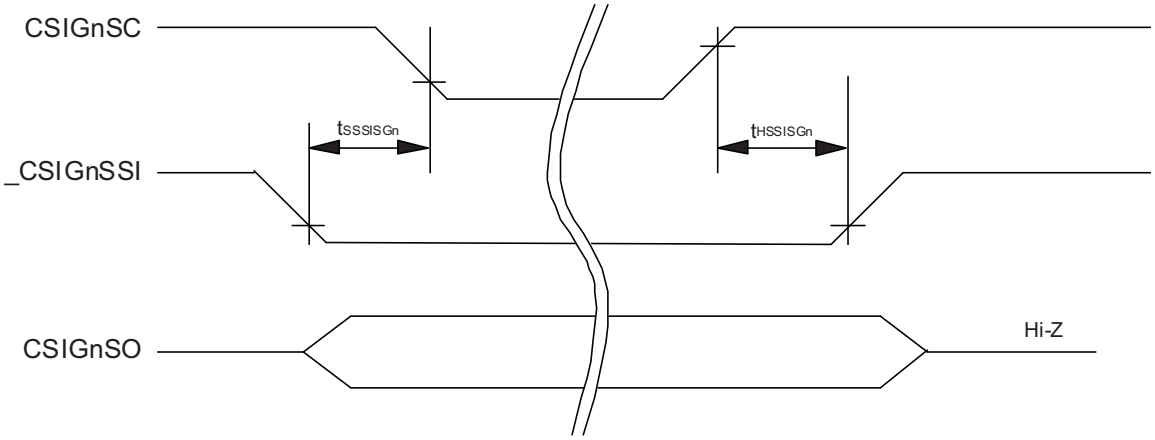


CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 1/1)

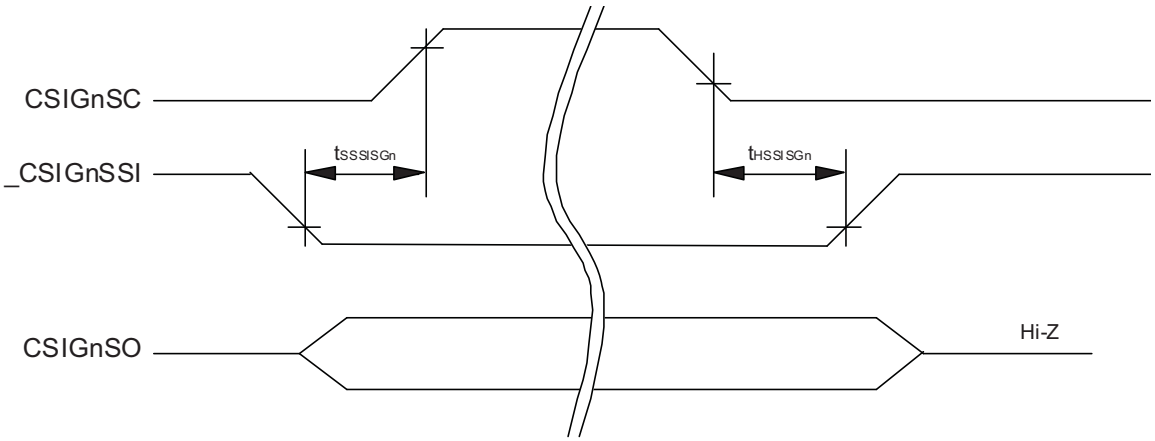


SSI:

CSIG (CSIGnCTL1 :CSIGnSSE=1, CSIGnCTL1 : CSIGnCKR,/ CSIGnCFG0 : CHIGnDAP0 = 0/0 or 1/1)



CSIG (CSIGnCTL1 :CSIGnSSE=1, CSIGnCTL1 : CSIGnCKR,/ CSIGnCFG0 : CHIGnDAP0 = 1/0 or 0/1) n=0, 4

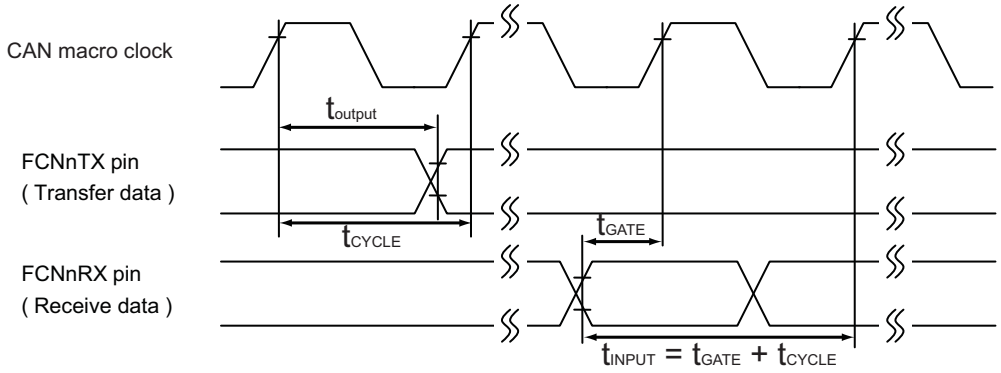


7.8 UART timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Transfer rate					1.5	Mbps

7.9 aFCAN timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Transfer rate					1	Mbps
Internal delay time	tINTDEL				37.5	ns
CAN Node delay time	tNODE	tCYCLE = 62.5ns			100	ns



CAN node delay time (t_{NODE}) = INPUT delay time (t_{input}) + Output delay time (t_{output})
Internal delay time (t_{INTDEL}) = Internal gate delay time (t_{GATE}) + Output delay time (t_{output})

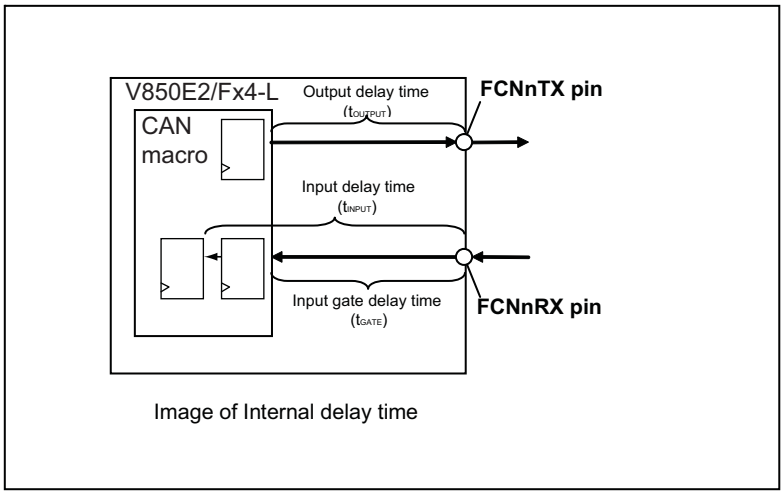


Image of Internal delay time

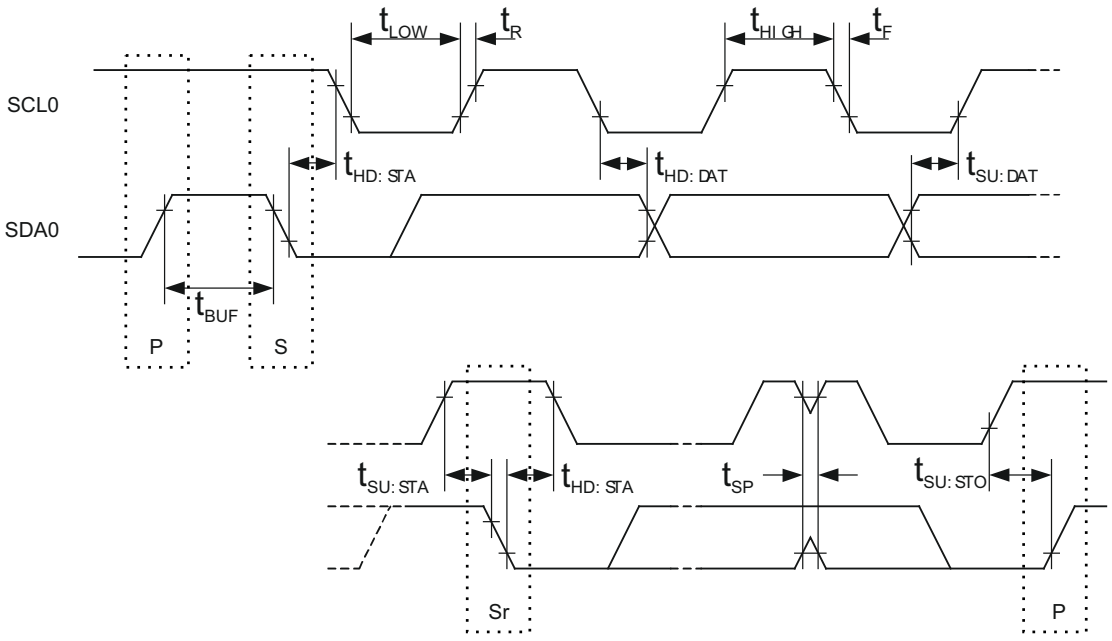
7.10 IIC timing

Table 7-4 Normal mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
SCL clock period	fCLK		0		100	kHz
Bus free time (between stop condition and start condition)	tBUF		4.7			µs
Start/Restart Hold time (New clock pulse is generated after this hold time as a master.)	tHD:STA		4			µs
SCL clock low state hold time	tLOW		4.7			µs
SCL clock high state hold time	tHIGH		4			µs
Setup time for start/restart condition	tSU:STA		4.7			µs
Data hold time	tHD:DAT	CBUS compatible	5			µs
		IIC bus	0			µs
Data setup time	tSU:DAT		250			ns
Rising transition time of SDA or SCL	tR				1000	ns
Falling transition time of SDA or SCL	tF				300	ns
Setup time of stop condition	tSU:STO		4			µs
Noise elimination width	tSP					ns
Bus capacitance	Cb				400	pF

Table 7-5 Fast mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
SCL clock period	fCLK		0		400	kHz
Bus free time (between stop condition and start condition)	tBUF		1.3			µs
Start/Restart Hold time (New clock pulse is generated after this hold time as a master.)	tHD:STA		0.6			µs
SCL clock low state hold time	tLOW		1.3			µs
SCL clock high state hold time	tHIGH		0.6			µs
Setup time for start/restart condition	tSU:STA		0.6			µs
Data hold time	tHD:DAT	CBUS compatible				µs
		IIC bus	0		0.9	µs
Data setup time	tSU:DAT		100			ns
Rising transition time of SDA or SCL	tR		20+0.1Cb		300	ns
Falling transition time of SDA or SCL	tF		20+0.1Cb		300	ns
Setup time of stop condition	tSU:STO		0.6			µs
Noise elimination width	tSP		0		50	ns
Bus capacitance	Cb				400	pF



Notes 1. P: Stop condition

Notes 1. S: Start condition

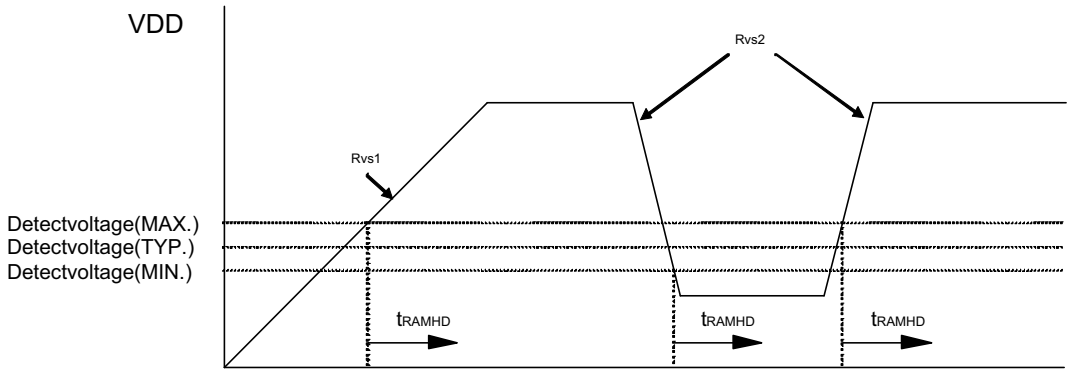
Notes 1. Sr: Restart condition

7.11 VLVI characteristics

Table 7-6 VLVI characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Detection voltage	VRAMHF		1.8	1.9	2.0	V
Voltage slope1	Rvs1		0.18		1800	V/ms
Voltage slope2	Rvs2		0.0018		1800	V/ms
Response time[a]	tRAMHD				2	ms

a) From detection voltage to setting of VLVF bit (VLVF.bit0)

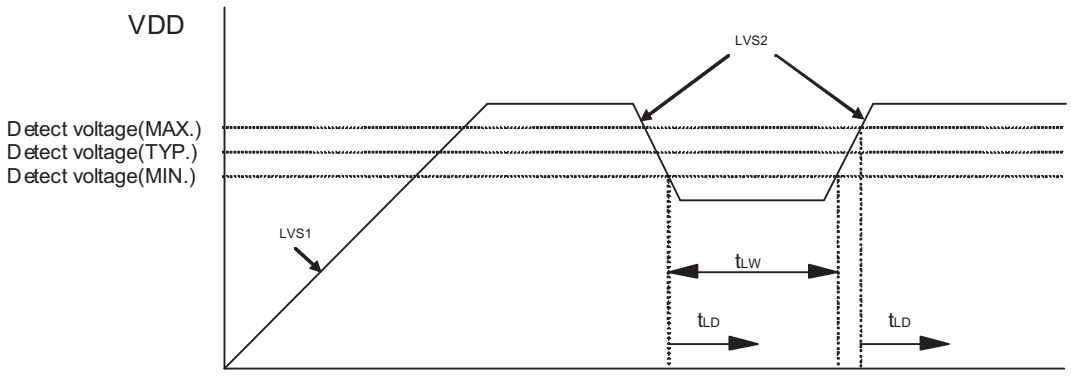


Note VDD: REG0VDD

7.12 LVI characteristics

Table 7-7 LVI characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Detection voltage	VLVI0	LVICNT.LVICNT[2:0]=001_B	3.9	4.0	4.1	V
	VLVI1	LVICNT.LVICNT[2:0]=010_B	3.6	3.7	3.8	V
	VLVI2	LVICNT.LVICNT[2:0]=011_B	3.4	3.5	3.6	V
Voltage slope2	LVS2		0.0018		1800	V/ms
Response time	tLD				2.0	ms
VDD minimum width	tLW		2			ms
Stabilization time	tLVIST	LVICNT0,1 is set to 1, then LVI is ready to operate			350	µs



7.13 A/D Converter characteristics

7.13.1 10bit A/D

Table 7-8 10 bit A/D

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RES0		10	10	10	bit
Total conversion time	TCON0		2		10	µs
Overall error	TOE0	Excluding quantization error			±3.5	LSB
Non-liniarity error	ILE0				±4.0	LSB
Differencial liniarity error	DLE0				±1.0	LSB
Zero scale error	ZSE0				±3.5	LSB
Full scale error	FSE0				±3.5	LSB
Analog input voltage	VAIN0		A0VSS		A0VDD	V
Power on stabilization time[a]				110	520	ns
A0VDD current[b]	AIDD0				4	mA
Conversion error by diagnosis function					+/-20[c]	LSB

a) 'Power on' refers to
- setting ADCA0GPS = 1 or
- STOP mode release

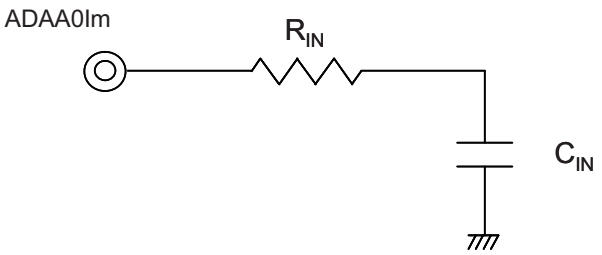
b) Excluding port currents

c) Value might change after device evaluation has finished

Notes
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
2. m: Number of channels. Refer to the User Manual for the detailed specification.

Notes
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
2. m: Number of channels. Refer to the User Manual for the detailed specification.

7.13.2 Equivalent circuit



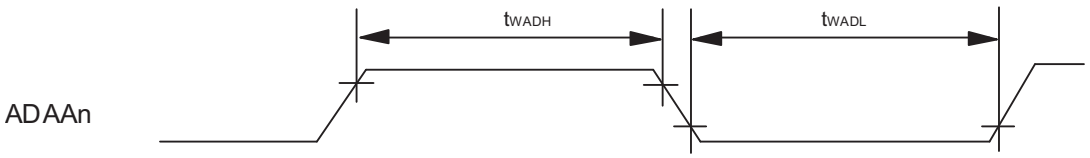
Terminals	Condition	R_{IN}[kΩ]	C_{IN}[pF]
ADAA0Im		1.2	11.9

Caution These specifications are not tested in outgoing inspection. Therefore R_{IN} and C_{IN} values are not guaranteed and are reference values only.
Additionally these values are specified as maximum values.

7.13.3 ADTRG timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
ADAAnTRGm input High level width	tWADH		300			ns
ADAAnTRGm input Low level width	tWADL		300			ns

Notes
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
2. m: Number of channels. Refer to the User Manual for the detailed specification.

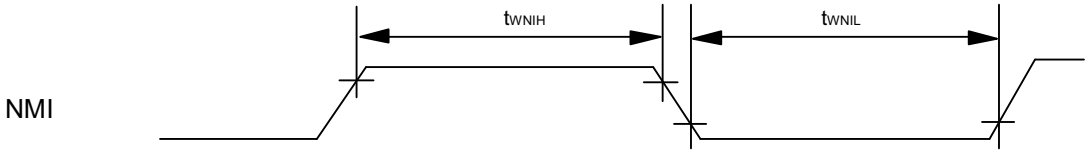


7.14 Key Return

Table 7-9

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
KRn input High level width	tWKRH		300			ns
KRn input Low level width	tWKRL		300			ns

Note n: Number of instances. Refer to the User Manual for the detailed specification.



Chapter 8 Memory specification

8.1 Code flash specification

Table 8-1 Code flash

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Number of Re-Writes[a]	CWRT	Data retention 20 years			1000	times
Programming Temperature	tPRG	(A) grade products	-40		85	°C
		(A1) grade products	-40		110	°C
		(A2) grade products	-40		125	°C

a) Please contact RENESAS sales office regarding specification other than the above.

8.2 Data flash specification

Table 8-2 Data flash

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Number of Re-Writes	DWRT	Data retention 20 years			100000	times
Programming Temperature	tPRG	(A) grade products	-40		85	°C
		(A1) grade products	-40		110	°C
		(A2) grade products	-40		125	°C

8.3 Serial write operation specification

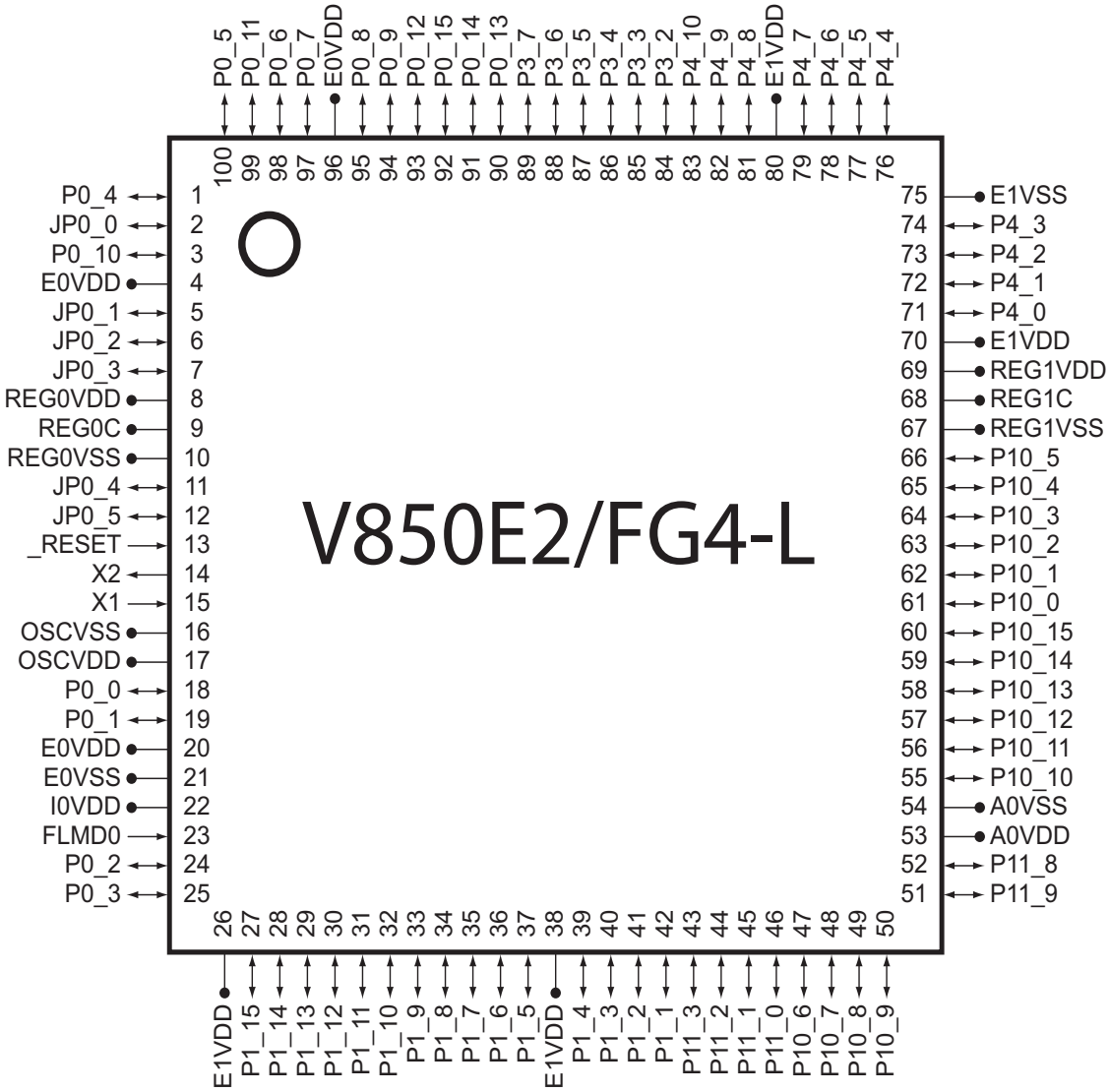
Serial write operation

Parameter	Symbol	Condition	Ratings[a]			Unit
			Min	Typ	Max	
Programming time		per 128KB			2.1	s
Erase time		per 128KB			1.92	s

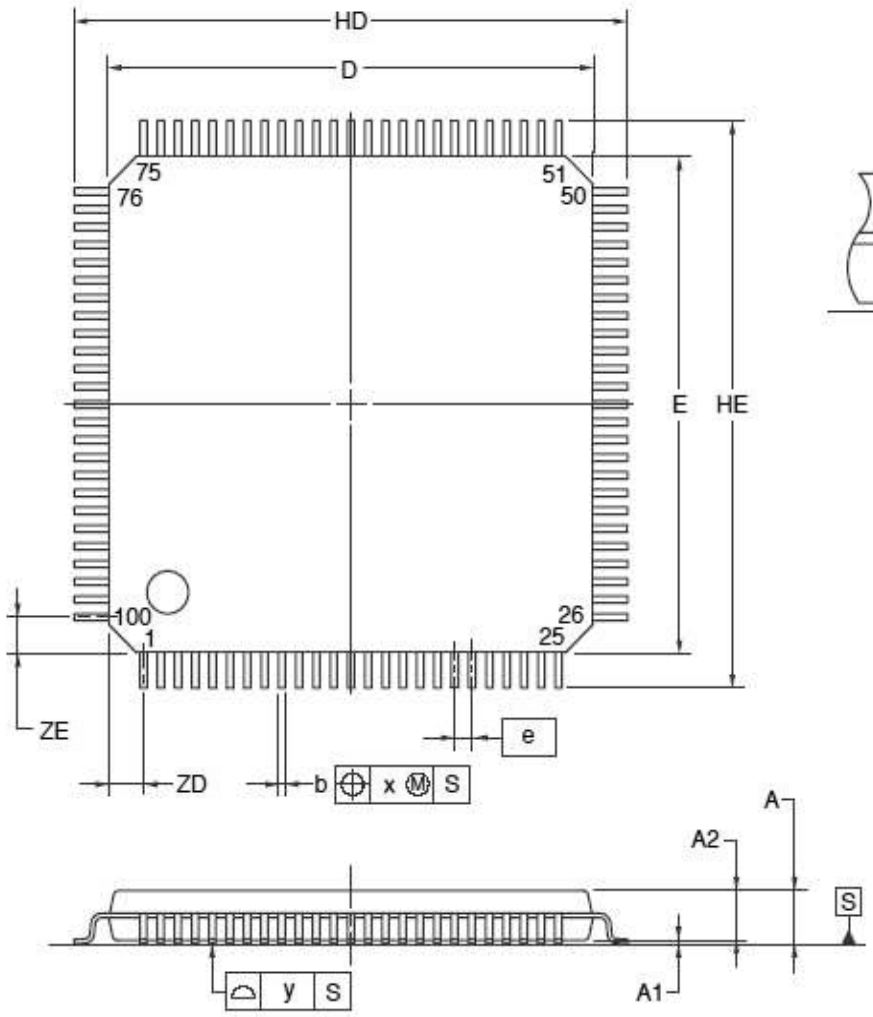
a) Values are for reference only

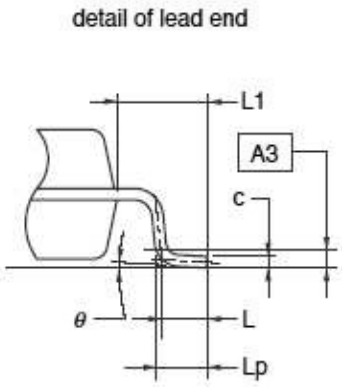
Chapter 9 Pinning and package specification

9.1 Pinning specification



9.2 Package specification





(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

P100GC-50-UEU-1

Revision History

Version	Date	Document number	Major changes
1.0	2012-08-30	R01DS0147ED0100	Initial release (previous document was EASE-DS-0035-1.2)