PRELIMINARY

Am29200™ and Am29205™

RISC Microcontrollers

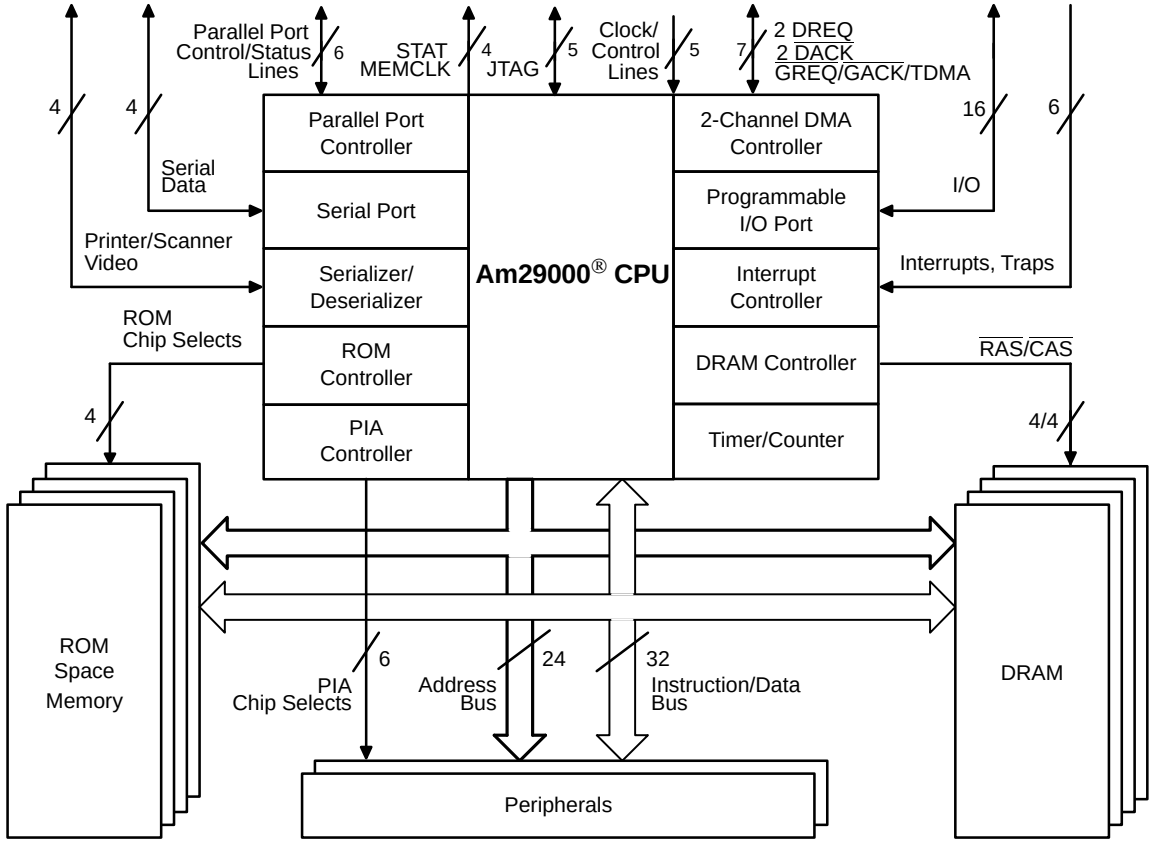
Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

Am29200 Microcontroller

- Completely integrated system for embedded applications
- Full 32-bit architecture
- CMOS technology/TTL-compatible
- 16- and 20-MHz operating frequencies
- 8 million instructions per second (MIPS) sustained at 16 MHz
- 304-Mbyte address space
- 192 general-purpose registers
- Three-address instruction architecture
- Fully pipelined
- Glueless system interfaces with on-chip wait state control
- Four banks of ROM, each separately programmable for 8-, 16-, or 32-bit interface
- Four banks of DRAM, each separately programmable for 16- or 32-bit interface
- Burst-mode and page-mode access support
- On-chip DRAM mapping
- Two-channel DMA controller with queuing on one channel
- 6-port peripheral interface adapter
- 16-line programmable I/O port

Am29200 MICROCONTROLLER BLOCK DIAGRAM



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- **Bidirectional bit serializer/deserializer (video interface)**
- **Serial port (UART)**
- **Bidirectional parallel port controller**
- **Interrupt controller**
- **On-chip timer**
- **Binary compatibility with all 29K™ Family microcontrollers and microprocessors**
- **Advanced debugging support**
- **IEEE Std 1149.1-1990 (JTAG) compliant Standard Test Access Port and Boundary Scan Architecture**

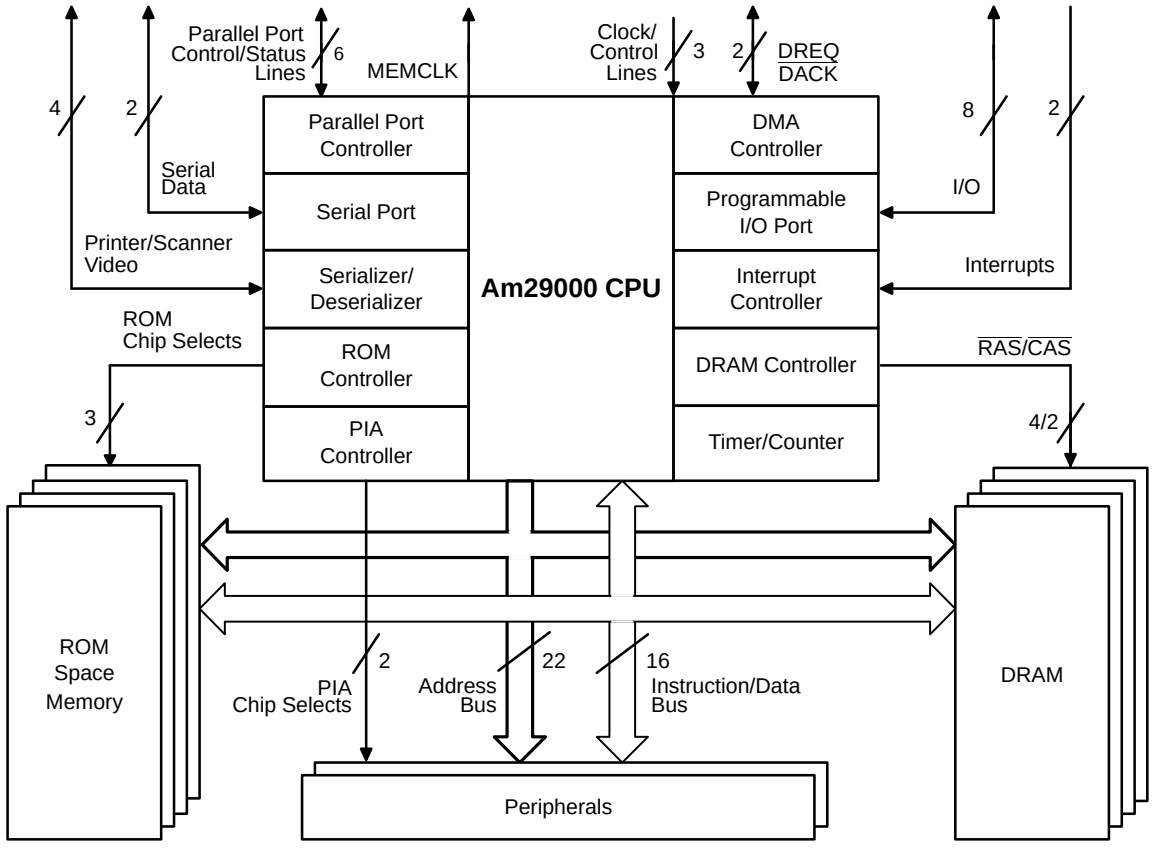
DISTINCTIVE CHARACTERISTICS

Am29205 Microcontroller

The low-cost Am29205 microcontroller is similar to the Am29200 microcontroller, with a 16-bit instruction/data bus, fewer peripheral ports, and no JTAG interface. It includes the following features:

- **Completely integrated system for embedded applications**
- **Full 16-bit external, 32-bit internal architecture**
- **Upgradeable to the Am29200 32-bit RISC microcontroller**
- **12- and 16-MHz operating frequencies**
- **68-Mbyte address space**
- **Two-channel DMA controller (one external)**
- **Three separately programmable ROM banks with 8- and 16-bit ROM interface**
- **Fully functional 16-bit DRAM interface complete with address MUXing, Refresh, and RAS/CAS generation**
  - —Page-mode access support
  - —On-chip DRAM mapping
- **Two-port peripheral interface adapter**
- **Eight-line programmable I/O port**
- **Bidirectional bit serializer/deserializer (video interface)**
- **Serial port (UART)**
- **Bidirectional parallel port controller**
- **Interrupt controller**
- **On-chip timer**
- **Binary compatibility with all 29K Family microcontrollers and microprocessors**

Am29205 MICROCONTROLLER BLOCK DIAGRAM



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GENERAL DESCRIPTION

The Am29200 and Am29205 RISC microcontrollers are highly integrated, 32-bit embedded processors implemented in complementary metal-oxide semiconductor (CMOS) technology. Based on the 29K architecture, the Am29200 and Am29205 microcontrollers are part of a growing family of RISC microcontrollers, which also includes the high-performance Am29240™, Am29245™, and Am29243™ RISC microcontrollers. A feature summary of the Am29200 RISC microcontroller family is included in Table 1.

Through submicron technology, the Am29200 and Am29205 microcontrollers incorporate a complete set of system facilities commonly found in printing, imaging, graphics, and other embedded applications. The on-chip functions include: a ROM controller, a DRAM controller, a peripheral interface adapter, a DMA controller, a serializer/deserializer, a programmable I/O port, a parallel port, a serial port, and an interrupt controller. For a complete description of the technical features, on-chip peripherals, programming interface, and instruction set, please refer to the *Am29200 and Am29205 RISC Microcontrollers User's Manual* (order #16362).

The Am29200 and Am29205 RISC microcontrollers are well suited for embedded applications since they provide better performance than the CISC processors typically used in these applications. Compared to the CISC processors, the Am29200 and Am29205 microcontrollers offer superior price/performance and design flexibility for the designer. Coupled with hardware and software development tools from AMD® and the AMD Fusion29K® Partners, the Am29200 and Am29205 microcontrollers provide very quick time-to-market.

Am29200 Microcontroller

The Am29200 microcontroller meets the common requirements of embedded applications such as industrial control, graphics processing, imaging applications, laser printers, and general purpose applications requiring high performance in a compact design.

The Am29200 microcontroller is available in a 168-lead Plastic Quad Flat Pack (PQFP) package. The PQFP has 140 signal pins and 28 power/ground pins.

Am29205 Microcontroller

The Am29205 RISC microcontroller is a highly integrated, low-cost derivative of the Am29200 32-bit RISC microcontroller. The Am29205 microcontroller is functionally very similar to an Am29200 microcontroller operating with 16-bit external memories.

The Am29205 microcontroller is designed specifically for low-cost general purpose embedded applications, as well as graphics processors, mass storage controllers, network interfaces, application program interface (API) accelerators, scanners, and laser printers.

The Am29205 microcontroller is available in a 100-lead PQFP package. The PQFP has 84 signal pins and 16 power/ground pins.

RELATED AMD PRODUCTS

29K Family Devices

Part No.	Description
Am29000®	32-bit RISC microprocessor
Am29005™	Low-cost 32-bit RISC microprocessor with no MMU and no branch target cache
Am29030™	32-bit RISC microprocessor with 8-Kbyte instruction cache
Am29035™	32-bit RISC microprocessor with 4-Kbyte instruction cache
Am29050™	32-bit RISC microprocessor with on-chip floating point
Am29240™	32-bit RISC microcontroller with 4-Kbyte instruction cache and 2-Kbyte data cache
Am29245™	Low-cost 32-bit RISC microcontroller with 4-Kbyte instruction cache
Am29243™	32-bit RISC data microcontroller with instruction and data caches and DRAM parity

Table 1. Product Comparison—Am29200 Microcontroller Family

FEATURE	Am29205 Microcontroller	Am29200 Microcontroller	Am29245 Microcontroller	Am29240 Microcontroller	Am29243 Microcontroller
Instruction Cache	—	—	4 Kbytes	4 Kbytes	4 Kbytes
Data Cache	—	—	—	2 Kbytes	2 Kbytes
Integer Multiplier	Software	Software	Software	32 x 32-bit	32 x 32-bit
Memory Management Unit (MMU)	—	—	1 TLB 16 Entry	1 TLB 16 Entry	2 TLBs 32 Entry
Data Bus Width					
Internal	32 bits	32 bits	32 bits	32 bits	32 bits
External	16 bits	32 bits	32 bits	32 bits	32 bits
ROM Interface					
Banks	3	4	4	4	4
Width	8, 16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	16, 32 bits
ROM Size (Max/Bank)	4 Mbytes	16 Mbytes	16 Mbytes	16 Mbytes	16 Mbytes
Boot-Up ROM Width	16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
Burst-Mode Access	Not Supported	Supported	Supported	Supported	Supported
DRAM Interface					
Banks	4	4	4	4	4
Width	16 bits only	16, 32 bits	16, 32 bits	16, 32 bits	8, 16, 32 bits
Size: 32-Bit Mode	—	16 Mbytes/bank	16 Mbytes/bank	16 Mbytes/bank	16 Mbytes/bank
Size: 16-Bit Mode	8 Mbytes/bank	8 Mbytes/bank	8 Mbytes/bank	8 Mbytes/bank	8 Mbytes/bank
Video DRAM	Not Supported	Supported	Supported	Supported	Not Supported
Access Cycles					
Initial/Burst	3/2	3/2	2/1	2/1	2/1
DRAM Parity	No	No	No	No	Yes
On-Chip DMA					
Width (ext. peripherals)	8, 16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
Externally Controlled	1 Channel	2 Channels	2 Channels	4 Channels	4 Channels
External Master Access	No	Yes	Yes	Yes	Yes
External Master Burst	No	No	Yes	Yes	Yes
External Terminate Signal	No	Yes	Yes	Yes	Yes
Double-Frequency CPU Option	No	No	No	Yes	Yes
Low Voltage Operation	No	No	Yes	Yes	Yes
Peripheral Interface Adapter (PIA)					
PIA Ports	2	6	6	6	6
Data Width	8, 16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
Min. Cycles Access	3	3	2	2	2
Programmable I/O Port (PIO)					
Signals	8	16	16	16	16
Signals programmable for interrupt generation	8	8	8	8	8
Serial Ports					
Ports $\overline{\text{DSR}}$/$\overline{\text{DTR}}$	1 Port PIO signals	1 Port Supported	1 Port Supported	2 Ports 1 Port Supported	2 Ports 1 Port Supported
Interrupt Controller					
External Interrupt Pins	2	4	4	4	4
External Trap and Warn Pins	0	3	3	3	3
Parallel Port Controller	Yes	Yes	Yes	Yes	Yes
32-Bit Transfer	No	Yes	Yes	Yes	Yes
JTAG Debug Support	No	Yes	Yes	Yes	Yes
Serializer/Deserializer	Yes	Yes	Yes	Yes	No
Pin Count and Package	100 PQFP	168 PQFP	196 PQFP	196 PQFP	196 PQFP
Processor Clock Rate	12, 16 MHz	16, 20 MHz	16 MHz	20, 25, 33 MHz	20, 25, 33 MHz

29K FAMILY DEVELOPMENT SUPPORT PRODUCTS

Contact your local AMD representative for information on the complete set of development support tools. The following software and hardware development products are available on several hosts:

- Optimizing compilers for common high-level languages
- Assembler and utility packages
- Source- and assembly-level software debuggers
- Target-resident development monitors
- Simulators
- Execution boards

THIRD-PARTY DEVELOPMENT SUPPORT PRODUCTS

The Fusion29K Program of Partnerships for Application Solutions provides the user with a vast array of products designed to meet critical time-to-market needs. Products and solutions available from the AMD Fusion29K Partners include

- Silicon products
- Software generation and debug tools
- Hardware development tools
- Board level products
- Laser printer solutions
- Networking and communication solutions
- Multiuser, kernel, and real-time operating systems
- Graphics solutions
- Manufacturing support
- Custom software consulting, support, and training

KEY FEATURES AND BENEFITS

Complete Set of Common System Peripherals

The Am29200 and Am29205 microcontrollers minimize system cost by incorporating a complete set of system facilities commonly found in embedded applications, eliminating the cost of additional components.

The on-chip functions include: a ROM controller, a DRAM controller, a peripheral interface adapter, a DMA controller, a programmable I/O port, a parallel port, a serial port, and an interrupt controller. A serializer/deserializer (video interface) is also included for printer, scanner, and other imaging applications.

By providing glueless interfacing to external memories and a complete set of common system peripherals on-chip, these microcontrollers let product designers capitalize on the very low system cost made possible by the integration of processor and peripherals. Many simple systems can be built using only the Am29200 or Am29205 microcontroller and external ROM and/or DRAM memory.

ROM Controller

The ROM controller supports four individual banks of ROM or other static memory in the Am29200 microcontroller and three banks in the Am29205 microcontroller. Each ROM bank has its own timing characteristics, and each bank may be of a different size: either 8, 16, or 32 bits wide in the Am29200 microcontroller and 8 or 16 bits wide in the Am29205 microcontroller. The ROM banks can appear as a contiguous memory area of up to 64 Mbytes in size on the Am29200 microcontroller. The ROM controller also supports writes to the ROM memory space for devices such as flash EPROMs and SRAMs.

DRAM Controller

The DRAM controller supports four separate banks of dynamic memory. On the Am29200 microcontroller, each bank can be a different size: either 16 or 32 bits wide. DRAM banks on the Am29205 microcontroller are 16 bits wide. The DRAM banks can appear as a contiguous memory area of up to 64 Mbytes in size on the Am29200 microcontroller and 32 Mbytes on the Am29205 microcontroller. To support system functions such as on-the-fly data compression and decompression, four 64-Kbyte regions of the DRAM can be mapped into a 16-Mbyte virtual address space.

DMA Controller

The DMA controller in the Am29200 microcontroller provides two channels for transfer of data between the DRAM and internal or external peripherals. One of the DMA channels is double buffered to relax the constraints on the reload time. On the Am29205 microcontroller, internal 32-bit transfers are supported on two DMA channels; external transfers are limited to 8- or 16-bit data accesses on one DMA channel.

Peripheral Interface Adapter (PIA)

The peripheral interface adapter allows for additional system features implemented by external peripheral chips. The PIA permits glueless interfacing from the Am29200 microcontroller to as many as six external peripheral regions and from the Am29205 microcontroller to two external peripherals.

Interrupt Controller

The interrupt controller generates and reports the status of interrupts caused by on-chip peripherals.

I/O Port

The Am29200 microcontroller's I/O port permits direct access to 16 individually programmable external input/output signals. Eight signals are available on the Am29205 microcontroller. These eight signals can be configured to cause interrupts on either microcontroller.

Serializer/Deserializer

The bidirectional bit serializer/deserializer (video interface) permits direct connection to a number of laser marking engines, video displays, or raster input devices such as scanners.

Serial Port

The serial port implements a full-duplex UART.

Parallel Port

The parallel port implements a bidirectional IBM PC-compatible parallel interface to a host processor.

Wide Range of Price/Performance Points

To reduce design costs and time-to-market, one basic system design can be used as the foundation for an entire product line. From this design, numerous implementations of the product at various levels of price and performance may be derived with minimum time, effort, and cost.

The Am29200 and Am29205 microcontrollers provide this capability through programmable memory widths, burst-mode and page-mode access support, programmable wait states, and hardware and 29K Family software compatibility. A system can be upgraded without hardware and software redesign using various memory architectures.

The ROM controller on the Am29205 microcontroller accommodates memories that are either 8 or 16 bits wide, while that of the Am29200 microcontroller supports either 8-, 16-, or 32-bit memories. The DRAM controller on the Am29205 microcontroller accommodates dynamic memories that are 16 bits wide; the Am29200 microcontroller supports either 16- or 32-bit memories.

These unique features provide a flexible interface to low-cost memory as well as a convenient, flexible upgrade path. For example, a system can start with a 16-bit memory design and can subsequently improve performance by migrating to a 32-bit memory design. One particular advantage is the ability to add memory in half-megabyte increments. This provides significant cost savings for applications that do not require larger memory upgrades.

The Am29200 microcontroller family allows users to address a wide range of cost performance points, with higher performance and lower cost than existing designs based on CISC microprocessors.

Glueless System Interfaces

The Am29200 and Am29205 microcontrollers minimize system cost by providing a glueless attachment to external ROMs, DRAMs, and other peripheral components. Processor outputs have edge-rate control that allows them to drive a wide range of load capacitances with low noise and ringing. This eliminates the cost of external logic and buffering.

Bus- and Binary-Compatibility

Compatibility within a processor family is critical for achieving a rational, easy upgrade path. The Am29200 and Am29205 microcontrollers are members of a bus-compatible family of RISC microcontrollers, which also includes the high-performance Am29240, Am29245, and Am29243 microcontrollers. Future members of this family will improve in price and performance and system capabilities without requiring that users redesign their system hardware or software. Bus compatibility ensures a convenient upgrade path for future systems.

The Am29200 microcontroller is binary compatible with the Am29240, Am29245, and Am29243 microcontrollers, as well as the Am29000, Am29005, Am29030, Am29035, and Am29050 microprocessors. The Am29200 microcontroller family provides a migration path to low-cost, highly integrated systems for products based on other 29K Family microprocessors, without requiring expensive rewrites of application software.

Complete Development and Support Environment

A complete development and support environment is vital for reducing a product's time-to-market. Advanced Micro Devices has created a standard development environment for the 29K Family of processors. In addition, the Fusion29K third-party support organization provides the most comprehensive customer/partner program in the embedded processor market.

Advanced Micro Devices offers a complete set of hardware and software tools for design, integration, debugging, and benchmarking. These tools, which are available now for the 29K Family, include the following:

- High C® 29K optimizing C compiler with assembler, linker, ANSI library functions, and 29K architectural simulator
- XRAY29K™ source-level debugger
- MiniMON29K™ debug monitor
- A complete family of demonstration and development boards

In addition, Advanced Micro Devices has developed a standard host interface (HIF) specification for operating system services, the Universal Debug Interface (UDI) for seamless connection of debuggers to ICEs and target

hardware, and extensions for the UNIX common object file format (COFF).

This support is augmented by an engineering hotline, an on-line bulletin board, and field application engineers.

PERFORMANCE OVERVIEW

The Am29200 and Am29205 microcontrollers offer a significant margin of performance over CISC microprocessors in existing embedded designs, since the majority of processor features were defined for the maximum achievable performance at a very low cost. This section describes the features of the Am29200 and Am29205 microcontrollers from the point of view of system performance.

Instruction Timing

The Am29200 and Am29205 microcontrollers use an arithmetic/logic unit, a field shift unit, and a prioritizer to execute most instructions. Each of these is organized to operate on 32-bit operands and provide a 32-bit result. All operations are performed in a single cycle.

The performance degradation of load and store operations is minimized in the Am29200 and Am29205 microcontrollers by overlapping them with instruction execution, by taking advantage of pipelining, and by organizing the flow of external data into the processor so that the impact of external accesses is minimized.

Pipelining

Instruction operations are overlapped with instruction fetch, instruction decode and operand fetch, instruction execution, and result write-back to the register file. Pipeline forwarding logic detects pipeline dependencies and routes data as required, avoiding delays that might arise from these dependencies.

Pipeline interlocks are implemented by processor hardware. Except for a few special cases, it is not necessary to rearrange programs to avoid pipeline dependencies, although this is sometimes desirable for performance.

Burst-Mode and Page-Mode Memories

The Am29200 microcontroller directly supports burst-mode memories in ROM address space. The burst-mode memory supplies instructions at the maximum bandwidth, without the complexity of an external cache or the performance degradation due to cache misses.

Both the Am29200 and Am29205 microcontrollers can also use the page-mode capability of common DRAMs to improve the access time in cases where page-mode accesses can be used. This is particularly useful in very low-cost systems with 16-bit-wide DRAMs, where the DRAM must be accessed twice for each 32-bit operand.

Instruction Set Overview

The Am29200 and Am29205 microcontrollers employ a three-address instruction set architecture. The compiler or assembly-language programmer is given complete freedom to allocate register usage. There are 192 general-purpose registers, allowing the retention of intermediate calculations and avoiding needless data destruction. Instruction operands may be contained in any of the general-purpose registers, and the results may be stored into any of the general-purpose registers.

The instruction set contains 117 instructions that are divided into nine classes. These classes are integer arithmetic, compare, logical, shift, data movement, constant, floating point, branch, and miscellaneous. The floating-point instructions are not executed directly, but are emulated by trap handlers.

All directly implemented instructions are capable of executing in one processor cycle, with the exception of interrupt returns, loads, and stores.

Data Formats

The Am29200 and Am29205 microcontrollers define a word as 32 bits of data, a half-word as 16 bits, and a byte as 8 bits. The hardware provides direct support for word-integer (signed and unsigned), word-logical, word-boolean, half-word integer (signed and unsigned), and character data (signed and unsigned).

Word-boolean data is based on the value contained in the most significant bit of the word. The values TRUE and FALSE are represented by the MSB values 1 and 0, respectively.

Other data formats, such as character strings, are supported by instruction sequences. Floating-point formats (single and double precision) are defined for the processor; however, there is no direct hardware support for these formats in the Am29200 or Am29205 microcontroller.

Protection

The Am29200 and Am29205 microcontrollers offer two mutually exclusive modes of execution, the user and supervisor modes, that restrict or permit accesses to certain processor registers and external storage locations.

The register file may be configured to restrict accesses to supervisor-mode programs on a bank-by-bank basis.

DRAM Mapping

The Am29200 and Am29205 microcontrollers provide a 16-Mbyte region of virtual memory that is mapped to one of four 64-Kbyte blocks in the physical DRAM memory. This supports system functions such as on-the-fly data compression and decompression, allowing a large data

structure such as a frame buffer to be stored in a compressed format while the application software operates on a region of the structure that is decompressed. Using a mechanism that is analogous to demand paging, system software moves data between the compressed and decompressed formats in a way that is invisible to the application software. This feature can greatly reduce the amount of memory required for printing, imaging, and graphics applications.

Interrupts and Traps

When the microcontroller takes an interrupt or trap, it does not automatically save its current state information in memory. This lightweight interrupt and trap facility greatly improves the performance of temporary interruptions such as simple operating-system calls that require no saving of state information.

In cases where the processor state must be saved, the saving and restoring of state information is under the control of software. The methods and data structures used to handle interrupts—and the amount of state information saved—may be tailored to the needs of a particular system.

Interrupts and traps are dispatched through a 256-entry vector table which directs the processor to a routine that handles a given interrupt or trap. The vector table may be relocated in memory by the modification of a processor register. There may be multiple vector tables in the system, though only one is active at any given time.

The vector table is a table of pointers to the interrupt and trap handlers and requires only 1 Kbyte of memory. The processor performs a vector fetch every time an interrupt or trap is taken. The vector fetch requires at least three cycles, in addition to the number of cycles required for the basic memory access.

DEBUGGING AND TESTING

Software debugging on the Am29200 and Am29205 microcontrollers is facilitated by the instruction trace facility and instruction breakpoints. Instruction tracing is accomplished by forcing the processor to trap after each instruction has been executed. Instruction breakpoints are implemented by the HALT instruction or by a software trap.

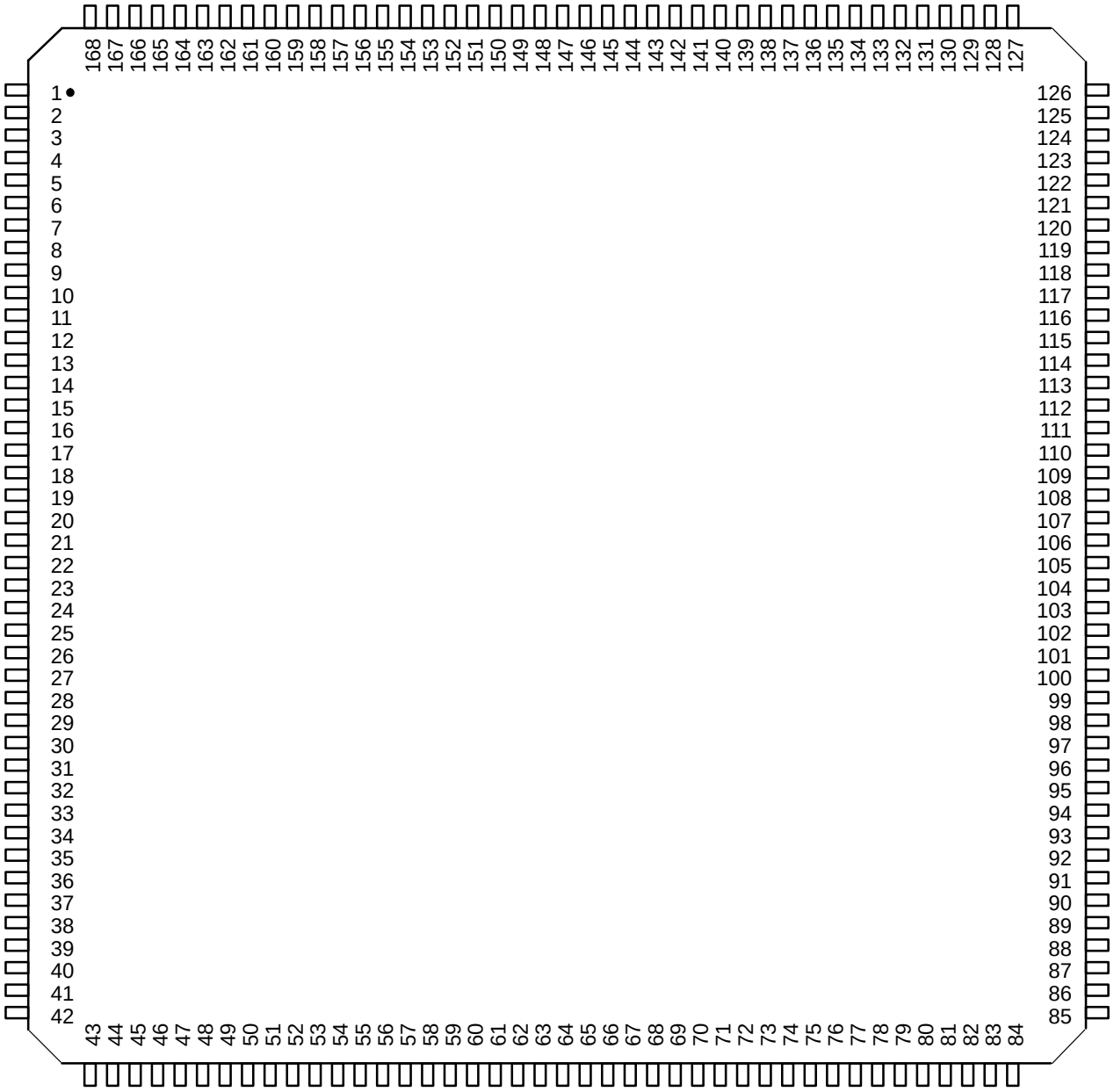
The Am29200 microcontroller provides two additional features to assist system debugging and testing:

- The test/development interface is composed of a group of pins that indicate the state of the processor and control the operation of the processor.
- An IEEE Std. 1149.1–1990 (JTAG) compliant Standard Test Access Port and Boundary-Scan Architecture provides a scan interface for testing system hardware in a production environment. It contains extensions that allow a hardware-development system to control and observe the processor without interposing hardware between the processor and system.

Hardware testing and debugging on the Am29205 microcontroller are supported by using an Am29200 microcontroller to emulate an Am29205 microcontroller.

CONNECTION DIAGRAMS

168-Lead Plastic Quad Flat Pack (PQR 168)—Am29200 Microcontroller
Top View



Note:
Pin 1 is marked for orientation.

PQFP PIN DESIGNATIONS (Sorted by Pin Number)—Am29200 Microcontroller

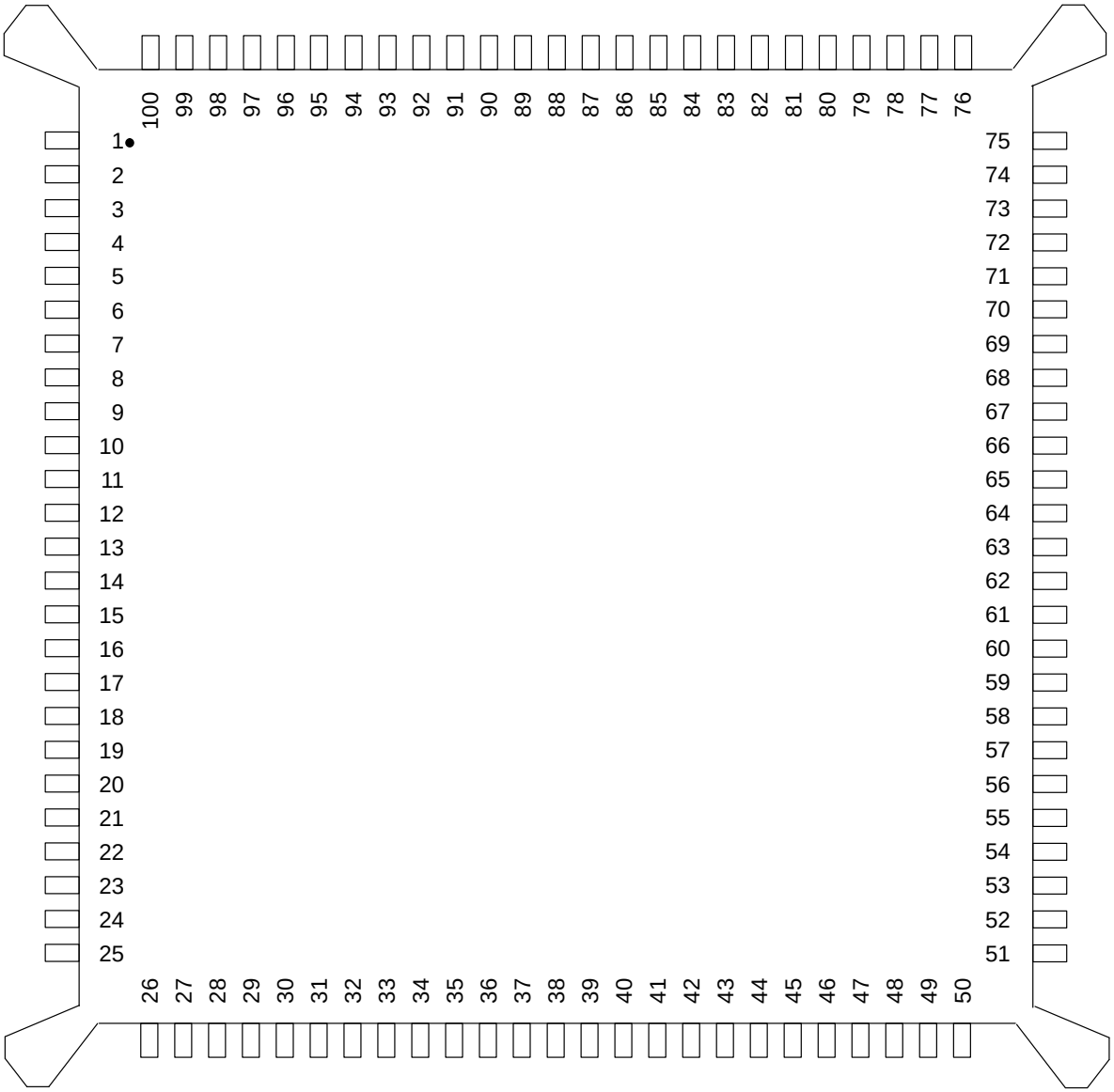
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	**43**	V_{CC}	**85**	GND	**127**	PIO12
2	GND	**44**	GND	**86**	V_{CC}	**128**	PIO11
3	MEMCLK	**45**	$\overline{DTR}$	**87**	A23	**129**	PIO10
4	INCLK	**46**	RXD	**88**	A22	**130**	PIO9
5	V_{CC}	**47**	UCLK	**89**	A21	**131**	PIO8
6	GND	**48**	V_{CC}	**90**	A20	**132**	PIO7
7	GND	**49**	GND	**91**	A19	**133**	V_{CC}
8	V_{CC}	**50**	$\overline{DSR}$	**92**	A18	**134**	GND
9	ID31	**51**	TXD	**93**	A17	**135**	PIO6
10	ID30	**52**	$\overline{ROMCS}$3	**94**	A16	**136**	PIO5
11	ID29	**53**	$\overline{ROMCS}$2	**95**	A15	**137**	PIO4
12	ID28	**54**	$\overline{ROMCS}$1	**96**	A14	**138**	PIO3
13	GND	**55**	$\overline{ROMCS}$0	**97**	A13	**139**	PIO2
14	ID27	**56**	$\overline{BURST}$	**98**	A12	**140**	PIO1
15	ID26	**57**	$\overline{RSWE}$	**99**	A11	**141**	PIO0
16	ID25	**58**	$\overline{ROMOE}$	**100**	A10	**142**	TDO
17	ID24	**59**	$\overline{RAS}$3	**101**	A9	**143**	STAT2
18	ID23	**60**	$\overline{RAS}$2	**102**	A8	**144**	STAT1
19	ID22	**61**	$\overline{RAS}$1	**103**	A7	**145**	STAT0
20	ID21	**62**	$\overline{RAS}$0	**104**	A6	**146**	VDAT
21	ID20	**63**	$\overline{CAS}$3	**105**	A5	**147**	PSYNC
22	ID19	**64**	$\overline{CAS}$2	**106**	A4	**148**	GND
23	V_{CC}	**65**	V_{CC}	**107**	A3	**149**	V_{CC}
24	ID18	**66**	GND	**108**	A2	**150**	$\overline{GREQ}$
25	ID17	**67**	$\overline{CAS}$1	**109**	A1	**151**	DREQ1
26	ID16	**68**	$\overline{CAS}$0	**110**	A0	**152**	DREQ0
27	ID15	**69**	$\overline{TR}/\overline{OE}$	**111**	V_{CC}	**153**	TDMA
28	ID14	**70**	$\overline{WE}$	**112**	GND	**154**	$\overline{TRAP}$0
29	ID13	**71**	$\overline{GACK}$	**113**	BOOTW	**155**	$\overline{TRAP}$1
30	ID12	**72**	$\overline{PIACS}$5	**114**	$\overline{WAIT}$	**156**	$\overline{INTR}$0
31	ID11	**73**	$\overline{PIACS}$4	**115**	PAUTOFD	**157**	$\overline{INTR}$1
32	ID10	**74**	$\overline{PIACS}$3	**116**	PSTROBE	**158**	$\overline{INTR}$2
33	ID9	**75**	$\overline{PIACS}$2	**117**	V_{CC}	**159**	$\overline{INTR}$3
34	ID8	**76**	$\overline{PIACS}$1	**118**	GND	**160**	$\overline{WARN}$
35	ID7	**77**	$\overline{PIACS}$0	**119**	$\overline{PWE}$	**161**	GND
36	ID6	**78**	$\overline{PIAWE}$	**120**	$\overline{POE}$	**162**	VCLK
37	ID5	**79**	$\overline{PIAOE}$	**121**	PACK	**163**	LSYNC
38	ID4	**80**	R/$\overline{W}$	**122**	$\overline{PBUSY}$	**164**	TMS
39	ID3	**81**	$\overline{DACK}$1	**123**	PIO15	**165**	$\overline{TRST}$
40	ID2	**82**	$\overline{DACK}$0	**124**	PIO14	**166**	TCK
41	ID1	**83**	GND	**125**	PIO13	**167**	TDI
42	ID0	**84**	V_{CC}	**126**	GND	**168**	$\overline{RESET}$

PQFP PIN DESIGNATIONS (Sorted by Pin Name)—Am29200 Microcontroller

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A0	110	GND	49	ID31	9	$\overline{\text{RAS2}}$	60
A1	109	GND	66	INCLK	4	$\overline{\text{RAS3}}$	59
A2	108	GND	83	$\overline{\text{INTR0}}$	156	$\overline{\text{RESET}}$	168
A3	107	GND	85	$\overline{\text{INTR1}}$	157	$\overline{\text{ROMCS0}}$	55
A4	106	GND	112	$\overline{\text{INTR2}}$	158	$\overline{\text{ROMCS1}}$	54
A5	105	GND	118	$\overline{\text{INTR3}}$	159	$\overline{\text{ROMCS2}}$	53
A6	104	GND	126	LSYNC	163	$\overline{\text{ROMCS3}}$	52
A7	103	GND	134	MEMCLK	3	$\overline{\text{ROMOE}}$	58
A8	102	GND	148	PACK	121	$\overline{\text{RSWE}}$	57
A9	101	GND	161	PAUTOFD	115	RXD	46
A10	100	$\overline{\text{GREQ}}$	150	$\overline{\text{PBUSY}}$	122	STAT0	145
A11	99	ID0	42	$\overline{\text{PIACS0}}$	77	STAT1	144
A12	98	ID1	41	$\overline{\text{PIACS1}}$	76	STAT2	143
A13	97	ID2	40	$\overline{\text{PIACS2}}$	75	TCK	166
A14	96	ID3	39	$\overline{\text{PIACS3}}$	74	TDI	167
A15	95	ID4	38	$\overline{\text{PIACS4}}$	73	TDMA	153
A16	94	ID5	37	$\overline{\text{PIACS5}}$	72	TDO	142
A17	93	ID6	36	$\overline{\text{PIAOE}}$	79	TMS	164
A18	92	ID7	35	$\overline{\text{PIAWE}}$	78	$\overline{\text{TR/OE}}$	69
A19	91	ID8	34	PIO0	141	$\overline{\text{TRAP0}}$	154
A20	90	ID9	33	PIO1	140	$\overline{\text{TRAP1}}$	155
A21	89	ID10	32	PIO2	139	$\overline{\text{TRST}}$	165
A22	88	ID11	31	PIO3	138	TXD	51
A23	87	ID12	30	PIO4	137	UCLK	47
BOOTW	113	ID13	29	PIO5	136	V_{CC}	1
$\overline{\text{BURST}}$	56	ID14	28	PIO6	135	V_{CC}	5
$\overline{\text{CAS0}}$	68	ID15	27	PIO7	132	V_{CC}	8
$\overline{\text{CAS1}}$	67	ID16	26	PIO8	131	V_{CC}	23
$\overline{\text{CAS2}}$	64	ID17	25	PIO9	130	V_{CC}	43
$\overline{\text{CAS3}}$	63	ID18	24	PIO10	129	V_{CC}	48
$\overline{\text{DACK0}}$	82	ID19	22	PIO11	128	V_{CC}	65
$\overline{\text{DACK1}}$	81	ID20	21	PIO12	127	V_{CC}	84
DREQ0	152	ID21	20	PIO13	125	V_{CC}	86
DREQ1	151	ID22	19	PIO14	124	V_{CC}	111
$\overline{\text{DSR}}$	50	ID23	18	PIO15	123	V_{CC}	117
$\overline{\text{DTR}}$	45	ID24	17	$\overline{\text{POE}}$	120	V_{CC}	133
$\overline{\text{GACK}}$	71	ID25	16	PSTROBE	116	V_{CC}	149
GND	2	ID26	15	PSYNC	147	VCLK	162
GND	6	ID27	14	$\overline{\text{PWE}}$	119	VDAT	146
GND	7	ID28	12	R/$\overline{\text{W}}$	80	$\overline{\text{WAIT}}$	114
GND	13	ID29	11	$\overline{\text{RAS0}}$	62	$\overline{\text{WARN}}$	160
GND	44	ID30	10	$\overline{\text{RAS1}}$	61	$\overline{\text{WE}}$	70

CONNECTION DIAGRAMS (continued)

100-Lead Plastic Quad Flat Pack (PQB 100)—Am29205 Microcontroller
Top View



Note:
Pin 1 is marked for orientation.

PQFP PIN DESIGNATIONS (Sorted by Pin Number)—Am29205 Microcontroller

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	$\overline{\text{WAIT}}/\overline{\text{TRIST}}$	**26**	RXD	**51**	A21	**76**	PAUTOFD
2	$\overline{\text{RESET}}$	**27**	UCLK	**52**	A20	**77**	PSTROBE
3	MEMCLK	**28**	TXD	**53**	A19	**78**	$\overline{\text{PWE}}$
4	INCLK	**29**	V_{CC}	**54**	A18	**79**	V_{CC}
5	V_{CC}	**30**	GND	**55**	A17	**80**	GND
6	GND	**31**	$\overline{\text{ROMCS}}2$	**56**	A16	**81**	$\overline{\text{POE}}$
7	GND	**32**	$\overline{\text{ROMCS}}1$	**57**	A15	**82**	PACK
8	ID31♦	**33**	$\overline{\text{ROMCS}}0$	**58**	A14	**83**	$\overline{\text{PBUSY}}$
9	ID30♦	**34**	$\overline{\text{RSWE}}$	**59**	A13	**84**	PIO15♦
10	ID29♦	**35**	$\overline{\text{ROMOE}}$	**60**	A12	**85**	PIO14♦
11	ID28♦	**36**	$\overline{\text{RAS}}3$	**61**	A11	**86**	PIO13♦
12	ID27♦	**37**	$\overline{\text{RAS}}2$	**62**	A10	**87**	PIO12♦
13	ID26♦	**38**	$\overline{\text{RAS}}1$	**63**	GND	**88**	PIO11♦
14	V_{CC}	**39**	$\overline{\text{RAS}}0$	**64**	V_{CC}	**89**	PIO10♦
15	GND	**40**	$\overline{\text{CAS}}3$♦	**65**	GND	**90**	PIO9♦
16	ID25♦	**41**	$\overline{\text{CAS}}2$♦	**66**	A9	**91**	PIO8♦
17	ID24♦	**42**	$\overline{\text{WE}}$	**67**	A8	**92**	VDAT
18	ID23♦	**43**	$\overline{\text{PIACS}}1$	**68**	A7	**93**	PSYNC
19	ID22♦	**44**	$\overline{\text{PIACS}}0$	**69**	A6	**94**	V_{CC}
20	ID21♦	**45**	$\overline{\text{PIAWE}}$	**70**	A5	**95**	GND
21	ID20♦	**46**	$\overline{\text{PIAOE}}$	**71**	A4	**96**	$\overline{\text{DREQ}}1$♦
22	ID19♦	**47**	GND	**72**	A3	**97**	$\overline{\text{INTR}}2$♦
23	ID18♦	**48**	V_{CC}	**73**	A2	**98**	$\overline{\text{INTR}}3$♦
24	ID17♦	**49**	R/$\overline{\text{W}}$	**74**	A1	**99**	VCLK
25	ID16♦	**50**	$\overline{\text{DACK}}1$♦	**75**	A0	**100**	LSYNC

Note:

♦ *The nomenclature of these pins is consistent with the functionally equivalent pins on the Am29200 microcontroller. This is done to simplify the ease of system design and to guarantee software compatibility between the Am29205 and Am29200 microcontrollers. ID31 is the most significant data bit and ID16 is the least significant.*

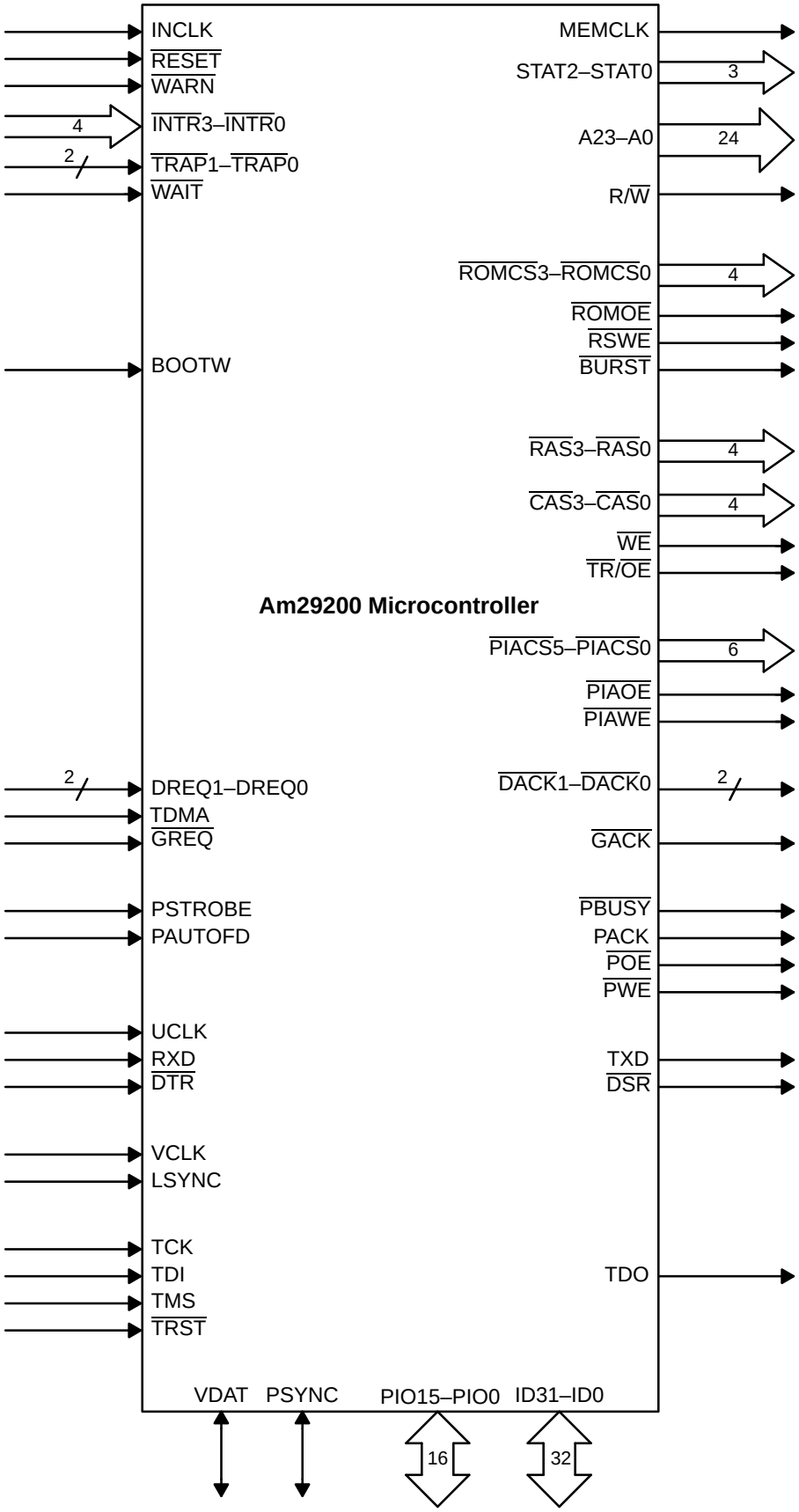
PQFP PIN DESIGNATIONS (Sorted by Pin Name)—Am29205 Microcontroller

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A0	75	**$\overline{\text{DREQ}}$1♦**	96	**$\overline{\text{PIACS}}$0**	44	**$\overline{\text{RSWE}}$**	34
A1	74	**ID16♦**	25	**$\overline{\text{PIACS}}$1**	43	**RXD**	26
A2	73	**ID17♦**	24	**$\overline{\text{PIAOE}}$**	46	**R/$\overline{\text{W}}$**	49
A3	72	**ID18♦**	23	**$\overline{\text{PIAWE}}$**	45	**TXD**	28
A4	71	**ID19♦**	22	**PIO8♦**	91	**UCLK**	27
A5	70	**ID20♦**	21	**PIO9♦**	90	**V_{CC}**	5
A6	69	**ID21♦**	20	**PIO10♦**	89	**V_{CC}**	29
A7	68	**ID22♦**	19	**PIO11♦**	88	**V_{CC}**	48
A8	67	**ID23♦**	18	**PIO12♦**	87	**V_{CC}**	79
A9	66	**ID24♦**	17	**PIO13♦**	86	**V_{CC}**	94
A10	62	**ID25♦**	16	**PIO14♦**	85	**V_{CC}**	64
A11	61	**ID26♦**	13	**PIO15♦**	84	**V_{CC}**	14
A12	60	**ID27♦**	12	**$\overline{\text{POE}}$**	81	**VCLK**	99
A13	59	**ID28♦**	11	**PSTROBE**	77	**VDAT**	92
A14	58	**ID29♦**	10	**PSYNC**	93	**GND**	7
A15	57	**ID30♦**	9	**$\overline{\text{PWE}}$**	78	**GND**	30
A16	56	**ID31♦**	8	**$\overline{\text{RAS}}$0**	39	**GND**	47
A17	55	**INCLK**	4	**$\overline{\text{RAS}}$1**	38	**GND**	63
A18	54	**$\overline{\text{INTR}}$2♦**	97	**$\overline{\text{RAS}}$2**	37	**GND**	80
A19	53	**$\overline{\text{INTR}}$3♦**	98	**$\overline{\text{RAS}}$3**	36	**GND**	95
A20	52	**LSYNC**	100	**$\overline{\text{RESET}}$**	2	**GND**	65
A21	51	**MEMCLK**	3	**$\overline{\text{ROMCS}}$0**	33	**GND**	15
$\overline{\text{CAS}}$2♦	41	**PACK**	82	**$\overline{\text{ROMCS}}$1**	32	**GND**	6
$\overline{\text{CAS}}$3♦	40	**PAUTOFD**	76	**$\overline{\text{ROMCS}}$2**	31	**$\overline{\text{WAIT}}$/$\overline{\text{TRIST}}$**	1
$\overline{\text{DACK}}$1♦	50	**$\overline{\text{PBUSY}}$**	83	**$\overline{\text{ROMOE}}$**	35	**$\overline{\text{WE}}$**	42

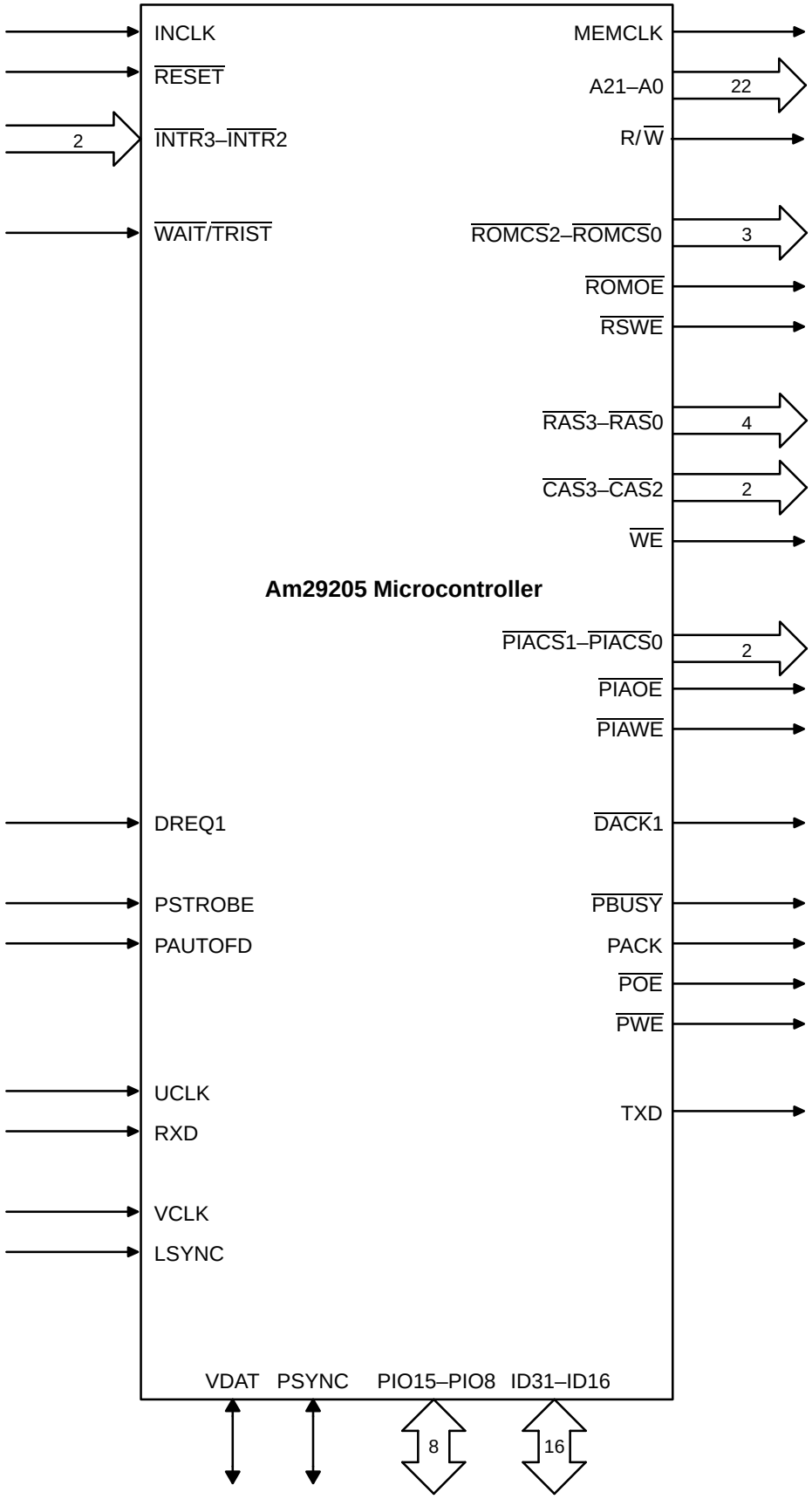
Note:

♦ The nomenclature of these pins is consistent with the functionally equivalent pins on the Am29200 microcontroller. This is done to simplify the ease of system design and to guarantee software compatibility between the Am29205 and Am29200 microcontrollers. ID31 is the most significant data bit and ID16 is the least significant.

Am29200 MICROCONTROLLER LOGIC SYMBOL



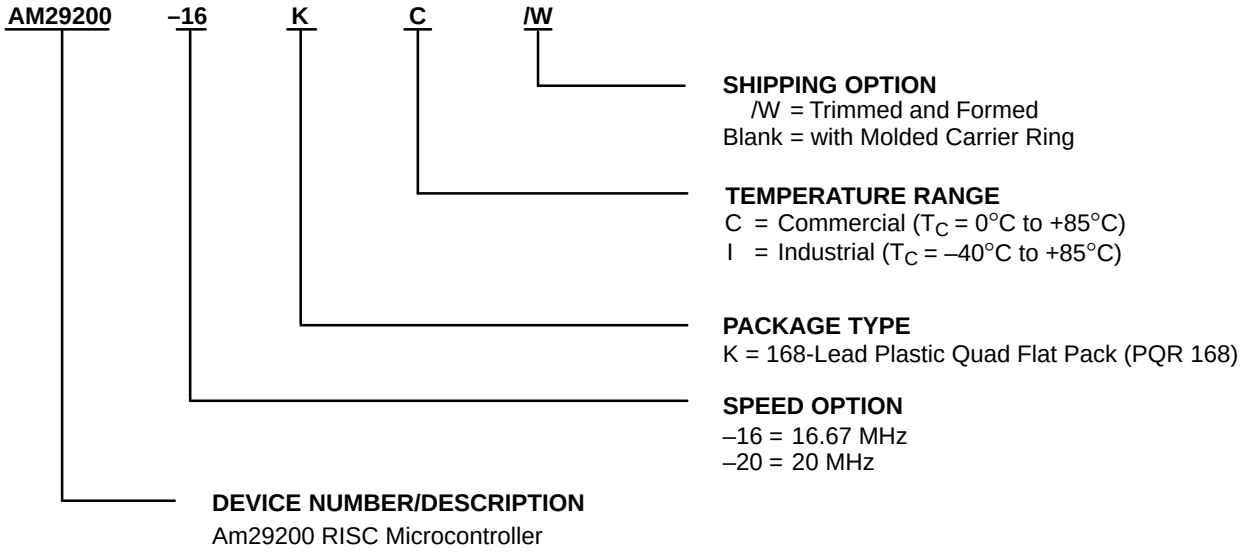
Am29205 MICROCONTROLLER LOGIC SYMBOL



ORDERING INFORMATION

Standard Products—Am29200 Microcontroller

AMD standard products are available in several packages and operating ranges. Valid order numbers are formed by a combination of the elements below.



Valid Combinations	
AM29200–16	KC, KI KC/W, KI/W
AM29200–20	

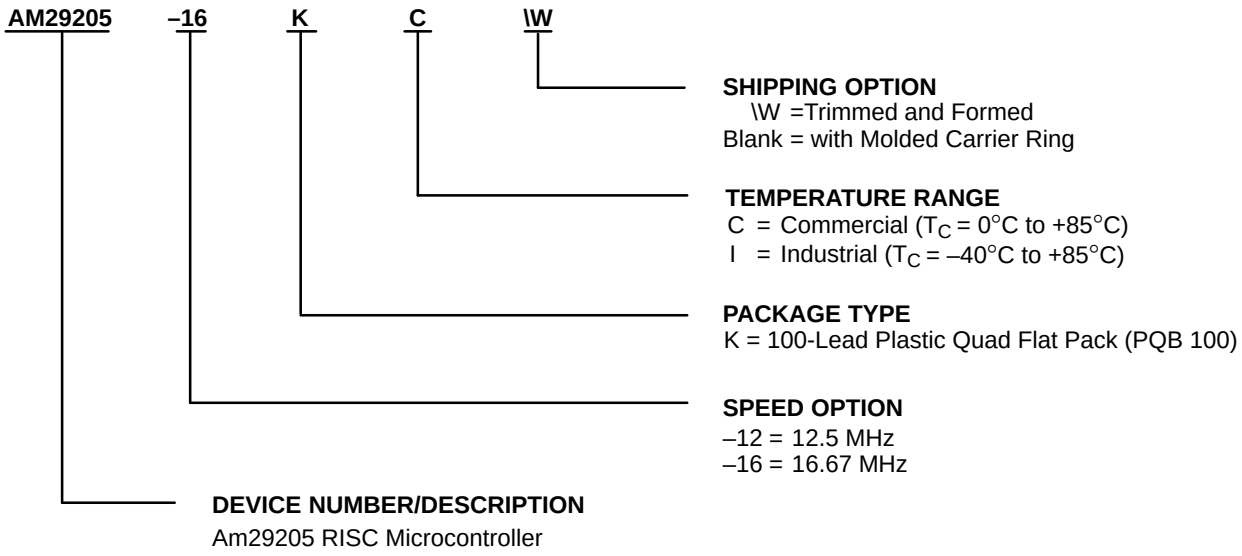
Valid Combinations

Valid Combinations list configurations planned to be supported in volume. Consult the local AMD sales office to confirm availability of specific valid combinations, and check on newly released combinations.

ORDERING INFORMATION

Standard Products—Am29205 Microcontroller

AMD standard products are available in several packages and operating ranges. Valid order numbers are formed by a combination of the elements below.



Valid Combinations	
AM29205–12	KC, KI, KC\W, KI\W
AM29205–16	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume. Consult the local AMD sales office to confirm availability of specific valid combinations, and check on newly released combinations.

ABSOLUTE MAXIMUM RATINGS
Am29200 and Am29205 Microcontrollers

Storage Temperature . . . . . –65°C to +125°C
Voltage on any Pin
with Respect to GND . . . . . –0.5 to V_{CC} +0.5 V
Maximum V_{CC} . . . . . 6.0 V DC

Stresses outside the stated ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device functionality.

OPERATING RANGES
Am29200 and Am29205 Microcontrollers

Commercial (C) and Industrial (I) Devices

Case Temperature (T_C) . . . . . 0°C to +85°C (C)
Case Temperature (T_C) . . . . . –40°C to +85°C (I)
Supply Voltage (V_{CC}) . . . . . +4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL Operating Ranges
Am29200 Microcontroller

Symbol	Parameter Description	Test Conditions	Notes	Preliminary		Unit
				Min	Max	
V_{IL}	Input Low Voltage		1	–0.5	0.8	V
V_{IH}	Input High Voltage		1	2.0	V_{CC} +0.5	V
$V_{ILINCLK}$	INCLK Input Low Voltage			–0.5	0.8	V
$V_{IHINCLK}$	INCLK Input High Voltage			2.4	V_{CC} +0.5	V
V_{OL}	Output Low Voltage for All Outputs except MEMCLK	I_{OL} = 3.2 mA			0.45	V
V_{OH}	Output High Voltage for All Outputs except MEMCLK	I_{OH} = –400 µA		2.4		V
I_{LI}	Input Leakage Current	0.45 V ≤ V_{IN} ≤ V_{CC} –0.45 V	2		±10 or +10/–200	µA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC} –0.45 V			±10	µA
I_{CCOP}	Operating Power Supply Current	V_{CC} = 5.25 V, Outputs Floating; Holding $\overline{RESET}$ active	3 4		234 280	mA mA
V_{OLC}	MEMCLK Output Low Voltage	I_{OLC} = 20 mA			0.6	V
V_{OHC}	MEMCLK Output High Voltage	I_{OHC} = –20 mA		V_{CC} –0.6		V

Notes:
1. *All inputs except* INCLK.
2. *The Low input leakage current is –200* µA *for the following inputs:* TCK, TDI, TMS, $\overline{TRST}$, DREQ1–DREQ0, $\overline{WAIT}$, $\overline{WARN}$, $\overline{INTR3}$–$\overline{INTR0}$, $\overline{TRAP1}$–$\overline{TRAP0}$, *and* $\overline{GREQ}$. *These pins have weak internal pull-up transistors.*
3. I_{CC} *measured at 16.7 MHz,* V_{cc}*=5.25 V, Reset Condition.*
4. I_{CC} *measured at 20.0 MHz,* V_{cc}*=5.25 V, Reset Condition.*

CAPACITANCE—Am29200 Microcontroller

Symbol	Parameter Description	Test Conditions	Preliminary		Unit
			Min	Max	
C_{IN}	Input Capacitance	fC = 10 MHz		15	pF
C_{INCLK}	INCLK Input Capacitance			15	pF
C_{MEMCLK}	MEMCLK Capacitance			20	pF
C_{OUT}	Output Capacitance			20	pF
$C_{I/O}$	I/O Pin Capacitance			20	pF

Note:
Limits guaranteed by characterization.

SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL Operating Ranges Am29200 Microcontroller

No.	Parameter Description	Test Conditions (Note 1)	Preliminary				Unit
			20 MHz		16 MHz		
			Min	Max	Min	Max	
1	INCLK Period (=0.5T)	Note 2, 9	25	62.5	30	62.5	ns
2	INCLK High Time	Note 2	9	53.5	9	53.5	ns
3	INCLK Low Time	Note 2	9	53.5	9	53.5	ns
4	INCLK Rise Time	Note 2		4		4	ns
5	INCLK Fall Time	Note 2		4		4	ns
6	MEMCLK Delay from INCLK		0	10	0	10	ns
7	Synchronous Output Valid Delay from MEMCLK Rising Edge	Note 3a	1	11	1	11	ns
7a	Synchronous Output Valid Delay from MEMCLK Rising Edge	Note 3a	1	12	1	12	ns
7b	Synchronous Output Valid Delay from MEMCLK Falling Edge	Note 3b	1	10	1	10	ns
8	Synchronous Output Disable Delay from MEMCLK Rising Edge	Note 8	1	10	1	10	ns
9	Synchronous Input Setup Time		10		10		ns
10	Synchronous Input Hold Time		0		0		ns
11	Asynchronous Pulse Width	Note 4a, 9	4T		4T		ns
11a	Asynchronous Pulse Width	Note 4b	Note 4b		Note 4b		ns
12	MEMCLK High Time	Note 5	0.5T–3	0.5T+3	0.5T–3	0.5T+3	ns
13	MEMCLK Low Time	Note 5	0.5T–3	0.5T+3	0.5T–3	0.5T+3	ns
14	MEMCLK Rise Time	Note 5	0	4	0	4	ns
15	MEMCLK Fall Time	Note 5	0	4	0	4	ns
16	UCLK, VCLK Period	Note 2	25		30		ns
17	UCLK, VCLK High Time	Note 2, 8	9		9		ns
18	UCLK, VCLK Low Time	Note 2, 8	9		9		ns
19	UCLK, VCLK Rise Time	Note 2		4		4	ns
20	UCLK, VCLK Fall Time	Note 2		4		4	ns
21	Synchronous Output Valid Delay from VCLK Edge	Note 6	1	15	1	15	ns
22	Input Setup Time to VCLK Edge	Note 6, 7	10		10		ns
23	Input Hold Time to VCLK Edge	Note 6, 7	0		0		ns
24	TCK Frequency			2		2	MHz

Notes:

1. *All outputs driving 80 pF, measured at V_{OL}=1.5 V and V_{OH}=1.5 V.*
2. *INCLK, VCLK, and UCLK can be driven with TTL inputs. If not used, UCLK must be tied High.*
3. a. *Parameter 7a applies only to the outputs PIO15–PIO0, STAT2–STAT0, and* $\overline{\text{DACK}}$1–$\overline{\text{DACK}}$0*. Parameter 7 applies to the remaining outputs.*
   b. *Parameter 7b applies only to the outputs* $\overline{\text{RAS}}$x, $\overline{\text{CAS}}$x, *A2–A0,* $\overline{\text{RSWE}}$, $\overline{\text{TR}}$/$\overline{\text{OE}}$, *and* $\overline{\text{ROMOE}}$*. Some of these signals can also be asserted during the rising edge of MEMCLK, depending on the type of access being performed.*
4. a. *Parameter 11 applies to all asynchronous inputs except LSYNC and PSYNC.*
   b. *The LSYNC and PSYNC minimum width time is two bit-times. One bit-time corresponds to one internal video clock period. The internal video clock period is a function of the VCLK period and the programmed VCLK divisor.*
5. *MEMCLK can drive an external load of 100 pF.*

Notes: (continued)

6. *Active VCLK edge depends on the CLKI bit in the Video Control Register.*
7. *LSYNC and PSYNC may be treated as synchronous signals by meeting setup and hold times. The synchrononization delay still applies.*
8. *Not production tested but guaranteed by design or characterization.*
9. *T=1 MEMCLK period, as defined by the actual frequency on the MEMCLK pin.*

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL Operating Ranges Am29205 Microcontroller

Symbol	Parameter Description	Test Conditions	Notes	Preliminary		Unit
				Min	Max	
V_{IL}	Input Low Voltage		1	–0.5	0.8	V
V_{IH}	Input High Voltage		1	2.0	V_{CC} +0.5	V
$V_{ILINCLK}$	INCLK Input Low Voltage			–0.5	0.8	V
$V_{IHINCLK}$	INCLK Input High Voltage			2.4	V_{CC} +0.5	V
V_{OL}	Output Low Voltage for All Outputs except MEMCLK	I_{OL} = 3.2 mA			0.45	V
V_{OH}	Output High Voltage for All Outputs except MEMCLK	I_{OH} = –400 µA		2.4		V
I_{LI}	Input Leakage Current	0.45 V ≤ V_{IN} ≤ V_{CC} –0.45 V	2		±10 or +10/–200	µA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC} –0.45 V			±10	µA
I_{CCOP}	Operating Power Supply Current with respect to MEMCLK	V_{CC} = 5.25 V, Outputs Floating; Holding $\overline{\text{RESET}}$ active	3 4		234 175	mA mA
V_{OLC}	MEMCLK Output Low Voltage	I_{OLC} = 20 mA			0.6	V
V_{OHC}	MEMCLK Output High Voltage	I_{OHC} = –20 mA		V_{CC} –0.6		V

Notes:

1. *All inputs except INCLK.*
2. *The Low input leakage current is –200* µA *for the following inputs:* $\overline{\text{INTR}}$3, $\overline{\text{INTR}}$2*, DREQ1, and* $\overline{\text{WAIT}}$/$\overline{\text{TRIST}}$*. These pins have weak internal pull-up transistors.*
3. *I_{CC} measured at 16.7 MHz, V_{cc}=5.25 V, Reset Condition.*
4. *I_{CC} measured at 12.5 MHz, V_{cc}=5.25 V, Reset Condition.*

CAPACITANCE—Am29205 Microcontroller

Symbol	Parameter Description	Test Conditions	Preliminary		Unit
			Min	Max	
C_{IN}	Input Capacitance	fC = 10 MHz		15	pF
C_{INCLK}	INCLK Input Capacitance			15	pF
C_{MEMCLK}	MEMCLK Capacitance			20	pF
C_{OUT}	Output Capacitance			20	pF
$C_{I/O}$	I/O Pin Capacitance			20	pF

Note:

Limits guaranteed by characterization.

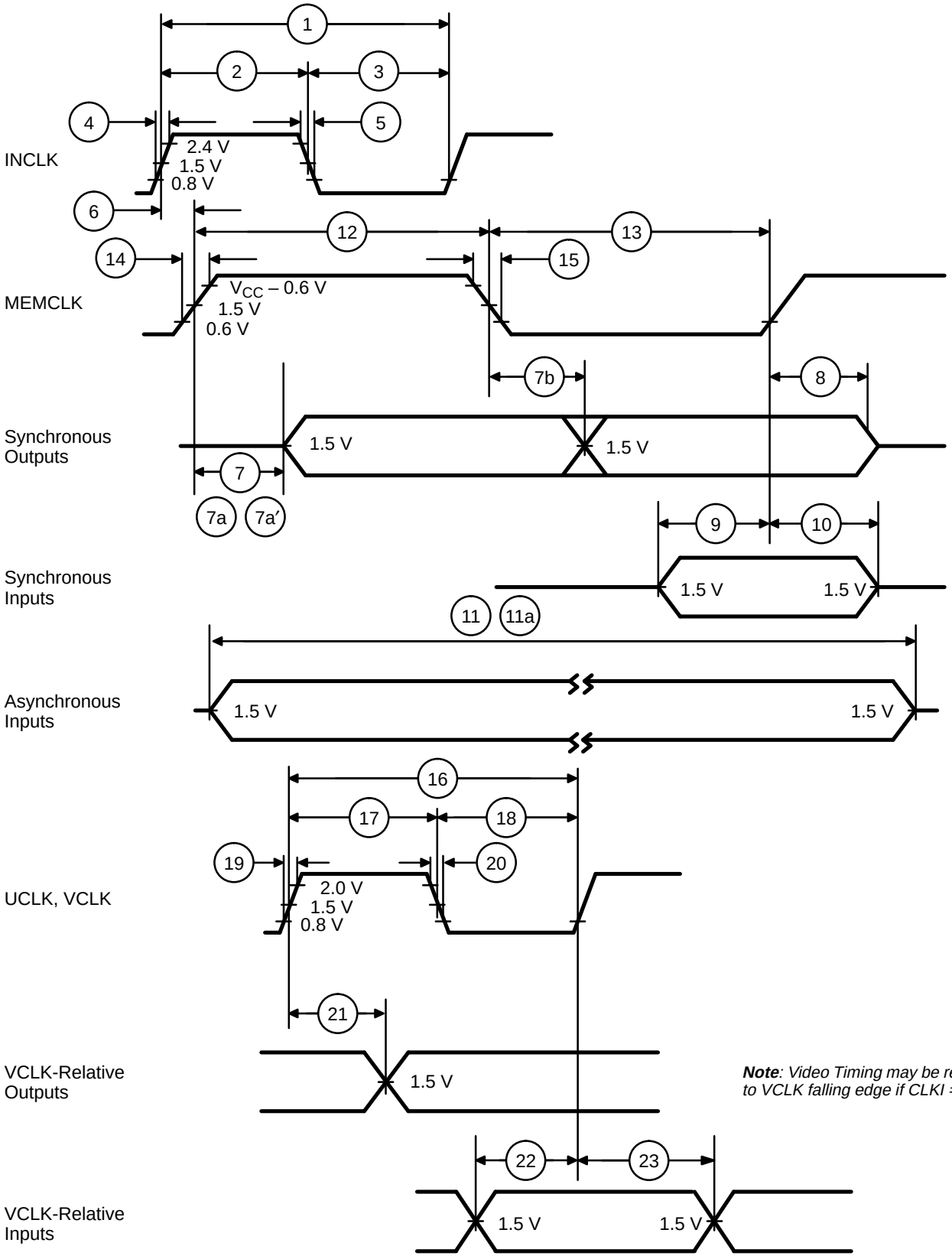
SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL Operating Ranges Am29205 Microcontroller

No.	Parameter Description	Test Conditions[1]	Preliminary				Unit
			16 MHz		12 MHz		
			Min	Max	Min	Max	
1	INCLK Period (= 0.5T)	Note 2, 9	30	62.5	40	62.5	ns
2	INCLK High Time	Note 2	9	53.5	12	53.5	ns
3	INCLK Low Time	Note 2	9	53.5	12	53.5	ns
4	INCLK Rise Time	Note 2		4		4	ns
5	INCLK Fall Time	Note 2		4		4	ns
6	MEMCLK Delay from INCLK		0	10	0	10	ns
7	Synchronous Output Valid Delay from MEMCLK Rising Edge	Note 3a	1	11	1	15	ns
7a	Synchronous Output Valid Delay from MEMCLK Rising Edge	Note 3b	1	12	1	15	ns
7a′	Synchronous Output Valid Delay from MEMCLK Rising Edge	Note 3c	1	12	1	15	ns
7b	Synchronous Output Valid Delay from MEMCLK Falling Edge	Note 3d	1	10	1	15	ns
8	Synchronous Output Disable Delay from MEMCLK Rising Edge	Note 8	1	10	1	15	ns
9	Synchronous Input Setup Time		8		12		ns
10	Synchronous Input Hold Time		0		0		ns
11	Asynchronous Pulse Width	Note 4a, 9	4T		4T		ns
11a	Asynchronous Pulse Width	Note 4b	Note 4b		Note 4b		
12	MEMCLK High Time	Note 5	0.5T –3	0.5T +3	0.5T –3	0.5T +3	ns
13	MEMCLK Low Time	Note 5	0.5T –3	0.5T +3	0.5T –3	0.5T +3	ns
14	MEMCLK Rise Time	Note 5	0	4	0	5	ns
15	MEMCLK Fall Time	Note 5	0	4	0	5	ns
16	UCLK, VCLK Period	Note 2, 8	30		40		ns
17	UCLK, VCLK High Time	Note 2, 8	9		12		ns
18	UCLK, VCLK Low Time	Note 2	9		12		ns
19	UCLK, VCLK Rise time	Note 2		4		4	ns
20	UCLK, VCLK Fall Time	Note 2		4		4	ns
21	Synchronous Output Valid Delay from VCLK Edge	Note 6	1	15	1	20	ns
22	Input Setup Time to VCLK Edge	Notes 6, 7	10		15		ns
23	Input Hold Time to VCLK Edge	Notes 6, 7	0		0		ns

Notes:

1. *All outputs driving 80 pF, measured at V_{OL} = 1.5 V and V_{OH} = 1.5 V.*
2. *INCLK, VCLK, and UCLK can be driven with TTL inputs. If not used, UCLK must be tied High.*
3. a. *Parameter 7 applies to all outputs except PIO15–PIO8,* $\overline{\text{PIACS1}}$– $\overline{\text{PIACS0}}$, $\overline{\text{DACK1}}$, *and A21–A0.*
   b. *Parameter 7a applies to PIO15–PIO8,* $\overline{\text{PIACS1}}$– $\overline{\text{PIACS0}}$, *and* $\overline{\text{DACK1}}$.
   c. *Parameter 7a′ applies to A21–A0.*
   d. *Parameter 7b applies only to the outputs* $\overline{\text{RAS}}$x, $\overline{\text{CAS}}$x, *A2–A0,* $\overline{\text{RSWE}}$, *and* $\overline{\text{ROMOE}}$. *Some of these signals can also be asserted during the rising edge of MEMCLK, depending on the type of access being performed.*
4. a. *Parameter 11 applies to all asynchronous inputs except LSYNC and PSYNC.*
   b. *LSYNC and PSYNC minimum width is two bit-times. A bit-time corresponds to one internal video clock period. The internal video clock period is a function of the VCLK period and the programmed VCLK divisor.*
5. *MEMCLK can drive an external load of 100 pF.*
6. *Active VCLK edge depends on CLKI bit in Video Control Register.*
7. *LSYNC and PSYNC may be treated as synchronous signals by meeting setup and hold times. The synchronization delay still applies.*
8. *Not production tested but guaranteed by design or characterization.*
9. *T=1 MEMCLK period, as defined by the actual frequency on the MEMCLK pin.*

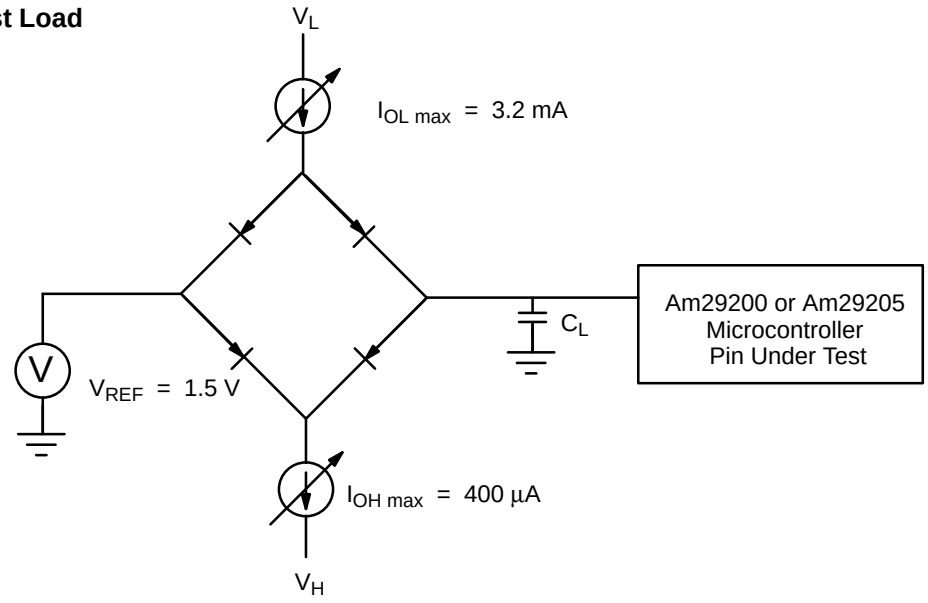
SWITCHING WAVEFORMS—Am29200 and Am29205 Microcontrollers



***Note**: Video Timing may be relative to VCLK falling edge if CLKI = 1.*

SWITCHING TEST CIRCUIT—Am29200 and Am29205 Microcontrollers

Model of Dynamic Test Load

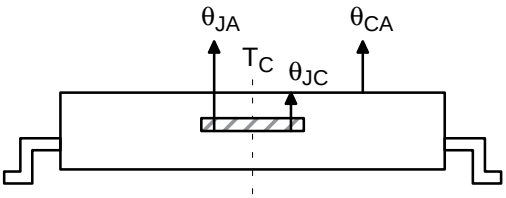


Note:
C_L is guaranteed to be a minimum 80-pF parasitic load. It represents the distributed load parasitic attributed to the test hardware and instrumentation present during production testing.

THERMAL CHARACTERISTICS—Am29200 and Am29205 Microcontrollers

PQFP Package

The Am29200 and Am29205 microcontrollers are specified for operation with case temperature ranges for a commercial or industrial temperature device. Case temperature is measured at the top center of the package as shown in the figure below.



$\theta_{JA} = \theta_{JC} + \theta_{CA}$

Thermal Resistance — °C/Watt

The various temperatures and thermal resistances can be determined using the following equations along with information given in Table 2.

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$
$$P = I_{CCOP} \cdot V_{CC}$$

$$T_J = T_C + P \cdot \theta_{JC}$$
$$T_J = T_A + P \cdot \theta_{JA}$$

$$T_C = T_J - P \cdot \theta_{JC}$$
$$T_C = T_A + P \cdot \theta_{CA}$$

$$T_A = T_J - P \cdot \theta_{JA}$$
$$T_A = T_C - P \cdot \theta_{CA}$$

Allowable ambient temperature curves for various airflows are given in Figures 1–3. These graphs assume a maximum V_{CC} and a maximum power supply current equal to I_{CCOP}. All calculations made using the above information should guarantee that the operating case temperature does not exceed the maximum case temperature. Since P is a function of operating frequency, calculations can also be made to determine the ambient temperature at various operating speeds.

Table 2. PQFP Thermal Characteristics (°C/Watt) Surface Mounted

		Airflow—ft./min. (m/sec)				
Am29200 Microcontroller		**0 (0)**	**200 (1.01)**	**400 (2.03)**	**600 (3.04)**	**800 (4.06)**
θ_{JA}	Junction-to-Ambient	36	32	29	27	—
θ_{JC}	Junction-to-Case	8	8	8	8	—
θ_{CA}	Case-to-Ambient	28	24	21	19	—
Am29205 Microcontroller						
θ_{JA}	Junction-to-Ambient	41	35	30	27	25
θ_{JC}	Junction-to-Case	8	8	8	8	8
θ_{CA}	Case-to-Ambient	33	27	22	19	17

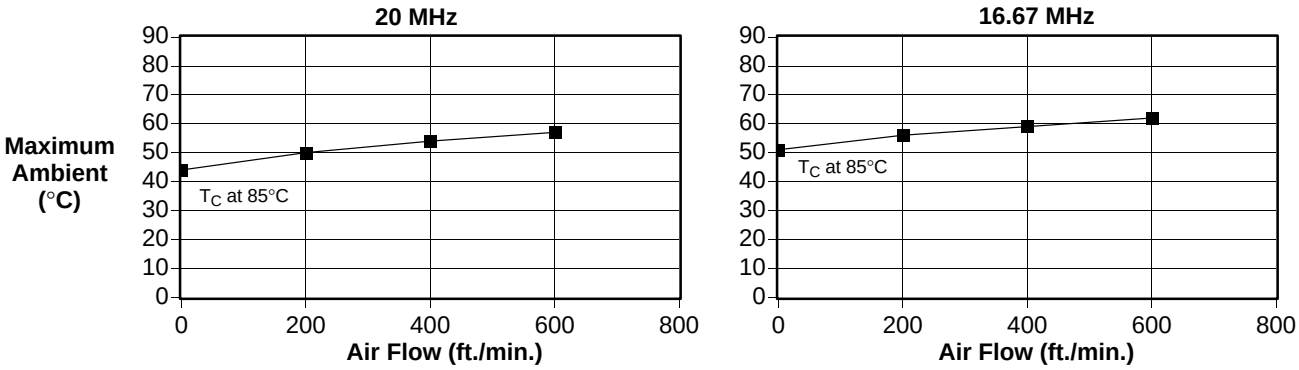


Figure 1. Am29200 Microcontroller—Maximum Allowable Ambient Temperature

(Data Sheet Limit, $I_{CCOPmax}$, V_{CC}=+5.25 V, Average Thermal Impedance)

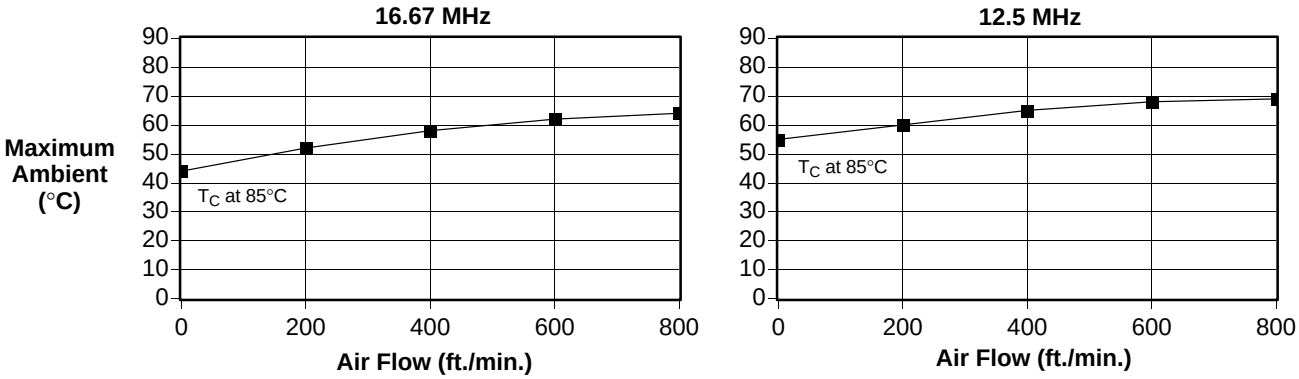


Figure 2. Am29205 Microcontroller—Maximum Allowable Ambient Temperature

(Data Sheet Limit, $I_{CCOPmax}$, V_{CC}=+5.25 V, Average Thermal Impedance)

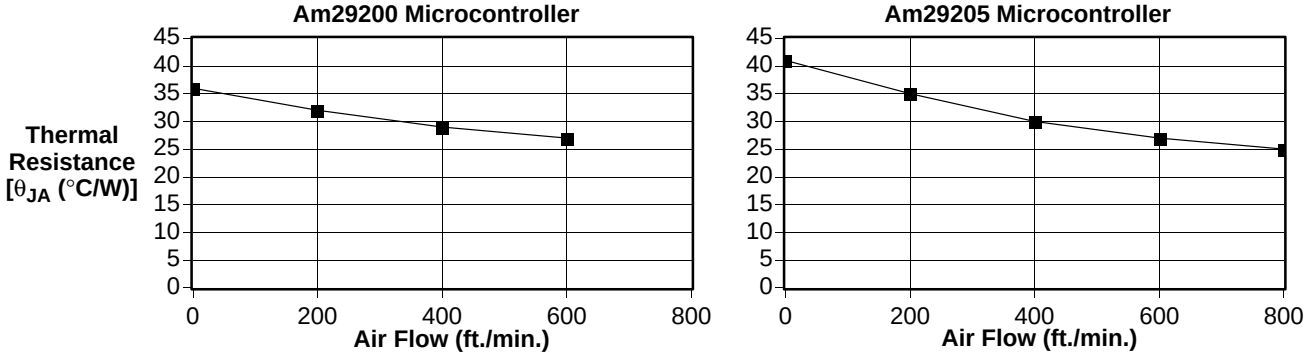
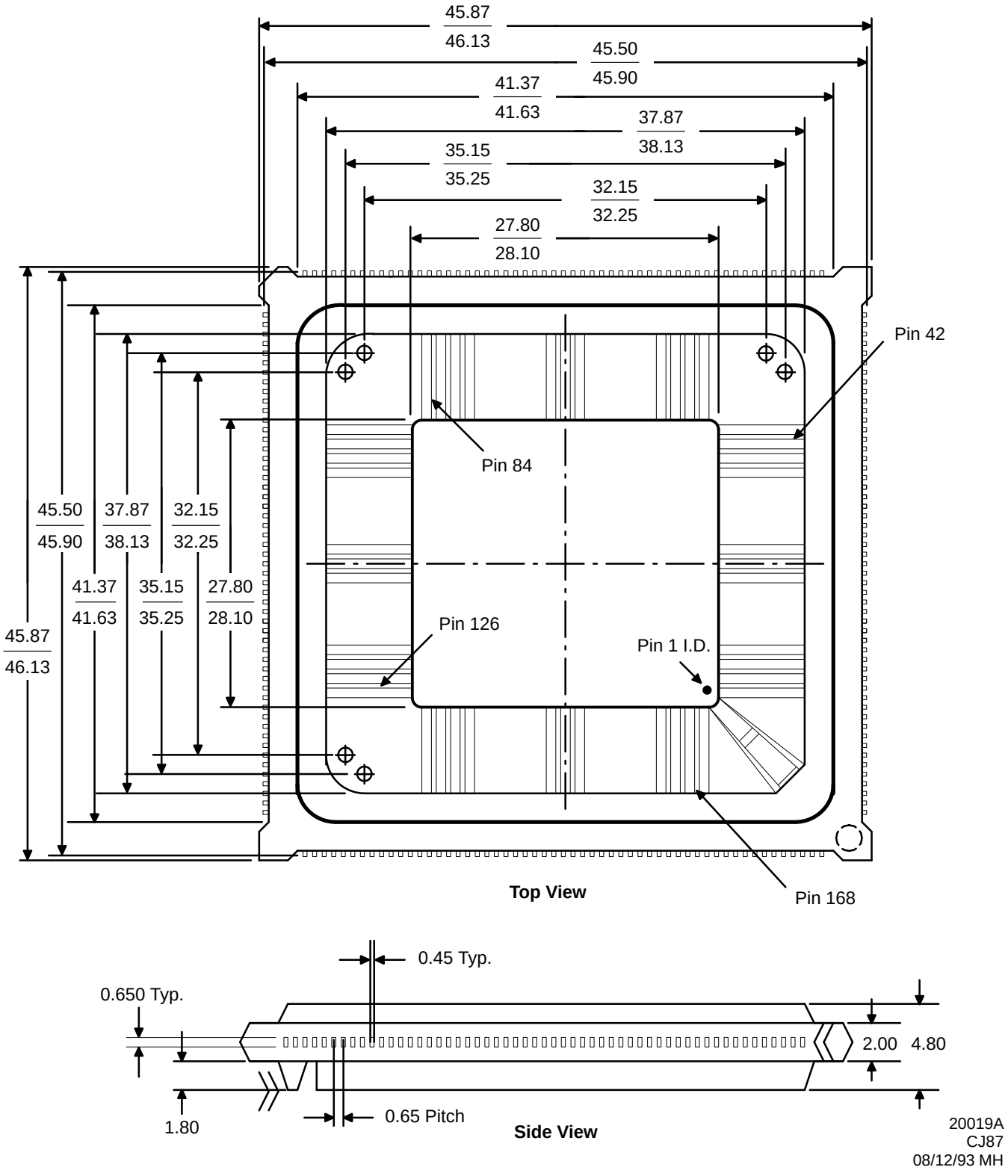


Figure 3. Thermal Impedance

PHYSICAL DIMENSIONS

PQR 168—Am29200 Microcontroller
Plastic Quad Flat Pack; Molded Carrier Ring

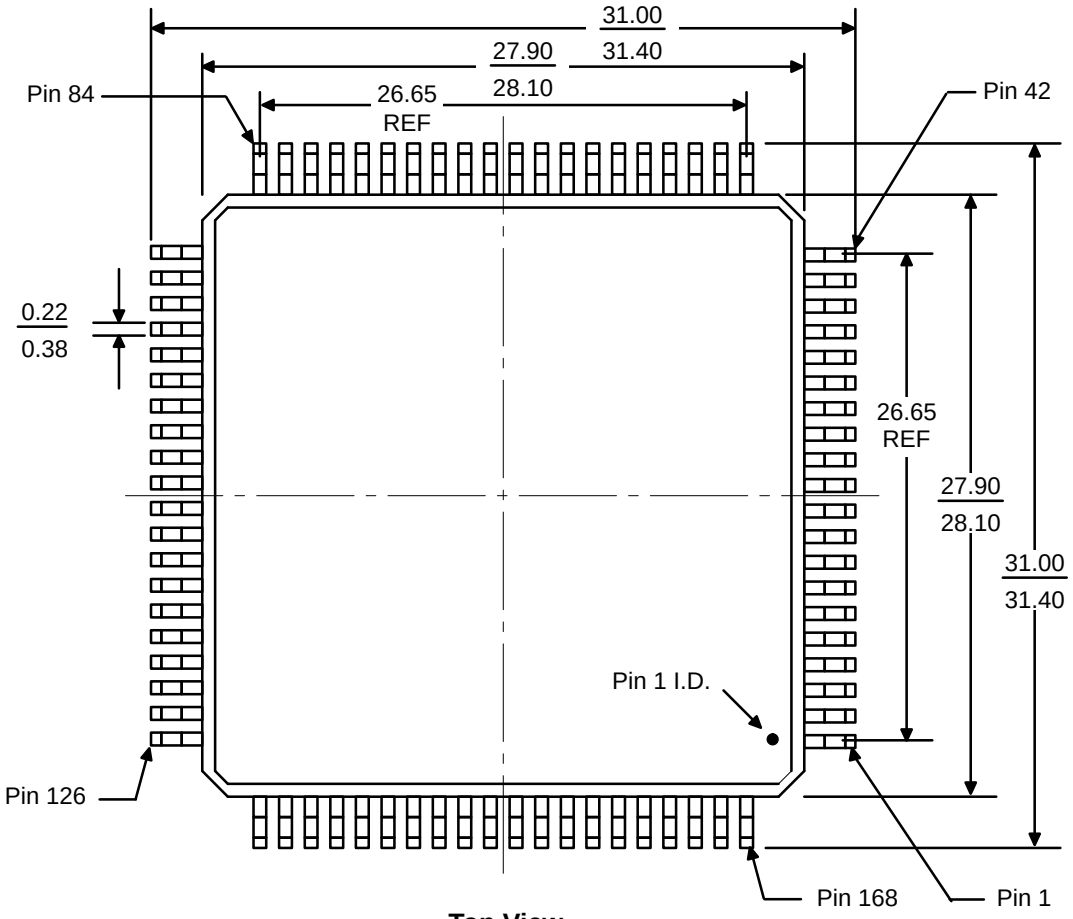
(Inner device measured in inches; outer ring measured in millimeters)



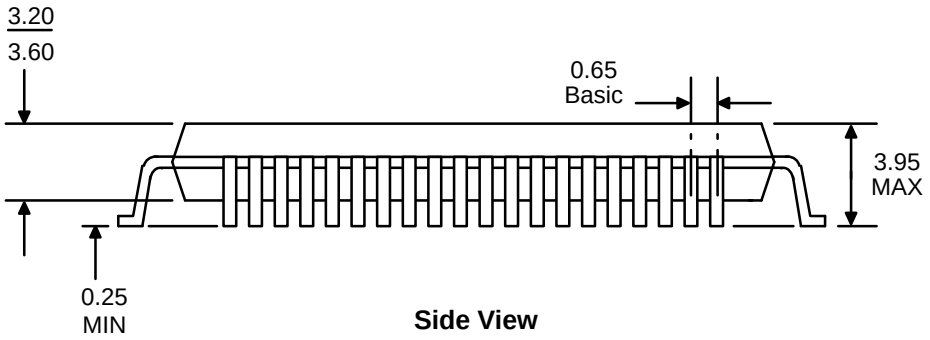
Note:
Not to scale. For reference only.

PQR 168—Am29200 Microcontroller
Plastic Quad Flat Pack; Trimmed and Formed

(All measurements are in millimeters)



Top View



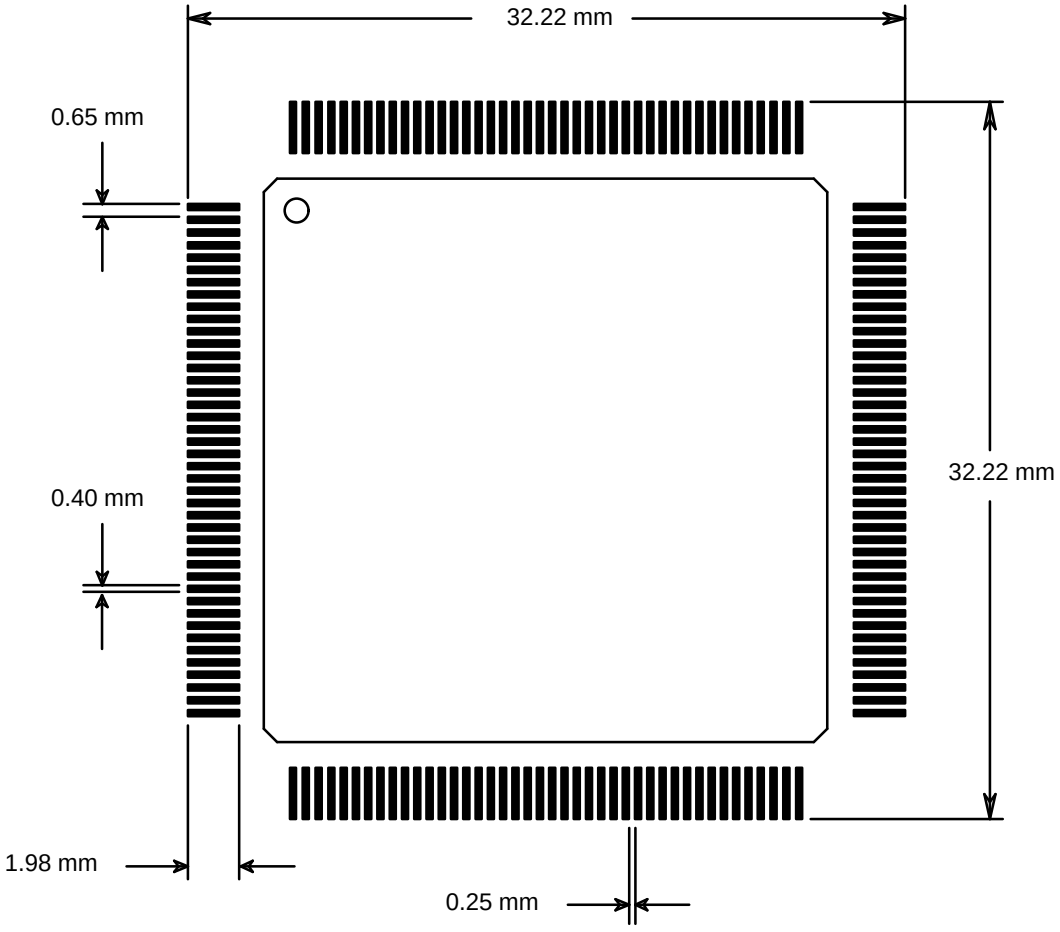
Side View

20028A
CL90
10/27/93 PM

Note:
Not to scale. For reference only.

Solder Land Recommendations
168-Lead PQFP—Am29200 Microcontroller

Top View

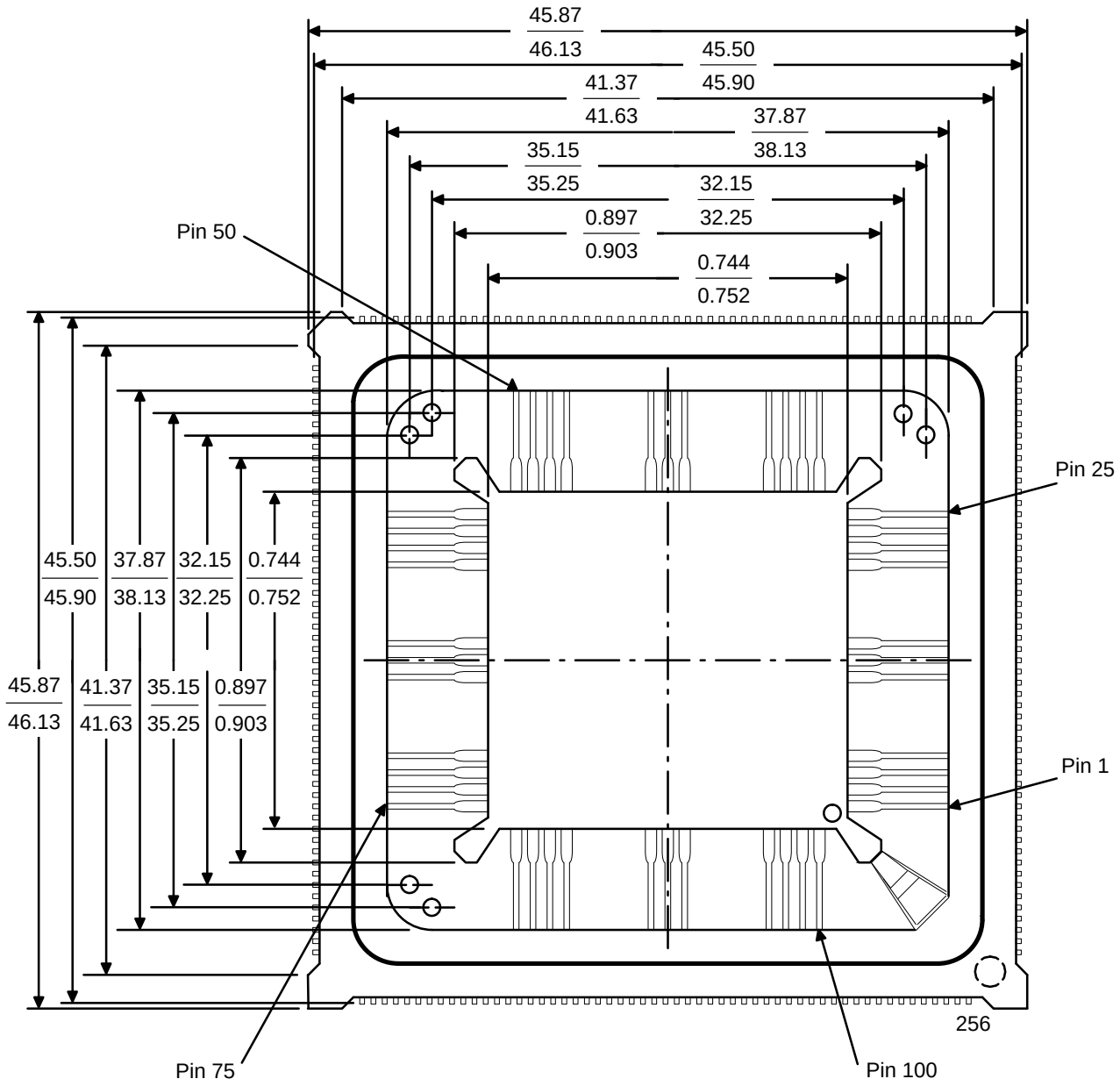


08/13/93 MH

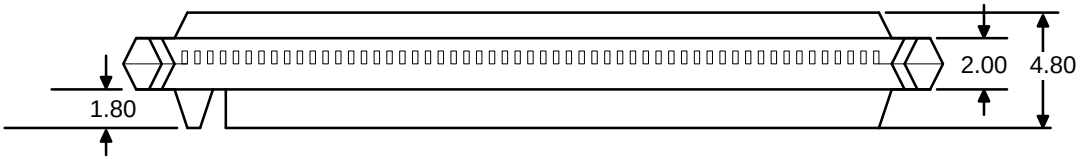
Note:
Not to scale. For reference only.

PQB 100—Am29205 Microcontroller
English Plastic Quad Flat Pack; Molded Carrier Ring

(Outer ring measured in millimeters)



Top View



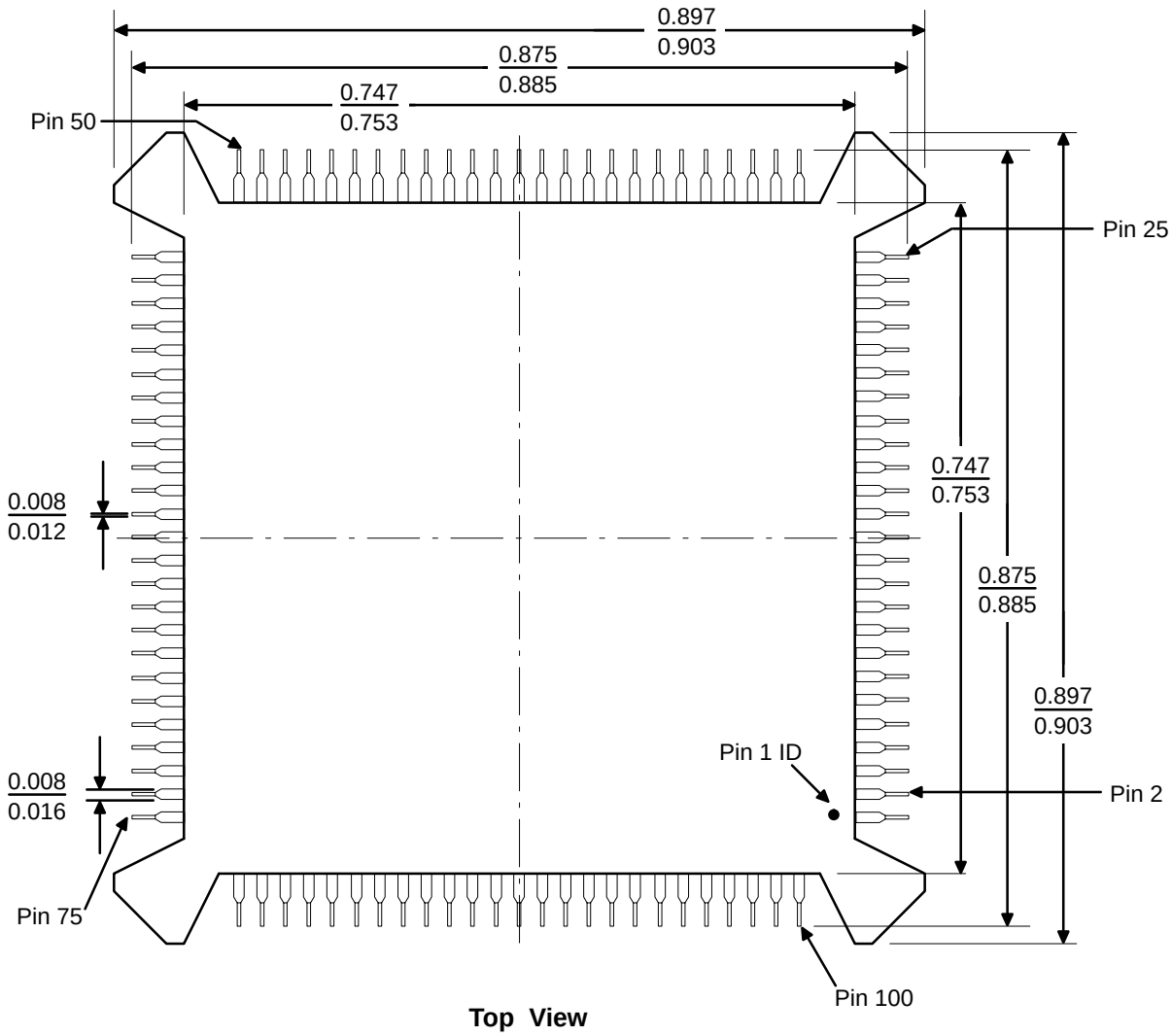
Side View

20009A
CJ83
12/13/93 PLM

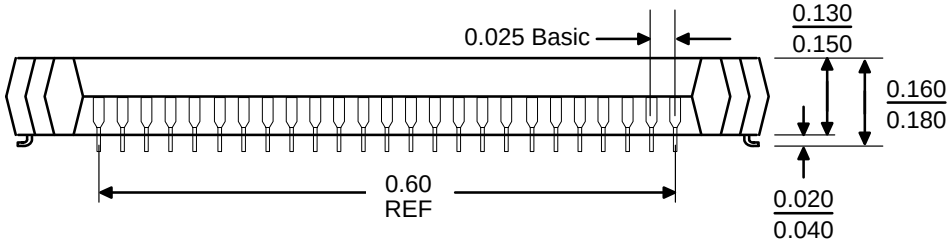
Note:
Not to scale. For reference only.

PQB 100—Am29205 Microcontroller
English Plastic Quad Flat Pack; Trimmed and Formed

(All measurements are in inches)



Top View



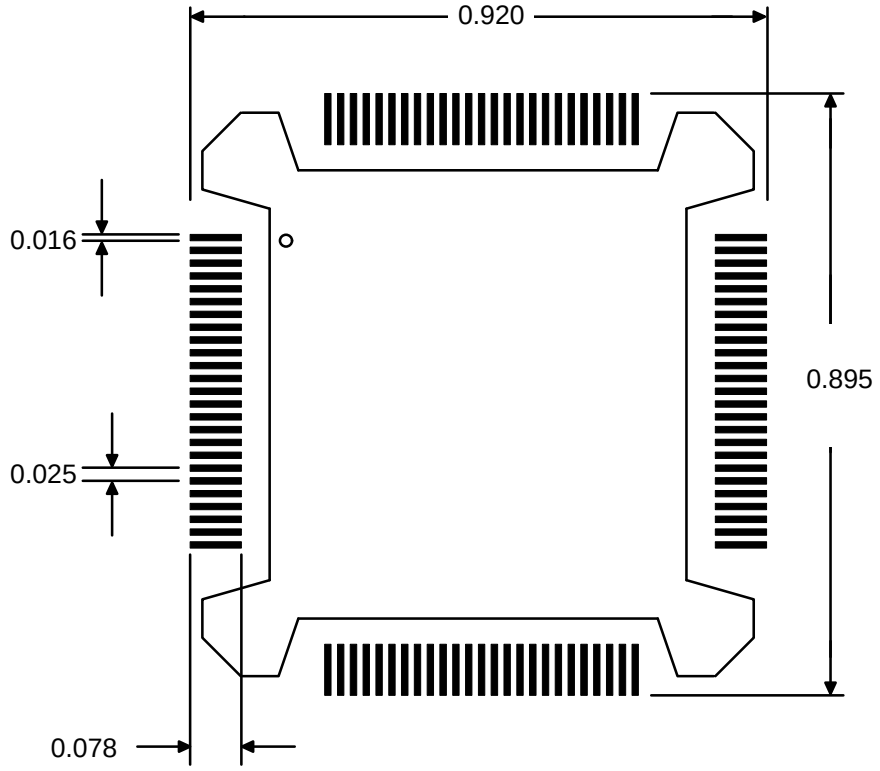
Side View

20010A
CL85
10/27/93 PM

Note:
Not to scale. For reference only.

Solder Land Recommendations
100-Lead PQFP—Am29205 Microcontroller

(All measurements are in inches)



Top View

10/27/93 PM

Note:
Not to scale. For reference only.