SIEMENS

ICs for Communication

ISDN Burst Transceiver Circuit
IBC
PEB 2095

Data Sheet

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IBC
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User´s Manual 06.92

PEB 2095 Revision History:	Original Version 06.92
Previous Releases:	
Page	Subjects (changes since last revision)

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about **"Processing Guidelines"** and **"Quality Assurance"** for ICs, see our **"Product Overview"**.

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Contents Page

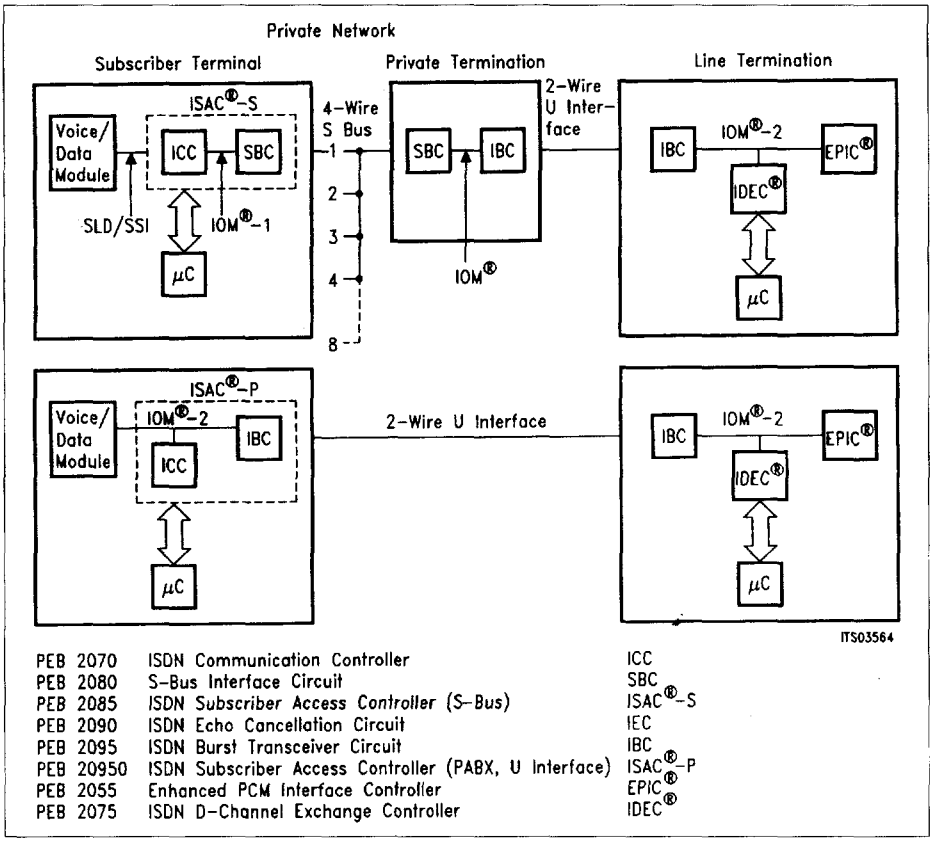
IBC Device Overview

The PEB 2095 ISDN burst transceiver circuit (IBC) is a full duplex transceiver for the 2-wire transmission line (CCITT U-reference point). Full duplex transmission is achieved using a time compression multiplex (ping-pong) technique. Furthermore the device links the 2-wire transmission line to the ISDN Oriented Modular (IOM®) interface and hence to the powerful Siemens ISDN device family. From the point of view of the OSI communications protocol model, the device manages layer-1 of the interface protocol and can communicate with other layer-1 or layer-2 devices over the IOM-interface. **Figure 1** illustrates the possible applications of the IBC within IOM-architecture.

As an alternative a second device, PEB 2090 ISDN Echo Cancellation Circuit (IEC), may also be used at the U-reference point. The device chosen depends on the application. The IBC proves more cost-effective for shorter range transmission applications (2 - 3.0 km), especially PABX.

It is available as a 24 pin CMOS device.

The device operates from a single 5 V power supply. The maximum power consumption is 100 mW.



PEB 2070	ISDN Communication Controller	ICC
PEB 2080	S-Bus Interface Circuit	SBC
PEB 2085	ISDN Subscriber Access Controller (S-Bus)	ISAC®-S
PEB 2090	ISDN Echo Cancellation Circuit	IEC
PEB 2095	ISDN Burst Transceiver Circuit	IBC
PEB 20950	ISDN Subscriber Access Controller (PABX, U Interface)	ISAC®-P
PEB 2055	Enhanced PCM Interface Controller	EPIC®
PEB 2075	ISDN D-Channel Exchange Controller	IDEC®

Figure 1
ISDN Oriented Modular (IOM®) Architecture

SIEMENS

ISDN Burst Transceiver Circuit (IBC)

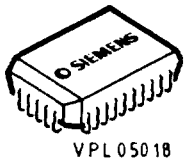
PEB 2095

Preliminary Data

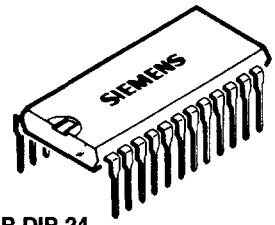
CMOS IC

1 Features

- Half duplex burst mode 2-wire U-interface transceiver
- Mode configurable to function at both ends of the line
- 144-kbit/s user bit rate (2B + D)
- 384-kHz line clock rate
- IOM®-1 and IOM®-2 compatible
- Clock and frame recovery
- Adaptive line equalization and amplification at receiver
- Implementation of activation/deactivation procedures
- Built-in wake-up function for activation from power-down state
- Switching of test loops
- Typical length of loop: up to 3.0 km with 0.6 mm diameter wire
- Advanced CMOS technology
- Low power consumption: 13 mW power down
  100 mW power up (maximum)



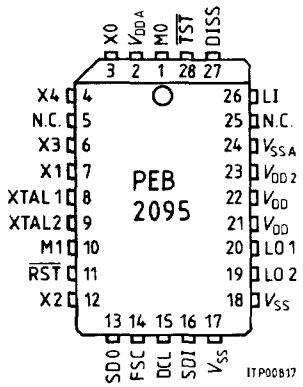
P-LCC-28-R

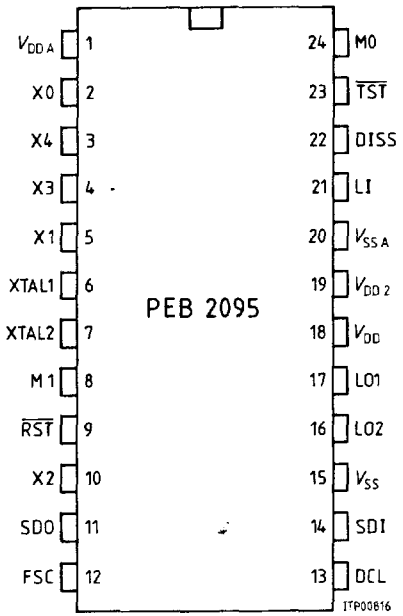


P-DIP-24

Type	Ordering Code	Package
PEB 2095-N	Q67100-H8396	P-LCC-28-R (SMD)
PEB 2095-P	Q67100-H8397	P-DIP-24

Pin Configurations
(top view)





P-LCC-28-R **P-DIP-24**

1.1 Pin Definitions and Functions

Pin No. P-LCC	Pin No. P-DIP	Symbol	Input (I) Output (O)	Function	
20	17	LO1	O	Line transmitter output 1	
19	16	LO2	O	Line transmitter output 2	U-interface
26	21	LI	I	Line receiver	
13	11	SDO	O	Serial Data Out	
16	14	SDI	I	Serial Data In	IOM-Interface
15	13	DCL	I/O	Serial Data Clock	
14	12	FSC	I/O	Frame Sync.	
1	24	MO	I	Operating Mode setup pins	
10	8	M1	I		
3	2	X0	I/O	Multifunctional pins; mode specific functions	
7	5	X1	I/O	(**see table 7**)	
12	10	X2	I		
6	4	X3	I		
4	3	X4	I/O		
8	6	XTAL1	I	External crystal or external oscillator input	
9	7	XTAL2	O	External crystal connection (N.C. when external oscillator is used)	
28	23	$\overline{TST}$	I	Device test pin; not for general use; tie high always	
27	22	DISS	O	Disable supply;	
11	9	$\overline{RST}$	I	Hardware reset pin; active low	
21, 22	18	V_{DD}	I	Digital Power Supply 5 V ± 5 %	
17, 18	15	V_{SS}	I	Digital Ground	
2	1	V_{DDA}	I	Analog Power Supply 5 V ± 5 %	
24	20	V_{SSA}	I	Analog Ground	
23	19	V_{DD2}	O	2.5 V output; connected to V_{DD} via 10 nF capacitor connected to V_{SSA} via 10 nF capacitor	
5, 25		N.C.		Not connected internally	

1.2 Logic Symbol

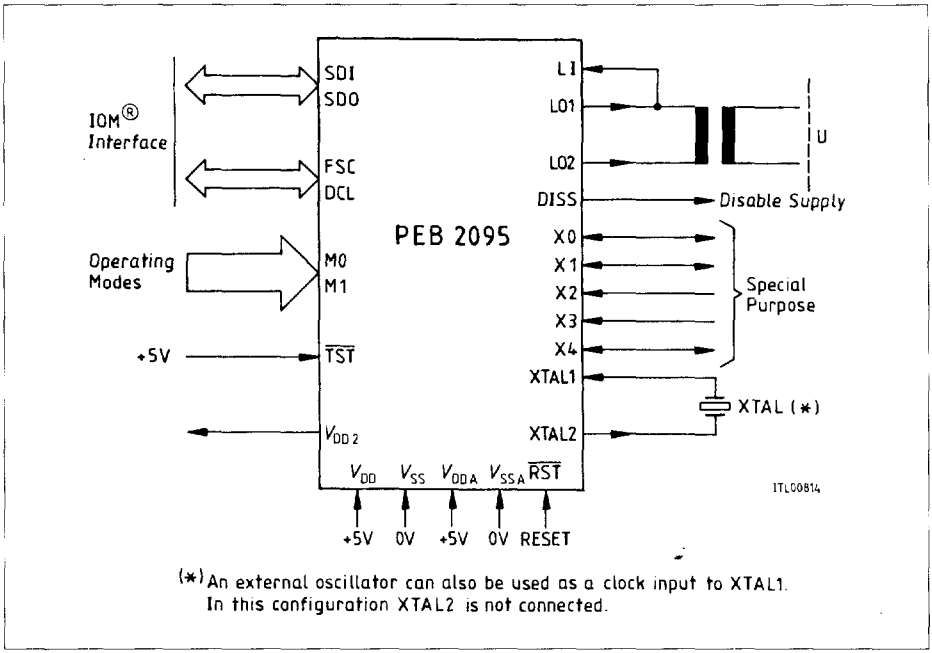


Figure 2
Logic Symbol of IBC PEB 2095

1.3 Functional Block Diagram

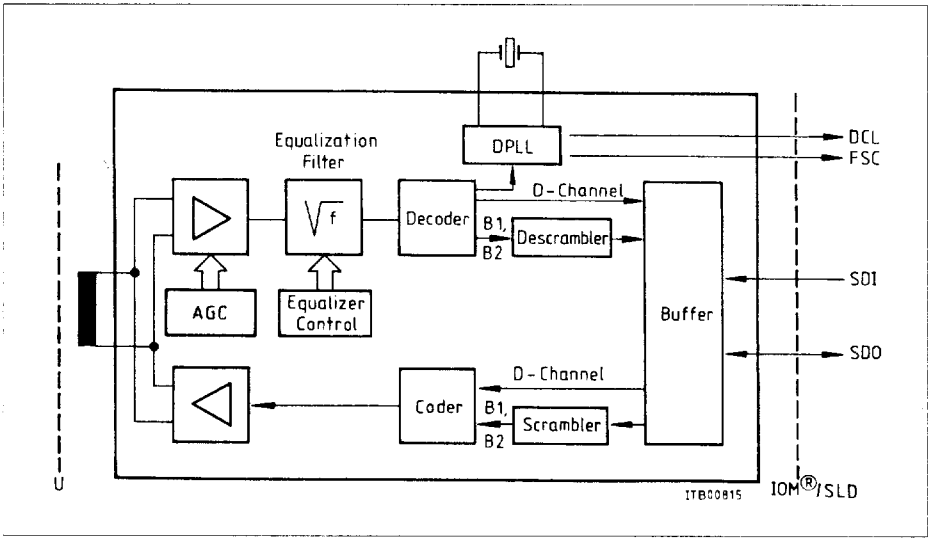


Figure 3
IBC Block Diagram

2 System Integration

Figure 1 illustrates the uses of the IBC in IOM-architecture. These constitute the 3 basic operating modes:

LT: Line Termination i.e. in the Local Exchange/PABX

TE: Terminal Equipment i.e. in the Subscriber Terminal

PT: Private Termination

In **figure 4**, two examples of LT-mode are illustrated, one connected directly to the terminal, one connected to a Private Termination. In the latter case the terminal is connected over the S-interface to the Private Termination. Because of the multiplexing facility on the S-bus up to eight terminals may be connected to one Private Termination and hence to one subscriber line. In the former case (without a Private Termination) only one terminal per subscriber line is possible.

In the LT-mode the IBC manages layer-1 functions and communicates over the IOM-interface with the ICC (ISDN Communication Controller) which handles most layer-2 functions. A microprocessor (handling higher layer functions) controls and communicates with the ICC. A similar configuration is required in the TE-mode, employing the same division of tasks (**figure 1**).

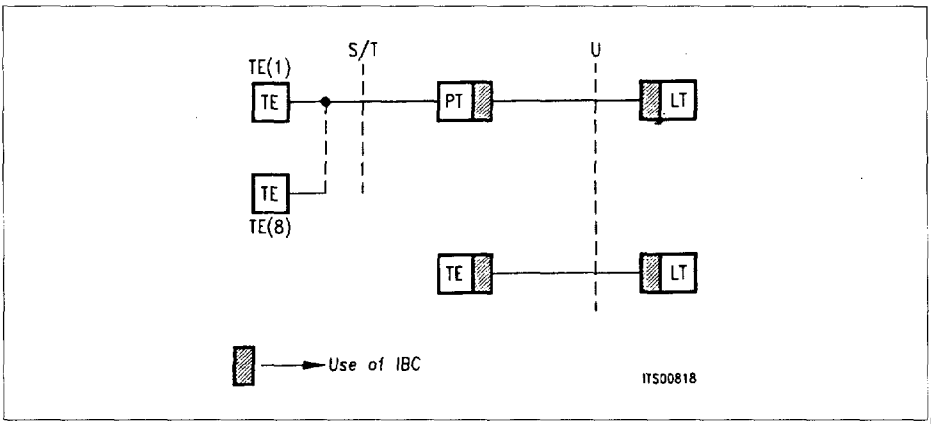


Figure 4
Basic IBC Modes

PT refers to a simple layer-1 translation between the U-interface and the S/T-interface. This is achieved by the simple pairing of the IBC with an IOM compatible bus interface circuit (e.g. the SBC PEB 2080), as illustrated in the first example in **figure 1**.

In this configuration no ICC or microprocessor is required because layer 2 and higher are passed transparently through PT. The IOM-interface acts as an intermediate interface common to both devices.

2.1 Operating Modes

The IBC may be configured for 3 basic operating modes.

- TE-mode: ISDN terminals
- PT-mode: ISDN Private Termination
- LT-mode: ISDN Line Termination

Furthermore in each of these operating modes further timing mode possibilities may be open.

Configuration is achieved by pinstrapping (pins M0, M1 and sometimes X2). Both the IOM-clock signals (DCL, FSC) and the multifunctional pins (X0, X1, X2, X3) have mode dependent functions (**refer table 1**).

Table 1
IBC Operation Modes and Mode Specific Pin Configurations

	Application						
	TE	**TE**	**TE**	**PT**	**LT**	**LT**	**LT**
Operation of IOM interface	inverted mode	IOM-1 mode	IOM-2 mode	normal mode	IOM-1 mode	inverted mode	IOM-2 mode
M1 M0	i:0 i:0	i:0 i:0	i:0 i:RST	i:0 i:1	i:1 i:0	i:1 i:1	i:1 i:1
DCL	o: 512 kHz* "Duty ratio" 1:1	o: 512 kHz* "Duty ratio" 1:1	o: 1.536 MHz* "Duty ratio" 1:1	o: 512 kHz* "Duty ratio" 1:1	i:512 kHz	i: 4096 kHz	i: 4096 kHz
FSC	o:8 kHz* "Duty ratio" 63:1	o:8 kHz* "Duty ratio" 1:1	o:8 kHz "Duty ratio" 1:2	o:8 kHz* "Duty ratio" 1:1	i:8 kHz	i:8 kHz "Duty ratio" 511:1	i:8 kHz
X4	o: 2.56 MHz "Duty ratio" 1:2 o: 7.68 MHz* "Duty ratio" 1:1	o: 2.56 MHz "Duty ratio" 1:2 o: 7.68 MHz* "Duty ratio" 1:1	o: 2.56 MHz "Duty ratio" 1:2 o: 7.68 MHz* "Duty ratio" 1:1	o: 7.68 MHz* "Duty ratio" 1:1	i:PFOFF	i:PFOFF	i:PFOFF
X3	i:$\overline{\text{ENCK}}$	i:$\overline{\text{ENCK}}$	i:$\overline{\text{ENCK}}$	i:$\overline{\text{ENCK}}$	i:MPF	i:MPF	i:MPF
X2	i:1	i:0	i:0	i:$\overline{\text{SCP}}$	i:0	i:TS2	i:TS2
X1	o: 1.536 MHz* "Duty ratio" 1:1	o: 1.536 MHz* "Duty ratio" 1:1	o: 768 kHz* "Duty ratio" 1:1	i:$\overline{\text{SSP}}$	o: 15.36 MHz "Duty ratio" 1:1	i:TS1	i:TS1
X0	o: 3.84 MHz	o: 3.84 MHz	o: 3.84 MHz	i:1	o:CONF4	i:TSO	i:TSO

*: synchronized to U i: = input o: = output

i: 0: input fixed to V_{SS}

i: 1: input fixed to V_{DD}

DCL: i/o: Data Clock, the frequency is equal to twice the data rate on the IOM-2 interface.

FSC: i/o: Frame Synchronization Clock.

RST: input: TE IOM-2 mode is selected by connecting pin M0 to pin $\overline{RST}$.

X4: In TE-mode the clock output at pin X4 (2.5 MHz after reset or 7.68 MHz) is programmable by CONF4 over the MONITOR Channel.

$\overline{ENCK}$: input: Enable Clocks. In TE- and PT-mode when $\overline{ENCK}$ = 0 the clocks are enabled in 'deactivated' state, and during $\overline{RST}$ = 0 the outputs are low impedance and high impedance otherwise.

$\overline{SSP}$ input: Send Single Pulses. In PT-mode a low sets the IBC to the state test mode 1.

$\overline{SCP}$: input: Send Continuous Pulses. In PT-mode a low sets the IBC to the state test mode 2.

PFOFF: input: Powerfeed Off. In LT-modes the IBC is put into a powerfeed off state with a high at PFOFF. This state is indicated by the C/I code HI.

MPF: input: Main Power Feed. In LT-modes this pin can be used for power supply control by the layer-2 device. The 8-bit supply current equivalent is read serially from the local power supply. The read is synchronous to the B1-channel in the IOM-frame or to time-slot 0 in LT-MUX mode respectively. The layer-2 device has access to the 8-bit supply current equivalent via the I(7:0) register. Tie MPF to low when not in use.

CONF4: Output: In LT-IOM-1 mode a high or a low is output at X0 according to the programming of CONF4. Useful to control other devices.

TSx: input: Time-slot number 0 to 7. In LT inverted and LT-IOM-2 mode the channel is selected by pin strap.

Table 2

	Time-Slot No.							
Pin	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
X2: TS2	0	0	0	0	1	1	1	1
X1: TS1	0	0	1	1	0	0	1	1
X0: TS0	0	1	0	1	0	1	0	1
Bit No.	0 ... 31	32 ... 63	64 ... 95	96 ... 127	128 ... 159	160 ... 191	192 ... 223	224 ... 255

Notes:

1. SDI-(IOM-interface)
   - the pin is connected to an internal pull-up resistor in TE and LT IOM-1 modes.

2. SDO-(IOM-interface)
   - open drain output in IOM-2 modes and LT-inverted mode.
   - open drain output with internal pull-up resistor in PT mode
   - push-pull otherwise

3. The following clock outputs are derived from the 15.36 MHz crystal/external oscillator: (i.e. unsynchronized)
   15.36 MHz

   3.84 MHz

   2.56 MHz

4. The following clock outputs are synchronized to the line
   7.68 MHz

   1.536 MHz

   768 kHz

   512 kHz

   8 kHz

5. Distinction between LT IOM-2 and LT-inverted mode is performed automatically, dependent on the FSC signal delivered. Distinction between TE IOM-1 and TE IOM-2 mode is performed using the rising edge of the $\overline{\text{RST}}$-signal to sample the M0 input. During $\overline{\text{RST}}$ = low, the IBC is always in IOM-1 mode.

2.2 Clock Generation

In all modes the system clocking is supplied by the upstream device to the downstream device. Hence, in some modes, the IBC provides DCL and FSC and in others, it receives DCL and FSC externally.

The clock outputs act as external oscillators for other devices. For example in **figure 5** (PT mode), the SBC uses the 7.68-MHz synchronized output from the IBC as an external oscillator. Further possible applications include:

- 15.36 MHz (LT) - external oscillator for other IBCs
- 1.536 MHz (TE) - CODEC clock supply
- 768 kHz (TE) - single bit clock for IOM-2 interface slave devices

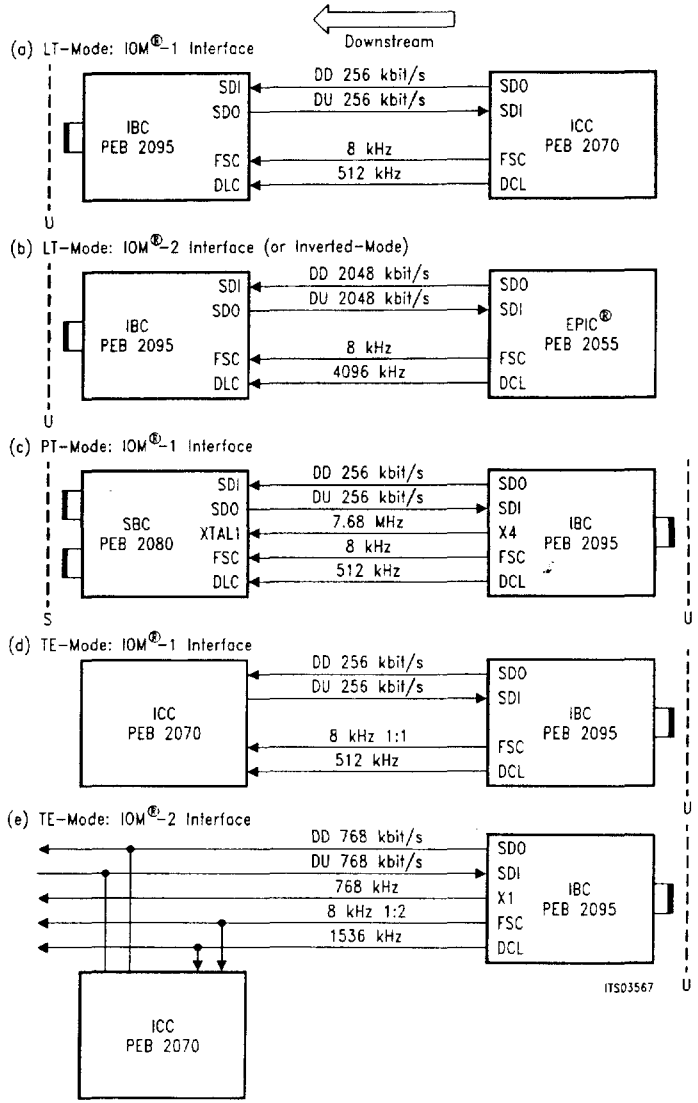


Figure 5
Clocking of the IBC in Different Modes

3 Functional Description

3.1 IBC Device Architecture and General Functions

The ISDN Burst Transceiver Circuit (IBC PEB 2095) performs the layer-1 functions of the time-division multiplex implementation of the U-interface. This is a half duplex technique (ping-pong) involving transmission by only one device at any one time. Furthermore the IBC acts a link between the U-interface to the IOM-interface and hence to other layer-1 or layer-2 devices within the system. **Figure 6** depicts the device architecture.

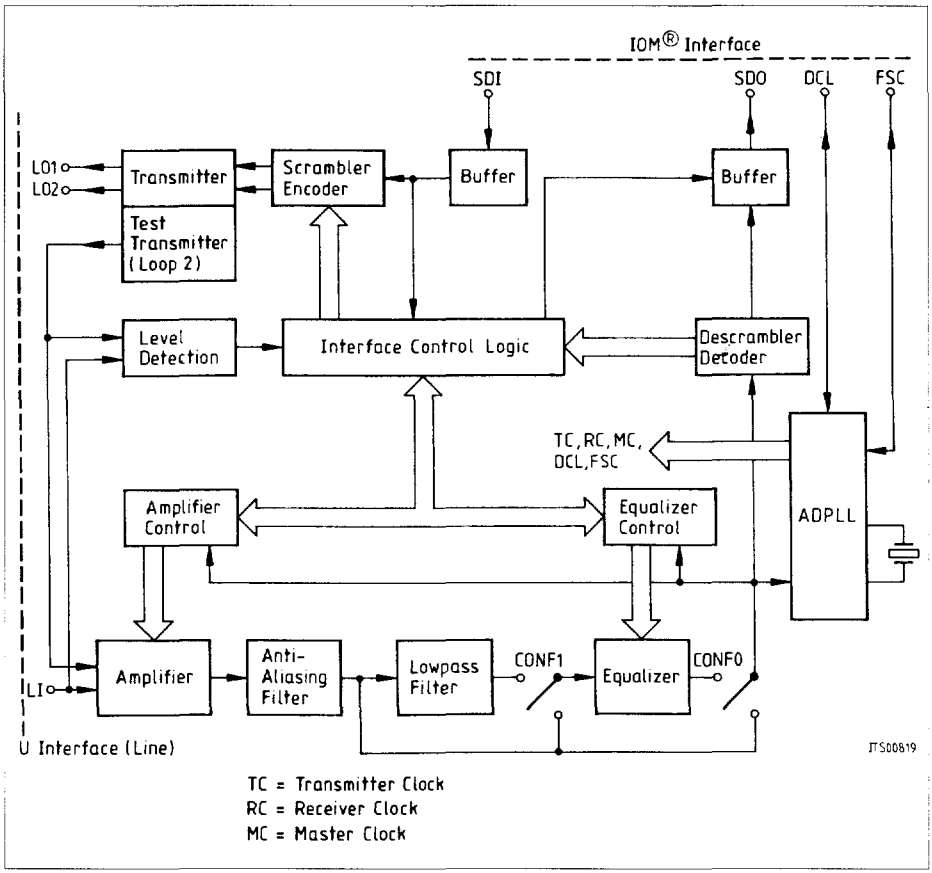


Figure 6
IBC Device Architecture

Some of the relationships between the blocks of the device architecture and the IBC functions outlined below can be traced at this stage. This section, however, will deal in more detail with these relationships.

The following are the main functions of the IBC:

- Activation/deactivation procedures. Activation may be initialized by either infos from the line or primitives from the IOM-interface
- To increase the quality of signal received from the line, the receiver stage contains both an *adaptive amplifier and equalizer*
- Synchronous timing must be maintained on both sides of the device. All internal clocks are synchronized to the upstream data clock (system clock). All generated downstream clocks are synchronized, in turn, to these internal clocks.
- Testing and diagnostic functions: Testloops may be closed, test signals may be generated

Furthermore the IBC must also link-2 contrasting interfaces, the IOM-interface and the U-interface. To do this transparently, the IBC must compensate for the following main differences between them:

- The U-interface is a burst mode interface while the IOM-interface is continuous
- The frame structure and data transmission techniques on both interfaces are different
- The B channels are scrambled on the U-interface and unscrambled on the IOM-interface
- The clock rates are different and the transmitted in a different manner. In the U-interface the clock is implicit in the data stream; in the IOM-interface 2 separate clocks, DCL and FSC, must be provided.

3.2 Analog Functions

Figure 7 depicts the analog and power connections to the IBC. Both analog and digital power may be connected to a single power source. The reference voltage V_{DD2} must be linked by two 10 nF capacitors to V_{SS} and V_{DDA}. External to the transmitter and receiver a transformer (ratio 1.25:1) and external resistance (R_{EXT} = 140 Ω ± 1 %) are connected as shown. Voltage overload protection is achieved splitting R_{EXT} into 130 Ω and 10 Ω (for current limitation) and adding clamping diodes. If required a resistor (100 Ω max.) may be added to the line signal input for overvoltage current limitation.

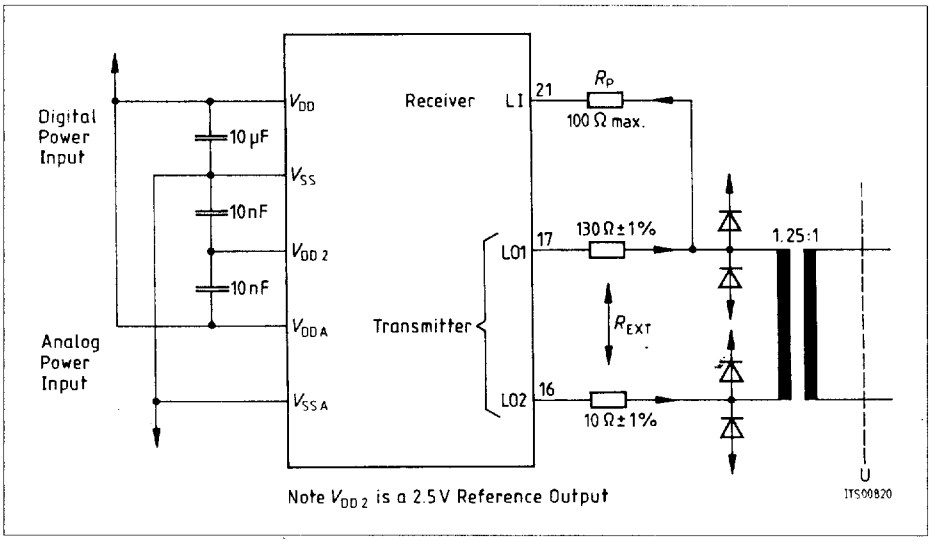


Figure 7
IBC Analog Connections

The transmitter stage is realized as a voltage source with an internal resistance $R_i = 15\ \Omega \pm 40\ \%$. It delivers a pulse of amplitude 2 V ± 10 % (0-to-peak). Assuming a transformer winding resistance of the order of 1 Ω, the output resistance seen from the U-interface will be 100 Ω.

Referring again to **figure 6**, the receiver input stages can be seen. They consist of a variable gain amplifier, to compensate for signal losses on the line (dynamic range 30 dB). This is followed by an anti-aliasing filter and a switched capacitor low pass filter. Finally a switched capacitor equalizer suppresses the out-of-band noise, which has passed the (anti-aliasing) filter stage, while keeping the pulse distortion low (dynamic range 15.36 dB).

Both the amplifier and the equalizer are adaptive. The amplifier has 128 possible settings and the equalizer 8 (in this sense they are digital). The adaptive logic can be stopped by externally setting the amplifier and equalizer over the IOM-interface. Once set in this way the settings remain constant. The MONITOR channel can also be used to program some other functions.

The level detection block MONITORS the receive line and informs the interface logic when an incoming signal is present. It also monitors the test transmitter to perform a similar function during test loop implementation.

3.3 Digital Functions

The DPLL circuitry works with an external oscillator or crystal of 15.36 MHz ± 100 ppm. This is used to synchronize all bit and frame clocks with the incoming system clock (i.e. from upstream). In the LT-mode the system clock is supplied over the IOM-interface. Generation of half-bauded AMI pulses for the line is accomplished by deriving a synchronous transmitter clock using the DPLL. At the PT/TE end of the line the data clock of 384 kHz is implicitly received in the data stream and is extracted by the IBC. From this all synchronous clocks are derived with the aid of the DPLL.

An incorporated finite state machine controls ISDN layer-1 activation/deactivation. This includes wake signal recognition in the "deactivated" state.

Due to the burst nature of U-interface communication and the continuous nature of communication on the IOM-interface a buffer memory is required to compensate for timing differences.

The digital control logic also sets the adaptive coefficients on the AGC amplifier and the SC equalization filter.

3.4 Scrambler/Descrambler

B-channel data on the U-interface is scrambled to give a flat continuous power density spectrum and to ensure enough pulses are present on the line for a reliable clock extraction to be performed at the downstream end.

The IBC therefore, contains a scrambler and descrambler, in the transmit and receive directions respectively. The basic form of these are illustrated in **figure 8**.

The form is in accordance with the CCITT V.27 scrambler/descrambler and contains supervisory circuitry which ensures no periodic patterns appear on the line.

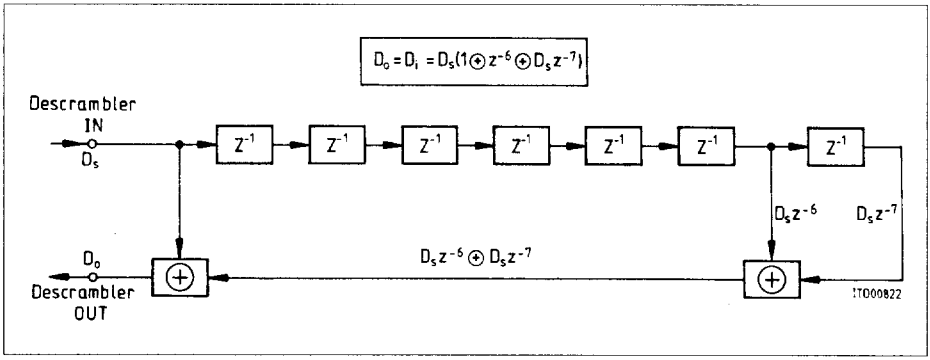
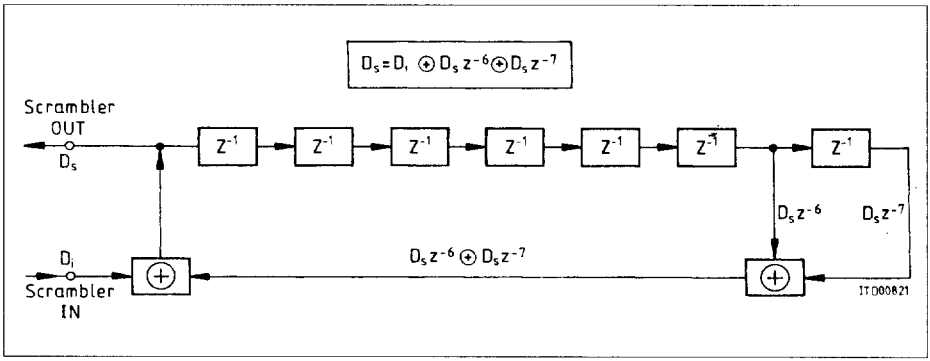


Figure 8
IBC Scrambler



IBC Descrambler

3.5 U-Interface

Figure 9 demonstrates the general principles of the U-interface burst mode communication technique. A frame transmitted by the exchange (LT) is received by the terminal equipment (TE) after a given propagation delay. The terminal equipment waits a minimum guard time (5.2 µs) while the line clears. It then transmits a frame to the exchange. The exchange will begin a transmission every 250 µs (known as the burst repetition period). However, the time between the reception of a frame from the TE and the beginning of transmission of the next frame by the LT must be greater than the minimum guard time. Communication between an LT and a PT follows the exact same procedure.

Within a burst, the data rate is 384 kbit/s and the 38-bit frame structure is as shown in **figure 9**. The framing bit (LF) is always logical '1'. The frame also contains the user channels (2B + D). Note that the B channels are scrambled. It can readily be seen that in the 250 µs burst repetition period, 4 D bits, 16 B1 bits and 16 B2 bits are transferred in each direction. This gives an effective full duplex data rate of 16 kbit/s for the D-channel and 64 kbit/s for each B-channel.

The final bit of the frame is called the M-bit. Four successive M-bits, from four successive U-frames, constitute a superframe (**figure 9**). Three signals are carried in this superframe. Every fourth M-bit is a code violation (CV) and is used for superframe synchronization. This can be regarded as the first bit of the superframe. From this reference, bit 3 of the superframe is the service channel bit (S). The S-channel bit is transmitted once in each direction in every fourth burst repetition period. Hence the duplex S-channel has a data rate of 1 kbit/s. It conveys test loop control information from the LT to the TE/PT and reports of transmission errors from the TE/PT to the LT. Bit 2 and bit 4 of the superframe are T-bits. These constitute the 2-kbit/s T-channel which extends the T-channel of the IOM-frame (**figure 13**) onto the U-interface.

In order to decrease DC-offset voltage on the line after transmission of a CV in the M-bit position, it is allowed to add a DC-balancing bit to the burst. The IBC transmits this DG-balancing bit in LT-mode, when transmitting INFO 4, and when line characteristics indicate potential decrease in performance. However this DC-balancing bit may generally be switched on by programming CONF1 to ZERO (cf. chapter 5).

Note that the guard time in TE is always defined with respect to the M-bit, whereas AMI coding includes always all bits going in the same direction.

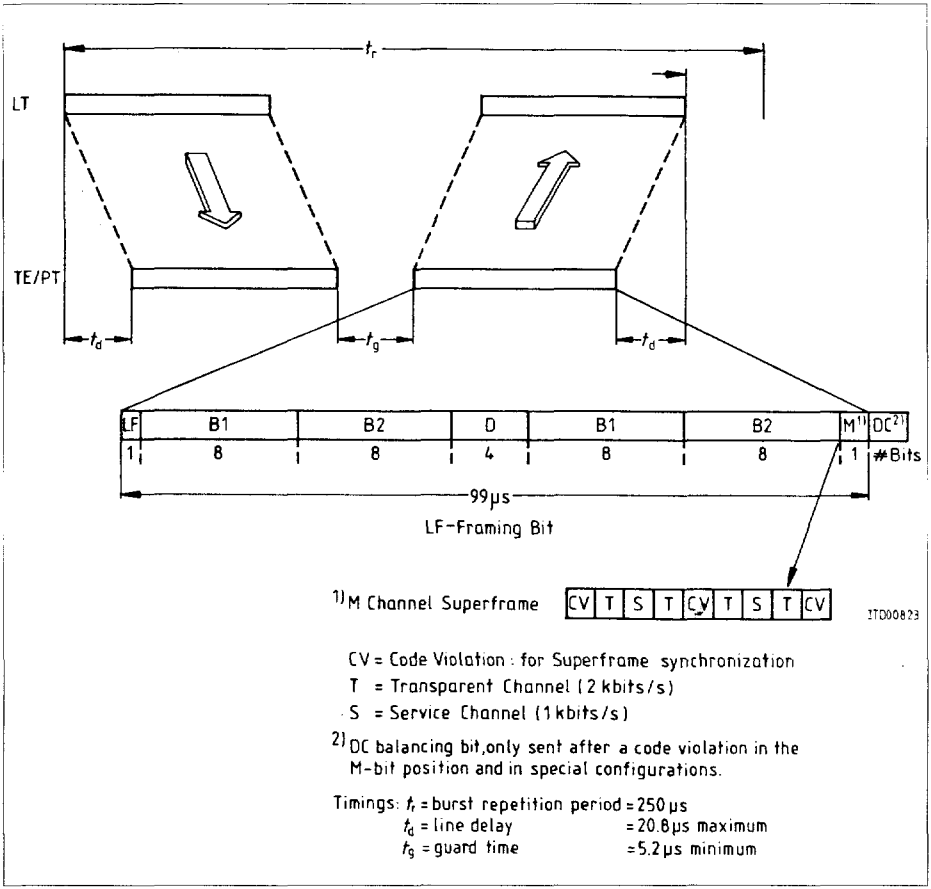


Figure 9
U-Interface Transmission/Reception

The coding technique used on the U-interface is half-bauded AMI code (i.e. with a 50 % pulse width). **Figure 10** illustrates the code. As can be seen, a logical '0' corresponds to a neutral level, a logical '1' is coded as alternate positive and negative pulses. The figure also illustrates how a code violation may be achieved (CV); either two successive positive (as shown) or negative pulses.

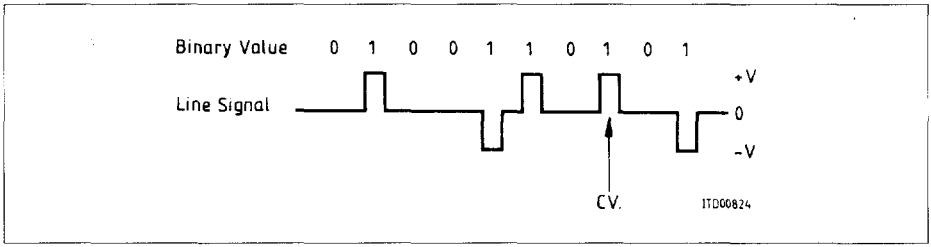


Figure 10
Half-Bauded AMI Code

3.6 IOM® -Interface

The IBC is provided with a digital interface, the IOM interface, for communication with other ISDN devices, in other words with units realizing OSI layer-1 functions (such as the ISDN S-bus Transceiver SBC PEB 2080) or layer-2 functions (such as the ISDN Communication Controller ICC PEB 2070). (**See figure 11**).

The IOM interface consists of 2 clocks; DCL (data clock) and FSC (Frame Synchronization Clock), and 2-data lines; data out and data in. The data in both directions is synchronous and in-phase.

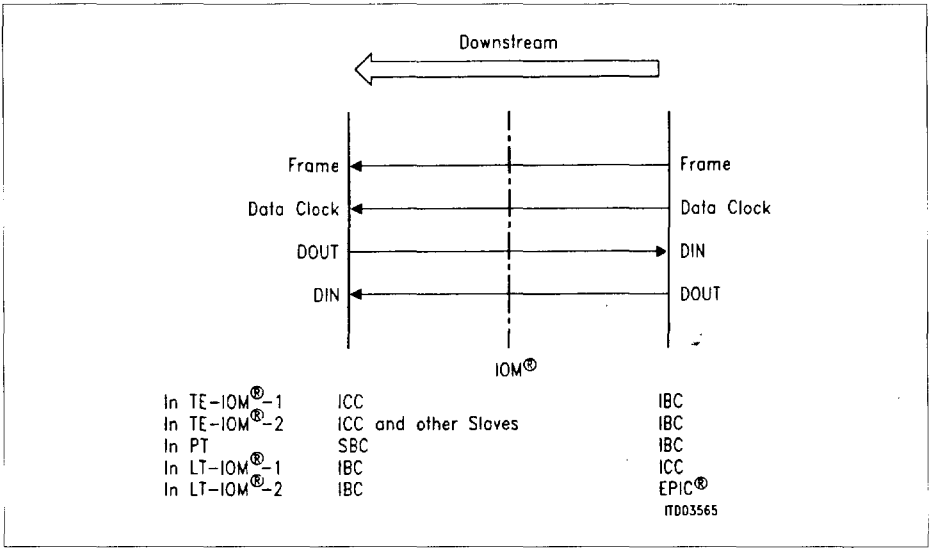


Figure 11
IOM®-Interface of IBC

The IOM-frame structure is illustrated below. It contains the 2B + D-channels, transmitted transparently over the interface at 144 kbit/s. In addition, it is necessary to interchange control information for activation and deactivation of OSI layer 1, for switching of test loops etc. This is transferred through the so-called B*-channel. The B*-channel is in fact made up of four channels:

- D: The D-channel (2 bits)
- C/I: The Command and Indication Channel (4 bits) is used to convey control information across the IOM-interface. This information refers directly to OSI model layer-1 - layer-2 communication. Chapter 5 lists the possible C/I codes.
- T: The "Transparent" bit

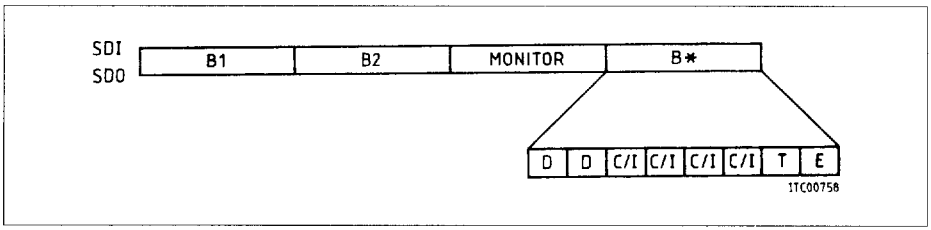


Figure 12
IOM®-Frame Structure

The 8-bit MONITOR channel handles information exchange between the layer-2 and layer-1 devices not covered by OSI e.g. AGC coefficient setting. Its use, however, may be restricted by the ICC Mode register's configuration. For a complete description of available MONITOR codes and their use, refer to section 5.

Note:

In IOM-2 mode the IBC doesn't acknowledge received MONITOR data. The T- and the E-bit are used as MR- and MX-bit respectively for MONITOR channel handling in this case.

Section 2 outlined the three basic operating modes of the IBC (LT, TE and PT) and their relationship to the system architecture. But, as will be seen, the IBC has seven operating modes. This is due to the existance of timing modes:

- IOM-1 Mode
- IOM-2 Mode
- Inverted Mode.

The different modes only effect the timing of the IOM interface and will now be discussed in detail. Section 2.1 will describe the seven operating modes in more detail.

3.6.1 IOM®-1 Mode

This timing mode is applicable in all three basic operating modes of the IBC.

Nominal bit rate of data (SDI and SDO):	256 kbit/s
Nominal frequency of DCL:	512 kHz
Nominal frequency of FSC:	8 kHz

Transitions of the data occur after even-numbered rising edges of DCL. Even-numbered rising edges of the clock are defined as the second rising edge following the rising edge of FSC and every second rising edge thereafter.

The frame is earmarked by the rising edge of FSC. **Figure 13** shows the position of the IOM frame with respect to the clocks.

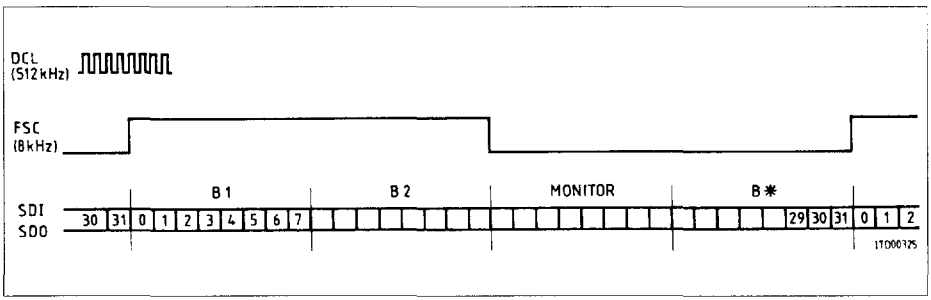


Figure 13
Timing of Data and Clocks of IOM® in the IOM®-1 Mode

3.6.2 IOM®-2 Mode

This timing mode is applicable only in TE-and LT-operating modes.

Nominal bit rate of data bursts (SDI and SDO)	2048 kbit/s in LT-mode 768 kbit/s in TE-mode
Nominal frequency of DCL	4096 kHz in LT-mode 1536 kHz in TE-mode
Nominal frequency of FSC	8 kHz

The data at the input SDI is valid on the odd-numbered falling edges of DCL. Transitions of the data on SDO occur after even-numbered rising edges of DCL. The rising edge earmarked by the frame strobe is an even-numbered rising edge of DCL. The following falling edge is an even-numbered falling edge.

The IBC sends an IOM-frame in the form of a burst, 1/8 or 1/3 of an FSC-period long. Hence, in LT-application up to 8 IBCs can be multiplexed on the SDO- and SDI-lines. Each IBC is allocated a time slot, by the static inputs X0(TS0), X1 (TS1) and X2(TS2). The IBC will both transmit and receive data in this time slot.

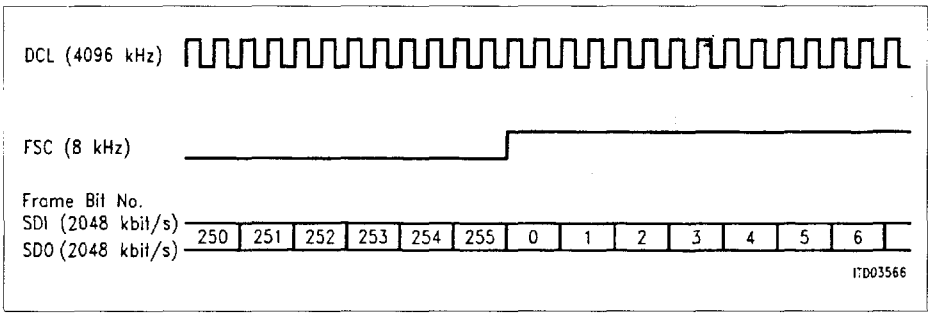


Figure 14
Timing of Data and Clocks of IOM® in the IOM®-2 Mode

In TE mode, the IBC uses the first third of the FSC-period to transmit the 256 kbit/s. The remaining two thirds of the period can be used by other devices.

3.6.3 Inverted Mode

This timing mode is only applicable in TE- and LT-operating modes.

Nominal bit rate of data bursts (SDI and SDO) 2048 kbit/s in LTmode
256 kbit/s in TE-mode

FSC is not a signal with 50 % duty cycle but rather an active low pulse, one DCL-clock period long, which occurs in the middle of the fourth bit of B*, of the last 256-kbit/s channel of a frame.

Transitions of data occur after even-numbered falling edges of DCL. Even-numbered falling edges are defined as the second falling edge following the rising edge of FSC and every second falling edge thereafter.

3.6.4 Activation/Deactivation of the IOM®-Interface

Power consumption is under 13 mW in the deactivated state (also called the "Power-Down" state) when the IOM-clocks, and hence the IOM-interface itself, are disabled. When disabled the clock lines are low and the data lines are high. When the IOM-interface is disabled no C/I commands can be passed to the IBC. To communicate over the C/I-channel the clocks must first be enabled.

For the TE/PT-case the deactivation procedure is shown in **figure 15**. After detecting the code DIU (Deactivate Indication Upstream) from the downstream unit, the IBC responds by transmitting DID (Deactivate Indication Downstream) during subsequent frames and stops the timing signals synchronously with the end of the last C/I-channel bit of the fourth frame.

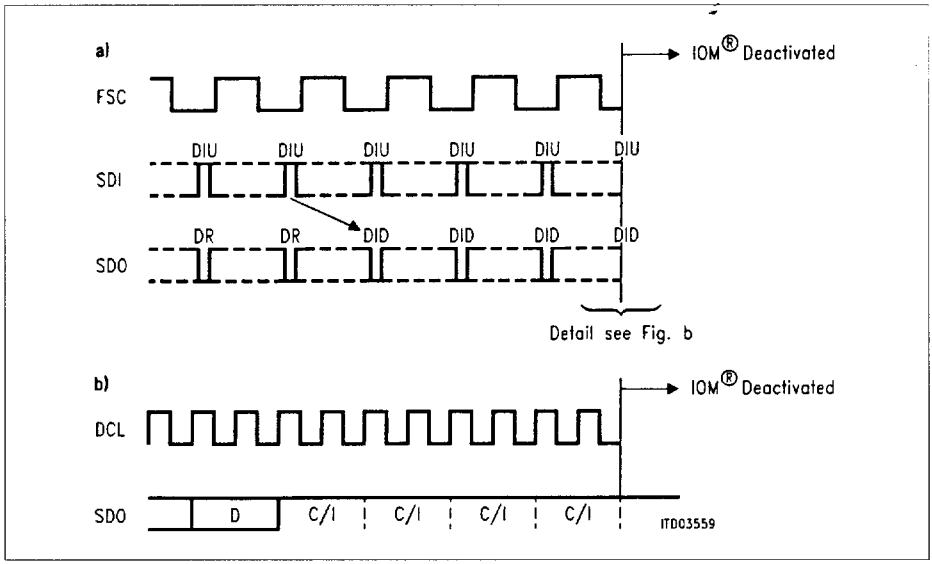


Figure 15
Deactivation of the IOM®-Interface

The clock pulses will be enabled again when the IBC recognizes a low level on SDI (equivalent to the C/I-command TIM = "0000") or when a non-zero level on the U-interface is detected.

When the clocks have been enabled the indication PU is sent in the C/I-channel. The downstream unit may then insert a valid code in the C/I-channel. The continuous supply of timing signals by the IBC is assured as long as there is no DIU-command in the C/I-channel. If timing signals are no longer required and activation is not yet requested, the downstream unit may indicate this by sending DIU.

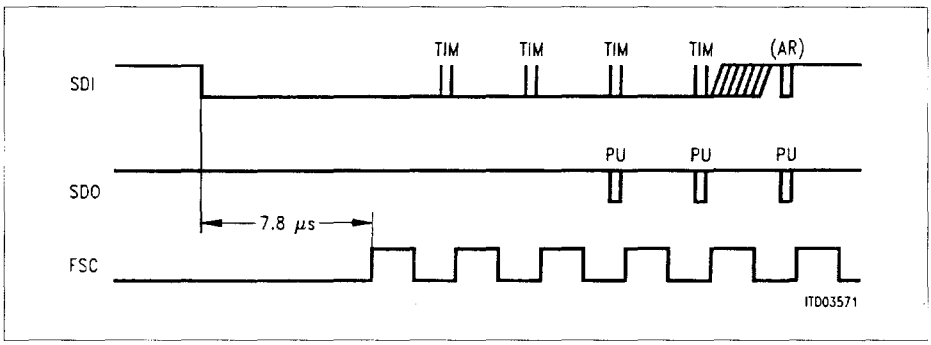


Figure 16
Activation of the IOM®-Interface

As an alternative to clock activation via SDI, the asynchronous wake-up pin $\overline{\text{ENCK}}$ (X3 in both TE- and PT-mode) can be grounded. In this case the timing given in **figure 16** applies. When $\overline{\text{ENCK}}$ is tied to ground the IOM-clock pulses are delivered by IBC at all times.

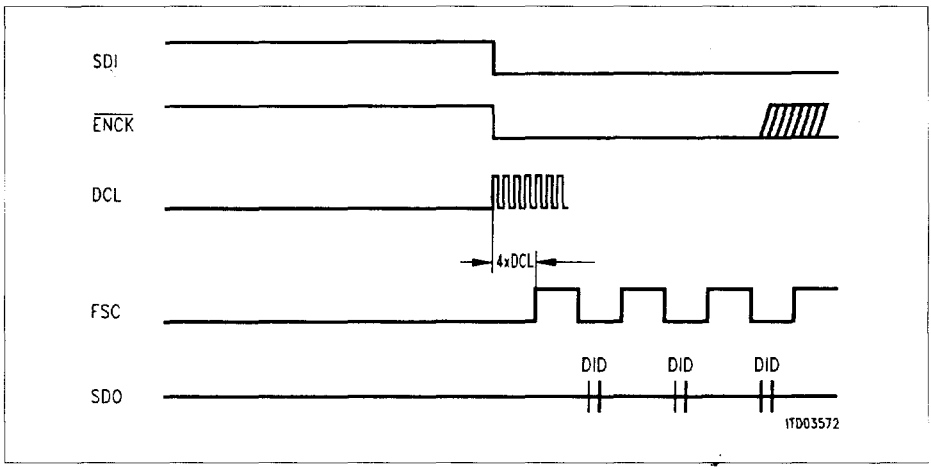


Figure 17
Activation of the IOM®-Interface via $\overline{\text{ENCK}}$ (pin X3) in TE/PT-Mode (NB: DCL out of scale)

4 Operational Description

4.1 Maintenance Functions

4.1.1 Test Loops

Three types of test loops may be closed in the IBC, depending on the operating mode. In all test loops, all 3 channels B1, B2 and D are looped back. In a "Transparent" loop the data is sent forward unmodified as well as being looped back. In a "non-transparent" loop the forward data path is blocked. In both cases, however, the incoming data path is blocked and only the looped data is received.

Figure 18 illustrates these test loop configurations and also shows where in the system test loops would occur.

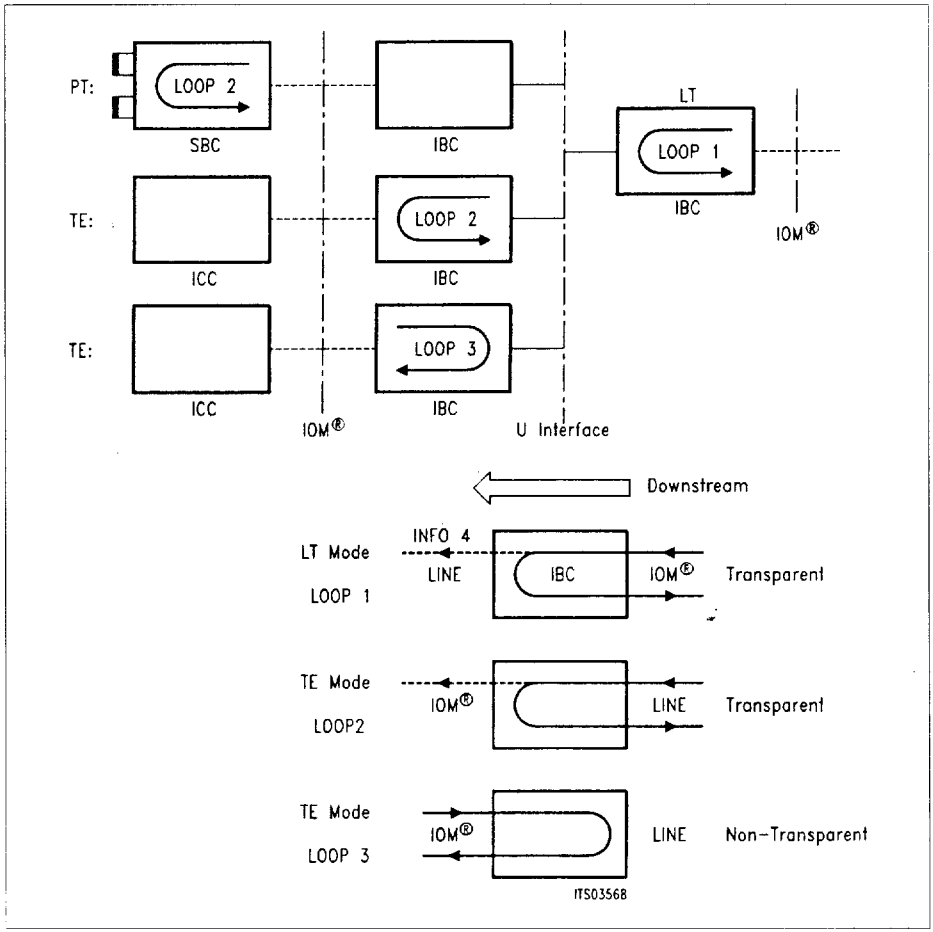


Figure 18
IBC Test Loops

Loop 1 and loop 3 are closed in the IBC itself, as close as possible to the line input/output. However activation of these loops will proceed normally whether the line is actually present or not. Loop 2 in the TE mode is closed within the IBC as close as possible to the IOM interface.

Both loop 1 and loop 3 are local loops, initiated by the local layer-2 device (ICC in **figure 18**) with an activate local loop command. In loop 1 all line signals are ignored but the looped infos are transmitted on the line simultaneously. In loop 3 the IBC doesn't transmit any looped data. It does however MONITOR the line and reports the presence of any signal to the layer-2 device by means of a RSYD indication. Only the layer-2 device can teminate the looping condition.

Loop 2 is initiated by the LT. Section 3 explains the activation of the U-interface by the LT both with and without loop 2. The S bit (service bit) on U-interface frame, sent by the LT, determines whether loop 2 is requested (S = 1) or not (S = 0). If the downstream IBC is in TE-mode then it will activate loop 2 while S = 1. If the downstream IBC is in PT mode it does not have a loop 2 mode. In this case, loop 2 should be closed as close as possible to the S-interface within the S-bus transceiver circuit (the SBC in **figure 18**). Hence, the presence of S = 1 during U-interface activation will cause the PT IBC to send an activate loop 2 request to the SBC which causes the latter to close the loop.

4.1.2 Test Signals

Two test signals can be sent by the IBC; send continuous pulses (also known as test mode 2) and send single pulses (test mode 1). In both cases half-bauded AMI coding is used, but only one of the IBCs at either end of the U-interface line transmits. Hence burst mode transmission is abandoned. In the first case a one is transmitted at 384 kbit/s. However, because of the alternate positive-negative nature of the coding, the signal on the line has a frequency of 192 kHz. In the second case, a one is transmitted at 4 kbit/s, yielding a signal of 2 kHz on the line.

4.1.3 Code Violation Monitoring

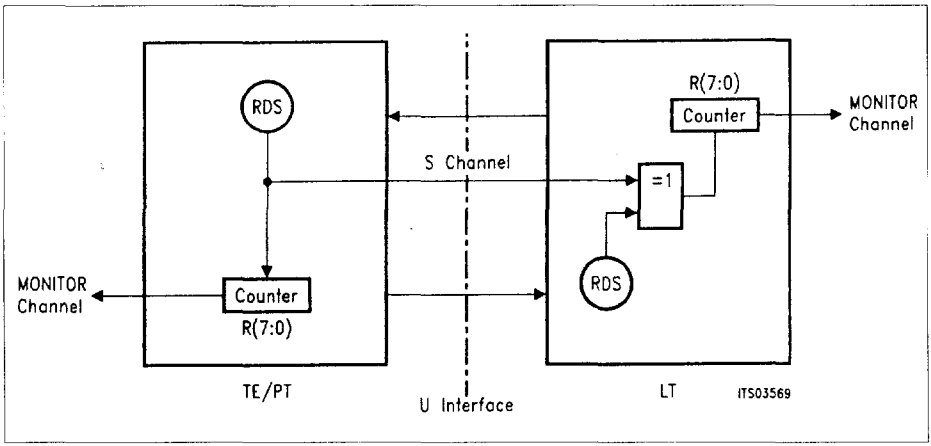


Figure 19
RDS: Running Digital Sum Operation

Once synchronization has been achieved, code violations are monitored on the line. This is achieved by means of the Running Digital Sum (RDS). The RDS is enabled in the synchronized state when the LT-indication is RDS and the TE/PT-indication is ARD. Both the code violation in the framing bit of info 1 and info 2 and the one used for superframe synchronization are ignored by the RDS (since they don't constitute errors).

In the TE/PT the RDS updates a counter (R7:0) every 1ms, incrementing it if an error has occured in that period. Similarly in the LT the RDS MONITORS the incoming signal and updates a counter. This update is OR´ed with the S-bit of the U-interface frame which contains the TE/PT update. Hence, the TE/PT-counter indicates code violations from the LT to TE/PT and the LT-counter indicates code violations in both directions. Note that because of the low frequency of the update neither counter contains an error count, only an indication that errors have occured. If the count reaches 255 (the maximum) it does not reset. It is reset only after a hardware/software reset or after the register itself is read. The counter is accessible over the MONITOR channel in all modes.

4.1.4 Power Supply Monitoring

In LT-modes the IBC can be used to MONITOR and control the power supply. In effect the IBC stands between the power supply and the higher OS-layer devices and through it the higher layers control the power supply. However the power supply must be able to communicate with the IBC in the following manner:

Pin X3, on the IBC, functions as the MPF (main power feed) pin in LT-modes. A "supply current equivalent" byte derived from the power supply can be read into register I(7:0) through the MPF pin. This read is synchronous to the B1-channel of the IOM-frame (in time-slot 0 if LT-MUX mode is used). The I(7:0) register can in turn be read by the ICC over the MONITOR channel. The ICC can use the information it contains to control the power supply. If the current value is too high the software issues a DIS-command. Pin DISS on the IBC goes high and, if properly connected, this pin can be used to disable the power supply. The IBC then goes into a reset state. If the power feed device is disabled either by DISS or by some overload condition (short circuit) it indicates this to the IBC by putting pin PFOFF on high. The IBC hands this information over to layer-2 device by putting the HI-indication in the C/I-channel.

The full operation of DISS-pin in the LT mode is governed by the following conditions:

DISS: output set = DIS + hardware reset.

DISS: output reset = software reset.

It acts as a flipflop output, once set it remains set until the occurance of one of the reset conditions. In the TE-and NT-modes a high on pin DISS indicates that the device is in the deactivated state and that the IOM-clocks are disabled.

Some or all of the above functions may be employed depending upon requirements. Alternatively Siemens also produce a power controller for the LT which can be directly controlled by a microprocessor (PEB 2025, the ISDN Exchange Power Controller).

4.2 Control of the Layer-1 Functions

The internal finite state machine of the IBC controls the activation/deactivation procedures, switching of test loops and transmission of special pulse patterns. Such actions can be initiated by signals on the U-transmission line (info's) or by control (C/I) codes sent over the IOM interface.

Once initiated such procedures normally involve passing through several states. Each successive state is entered on receiving a particular info (U-interface) or command (IOM-interface) and results in a particular info (U-interface) or indication (IOM interface) being transmitted.

In the IBC there are three possible state machines corresponding to the three basic operating modes: LT, TE and PT. In this section the interworkings of these mode dependent state machines will be focused on in detail.

4.2.1 Activation/Deactivation of the U-Interface

Figure 20 illustrates an activation and deactivation procedure between an IBC in LT-mode and an IBC in TE-mode over the U-interface line. It illustrates how the state machines of the respective modes interwork to facilitate activation and deactivation. In this case activation was initiated by an ARN-request at the terminal and deactivation by a DR-command at the LT. Activation could also have been initialized at the LT using an ARN-request.

Notes for **figure 20**

- T1: 1.5 ms; time for error free level detection
- T2: < 80ms; time for synchronization and equalizer adaption
- T3: 1 ms; four subsequent bursts with no CV in F-bit
- T4: 2ms; time for error free detection of INFO 0

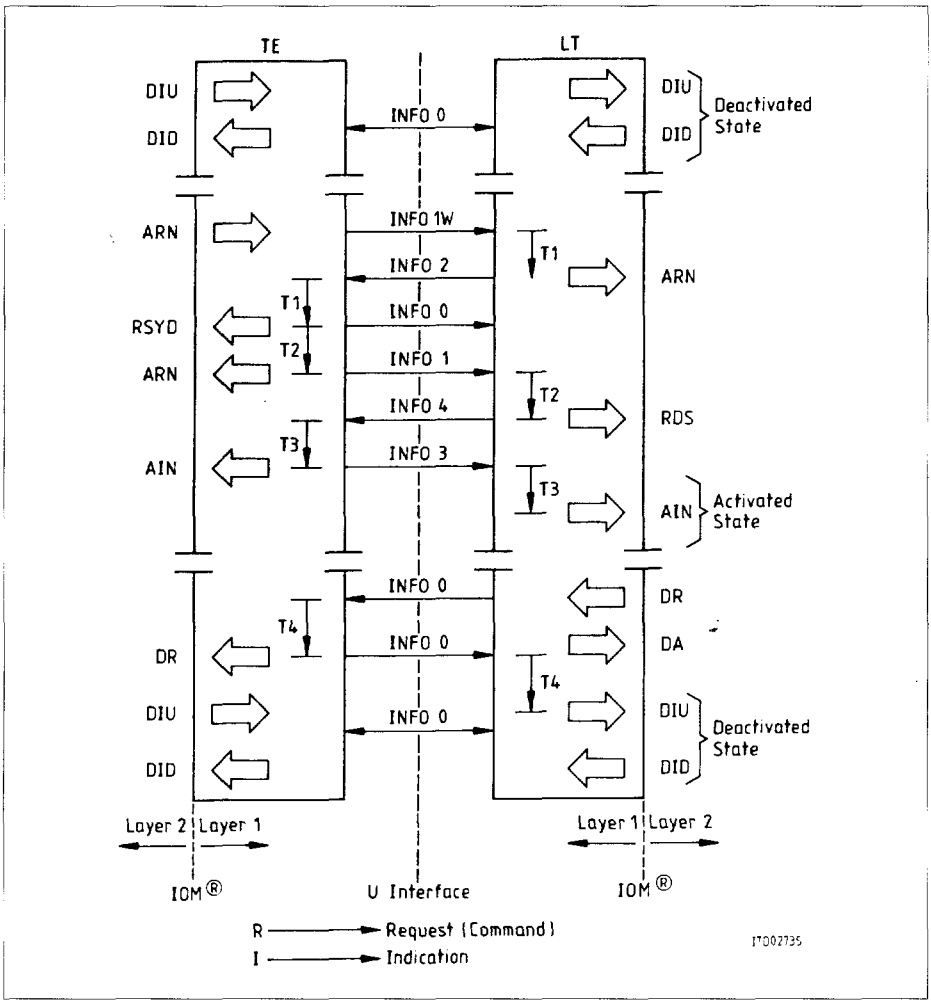


Figure 20
Example of IBC Activation/Deactivation

4.2.2 Info Structure on the U-Interface

The signals controlling the internal state machine on the U-interface are called infos. In effect, these pass information regarding the status of the sending IBC to the IBC at the other end of the line. They are based upon the same format as the U-interface frames described in section IOM® Interface and their precise form is shown in **table 3**.

When the line is deactivated info 0 is exchanged by the IBCs at either end of the line. Info 0 effectively means there is no signal sent on the line in either direction.

When the line is activated info 3 upstream and info 4 downstream are continually exchanged. Both info 3 and info 4 are effectively normal U-interface data frames containing user data and exchanged in normal burst mode.

Note that the structure of info1 and info 2 are the same, they only differ in the direction of transmission. Similarily info 3/info 4 and info 1w/info 2w also constitute info pairs. This will be important when considering looped states.

As we will see, the other infos are exchanged during the various states which occur between activation and deactivation of the line.

Table 3
U-Interface Info Signal

Name	Direction	Description
Info 0	Upstream Downstream	No signal on the line
Info 1W	Upstream	Asynchronous Wake Signal 2-kHz burst rate F000100010001000100010101010001011111 1 Code violation in the framing bit (F)
Info 1	Upstream	4-kHz burst rate F000100010001000100010101010001011111M [1] DC [2] Code violation in the framing bit
Info 2W	Downstream	Synchronous Wake Signal 2-kHz burst rate F000100010001000100010101010001011111 1 Code violation in the framing bit Only used for loop 1
Info 2	Downstream	4-kHz burst rate F000100010001000100010101010001011111M [1] DC [2] Code violation in the framing bit
Info 3	Upstream	4-kHz burst rate No code violation in the framing bit User data in B-, D- and M-channels B-channels scrambled, DC-bit [2] optional
Info 4	Downstream	4-kHz burst rate No code violation in the framing bit User data in B-, D- and M-channels B-channels scrambled, DC-bit [2] optional

Notes:

[1] The M-channel superframe is semitransparent:
S bits transparent [1 kbit/s channel]
T bits set to one [2 kbit/s channel]

[2] DC-balancing bit

4.3 State Diagrams

The state diagrams describe and define the state machine for each of the modes in an easily understandable manner.

Figure 21 illustrates the notation used

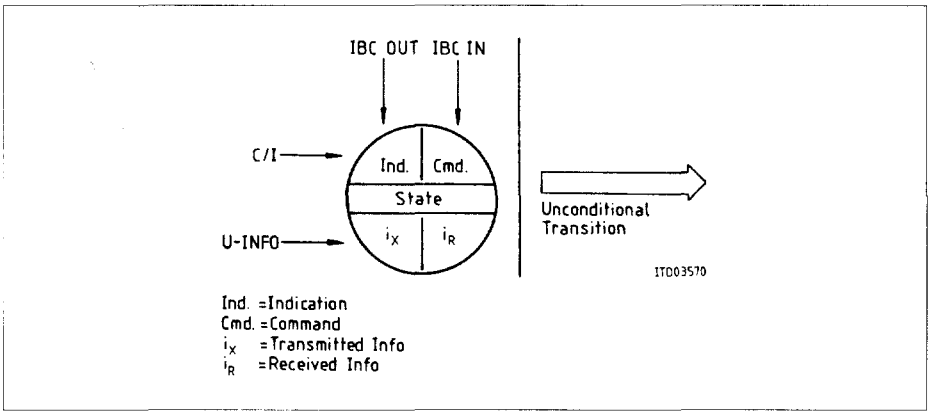


Figure 21
State Diagram Format

When in a particular state, the IBC will continually output the relevant C/I-indication and info. When considering the inputted C/I-command the IBC operates a double last look criterion. This means that a new code is only considered valid if it is found in two consecutive IOM-frames.

Finally for each mode there are some events which cause unconditional transitions to some particular state, regardless of the current state. Such an event may be a specific C/I-command or an active signal being present on an external pin.

4.3.1 Layer-1 Command/Indication Codes and State Diagrams in LT-Mode

Command (downstream) LT	Abbr.	Code	Remark
Deactivate Request	DR	0000	(x)
Activate Request No loop	ARN	1000	
Activate Request Local loop	ARL	1001	Loop 1 activation requested
Activate Request loop 2	AR2	1010	
Deactivate Indication	DID	1111	
Reset	RES	1101	Software Reset (x)
Disable Supply	DIS	0011	used to control the drain on local power supply (x)
Send Single Pulses	SSP	0101	Ones (AMI pulses) transmitted at 2 kHz (TEST MODE 1) (x)
Send Continuous Pulses	SCP	0111	Ones (AMI pulses) transmitted at 192 kHz (TEST MODE 2) (x)
Indication (upstream) LT	**Abbr.**	**Code**	**Remark**
Deactivate Indication	DIU	1111	
Deactivate Acknowledge	DA	0001	
RDS Indication	RDS	0111	Running Digital Sum. Code Violation register enabled. Receiver synchronized
Activate Request	ARU	1000	
Activate Indication	AIU	1100	
Resynchronisation	RSYU	0100	Lost Framing: receiver not synchronized to the input signal
High Impedance	HI	0011	After PFOFF the phantom power supply becomes high impedance

(x) unconditional commands

Unconditional States (LT):

Reset

This state is entered unconditionally after a low appears on the $\overline{RST}$ pin or after the receipt of command RES (software reset) or DIS (disable power supply). The analog section is disabled (transmission of info 0) and the U-interface awake detector is inactive. Hence, activation from PT or TE is not possible.

Test Mode

The test signal (it_i), sent to the U-interface in this state, is dependant on the command which originally invoked the state. SSP causes single alternating pulses to be transmitted (it_1); SCP causes continuous alternating pulses to be transmitted (it_2) (For signal description see section 4.1.2). The burst mode technique normally employed on the U-interface, is suspended in this state and the test signals are transmitted continuously.

Power Feed Off

When a high appears on the PFOFF external pin the phantom power supply is switched to high impedance. This is indicated to the layer-2 device by a HI-indication.

Pending Deactivation

To access any of the conditional states from any of the above unconditional states the pending deactivation state must be entered. This occurs after the receipt of a DR-command. In this state the awake detector is activated and the state is exited only when the line has settled (i.e. info 0 has been detected for 2 ms).

Although, for clarity, DR is shown as a normal command it is in fact an unconditional command: No matter which state the LT is in, the reception of a DR-command will always result in the pending deactivation state being entered.

Conditional States (LT):

Pending Loop 1

The receipt of ARL (activate request local loop) when in either the deactivated state, the pending deactivated state or the wait for $\overline{DR}$-state causes this state to be entered. Info 2w is sent out on the line and also looped back into the receiver where eventually it is recognized as info 1w (i.e. the format is the same, the direction has simply changed). From here the IBC moves into the pending activation state. The loop however remains closed and, hence, every info sent will become its own response and the device will self-activate. Note that the transmitted infos also appear on the line itself.

Wait for $\overline{DR}$

This state is entered from the pending deactivation state once info 0 has been identified. From here the line may be either activated, deactivated or a test loop may be entered.

Deactivated

This is the power down state of the physical protocol. Power consumption is cut to a minimum. The awake detection is active and the device will respond to an info 1w (wake signal) by initiating activation.

Pending Activation

This state results from a request for activation of the line, either from the terminal (info 1w) or from the layer-2 device (ARN or AR2). In the case of info1w a delay of 1.5 ms is implemented before this state is entered to allow error-free level detect and prevent accidental activation. Info 2 is then transmitted and the LT waits for the responding info 1 from the remote device.

Synchronized

Upon receipt of info 1 the LT must synchronize itself to the signal. To this end, both the equalizer and gain settings adapt to improve the quality of the incoming signal. This process takes at most 80 ms after which the LT supplies info 2 to the remote. The remote then synchronizes to the LT.

Activated

Info 1 has a code violation in the framing bit (F-bit) whereas info 3 has none. Upon the receipt of 2 frames without a code violation in the F-bit, the LT enters the activated state and outputs info 4. The line is now activated; the LT sends info 4 to the remote, the remote sends info 3 to the LT.

Resynchronization

If the LT fails to recognize info 3, for whatever reason, it will attempt to resynchronize. Entering this state it will output info 2. This is similar to the original synchronization procedure in the pending activation state (the indication given to layer 2 is different). However as before recognition of info 1 leads to the synchronized state.

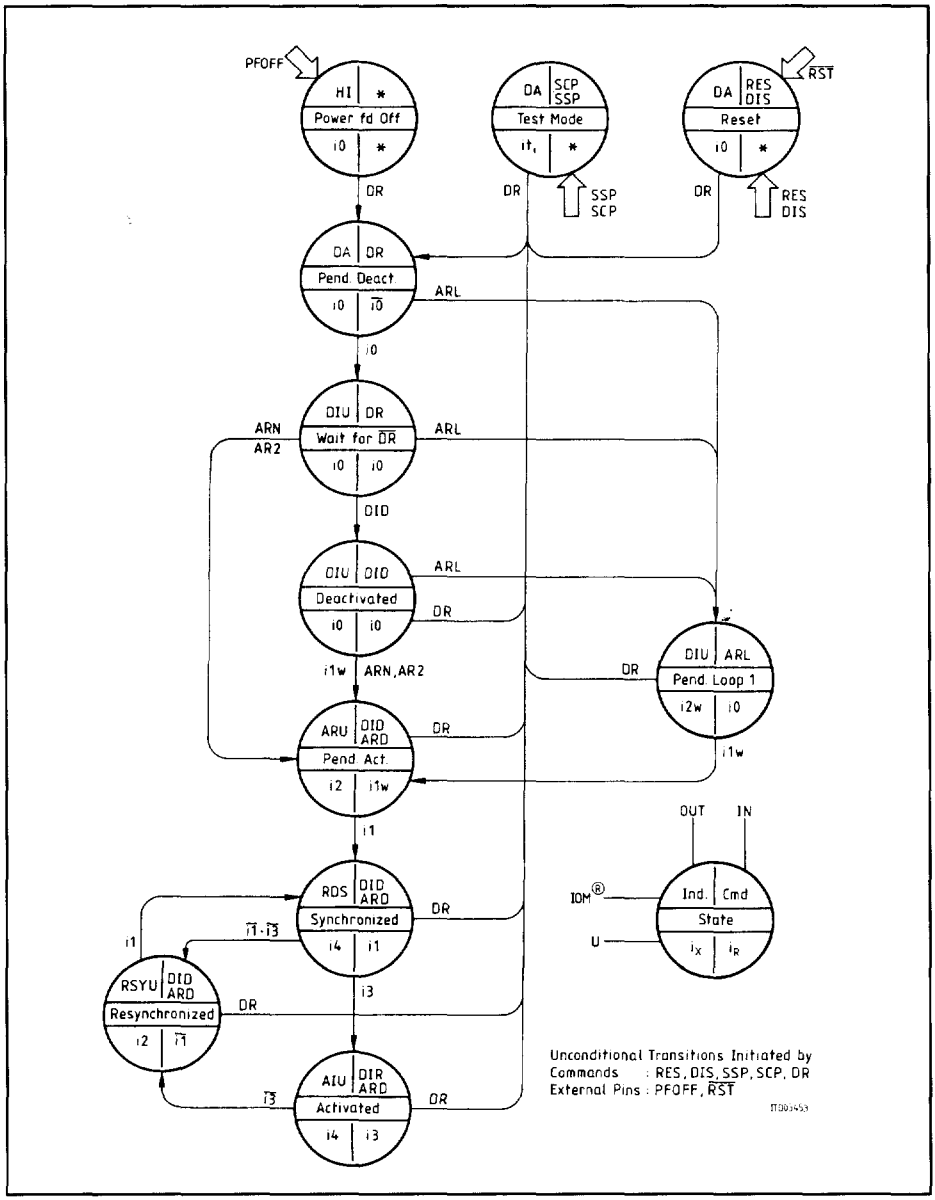


Figure 22
LT: State Diagram

4.3.2 Layer-1 Command/Indication Codes and State Diagrams in PT/TE-Modes

Command (upstream) PT/TE	Abbr.	Code	Remark
Timing	TIM	0000	Layer-2 device requires clocks to be activated
Activate Request No loop	ARN	1000	
Activate Request Local loop	ARL	1001	* Test loop 3 activation request
Activate Indication	AIN	1100	**
Deactivate Indication	DIU	1111	
Reset	RES	1101	Software Reset (x)
Send Single Pulses	SSP	0101	Ones (AMI pulses) transmitted at 2 kHz (TEST MODE 1) (x)
Send Continuous Pulses	SCP	0111	Ones (AMI pulses) transmitted at 192 kHz (TEST MODE 2) (x)
Indication (downstream) PT/TE	**Abbr.**	**Code**	**Remark**
Deactivate Request	DR	0000	
Power Up	PU	0111	
Resynchronisation	RSYD	0100	Lost Framing: receiver not synchronized with input
Activate Request No loop	ARN	1000	
Act. Request Local loop	ARL	1001	*
Activate Request loop 2	AR2	1010	
Act. Indication No loop	AIN	1100	
Act. Indication Local loop	AIL	1101	*Test loop 3 activated
Act. Indication loop 2	AI2	1110	
Testmode Acknowledge	TMA	0101	*
Deactivate Indication	DID	1111	

(x) unconditional commands

* only in TE
** only in PT

Unconditional States (TE):

Test Mode

This state results from the recognition of C/I commands SCP or SSP. After SCP continuous alternating pulses are outputted on the line (it_2); after SSP single alternating pulses are outputted (it_1) (see section 4.1.2 for the signal description). The burst mode is suspended during this mode and the test signal is sent continuously.

Reset

This state is entered after a RES (software reset) or after pin $\overline{RST}$ is brought low (hardware reset). Both the transmitter and the awake detector are disabled and activation from the LT is not possible.

Conditional States (TE):

Deactivated

This is the power down state of the physical protocol. The receive line awake unit is active. Clocks are disabled if $\overline{ENCK}$ = 1 . The power consumption in this state is cut to a minimum.

Power Up

This state is identical to the deactivated state except for the indication and the fact that the clocks are enabled regardless of the status of the $\overline{ENCK}$ pin. It is envoked by the TIM (0000) command and its significance will be explained further in section 4.4.

Note that MONITOR channel communication is not possible in this state.

Pending Activation

In response to an ARN command from the layer-2 device the TE initiates activation on the line by sending info 1w to the LT.

Level Detect

If the TE, in certain states, detects a signal on the line other than info 0, for longer than 1.5 ms, it enters this state. This happens if the LT initiates an activation of a deactivated link, or the TE itself has requested an activation and the LT has responded. In both cases, the TE must synchronize to the incoming signal and in the latter case the TE ceases transmitting info 1w to increase the quality of the incoming signal. After at most 80 ms, synchronization is achieved and info 2 is recognized.

Note that MONITOR channel communication is not possible in this state.

Synchronized

Detection of info 2 allows the TE to synchronize itself to the line. If the LT had initiated the activation it could request either normal activation (ARN) or activation of loop 2 at the TE (AR2). If the S-bit in the U-interface frame is set, then loop 2 is initiated at the TE; info 1 is transmitted on the U-interface and AR2 is sent to the layer-2 device. If the S-bit is zero, ordinary activation is initialized; info 1 is transmitted on the U-interface and ARN is sent to the layer-2 device.

Activation

Once the LT synchronizes to info 1 it sends info 4. Info 2 contains a code violation in the framing bit (F- bit) and info 4 does not. After detection of two frames without code violations in the F-bit, the TE concludes that info 4 is now being received and that the LT is synchronized. It then sends info 3. The exchange of info 3 and info 4 over the line constitutes as activated line and the IBC´s at either end are in the activated state. The indication downstream is AIN (activation indication normal) during normal activation and AIL (activation indication loop 2) during test loop 2 activation. If the TE looses synchronization to info 4 this state is left and the state corresponding to the signal it now receives is entered; if the TE recognizes info 2 it goes to the synchronized state (as with normal activation); if it recognizes a signal is present but can't identify it it goes to level detect; if it recognizes no signal present (info 0) it goes to "pending deactivation" and prepares to deactivate.

Pending Deactivation

If info 0 (no signal) is detected on the line once the activation process begins, the TE will enter this state and transmit info 0 itself. However it will only deactivate upon receipt of DIU from layer-2 device.

Pending Loop 3

Loop 3, the local TE-loop, is initialized after the layer-2 device issues an ARL command. If the IBC is in any other state except those associated with loop 2 (either loop 2 activated or loop 2 synchronized) ARL will cause the pending loop 3 state to be entered. In this state info 1 is not actually transmitted on the line but simply looped from the TE-transmitter back to the TE-receiver.

Loop 3 Synchronized

To enter the synchronized state in loop 3, the TE must synchronize to info 1 rather than info 2 as in normal operation. But as outlined in section info 2 and info 1 are structurally the same and hence the synchronization procedures can be considered equivalent. Info 3 is now transmitted and, as before, looped back to the receiver.

Loop 3 Activated

In this case info 3 is detected and activation is achieved. Loop 3 activation refers to a clear passage of info 3 between transmitter and receiver of the TE and is indicated by AIL to the layer-2 device. If however, a signal is detected on the line from the LT the indication changes to RSYD. The loop isn't broken but the change in indication allows higher software layers to decide whether the loop or the line signal is the more important.

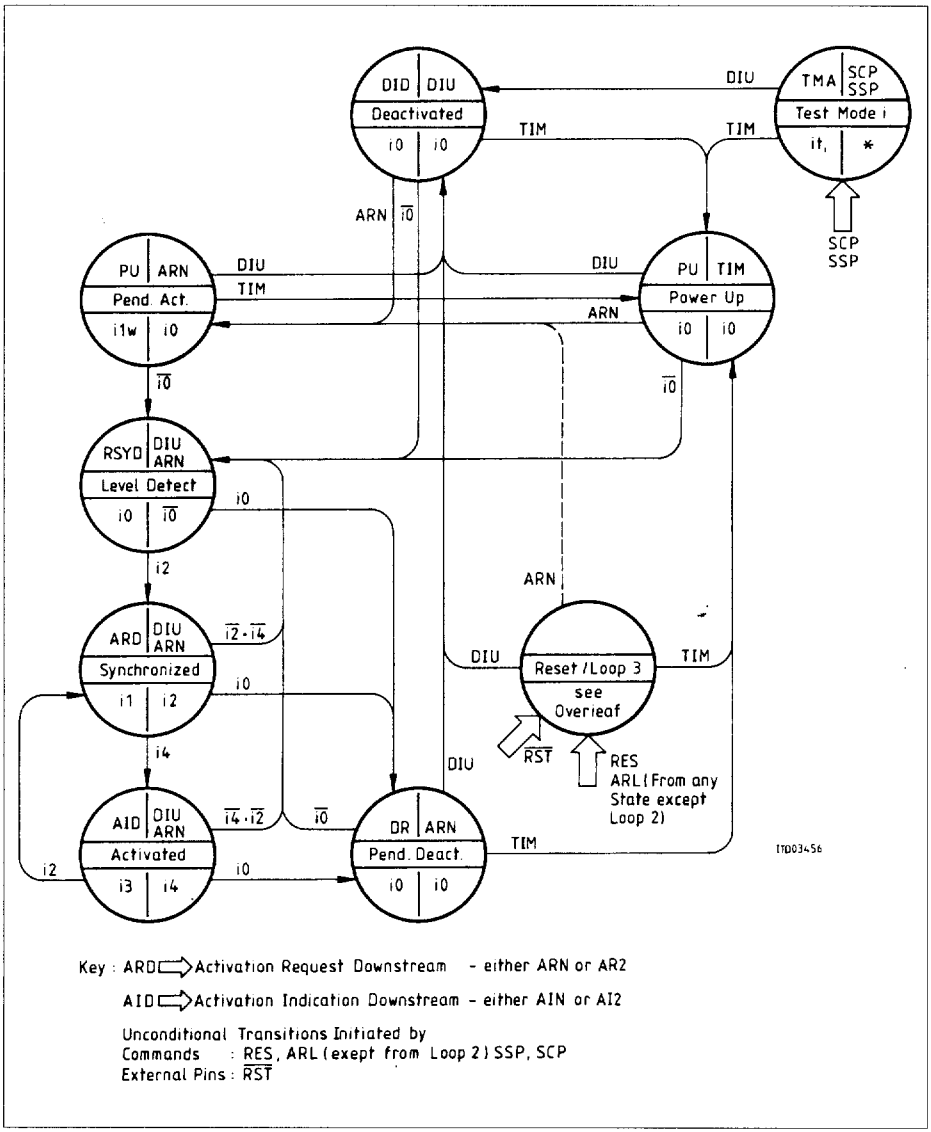


Figure 23
TE: State Diagram

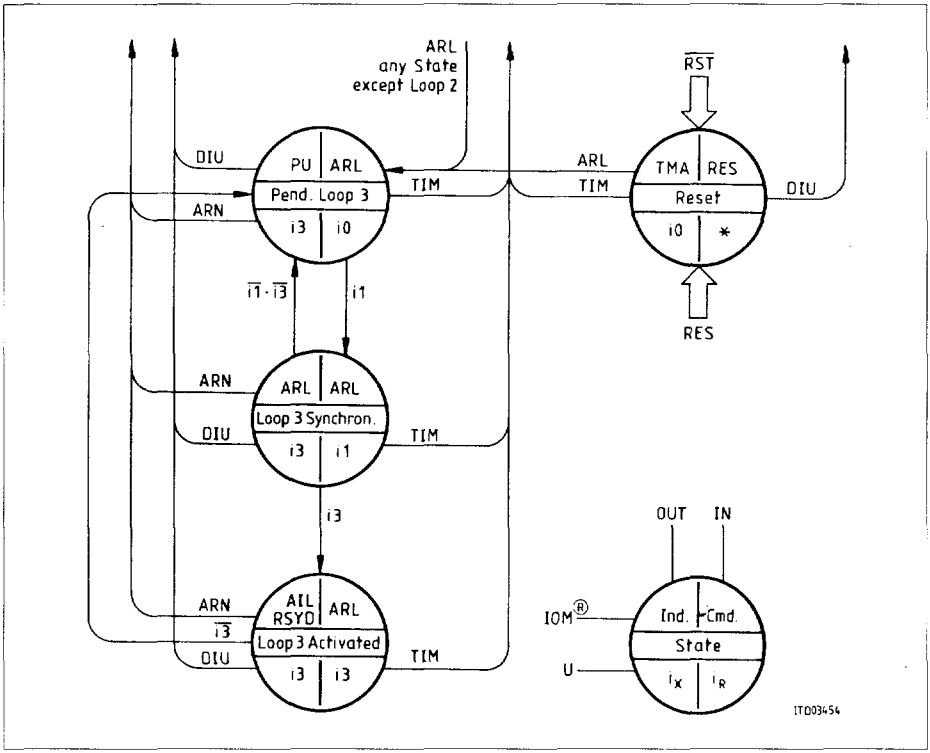


Figure 24
TE: State Diagram; Reset/Loop 3

Unconditional States (PT):

Reset

This state is entered unconditionally after a reset; this may be a software reset (RES) or a hardware reset applied to the $\overline{RST}$-pin.

Test Mode

The test signal (it_i) outputted to the interface in this state is dependent upon the command which originally invoked the state. SSP causes single alternating pulses to be transmitted (it_1); SCP causes continuous alternating pulses to be transmitted (it_2). During this state the test signal is transmitted continuously over the U-interface (burst mode is suspended).

Conditional States (PT):

Deactivated

The physical interface is in a low power state. The IOM-clocks are disabled (if ENCK = 1) and power consumption is cut to a minimum. The receive line awake detector unit is active.

Power Up

This state is identical to the deactivated state outlined above, except that the IOM-clocks are running and the power consumption is higher. This state is entered after the TIM-command (0000) has been recognized and the S-bus layer-1 device can now communicate with the IBC over the IOM-interface. This mechanism is described in section 4.4.

Note that MONITOR channel communication is not possible in this state.

Pending Activation

The reception of an ARN command indicates that a device on the S-bus wishes to activate the link to the LT. The PT passes this signal on to the LT in the form of info1w (awake signal).

Level Detect

When the LT responds to info 1w or when it wishes to activate the link of its own accord, it sends info 2. This is initially detected at the PT as simply a line signal. After 1.5 ms the PT goes to the level detect state and stops transmitting anything on the line (i.e. if it had been in pending activation). This allows it to synchronize to the incoming signal.

Note that MONITOR channel communication is not possible in this state.

Synchronized

Once the PT has identified the line signal as info 2 it is synchronized (this detection takes less than 80 ms). If the S-bit (service bit) in info 2 is set then the LT wants loop 2 activated as close as possible to the S-interface and hence not in the IBC (see section 4.1.1). The IBC simply passes this information on to the S-bus layer-1 device by sending indication AR2 (activation request loop 2) over the C/I-channel. If the S-bit in info 2 is zero then normal activation is assumed and the indication ARN (activation request no loop) is sent.

Wait for AIU

This state is entered upon receipt of info 4 from LT (implying that the LT has synchronized with info 1). Nothing new is outputted. The indication on the C/I-channel again depends on the S-bus state. The PT must wait for confirmation of S-bus activation before fully activating the interface. It must wait for AIU.

Activated

Confirmation of successful S-bus activation comes, in the form of an AIU command, from the S-bus layer-1 device. Only now will the PT-transmit info 3 to the LT, thereby activating the U-interface. An activation indication is sent downstream; either AIN, Activation Indication Noloop (S-bit of info 4 = 0) or AI2, Activation Indication Loop 2 (S-bit of info 4 = 1).

Pending Deactivation

If during an activation procedure the PT, for some reason, "looses" the info it has been receiving from the line, one of two things happen. If it detects that there is a signal still on the line but it doesn't recognize what it is, it returns to the level detect state. If it sees no signal at all, it then assumes info 0 is being transmitted and interprets this as a deactivation request. The pending deactivation state is entered and the S-bus layer-1 device is sent a deactivation request DR. The PT transmits info 0 on the line. Only a DIU-command from the SBC (indicating that the S-bus has been deactivated) will cause the PT to enter the deactivated state.

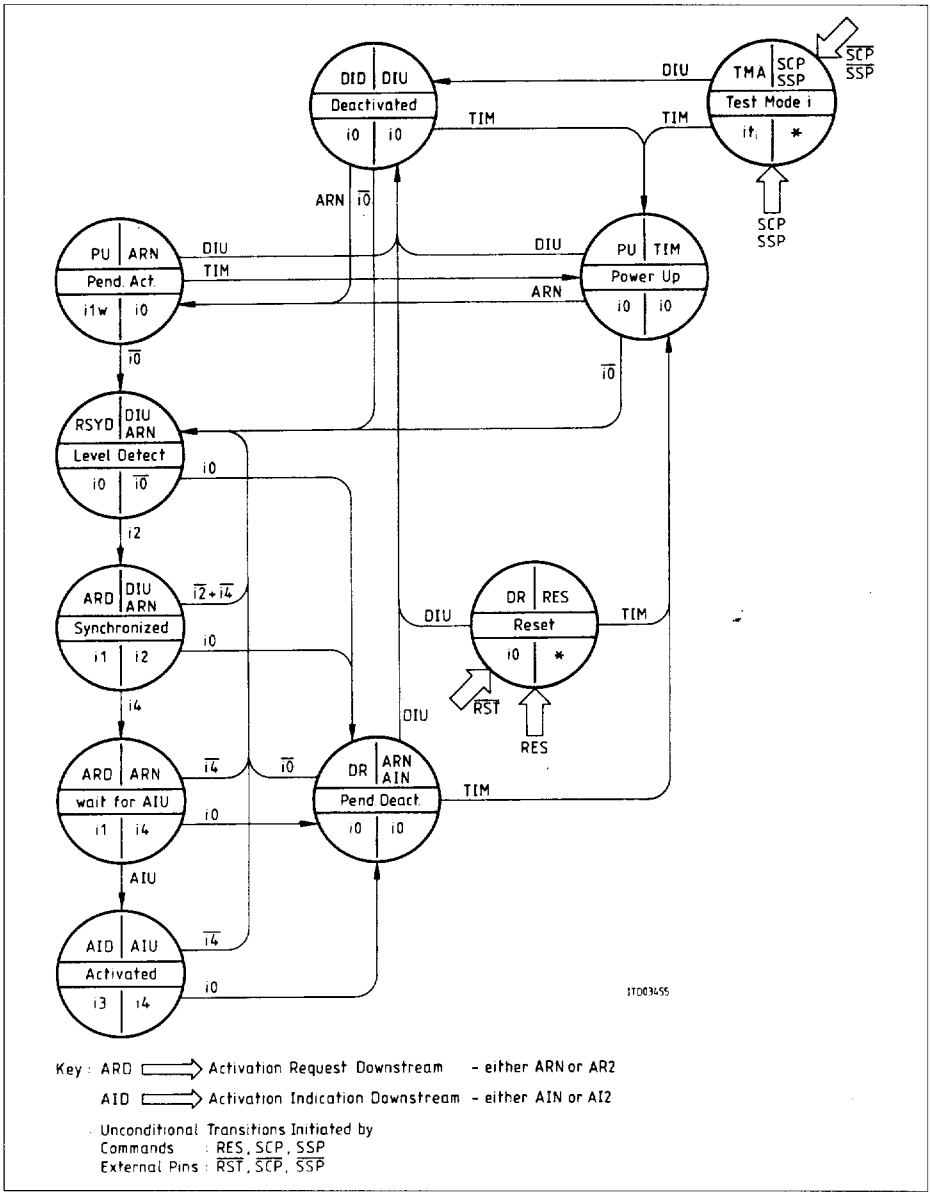


Figure 25
PT: State Diagram

4.4 Reset

In accordance with the state diagrams the reset state is entered unconditionally after either a software RES-command is received or after the $\overline{RST}$-pin is set to 0. After power up a reset should be applied to the IBC to bring it to a well-defined state.

In the LT-mode all outputs are high impedance during $\overline{RST}$ = 0. However the IOM-clocks must always be enabled.

In the TE/PT-modes $\overline{RST}$ acts with $\overline{ENCK}$ to give the following of states.

$\overline{RST}$	$\overline{ENCK}$	
0	1	Reset; Outputs high impedance
0	0	Reset; Outputs low impedance Clocks are running
1	1	Normal Operation; IOM-clocks disabled in deactivated state
1	0	Normal Operation; IOM-clocks not disabled in "deactivated" state

5 Description of MONITOR Commands and Registers

Besides the C/I-channel, inter-device communication on the IOM-interface is also possible via the MONITOR channel. However the MONITOR channel protocol is more straight-forward; the layer-2 device commands, the layer-1 device responds. Furthermore the monitor codes deal mainly with auxiliary tasks not directly related to the maintenance of the link. Finally they are totally under the control of the user and contain 17 NOP codes (00H and FXH). **Table 4** lists all IBC monitor codes.

Upon receipt of a message the IBC will send a response in the MONITOR channel. Availability of the response is indicated by setting the bit of the IOM-frame to zero. (IOM-1 or inverted modes) or by looping back the received MX-bit into the M) bit transmitted (IOM-2 mode).

The MONITOR channel is used to read the IBC internal registers (I(7:0) and R(7:0)) and to set or simply read the adaptive amplifier and equalizer settings. Note, however, that once both amplifier and equalizer coefficients have been set, the adaptive logic is turned off and the given settings remain constant regardless of any changes to the input signal.

However the coefficients are zeroed and hence must be reprogrammed after either:

- the device has been through the deactivated (power-down) state.
- a local loop has been implemented (i.e. loop 1 in LT-mode and loop 3 in TE-mode).

The adaptive logic is turned on again only after a hardware or software reset (coefficients again zeroed).

Merely reading the values however does not affect the adaptive nature of the settings.

To protect the chip from reading erroneous data from the MONITOR channel during the synchronization period, the MONITOR channel is ignored by the device during the following states:

- Power Up. TE- and PT-modes.
- Level Detect. TE-and PT-modes.
- Deactivated LT-modes.

5.1 IBC MONITOR Commands

Table 4

Message	Response	Exploration
00000000	-	NOP
1111XXXX	-	NOP
10000000	00111110	Identification
11101110	I(7:0)	Supply Current Equivalent
11101111	R(7:0)	Code Violation Register
00000010	1XX,A(6:2)	Gain Factor (part I)
00000011	1XX,C(2:0),A(1:0)	Equalizer coefficient and gain factor (part II)
001,A(6:2)	101,A(6:2)	External Programming of gain factor (part I)
010,C(2:0),A(1:0)	110,C(2:0),A(1:0)	Programming of gain factor (past II) and equalizer coefficient
011,CONF(4:0)	111,CONF(4:0)	Programming of Conf(4:0)

To implement any of the following integrated functions set the corresponding bit to 0 (reset values all high).

CONF4: TE-mode: clock output at pin X4 : 2.56 MHz (CONF4 = 1) or 7.68 MHz (CONF4 = 0)
LT-IOM-1 mode: programmable output X0

CONF3: Equalizer output signal at pin DISS

CONF2: Descrambler disable

CONF1: DC-balancing bit enable

CONF0: Amplifier gain modification during data transmission

Note

1. Messages are sent by the layer-2 device to the IBC (in the ICC by writing to the MONR-register).
2. Responses are sent by the IBC to the layer-2 device (in the ICC the MODE: HMD1 must be set to enable the ICC to read the incoming MONITOR byte).

5.2 I(7:0) Supply Current Equivalent Register

This register is only useful in the LT-mode when the power supply control functions are active. In this mode X3 functions as the MPF pin (Main Power Feed). Through this pin the 8-bit supply current equivalent from the local power supply can be read into the I(7:0) register. After reset I(7:0) = 00H.

5.3 R(7:0) Code Violation Register

This register counts the number of erroreous code violations in the data channels encountered by the RDS-function of the IBC and this information may be used by the software to estimate the bit error rate.

6 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4 V	V

Note:

Stresses above those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse (**figure 26**).

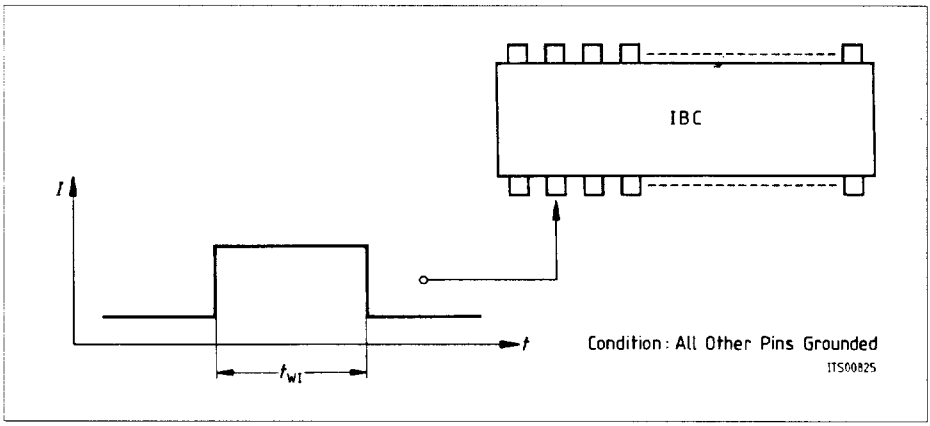


Figure 26
Test Condition for Maximum Input Current

The destruction limits are given in **figure 27**.
R_l 1 Ω.

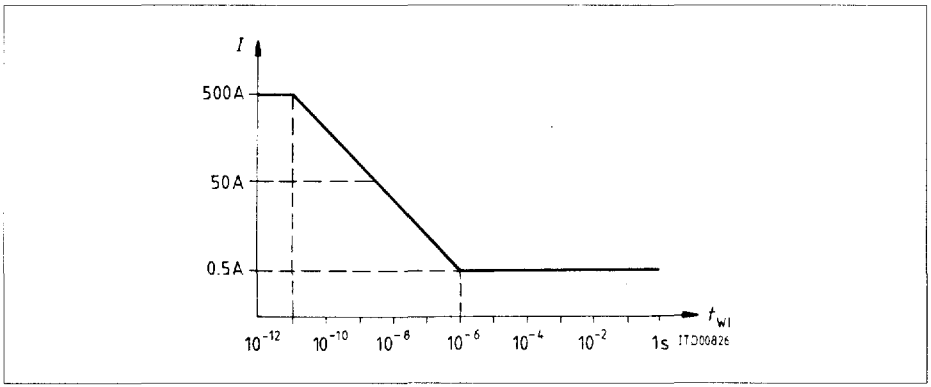


Figure 27
Transmitter Input Current

The destruction limits are given in **figure 28**.

R_l 250 Ω.

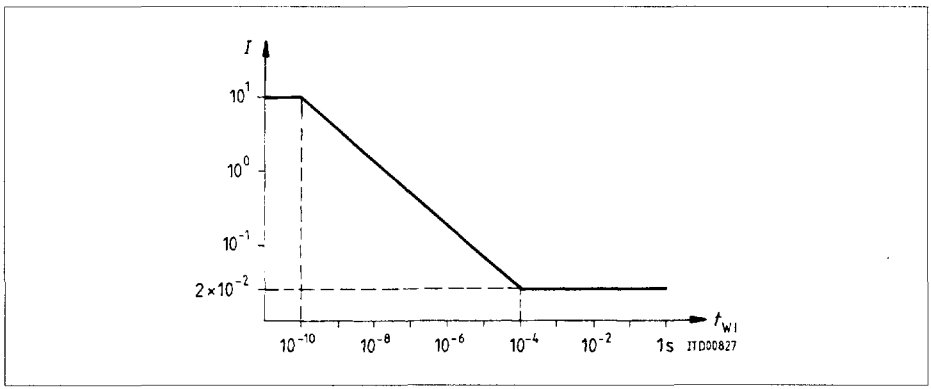


Figure 28
Receiver Input Current

DC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V

Parameter		Symbol	Limit Values		Unit	Test Condition	Remarks
			min.	max.			
L-input voltage		V_{IL}	V_{SS} − 0.4	0.8	V		
H-input voltage		V_{IH}	2.0	V_{DD} + 0.4	V		
L-output voltage [1] H-output voltage [2]		V_{OL1} V_{OL2}		0.45 0.45	V V	I_{OL} = 2 mA I_{OL} = 7 mA	All pins except L01,2 LI1 XTAL1 XTAL2
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 V_{DD} − 0.5		V V	I_{OH} = − 400 µA I_{OH} = − 200 µA	
Power supply current	operational	I_{CC}		20	mA	V_{DD} = 5 V, inputs at 0 V or V_{DD}, no output loads	
	power down	I_{CC}		2.5	mA		
Input leakage current		I_{LI}		10	µA	0 V < V_{IN} < V_{DD} to 0 V	
Output leakage current		I_{LO}		10	µA	0 V < V_{OUT} < V_{DD} to 0 V	
Absolute value of output pulse amplitude (V_{L01} - V_{L02})		V_X	4.75 − 5.25 0	5.25 − 4.75 0	V [3] V [4] V [5]		L01,2
Pulse width		P_W	1.22	1.38	s		
Transmitter output impedance		R_X	9	21	Ω		
L-input voltage H-input voltage		V_{IL} V_{IH}	V_{DD} − 0.5 V_{DD} − 0.5	0.5 0.5	V V		XTAL1
L-output voltage H-output voltage		V_{OL} V_{OH}	V_{DD} − 0.5 V_{DD} − 0.5	0.5 0.5	V V	I_O ≤ 100 µA C_L ≤ 100 pF	XTAL2

Notes:

[1] All outputs except SDO
[2] Output SDO only
[3] Positive pulse
[4] Negative pulse
[5] No pulse

Capacitances

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; V_{SSA} = 0 V, f_C = 1 MHz, unmeasured pins returned to ground

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input capacitance	C_{IN}		7	pF	
Output capacitance	C_{IO}		7	pF	
Output capacitance against V_{SSA}	C_{OUT}		10	pF	L01,2
Load capacitance	C_L		50	pF	XTAL1,2

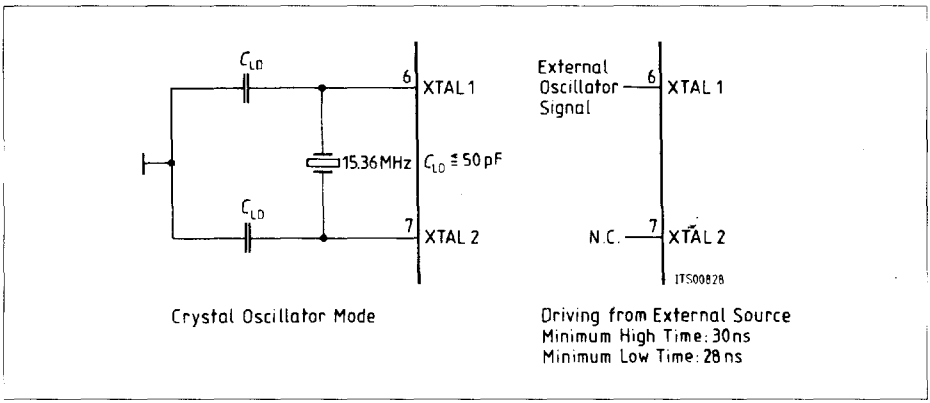


Figure 29
Recommended Oscillator Circuit

AC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %

Inputs are driven at 2.4 V for a logic "1" and at 0.4 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".

The AC testing input output waveforms are shown below.

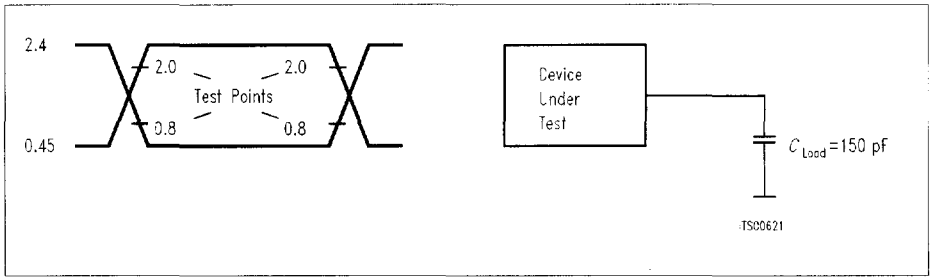


Figure 30
Input/Output Waveform for AC Tests

Figure 31 shows the relationship between the various clock outputs from the IBC. The crystal frequency is 15.36 MHz. All clock outputs have a duty cycle of 1:1 except 2.56 MHz (1:2). Note that the following are derived directly from the crystal oscillator: 15.36 MHz, 3.84 MHz and 2.56 MHz. They are not synchronized to the line. Their accuracy will be, to a first order, governed by the crystal accuracy (100 ppm maximum).

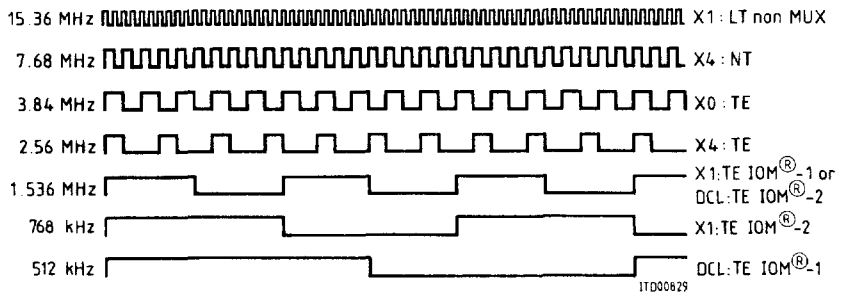


Figure 31
Output Clock Relationship

The following clocks are derived both from the crystal and, with the help of the DPLL, from the line; 7.68 MHz, 1.536 MHz, DCL and FSC. Synchronization may be regarded as a two stage process. Firstly, a synchronous 7.68-MHz signal is derived using the DPLL. Secondly, all other synchronous clocks are derived, by simple division, from 7.68 MHz synchronous. Because of the internal method of synchronization employed, the 7.68 MHz signal may "step forward or back" by 1 crystal period (**see figure 32**). Hence the period of 7.68 MHz, and all synchronous clocks derived from it, may vary by one crystal period (± 65 ns). This, to a first order, gives the accuracy of the various synchronous clocks. **Table 33** detail the accuracy of the clock outputs with respect to the symbols defined in **figure 5 to 9**.

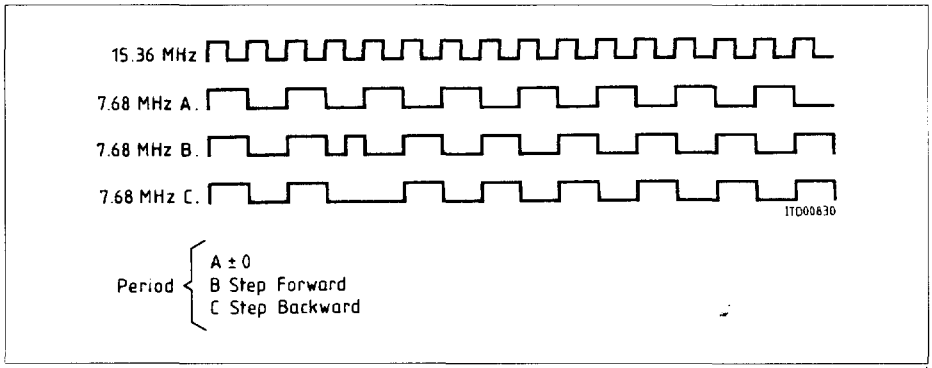


Figure 32
Possible 7.68-MHz Clocks

Timing Characteristics

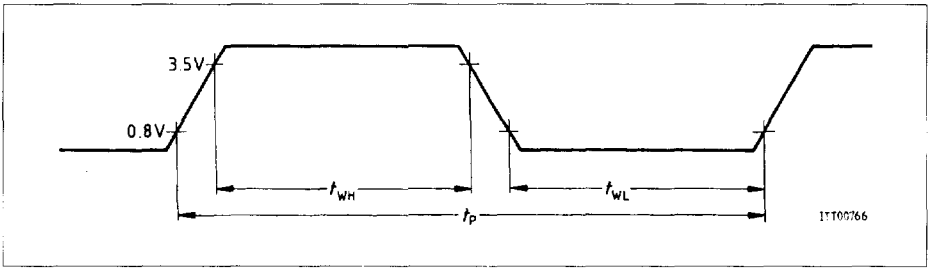


Figure 33
Clock Timing Symbols

Table 5
DCL Timing

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
TE/PT 512 kHz	t_P	1888	1953	2019	ns	Output
TE/PT 512 kHz	t_{WH}	944	977	1009	ns	
TE/PT 512 kHz	t_{WL}	944	977	1009	ns	
TE: 1.536 MHz	t_P	585	651	717	ns	
TE: 1.536 MHz	t_{WH}	260	326	391	ns	
TE: 1.536 MHz	t_{WL}	260	326	391	ns	
LT-mode	t_{WH}	90			ns	Input
LT-mode	t_{WL}	90			ns	

Table 6
FSC Timing

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
TE/PT 8 kHz 1:1	t_P	124.93	125	125.07	µs	Output
TE/PT 8 kHz 1:1	t_{WH}	62.46	62.5	62.54	µs	
TE/PT 8 kHz 1:1	t_{WL}	62.46	62.5	62.54	µs	
TE: 8 kHz 1:2	t_P	124.53	125	125.07	µs	
TE: 8 kHz 1:2	t_{WH}	41.6	41.67	42.74	µs	
TE: 8 kHz 1:2	t_{WL}	83.2	83.3	83.4	µs	
TE(SEL) 8 kHz 63:1	t_P	124.93	125	125.07	µs	Input
TE(SEL) 8 kHz 63:1	t_{WH}	122.08	123.05	124.02	µs	
TE(SEL) 8 kHz 63:1	t_{WL}	1888	1953	2019	ns	

Table 7
X4 Clock Timing

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
TE 2.56 MHz 1:2	t_P	– 100 ppm	390	+ 100 ppm	ns	OSC ± 100 ppm
TE 2.56 MHz 1:2	t_{WH}	– 100 ppm	130	+ 100 ppm	ns	OSC ± 100 ppm
TE 2.56 MHz 1:2	t_{WL}	– 100 ppm	260	+ 100 ppm	ns	OSC ± 100 ppm
PT 7.68 MHz 1:1	t_P	65	130	196	ns	
PT 7.68 MHz 1:1	t_{WH}	65	65	131	ns	
PT 7.68 MHz 1:1	t_{WL}	65	65	131	ns	

Table 8
X1 Clock Timing

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
TE: 1.536 MHz	t_P	585	651	717	ns	
TE: 1.536 MHz	t_{WH}	260	326	391	ns	
TE: 1.536 MHz	t_{WL}	260	326	391	ns	
TE: 768 kHz	t_P	1235	1302	1370	ns	
TE: 768 kHz	t_{WH}	585	651	717	ns	
TE: 768 kHz	t_{WL}	585	651	717	ns	
LT: 15.36 MHz	t_P	– 100	65.1	100	ns	OSC ± 100 ppm
LT: 15.36 MHz	t_{WH}	– 100	65.1	100	ns	OSC ± 100 ppm
LT: 15.36 MHz	t_{WL}	– 100	65.1	100	ns	OSC ± 100 ppm

Table 9
X0 Clock Timing

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
TE: 3.84 MHz	t_P	– 100	260	100	ns	OSC ± 100 ppm
TE: 3.84 MHz	t_{WH}	– 100	130	100	ns	OSC ± 100 ppm
TE: 3.84 MHz	t_{WL}	– 100	130	100	ns	OSC ± 100 ppm

Finally **table 10** defines the rise and fall times of DCL- and FSC-clocks in the various modes.

Table 10
DCL/FSC-Rise and Fall Timing

Parameter	Symbol	Limit Values			Unit	Mode
		min.	typ.	max.		
TRD; DCL rise time	t_r			50	ns	PT/TE
				60	ns	LT IOM-1
				25	ns	else
TFD; DCL fall time	t_f			50	ns	PT/TE
				60	ns	LT IOM-1
				25	ns	else
TFR; FSC rise time	t_r			50	ns	PT/TE
				60	ns	LT IOM-1
				50	ns	else
TFF; FSC fall time	t_f			50	ns	PT/TE
				60	ns	LT IOM-1
				50	ns	else

Timing Characteristics IOM®-Interface TE- and PT-Modes

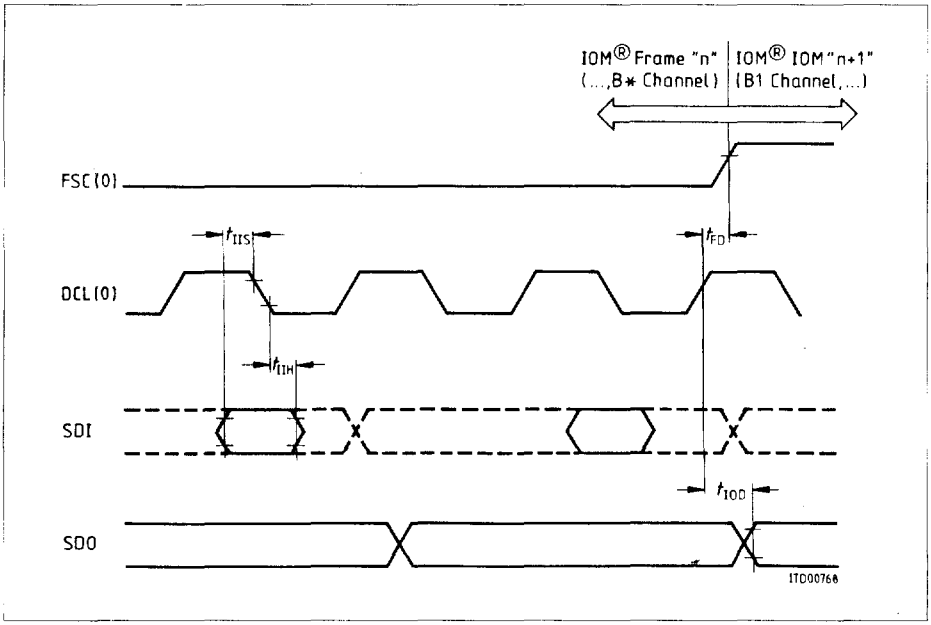


Figure 34
TE/PT IOM®-1 and IOM®-2 Mode Timing Diagram

Table 11
TE/PT Mode Timing (IOM®-1 and IOM®-2 Mode)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	typ.		
Frame sync. delay	t_{FD}	– 20	20	ns	C_L = 100 pF
IOM output data delay	t_{IOD}		200	ns	C_L = 100 pF
IOM input data setup	t_{IIS}	20		ns	
IOM input data hold	t_{IIH}	50		ns	

TE-Inverted Mode

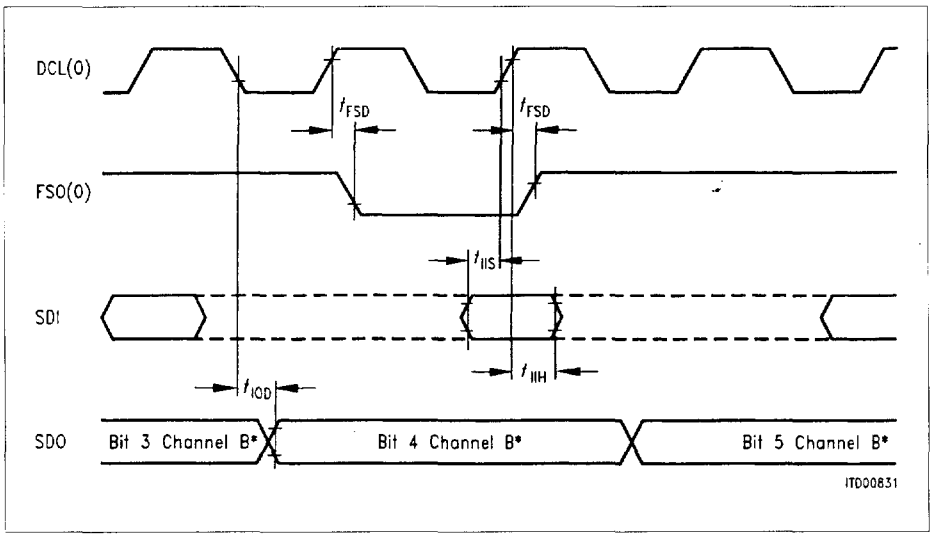


Figure 35
Inverted TE-Mode Timing Diagram

Inverted TE-Mode Timing

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	typ.		
Frame sync. delay	t_{FSD}	– 20	20	ns	C_L = 100 pF
IOM data output delay	t_{IOD}		200	ns	C_L = 100 pF
IOM input data setup	t_{IIS}	20		ns	
IOM input data hold	t_{IIH}	50		ns	

Timing Characteristics IOM®-Interface LT-Modes

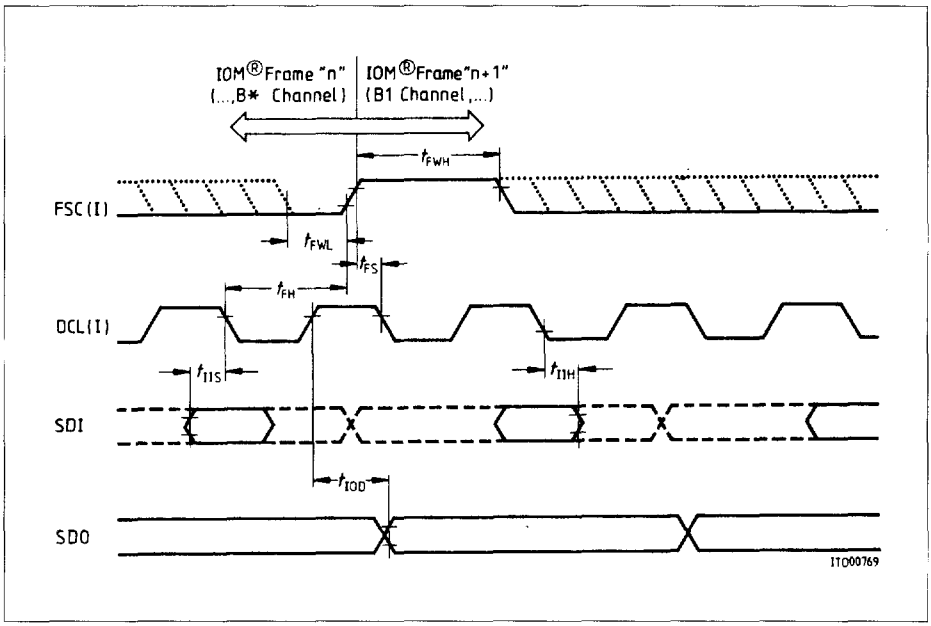


Figure 36
LT-IOM®-1 and IOM®-2 Mode Timing Diagram

LT-IOM®-1 and IOM®-2 Mode Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync hold	t_{FH}	50		ns
Frame sync setup	t_{FS}	30		ns
Frame sync high	t_{FWH}	80		ns
Frame sync low	t_{FWL}	2150		ns
IOM output data delay	t_{IOD}		200	ns
IOM input data setup	t_{IIS}	20		ns
IOM input data hold	t_{IIH}	50		ns

LT-Inverted Mode

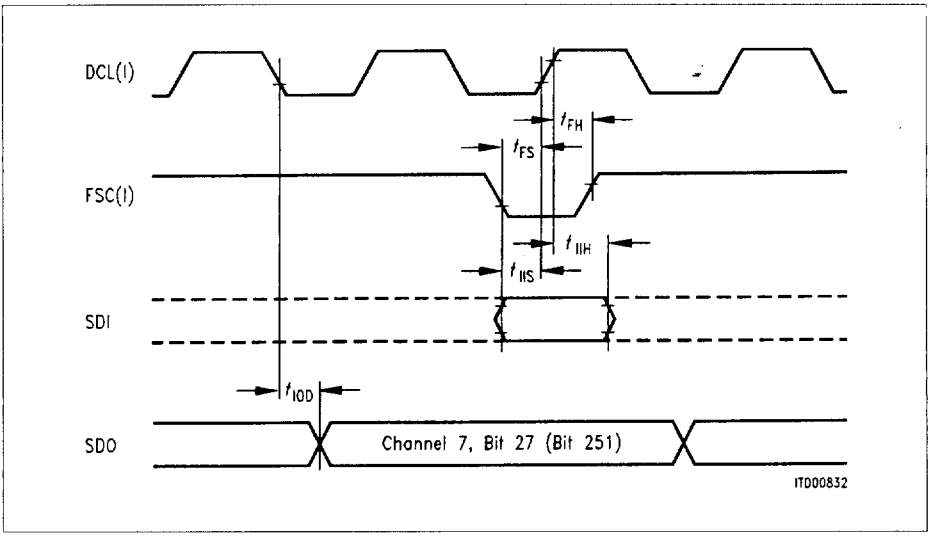


Figure 37
LT-Inverted Mode Timing Diagram

LT-Inverted Mode Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync hold	t_{FH}	50		ns
Frame sync setup	t_{FS}	20		ns
Frame sync high	t_{FH}	124.8		µs
Frame sync low	t_{EL}	70	200	ns
IOM output data delay	t_{IOM}		200	ns
IOM input data setup	t_{IIS}	20		ns
IOM input data hold	t_{IIH}	50		ns

Receiver Stage Properties

Input Stage / Measured Property		dB
Line amplifier	– dynamic range – resolution (128 setting)	0 - 30 0.236
Anti-aliasing filter and low pass filters		
> 1.1 MHz	– minimum attenuation	30
> 1.1 MHz	– typical attenuation	35
Equalizer	– dynamic range – resolution (8 settings)	0 - 15.36 dB 2.194

7 Appendix

Appendix A

Features	Version	
	A4	**A5**
IOM-2 interface timing	TE: 1.536 MHz DCL LT: 4.096 MHz DCL	TE: 1.536 MHz DCL LT: 4.096 MHz DCL
IOM-2 MONITOR handling	No	Yes
DC balancing bit	No	Yes
Reset condition of pin DISS	commands RES or DR	command RES
TE IOM-2 mode power down	clocks disabled at the end of C/I-channel 1	clocks disabled at the end of C/I-channel 0
Pin X4/TE	2.56 MHz	2.56 MHz for CONF4 = 1 7.68 MHz for CONF4 = 0

Appendix B

PEB 2095 (IBC), Version A5

Based on a single site system evaluation of the transmission performance of the PEB 2095 IBC, the full spec performance (10 µV/ Hz noise superimposed) is not reached.

The performance of the current design is as follows:

0.6 mm diameter cable; 45 nF/km capacitance:

No errors with 10 µV/ Hz up to 3km

No errors with 8 µV/ Hz from 3 to 3.5km

0.6 mm diameter cable; 120 nF/km capacitance:

No errors with 10 µV/ Hz up to 1.8km

No errors with 8 µV/ Hz from 1.8 to 2.1km

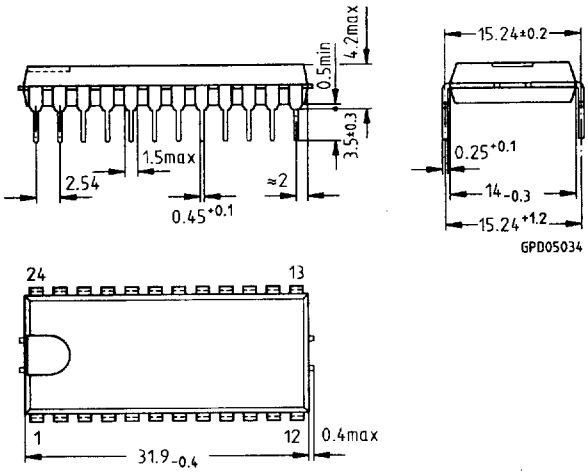
0.4 mm diameter cable; 45 nF/km capacitance:

No errors with 10 µV/ Hz up to 2km

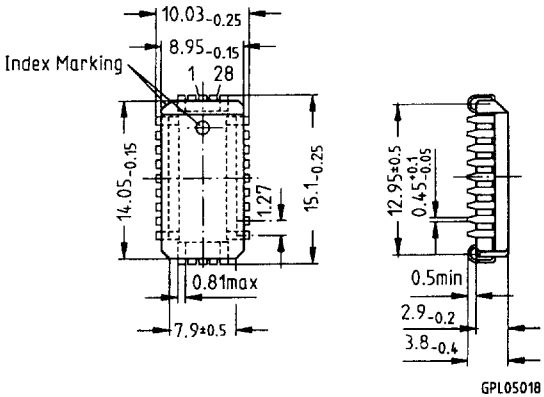
No errors with 4 µV/ Hz from 2 to 2.8km

8 Package Outlines

Plastic Dual-in-Line Package, P-DIP-24



Plastic-Leaded Chip Carrier, P-LCC-28-R (SMD)



SMD = Surface Mounted

Dimensions in mm

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Analog Telephone Sets	B115-H6244-X-X-7400	10.-
Benutzer-Handbuch / User's Manual		
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