The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

For More Information

Please contact your local sales office for additional information about Cypress products and solutions.

About Cypress

Cypress is the leader in advanced embedded system solutions for the world's most innovative automotive, industrial, smart home appliances, consumer electronics and medical products. Cypress' microcontrollers, analog ICs, wireless and USB-based connectivity solutions and reliable, high-performance memories help engineers design differentiated products and get them to market first. Cypress is committed to providing customers with the best support and development resources on the planet enabling them to disrupt markets by creating new product categories in record time. To learn more, go to www.cypress.com.

MB95650L Series

New 8FX 8-bit Microcontrollers

The MB95650L Series is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral functions.

Features

F²MC-8FX CPU core

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

Clock

- Selectable main clock source
  - Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
  - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
  - Main CR clock (4 MHz ±2%)
  - Main CR PLL clock
    - The main CR PLL clock frequency becomes 8 MHz ±2% when the PLL multiplication rate is 2.
    - The main CR PLL clock frequency becomes 10 MHz ±2% when the PLL multiplication rate is 2.5.
    - The main CR PLL clock frequency becomes 12 MHz ±2% when the PLL multiplication rate is 3.
    - The main CR PLL clock frequency becomes 16 MHz ±2% when the PLL multiplication rate is 4.
  - Main PLL clock (maximum machine clock frequency: 16 MHz)
- Selectable subclock source
  - Suboscillation clock (32.768 kHz)
  - External clock (32.768 kHz)
  - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)

Timer

- 8/16-bit composite timer × 2 channels
- Time-base timer × 1 channel
- Watch prescaler × 1 channel

UART/SIO × 1 channel (The channel can be used either as a UART/SIO channel or as an I²C bus interface channel.)

- The function of this channel can be switched between UART/SIO and I²C bus interface.
- Full duplex double buffer
- Capable of clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer

I²C bus interface × 2 channels (One of the two channels can be used either as an I²C bus interface channel or as a UART/SIO channel.)

- Supports Standard-mode and Fast-mode (400 kHz).
- Built-in wake-up function

LIN-UART

- Full duplex double buffer
- Capable of clock asynchronous serial data transfer and clock synchronous serial data transfer

External interrupt × 6 channels

- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes

8/12-bit A/D converter × 6 channels

8-bit or 12-bit resolution can be selected.

Low power consumption (standby) modes

There are four standby modes as follows:

- Stop mode
- Sleep mode
- Watch mode
- Time-base timer mode

I/O port

- MB95F652E/F653E/F654E/F656E (number of I/O ports: 21)
  - General-purpose I/O ports (CMOS I/O) : 17
  - General-purpose I/O ports (N-ch open drain) : 4
- MB95F652L/F653L/F654L/F656L (number of I/O ports: 20)
  - General-purpose I/O ports (CMOS I/O) : 17
  - General-purpose I/O ports (N-ch open drain) : 3

On-chip debug

- 1-wire serial control
- Serial writing supported (asynchronous mode)

Hardware/software watchdog timer

- Built-in hardware watchdog timer
- Built-in software watchdog timer

Power-on reset

A power-on reset is generated when the power is switched on.

Low-voltage detection reset circuit and low-voltage detection interrupt circuit (only available on MB95F652E/F653E/F654E/F656E)

Built-in low-voltage detection function

Clock supervisor counter

Built-in clock supervisor counter

Dual operation Flash memory

The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

Flash memory security function

Protects the content of the Flash memory.

Contents

1. Product Line-up

Part number / Parameter	MB95F652E	MB95F653E	MB95F654E	MB95F656E	MB95F652L	MB95F653L	MB95F654L	MB95F656L
Type	Flash memory product							
Clock supervisor counter	It supervises the main clock oscillation and the subclock oscillation.							
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	36 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte	36 Kbyte
RAM capacity	256 bytes	512 bytes	1024 bytes	1024 bytes	256 bytes	512 bytes	1024 bytes	1024 bytes
Power-on reset	Yes							
Low-voltage detection reset	Yes				No			
Reset input	Selected through software				With dedicated reset input			
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)							
General-purpose I/O	• I/O port : 21 • CMOS I/O : 17 • N-ch open drain : 4				• I/O port : 20 • CMOS I/O : 17 • N-ch open drain : 3			
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)							
Hardware/software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the software watchdog timer.							
Wild register	It can be used to replace 3 bytes of data.							
LIN-UART	• A wide range of communication speed can be selected by a dedicated reload timer. • It has a full duplex double buffer. • Both clock synchronous serial data transfer and clock asynchronous serial data transfer are enabled. • The LIN function can be used as a LIN master or a LIN slave.							
8/12-bit A/D converter	6 channels							
	8-bit or 12-bit resolution can be selected.							
8/16-bit composite timer	2 channels							
	• The timer can be configured as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.							
External interrupt	6 channels							
	• Interrupt by edge detection (The rising edge, falling edge, and both edges can be selected.) • It can be used to wake up the device from different standby modes.							
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).							

(Continued)

(Continued)

<table>
<tr><th>Part number
Parameter</th><th>MB95F652E</th><th>MB95F653E</th><th>MB95F654E</th><th>MB95F656E</th><th>MB95F652L</th><th>MB95F653L</th><th>MB95F654L</th><th>MB95F656L</th></tr>
<tr><td rowspan="2">UART/SIO</td><td colspan="8">1 channel (The channel can be used either as a UART/SIO channel or as an I²C bus interface channel.)</td></tr>
<tr><td colspan="8">• Data transfer with UART/SIO is enabled.
• It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function.
• It uses the NRZ type transfer format.
• LSB-first data transfer and MSB-first data transfer are available to use.
• Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.</td></tr>
<tr><td rowspan="2">I²C bus interface</td><td colspan="8">2 channels (One of the two channels can be used either as an I²C bus interface channel or as a UART/SIO channel.)</td></tr>
<tr><td colspan="8">• Master/slave transmission and reception
• It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.</td></tr>
<tr><td>Watch prescaler</td><td colspan="8">Eight different time intervals can be selected.</td></tr>
<tr><td>Flash memory</td><td colspan="8">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.
• It has a flag indicating the completion of the operation of Embedded Algorithm.
• Flash security feature for protecting the content of the Flash memory
<table>
<tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr>
<tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr>
</table></td></tr>
<tr><td>Standby mode</td><td colspan="8">There are four standby modes as follows:
• Stop mode
• Sleep mode
• Watch mode
• Time-base timer mode</td></tr>
<tr><td>Package</td><td colspan="8">FPT-24P-M10
FPT-24P-M34
LCC-32P-M19</td></tr>
</table>

2. Packages and Corresponding Products

Part number / Package	MB95F652E	MB95F653E	MB95F654E	MB95F656E	MB95F652L	MB95F653L	MB95F654L	MB95F656L
FPT-24P-M10	O	O	O	O	O	O	O	O
FPT-24P-M34	O	O	O	O	O	O	O	O
LCC-32P-M19	O	O	O	O	O	O	O	O

O: Available

3. Differences among Products and Notes on Product Selection

Current consumption

When using the on-chip debug function, take account of the current consumption of Flash memory program/erase.

For details of current consumption, see “18. Electrical Characteristics”.

Package

For details of information on each package, see “2. Packages and Corresponding Products” and “22. Package Dimension”.

Operating voltage

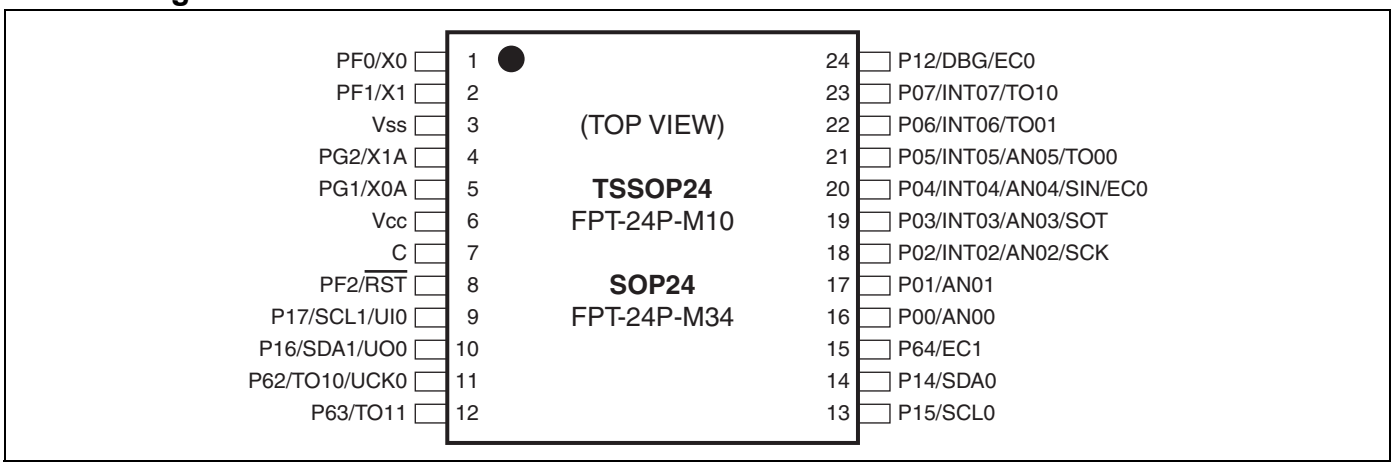
The operating voltage varies, depending on whether the on-chip debug function is used or not.

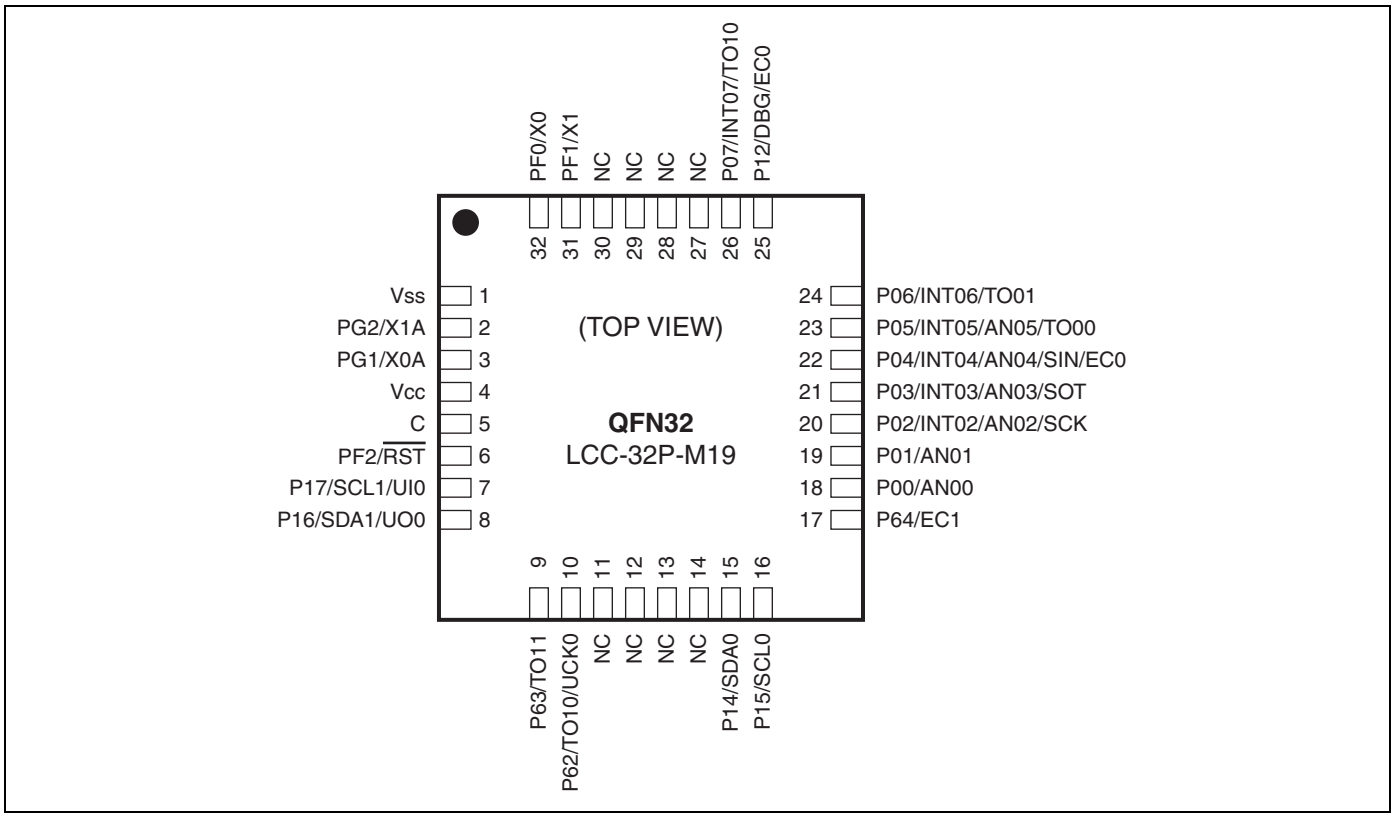
For details of operating voltage, see “18. Electrical Characteristics”.

On-chip debug function

The on-chip debug function requires that V_{CC}, V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “Chapter 20 Example Of Serial Programming Connection” in “New 8FX MB95650L Series Hardware Manual”.

4. Pin Assignment





5. Pin Functions

Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
SOP24*1, TSSOP24*2	QFN32*3				Input	Output	OD*5	PU*6
1	32	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X0		Main clock input oscillation pin				
2	31	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X1		Main clock I/O oscillation pin				
3	1	V_{SS}	—	Power supply pin (GND)	—	—	—	—
4	2	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
		X1A		Subclock I/O oscillation pin				
5	3	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
		X0A		Subclock input oscillation pin				
6	4	V_{CC}	—	Power supply pin	—	—	—	—
7	5	C	—	Decoupling capacitor connection pin	—	—	—	—
8	6	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
		$\overline{RST}$		Reset pin Dedicated reset pin on MB95F652L/F653L/F654L/F656L				
9	7	P17	J	General-purpose I/O port	CMOS	CMOS	—/O*7	—
		SCL1		I^2C bus interface ch. 1 clock I/O pin				
		UI0		UART/SIO ch. 0 data input pin				
10	8	P16	J	General-purpose I/O port	CMOS	CMOS	—/O*7	—
		SDA1		I^2C bus interface ch. 1 data I/O pin				
		UO0		UART/SIO ch. 0 data output pin				
11	10	P62	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		TO10		8/16-bit composite timer ch. 1 output pin				
		UCK0		UART/SIO ch. 0 clock I/O pin				
12	9	P63	D	General-purpose I/O port High-current output	Hysteresis	CMOS	—	O
		TO11		8/16-bit composite timer ch. 1 output pin				
13	16	P15	I	General-purpose I/O port	CMOS	CMOS	O	—
		SCL0		I^2C bus interface ch. 0 clock I/O pin				
14	15	P14	I	General-purpose I/O port	CMOS	CMOS	O	—
		SDA0		I^2C bus interface ch. 0 data I/O pin				
15	17	P64	D	General-purpose I/O port	Hysteresis	CMOS	—	O
		EC1		8/16-bit composite timer ch. 1 clock input pin				

(Continued)

Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
SOP24*1, TSSOP24*2	QFN32*3				Input	Output	OD*5	PU*6
16	18	P00	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		AN00		8/12-bit A/D converter analog input pin				
17	18	P01	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		AN01		8/12-bit A/D converter analog input pin				
18	20	P02	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT02		External interrupt input pin				
		AN02		8/12-bit A/D converter analog input pin				
		SCK		LIN-UART clock I/O pin				
19	21	P03	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT03		External interrupt input pin				
		AN03		8/12-bit A/D converter analog input pin				
		SOT		LIN-UART data output pin				
20	22	P04	F	General-purpose I/O port	CMOS/ analog	CMOS	—	O
		INT04		External interrupt input pin				
		AN04		8/12-bit A/D converter analog input pin				
		SIN		LIN-UART data input pin				
		EC0		8/16-bit composite timer ch. 0 clock input pin				
21	23	P05	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
		INT05		External interrupt input pin				
		AN05		8/12-bit A/D converter analog input pin				
		TO00		8/16-bit composite timer ch. 0 output pin				
22	24	P06	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		INT06		External interrupt input pin				
		TO01		8/16-bit composite timer ch. 0 output pin				
23	26	P07	K	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		INT07		External interrupt input pin				
		TO10		8/16-bit composite timer ch. 1 output pin				

(Continued)

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Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
SOP24*1, TSSOP24*2	QFN32*3				Input	Output	OD*5	PU*6
24	25	P12	H	General-purpose I/O port	Hysteresis	CMOS	O	—
		DBG		DBG input pin				
		EC0		8/16-bit composite timer ch. 0 clock input pin				
—	11	NC	—	It is an internally connected pin. Always leave it unconnected.	—	—	—	—
	12							
	13							
	14							
	27							
	28							
	29							
	30							

O: Available

*1: FPT-24P-M34

*2: FPT-24P-M10

*3: LCC-32P-M19

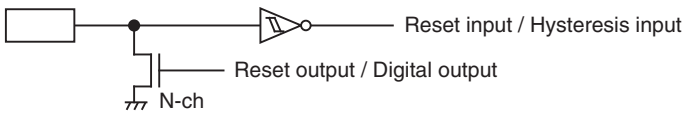
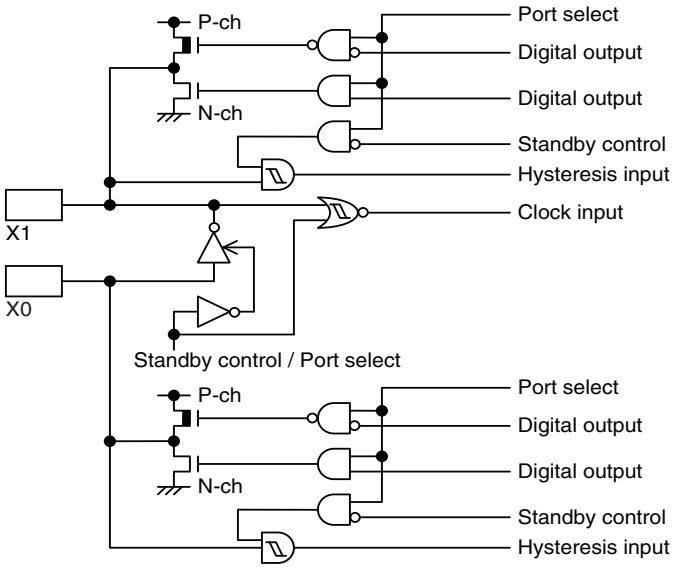
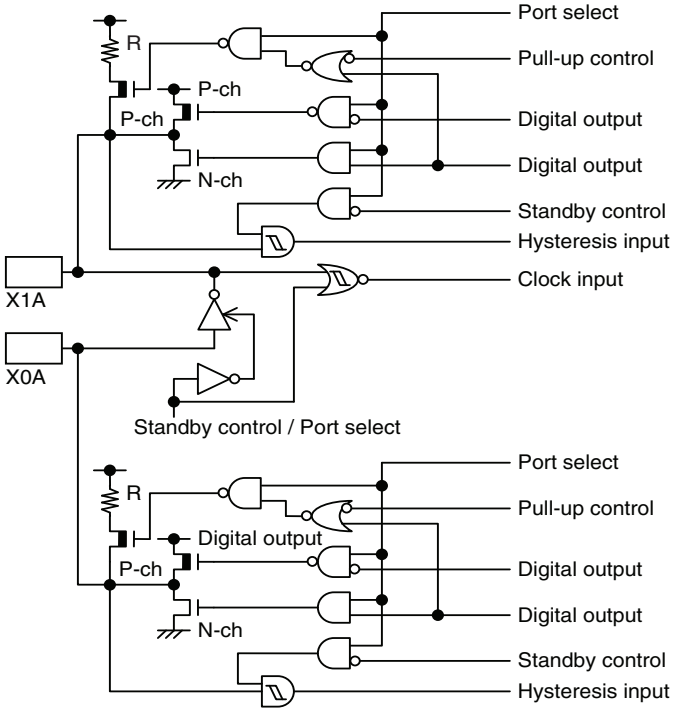
*4: For the I/O circuit types, see “6. I/O Circuit Type”.

*5: N-ch open drain

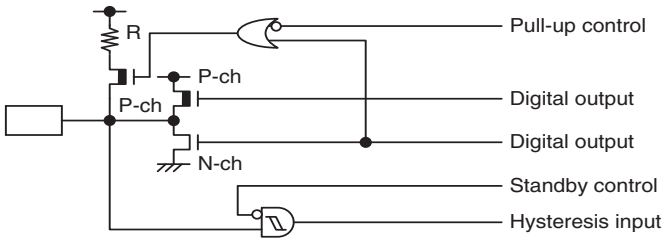
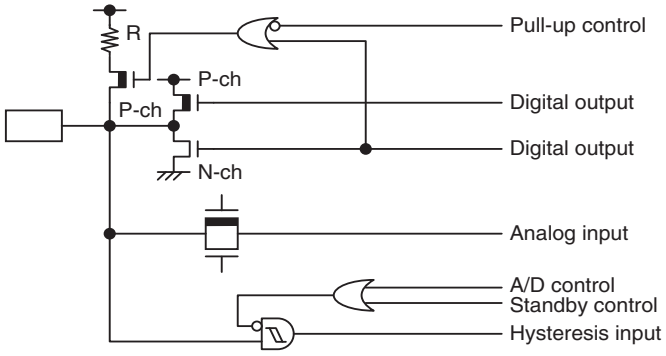
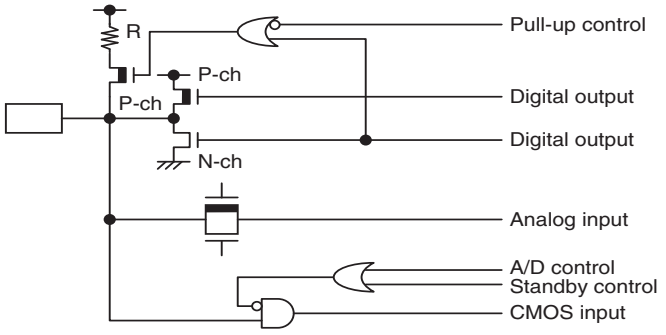
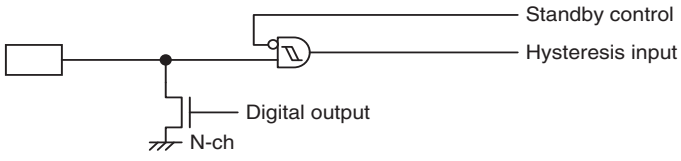
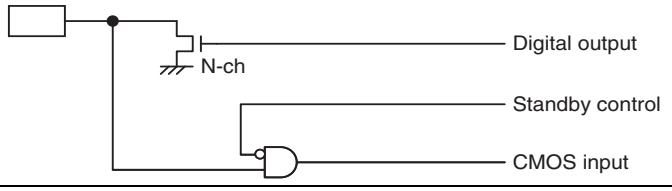
*6: Pull-up

*7: In I^2C mode, the pin becomes an N-ch open drain pin.

6. I/O Circuit Type

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx. 5 MΩ • CMOS output • Hysteresis input • Pull-up control

(Continued)

Type	Circuit	Remarks
D		• CMOS output • Hysteresis input • Pull-up control • High current output
E		• CMOS output • Hysteresis input • Pull-up control • Analog input
F		• CMOS output • CMOS input • Pull-up control • Analog input
H		• N-ch open drain output • Hysteresis input
I		• N-ch open drain output • CMOS input

(Continued)

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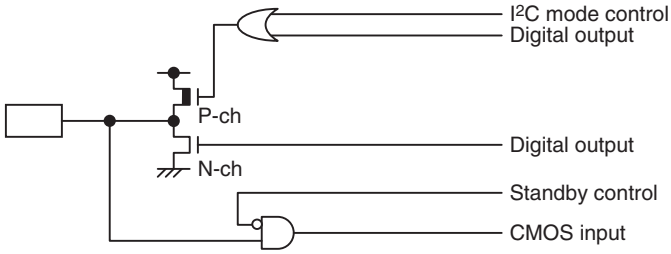
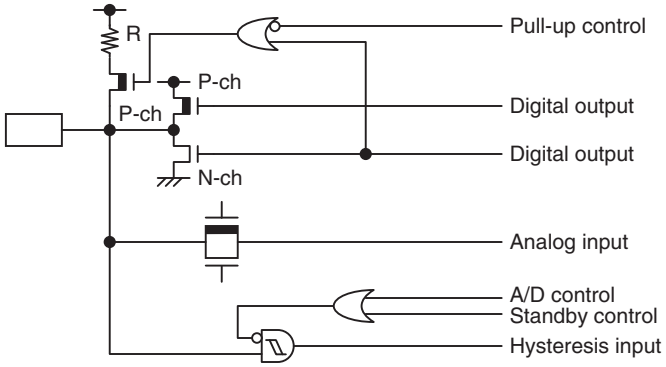
Type	Circuit	Remarks
J		• CMOS output • CMOS input • N-ch open drain output in I2C mode
K		• CMOS output • Hysteresis input • Pull-up control • Analog input • High current output

7. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

7.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

   Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

7.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%.
   Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

7.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

8. Notes On Device Handling

Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in “18.1 Absolute Maximum Ratings” of “18. Electrical Characteristics” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

9. Pin Connection

Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 1.0 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

DBG pin

Connect the DBG pin to an external pull-up resistor of 2 kΩ or above.

After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released.

The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

$\overline{\text{RST}}$ pin

Connect the $\overline{\text{RST}}$ pin to an external pull-up resistor of 2 kΩ or above.

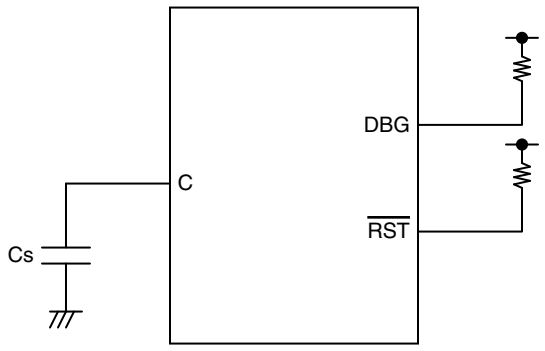
To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the $\overline{\text{RST}}$ pin and that between a pull-up resistor and the V_{CC} pin when designing the layout of the printed circuit board.

The PF2/$\overline{\text{RST}}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{\text{RST}}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

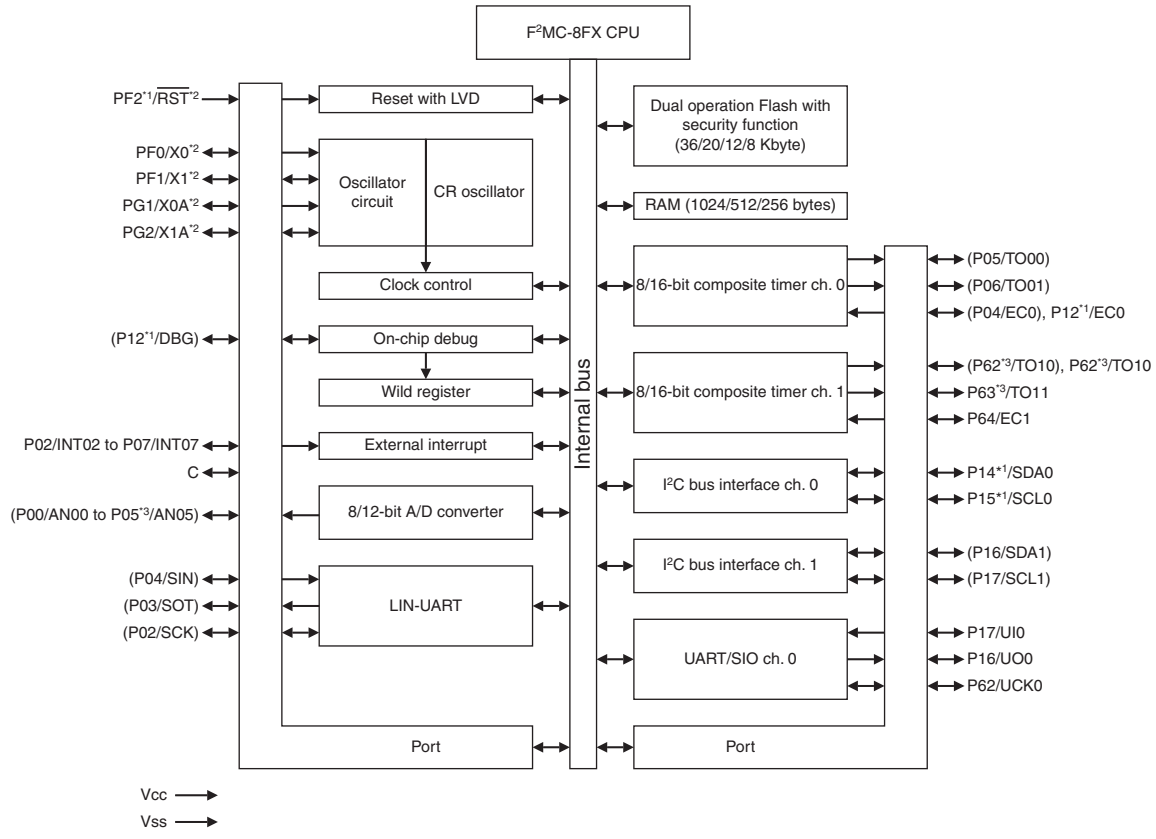
DBG/$\overline{\text{RST}}$/C pins connection diagram



Note on serial communication

In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, take measures such as adding a checksum to the end of data in order to detect errors. If an error is detected, retransmit the data.

10. Block Diagram



*1: P12, P14, P15 and PF2 are N-ch open drain pins.
*2: Software select
*3: P05 to P07, P62 and P63 are high-current pins.

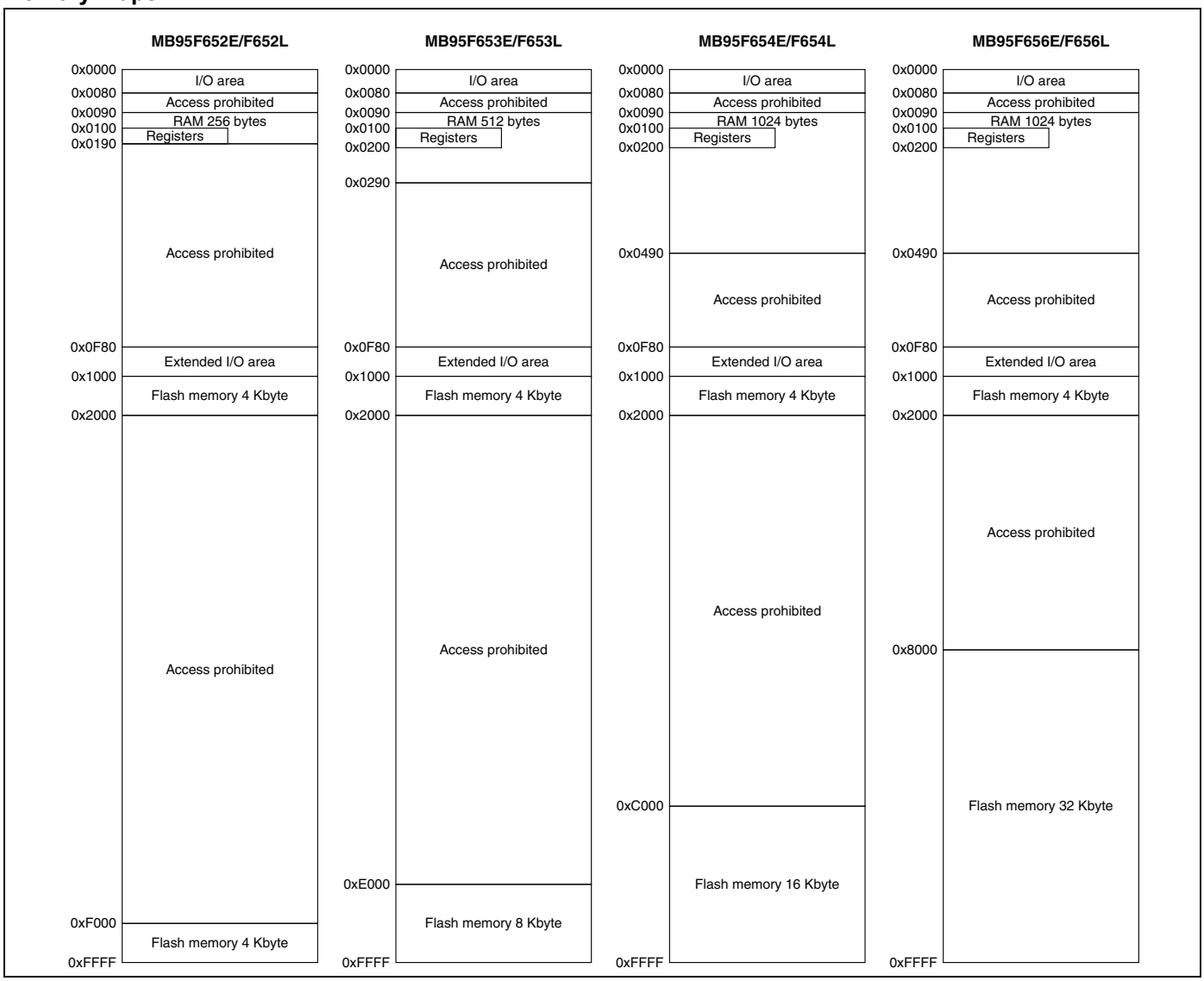
Note: Pins in parentheses indicate that those pins are shared among different peripheral functions.

11. CPU Core

Memory space

The memory space of the MB95650L Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95650L Series are shown below.

Memory maps



12. Memory Space

The memory space of the MB95650L Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas for specific applications such as general-purpose registers and a vector table.

I/O area (addresses: 0x0000 to 0x007F)

- This area contains the control registers and data registers for built-in peripheral functions.
- As the I/O area forms part of the memory space, it can be accessed in the same way as the memory. It can also be accessed at high-speed by using direct addressing instructions.

Extended I/O area (addresses: 0x0F80 to 0x0FFF)

- This area contains the control registers and data registers for built-in peripheral functions.
- As the extended I/O area forms part of the memory space, it can be accessed in the same way as the memory.

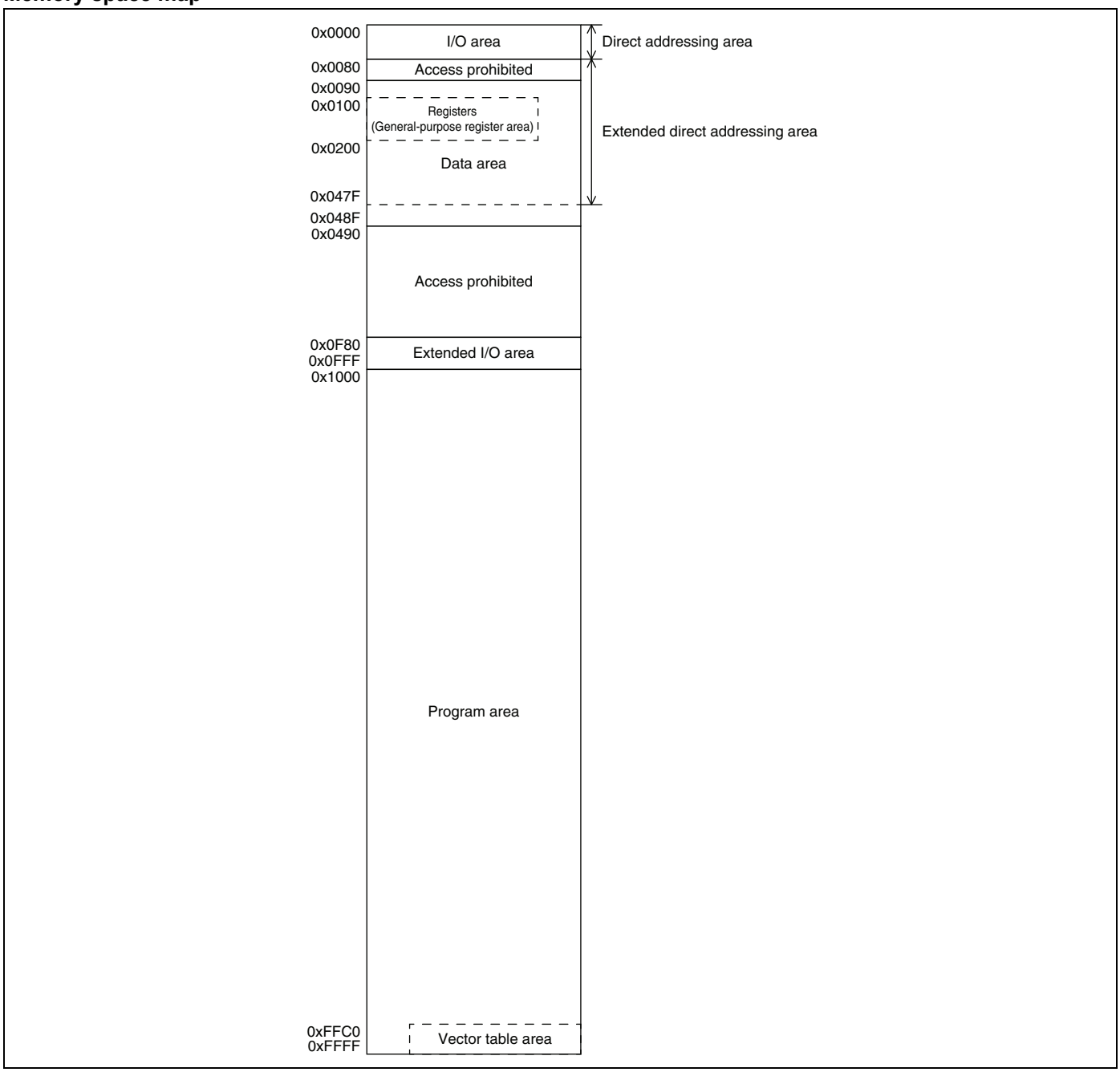
Data area

- Static RAM is incorporated in the data area as the internal data area.
- The internal RAM size varies according to product.
- The RAM area from 0x0090 to 0x00FF can be accessed at high-speed by using direct addressing instructions.
- In MB95F656E/F656L, the area from 0x0090 to 0x047F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- In MB95F654E/F654L, the area from 0x0090 to 0x047F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- In MB95F653E/F653L, the area from 0x0090 to 0x028F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- In MB95F652E/F652L, the area from 0x0090 to 0x018F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- In MB95F653E/F653L/F654E/F654L/F656E/F656L, the area from 0x0100 to 0x01FF can be used as a general-purpose register area.
- In MB95F652E/F652L, the area from 0x0100 to 0x018F can be used as a general-purpose register area.

Program area

- The Flash memory is incorporated in the program area as the internal program area.
- The Flash memory size varies according to product.
- The area from 0xFFC0 to 0xFFFF is used as the vector table.
- The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register.

Memory space map



13. Areas for Specific Applications

The general-purpose register area and vector table area are used for the specific applications.

General-purpose register area (Addresses: 0x0100 to 0x01FF*1)

- This area contains the auxiliary registers used for 8-bit arithmetic operations, transfer, etc.
- As this area forms part of the RAM area, it can also be used as conventional RAM.
- When the area is used as general-purpose registers, general-purpose register addressing enables high-speed access with short instructions.

Non-volatile register data area (Addresses: 0xFFBB to 0xFFBF)

- The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register. For details, refer to “Chapter 23 Non-volatile Register (NVR) Interface” in “New 8FX MB95650L Series Hardware Manual”.

Vector table area (Addresses: 0xFFC0 to 0xFFFF)

- This area is used as the vector table for vector call instructions (CALLV), interrupts, and resets.
- The top of the Flash memory area is allocated to the vector table area. The start address of a service routine is set to an address in the vector table in the form of data.

“16. Interrupt Source Table” lists the vector table addresses corresponding to vector call instructions, interrupts, and resets.

For details, refer to “Chapter 4 Reset”, “Chapter 5 Interrupts” and “A.2 Special Instruction Special Instruction CALLV #vct” in “New 8FX MB95650L Series Hardware Manual”.

Direct bank pointer and access area

Direct bank pointer (DP[2:0])	Operand-specified dir	Access area
0bXXX (It does not affect mapping.)	0x0000 to 0x007F	0x0000 to 0x007F
0b000 (Initial value)	0x0090 to 0x00FF	0x0090 to 0x00FF
0b001	0x0080 to 0x00FF	0x0100 to 0x017F
0b010		0x0180 to 0x01FF*1
0b011		0x0200 to 0x027F
0b100		0x0280 to 0x02FF*2
0b101		0x0300 to 0x037F
0b110		0x0380 to 0x03FF
0b111		0x0400 to 0x047F

*1: Due to the memory size limit, the available access area is up to “0x018F” in MB95F652E/F652L.

*2: Due to the memory size limit, the available access area is up to “0x028F” in MB95F653E/F653L.

14. I/O Map

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E to 0x0015	—	(Disabled)	—	—
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018 to 0x0027	—	(Disabled)	—	—
0x0028	PDRF	Port F data register	R/W	0b00000000
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C	PUL0	Port 0 pull-up register	R/W	0b00000000
0x002D to 0x0032	—	(Disabled)	—	—
0x0033	PUL6	Port 6 pull-up register	R/W	0b00000000
0x0034	—	(Disabled)	—	—
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A to 0x0048	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C to 0x004E	—	(Disabled)	—	—
0x004F	LVDC	LVD control register	R/W	0b00000100
0x0050	SCR	LIN-UART serial control register	R/W	0b00000000
0x0051	SMR	LIN-UART serial mode register	R/W	0b00000000
0x0052	SSR	LIN-UART serial status register	R/W	0b00001000
0x0053	RDR	LIN-UART receive data register	R/W	0b00000000
	TDR	LIN-UART transmit data register		
0x0054	ESCR	LIN-UART extended status control register	R/W	0b00000100
0x0055	ECCR	LIN-UART extended communication control register	R/W	0b000000XX
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B to 0x005F	—	(Disabled)	—	—
0x0060	IBCR00	I^2C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I^2C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I^2C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I^2C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I^2C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I^2C clock control register ch. 0	R/W	0b00000000
0x0066	IBCR01	I^2C bus control register 0 ch. 1	R/W	0b00000000
0x0067	IBCR11	I^2C bus control register 1 ch. 1	R/W	0b00000000
0x0068	IBSR1	I^2C bus status register ch. 1	R/W	0b00000000
0x0069	IDDR1	I^2C data register ch. 1	R/W	0b00000000
0x006A	IAAR1	I^2C address register ch. 1	R/W	0b00000000
0x006B	ICCR1	I^2C clock control register ch. 1	R/W	0b00000000
0x006C	ADC1	8/12-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/12-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/12-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/12-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	ADC3	8/12-bit A/D converter control register 3	R/W	0b01111100

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000
0x0078	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89 to 0x0F91	—	(Disabled)	—	—
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register	R/W	0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	0b00000000
0x0F98	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	0b00000000
0x0F99	T11DR	8/16-bit composite timer 11 data register	R/W	0b00000000
0x0F9A	T10DR	8/16-bit composite timer 10 data register	R/W	0b00000000
0x0F9B	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0b00000000

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0x0F9C to 0x0FBB	—	(Disabled)	—	—
0x0FBC	BGR1	LIN-UART baud rate generator register 1	R/W	0b00000000
0x0FBD	BGR0	LIN-UART baud rate generator register 0	R/W	0b00000000
0x0FBE	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	0b00000000
0x0FBF	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	0b00000000
0x0FC0 to 0x0FC2	—	(Disabled)	—	—
0x0FC3	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FC4 to 0x0FE3	—	(Disabled)	—	—
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	SYSC2	System configuration register 2	R/W	0b00000000
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b00111111
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED to 0x0FFF	—	(Disabled)	—	—

R/W access symbols

R/W : Readable/Writable

R : Read only

Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

15. I/O Ports

List of port registers

Register name		Read/Write	Initial value
Port 0 data register	PDR0	R, RM/W	0b00000000
Port 0 direction register	DDR0	R/W	0b00000000
Port 1 data register	PDR1	R, RM/W	0b00000000
Port 1 direction register	DDR1	R/W	0b00000000
Port 6 data register	PDR6	R, RM/W	0b00000000
Port 6 direction register	DDR6	R/W	0b00000000
Port F data register	PDRF	R, RM/W	0b00000000
Port F direction register	DDRF	R/W	0b00000000
Port G data register	PDRG	R, RM/W	0b00000000
Port G direction register	DDRG	R/W	0b00000000
Port 0 pull-up register	PUL0	R/W	0b00000000
Port 6 pull-up register	PUL6	R/W	0b00000000
Port G pull-up register	PULG	R/W	0b00000000
A/D input disable register (lower)	AIDRL	R/W	0b00000000

R/W : Readable/writable (The read value is the same as the write value.)
R, RM/W : Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)

15.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95650L Series Hardware Manual”.

15.1.1 Port 0 configuration

Port 0 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 0 data register (PDR0)
- Port 0 direction register (DDR0)
- Port 0 pull-up register (PUL0)
- A/D input disable register (lower) (AIDRL)

15.1.2 Block diagrams of port 0

P00/AN00 pin

This pin has the following peripheral function:

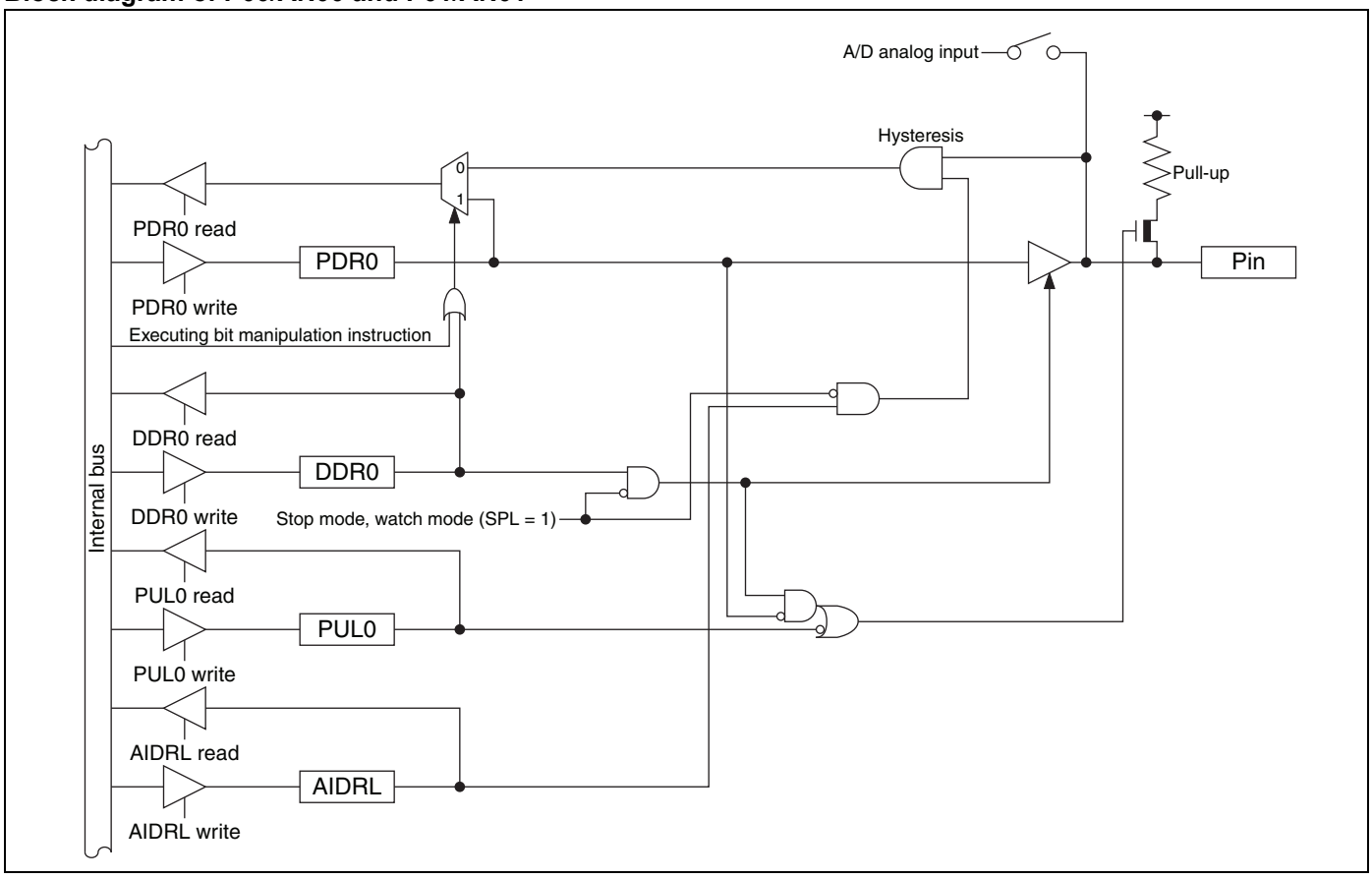
- 8/12-bit A/D converter analog input pin (AN00)

P01/AN01 pin

This pin has the following peripheral function:

- 8/12-bit A/D converter analog input pin (AN01)

Block diagram of P00/AN00 and P01/AN01



P02/INT02/AN02/SCK pin

This pin has the following peripheral functions:

- External interrupt input pin (INT02)
- 8/12-bit A/D converter analog input pin (AN02)
- LIN-UART clock I/O pin (SCK)

P03/INT03/AN03/SOT pin

This pin has the following peripheral functions:

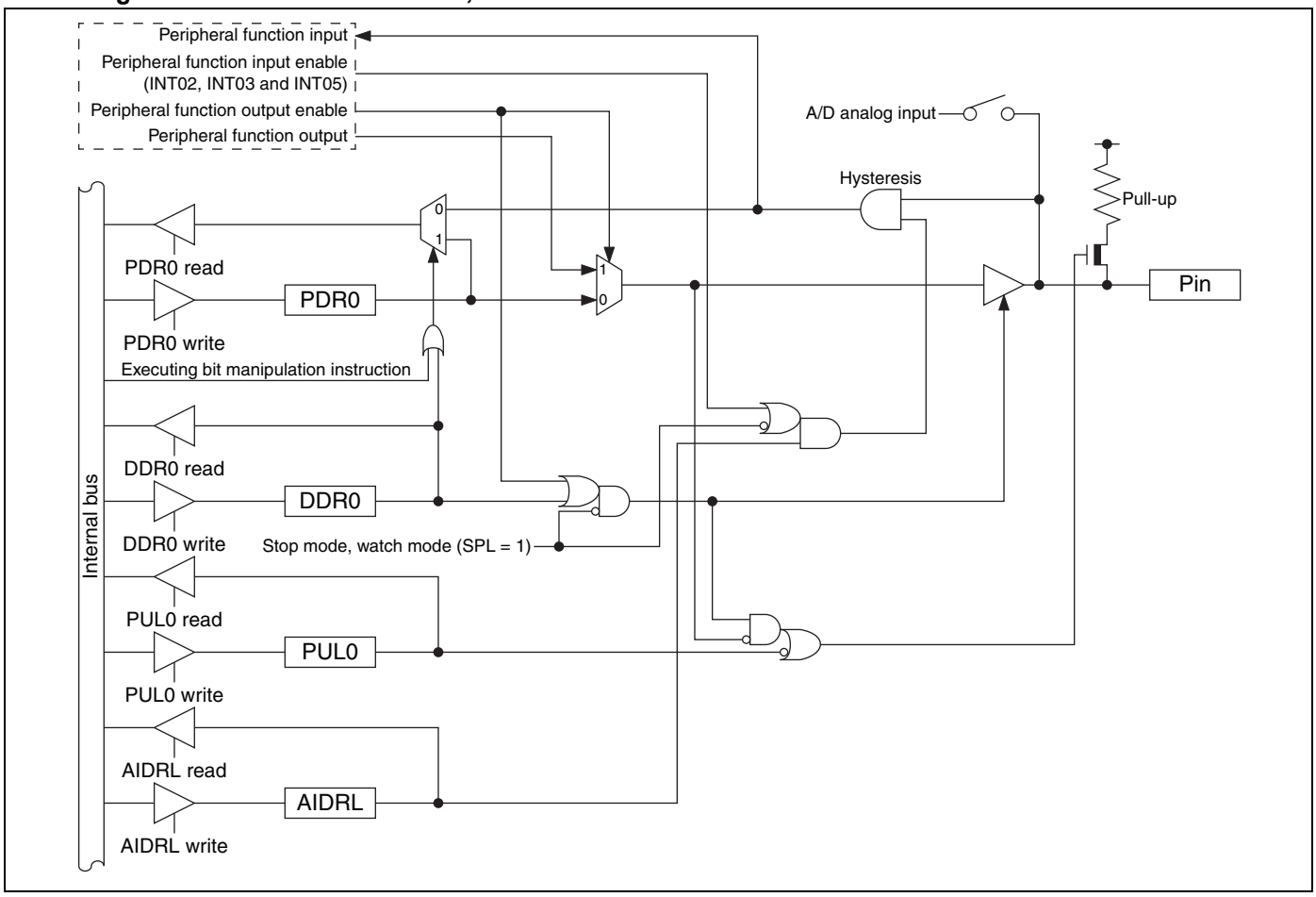
- External interrupt input pin (INT03)
- 8/12-bit A/D converter analog input pin (AN03)
- LIN-UART data output pin (SOT)

P05/INT05/AN05/TO00 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT05)
- 8/16-bit composite timer ch. 0 output pin (TO00)

Block diagram of P02/INT02/AN02/SCK, P03/INT03/AN03/SOT and P05/INT05/AN05/TO00

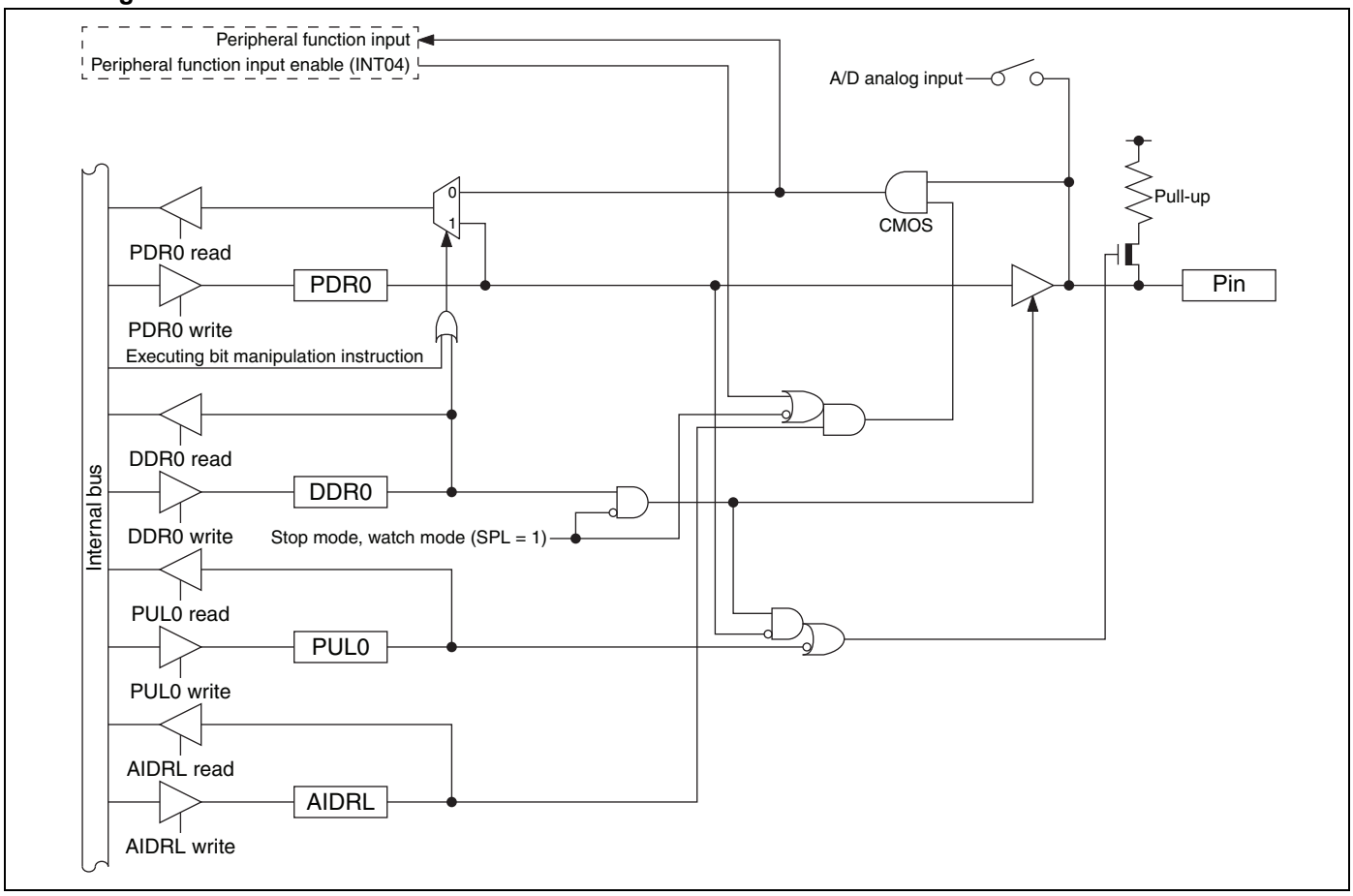


P04/INT04/AN04/SIN/EC0 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT04)
- 8/12-bit A/D converter analog input pin (AN04)
- LIN-UART data input pin (SIN)
- 8/16-bit composite timer ch. 0 clock input pin (EC0)

Block diagram of P04/INT04/AN04/SIN/EC0



P06/INT06/TO01 pin

This pin has the following peripheral functions:

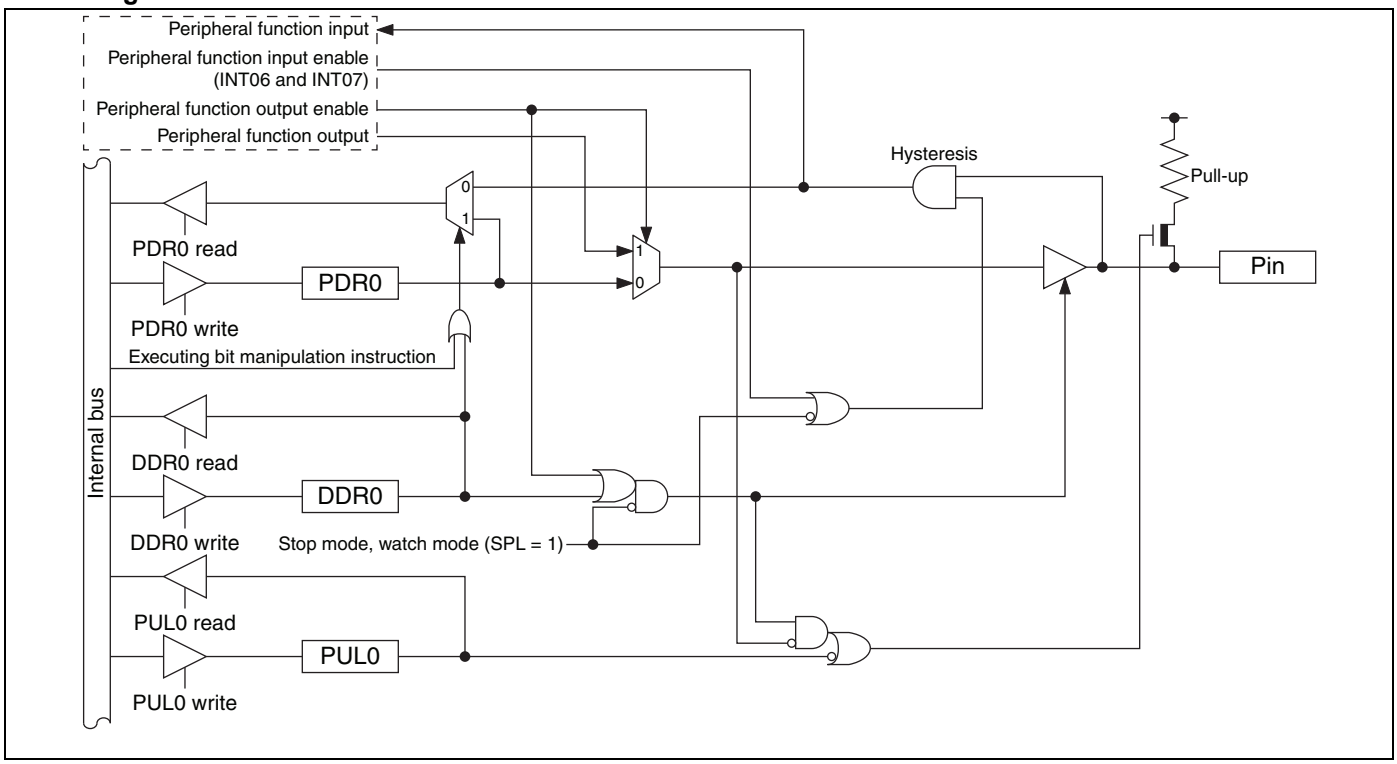
- External interrupt input pin (INT06)
- 8/16-bit composite timer ch. 0 output pin (TO01)

P07/INT07/TO10 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT07)
- 8/16-bit composite timer ch. 1 output pin (TO10)

Block diagram of P06/INT06/TO01 and P07/INT07/TO10



15.1.3 Port 0 registers

Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR0	0	Pin state is “L” level.	PDR0 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR0 value is “1”.	As output port, outputs “H” level.
DDR0	0	Port input enabled		
	1	Port output enabled		
PUL0	0	Pull-up disabled		
	1	Pull-up enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

Correspondence between registers and pins for port 0

	Correspondence between related register bits and pins							
Pin name	**P07**	**P06**	**P05**	**P04**	**P03**	**P02**	**P01**	**P00**
PDR0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR0								
PUL0								
AIDRL	-	-						

15.1.4 Port 0 operations

Operation as an output port
- A pin becomes an output port if the bit in the DDR0 register corresponding to that pin is set to “1”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- When a pin is used as an output port, it outputs the value of the PDR0 register to external pins.
- If data is written to the PDR0 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- Reading the PDR0 register returns the PDR0 register value.

Operation as an input port
- A pin becomes an input port if the bit in the DDR0 register corresponding to that pin is set to “0”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- When using a pin shared with the analog input function as an input port, set the corresponding bit in the A/D input disable register (lower) (AIDRL) to “1”.
- If data is written to the PDR0 register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDR0 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

Operation as a peripheral function output pin
- A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- The pin value can be read from the PDR0 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR0 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

Operation as a peripheral function input pin
- To set a pin as an input port, set the bit in the DDR0 register corresponding to the input pin of a peripheral function to “0”.
- When using a pin shared with the analog input function as another peripheral function input pin, configure it as an input port by setting the bit in the AIDRL register corresponding to that pin to “1”.
- Reading the PDR0 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

Operation at reset

If the CPU is reset, all bits in the DDR0 register are initialized to “0” and port input is enabled. As for a pin shared with analog input, its port input is disabled because the AIDRL register is initialized to “0”.

Operation in stop mode and watch mode
- If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR0 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT02 to INT07), the input is enabled and not blocked.
- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

Operation as an analog input pin
- Set the bit in the DDR0 register bit corresponding to the analog input pin to “0” and the bit corresponding to that pin in the AIDRL register to “0”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions. In addition, set the corresponding bit in the PUL0 register to “0”.

Operation as an external interrupt input pin
- Set the bit in the DDR0 register corresponding to the external interrupt input pin to “0”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

Operation of the pull-up register

Setting the bit in the PUL0 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL0 register.

15.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95650L Series Hardware Manual”.

15.2.1 Port 1 configuration

Port 1 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)

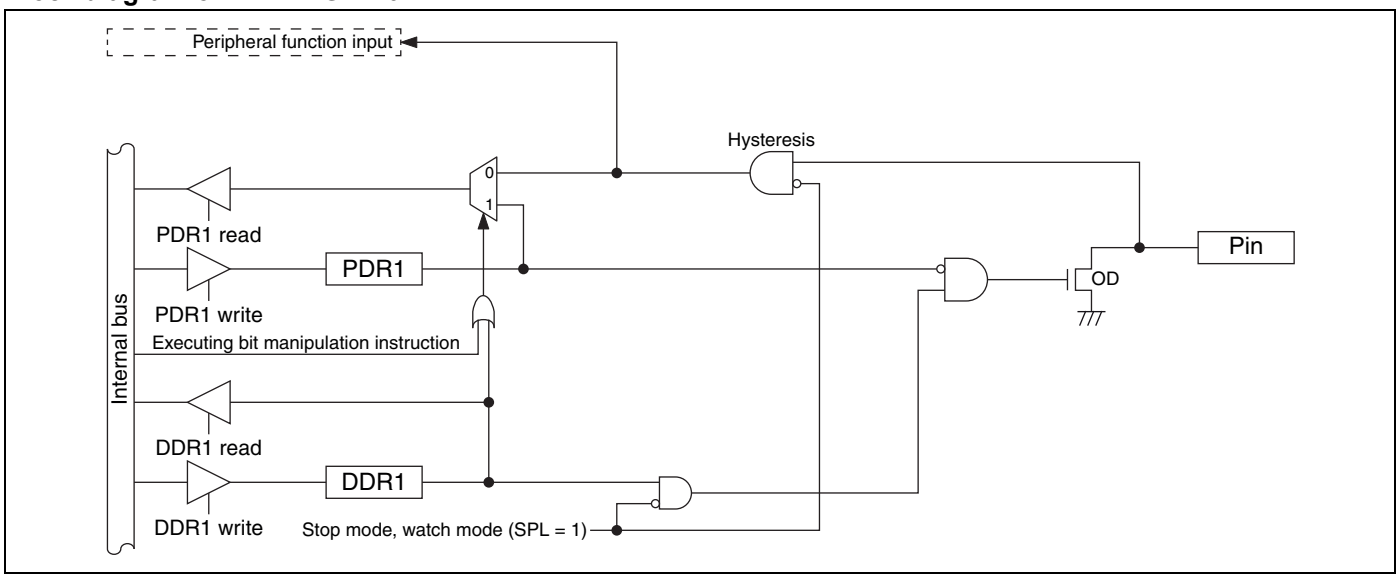
15.2.2 (2)Block diagrams of port 1

P12/DBG/EC0 pin

This pin has the following peripheral functions:

- DBG input pin (DBG)
- 8/16-bit composite timer ch. 0 clock input pin (EC0)

Block diagram of P12/DBG/EC0



P14/SDA0 pin

This pin has the following peripheral function:

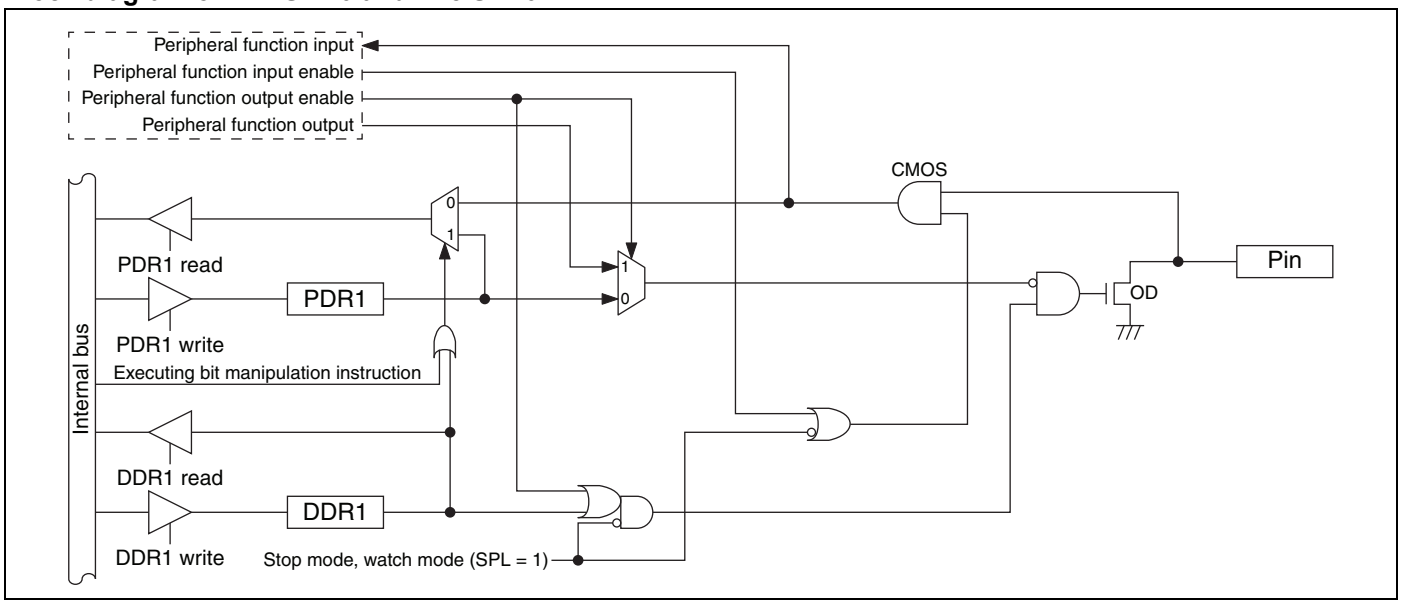
- I^2C bus interface ch. 0 data I/O pin (SDA0)

P15/SCL0 pin

This pin has the following peripheral function:

- I^2C bus interface ch. 0 clock I/O pin (SCL0)

Block diagram of P14/SDA0 and P15/SCL0

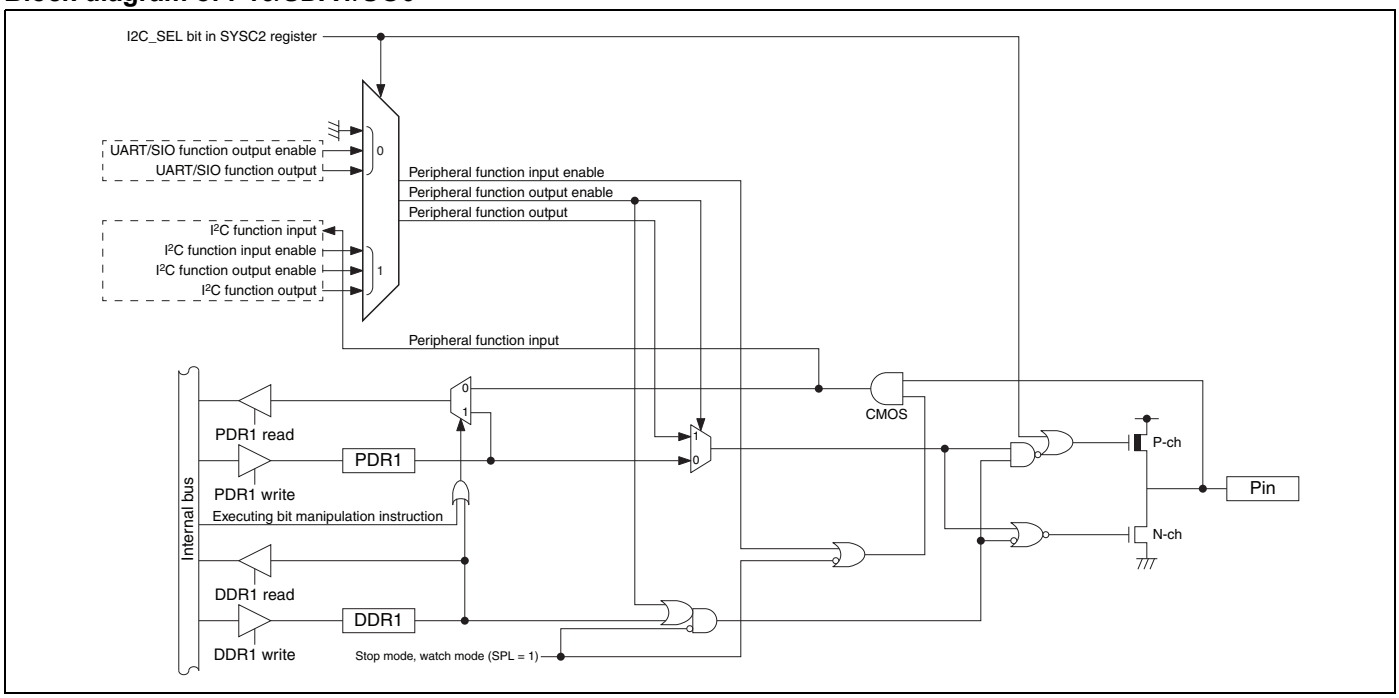


P16/SDA1/UO0 pin

This pin has the following peripheral functions:

- I²C bus interface ch. 1 data I/O pin (SDA1)
- UART/SIO ch. 0 data output pin (UO0)

Block diagram of P16/SDA1/UO0

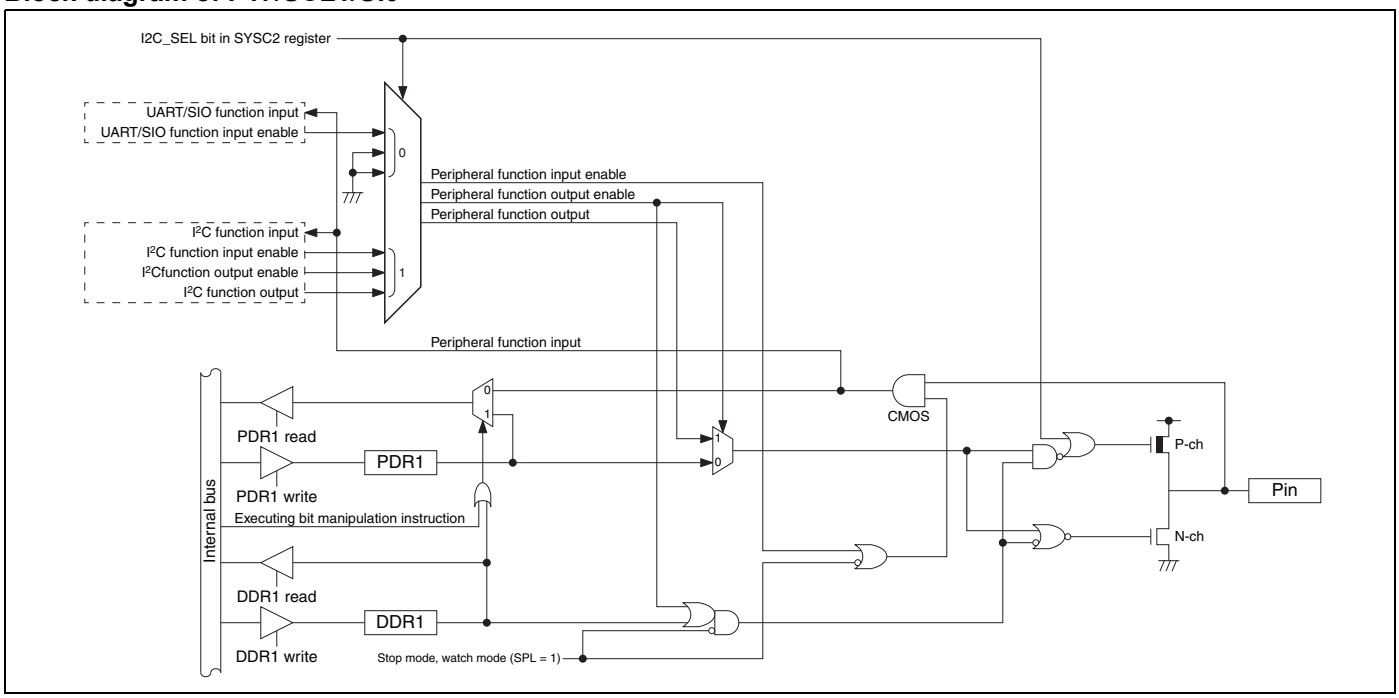


P17/SCL1/UI0 pin

This pin has the following peripheral functions:

- I²C bus interface ch. 1 clock I/O pin (SCL1)
- UART/SIO ch. 0 data input pin (UI0)

Block diagram of P17/SCL1/UI0



15.2.3 Port 1 registers

Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

Correspondence between registers and pins for port 1

	Correspondence between related register bits and pins							
Pin name	**P17**	**P16**	**P15**	**P14**	**-**	**P12**	**-**	**-**
PDR1	bit7	bit6	bit5	bit4	-	bit2	-	-
DDR1								

15.2.4 Port 1 operations

Operation as an output port

- A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to “1”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
- If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- Reading the PDR1 register returns the PDR1 register value.

Operation as an input port

- A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to “0”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

Operation as a peripheral function output pin

- A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

Operation as a peripheral function input pin

- To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function to “0”.
- Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

Operation at reset

If the CPU is reset, all bits in the DDR1 register are initialized to “0” and port input is enabled.

Operation in stop mode and watch mode

- If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

15.3 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95650L Series Hardware Manual”.

15.3.1 Port 6 configuration

Port 6 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 6 data register (PDR6)
- Port 6 direction register (DDR6)
- Port 6 pull-up register (PUL6)

15.3.2 Block diagrams of port 6

P62/TO10/UCK0 pin

This pin has the following peripheral functions:

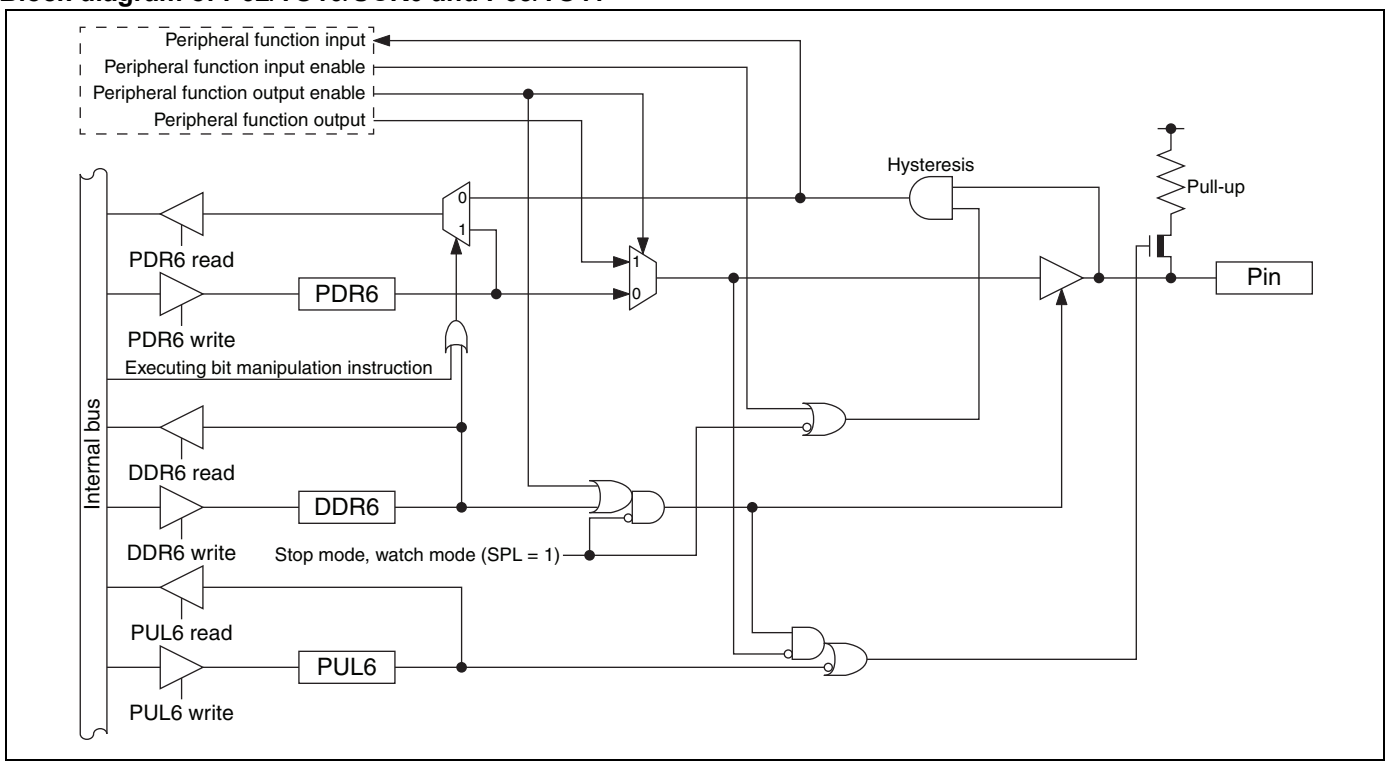
- 8/16-bit composite timer ch. 1 output pin (TO10)
- UART/SIO ch. 0 clock I/O pin (UCK0)

P63/TO11 pin

This pin has the following peripheral function:

- 8/16-bit composite timer ch. 1 output pin (TO11)

Block diagram of P62/TO10/UCK0 and P63/TO11

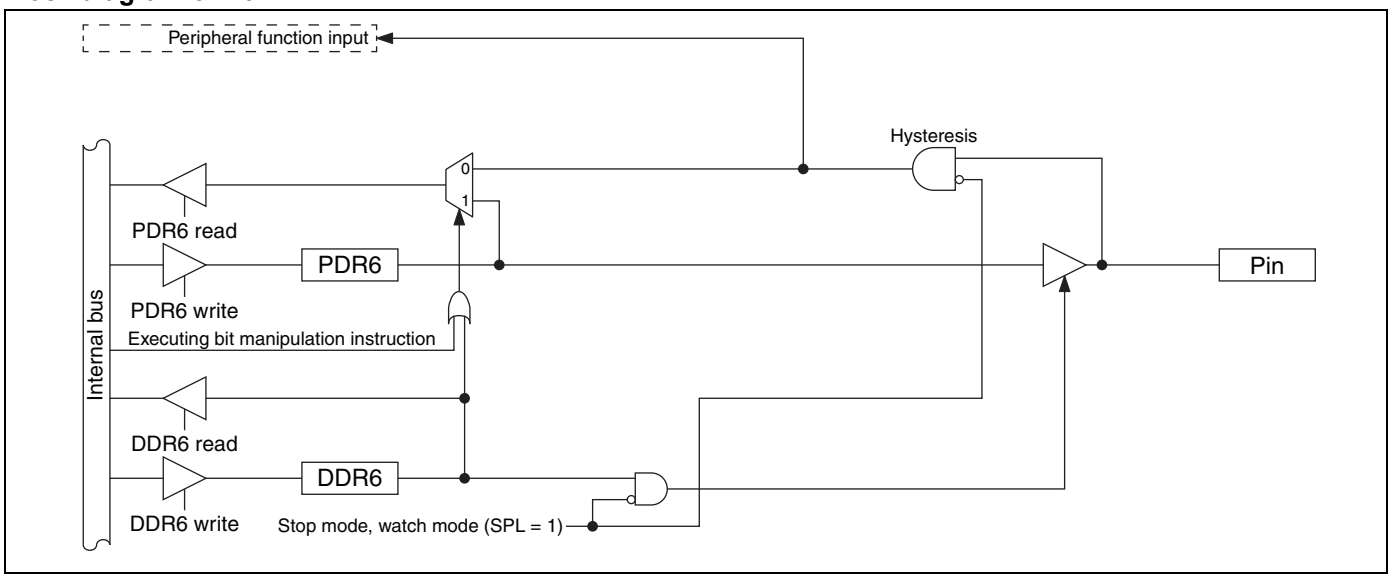


P64/EC1 pin

This pin has the following peripheral function:

- 8/16-bit composite timer ch. 1 clock input pin (EC1)

Block diagram of P64/EC1



15.3.3 Port 6 registers

Port 6 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR6	0	Pin state is “L” level.	PDR6 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR6 value is “1”.	As output port, outputs “H” level.*
DDR6	0	Port input enabled		
	1	Port output enabled		
PUL6	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

Correspondence between registers and pins for port 6

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**P64**	**P63**	**P62**	**-**	**-**
PDR6	-	-	-	bit4	bit3	bit2	-	-
DDR6								
PUL6								

15.3.4 Port 6 operations

Operation as an output port
- A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to “1”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
- If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- Reading the PDR6 register returns the PDR6 register value.

Operation as an input port
- A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to “0”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

Operation as a peripheral function output pin
- A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- The pin value can be read from the PDR6 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR6 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

Operation as a peripheral function input pin
- To set a pin as an input port, set the bit in the DDR6 register corresponding to the input pin of a peripheral function to “0”.
- Reading the PDR6 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

Operation at reset

If the CPU is reset, all bits in the DDR6 register are initialized to “0” and port input is enabled.

Operation in stop mode and watch mode
- If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

Operation of the pull-up register

Setting the bit in the PUL6 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL6 register.

15.4 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95650L Series Hardware Manual”.

15.4.1 Port F configuration

Port F is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port F data register (PDRF)
- Port F direction register (DDRF)

15.4.2 Block diagrams of port F

PF0/X0 pin

This pin has the following peripheral function:

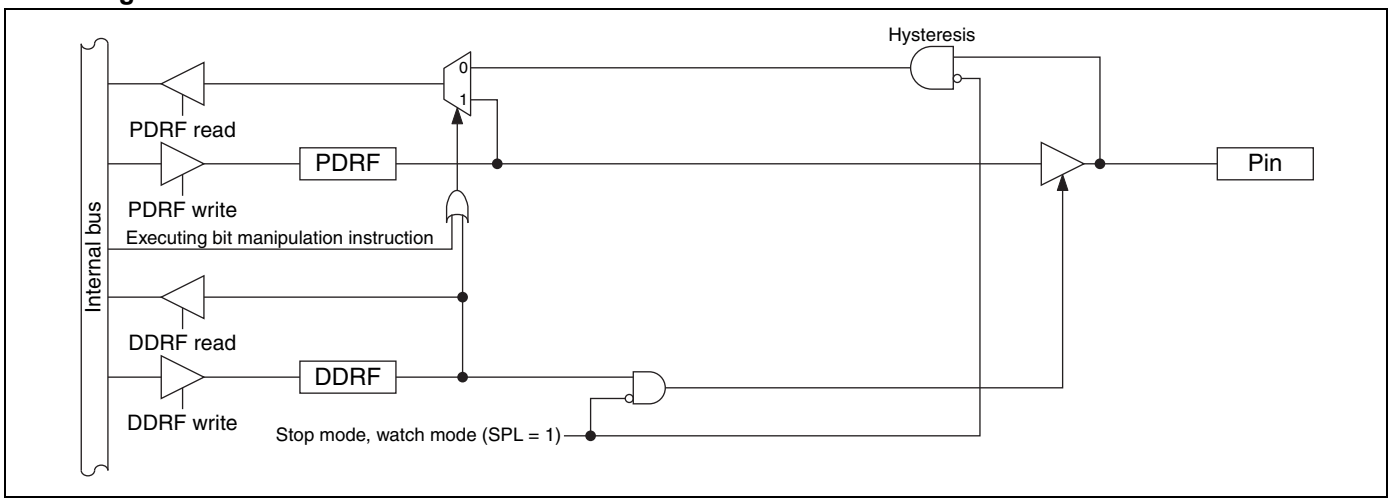
- Main clock input oscillation pin (X0)

PF1/X1 pin

This pin has the following peripheral function:

- Main clock I/O oscillation pin (X1)

Block diagram of PF0/X0 and PF1/X1

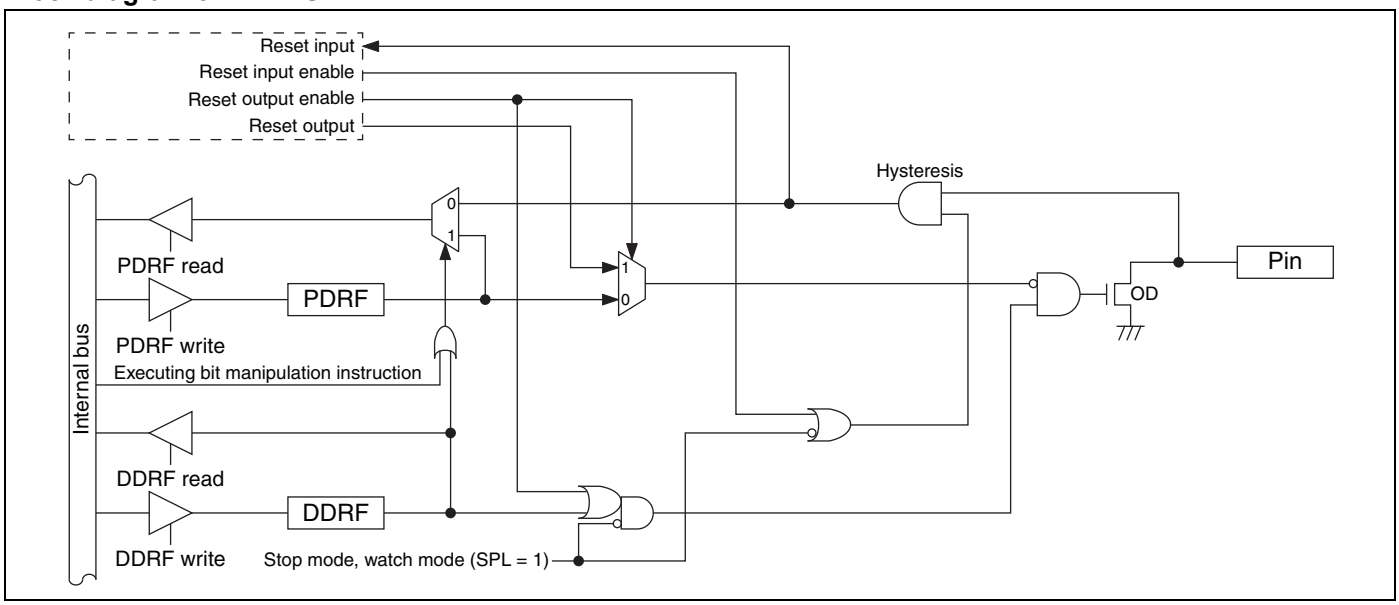


PF2/$\overline{\text{RST}}$ pin

This pin has the following peripheral function:

- Reset pin ($\overline{\text{RST}}$)

Block diagram of PF2/$\overline{\text{RST}}$



15.4.3 Port F registers

Port F register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRF	0	Pin state is “L” level.	PDRF value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRF value is “1”.	As output port, outputs “H” level.*
DDRF	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

Correspondence between registers and pins for port F

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PF2***	**PF1**	**PF0**
PDRF	-	-	-	-	-	bit2	bit1	bit0
DDRF								

*: PF2/$\overline{\text{RST}}$ is the dedicated reset pin on MB95F652L/F653L/F654L/F656L.

15.4.4 Port F operations

Operation as an output port

- A pin becomes an output port if the bit in the DDRF register corresponding to that pin is set to “1”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- When a pin is used as an output port, it outputs the value of the PDRF register to external pins.
- If data is written to the PDRF register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- Reading the PDRF register returns the PDRF register value.

Operation as an input port

- A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to “0”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.

Operation at reset

If the CPU is reset, all bits in the DDRF register are initialized to “0” and port input is enabled.

Operation in stop mode and watch mode

- If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

15.5 Port G

Port G is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95650L Series Hardware Manual”.

15.5.1 Port G configuration

Port G is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port G data register (PDRG)
- Port G direction register (DDRG)
- Port G pull-up register (PULG)

15.5.2 Block diagram of port G

PG1/X0A pin

This pin has the following peripheral function:

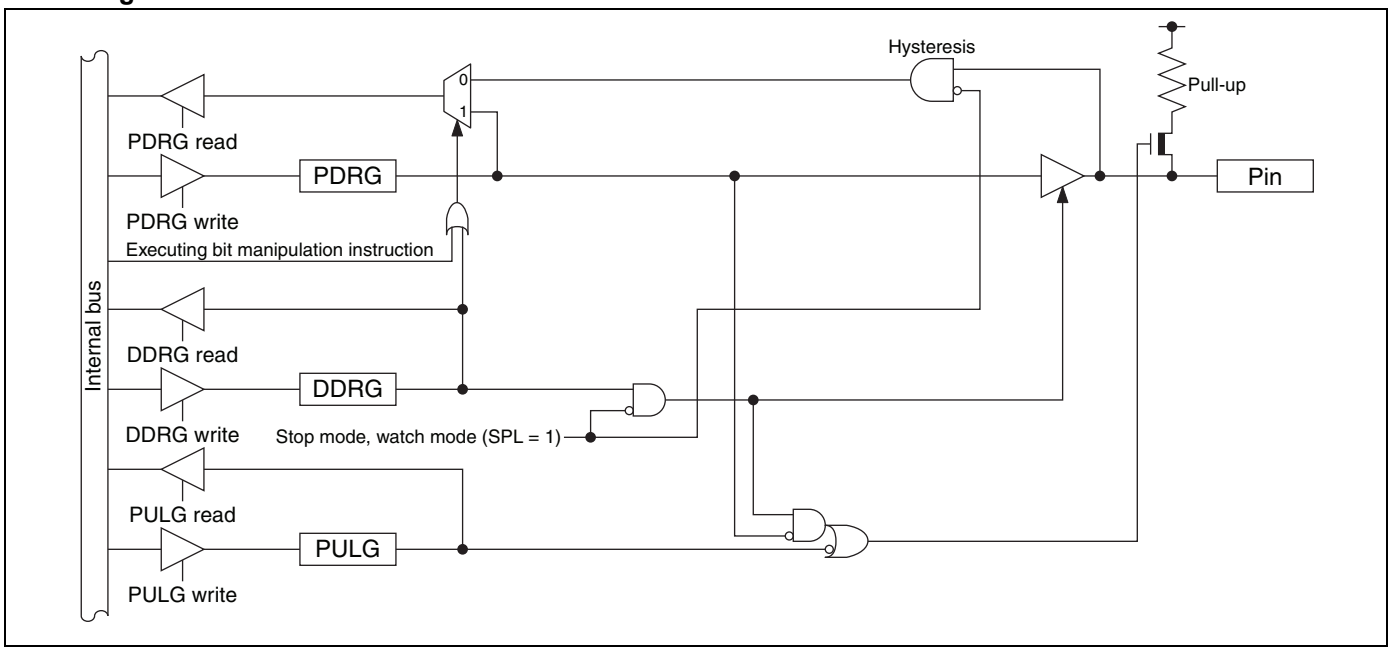
- Subclock input oscillation pin (X0A)

PG2/X1A pin

This pin has the following peripheral function:

- Subclock I/O oscillation pin (X1A)

Block diagram of PG1/X0A and PG2/X1A



15.5.3 Port G registers

Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

Correspondence between registers and pins for port G

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PG2**	**PG1**	**-**
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

15.5.4 Port G operations

Operation as an output port

- A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to “1”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
- If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- Reading the PDRG register returns the PDRG register value.

Operation as an input port

- A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to “0”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

Operation at reset

If the CPU is reset, all bits in the DDRG register are initialized to “0” and port input is enabled.

Operation in stop mode and watch mode

- If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

Operation of the pull-up register

Setting the bit in the PULG register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULG register.

16. Interrupt Source Table

Interrupt source	Interrupt request number	Vector table address		Interrupt level setting register		Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower	Register	Bit	
External interrupt ch. 4	IRQ00	0xFFFA	0xFFFB	ILR0	L00 [1:0]	High
External interrupt ch. 5	IRQ01	0xFFF8	0xFFF9	ILR0	L01 [1:0]	
External interrupt ch. 2	IRQ02	0xFFF6	0xFFF7	ILR0	L02 [1:0]	
External interrupt ch. 6						
External interrupt ch. 3	IRQ03	0xFFF4	0xFFF5	ILR0	L03 [1:0]	
External interrupt ch. 7						
Low-voltage detection interrupt circuit	IRQ04	0xFFF2	0xFFF3	ILR1	L04 [1:0]	
UART/SIO ch. 0						
8/16-bit composite timer ch. 0 (lower)	IRQ05	0xFFF0	0xFFF1	ILR1	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	0xFFEE	0xFFEF	ILR1	L06 [1:0]	
LIN-UART (reception)	IRQ07	0xFFEC	0xFFED	ILR1	L07 [1:0]	
LIN-UART (transmission)	IRQ08	0xFFEA	0xFFEB	ILR2	L08 [1:0]	
—	IRQ09	0xFFE8	0xFFE9	ILR2	L09 [1:0]	
I^2C bus interface ch. 1	IRQ10	0xFFE6	0xFFE7	ILR2	L10 [1:0]	
—	IRQ11	0xFFE4	0xFFE5	ILR2	L11 [1:0]	
—	IRQ12	0xFFE2	0xFFE3	ILR3	L12 [1:0]	
—	IRQ13	0xFFE0	0xFFE1	ILR3	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	0xFFDE	0xFFDF	ILR3	L14 [1:0]	
—	IRQ15	0xFFDC	0xFFDD	ILR3	L15 [1:0]	
I^2C bus interface ch. 0	IRQ16	0xFFDA	0xFFDB	ILR4	L16 [1:0]	
—	IRQ17	0xFFD8	0xFFD9	ILR4	L17 [1:0]	
8/12-bit A/D converter	IRQ18	0xFFD6	0xFFD7	ILR4	L18 [1:0]	
Time-base timer	IRQ19	0xFFD4	0xFFD5	ILR4	L19 [1:0]	
Watch prescaler	IRQ20	0xFFD2	0xFFD3	ILR5	L20 [1:0]	
—	IRQ21	0xFFD0	0xFFD1	ILR5	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	0xFFCE	0xFFCF	ILR5	L22 [1:0]	
Flash memory	IRQ23	0xFFCC	0xFFCD	ILR5	L23 [1:0]	Low

17. Pin States in each Mode

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PF0/X0	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PF1/X1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PF2/$\overline{\text{RST}}$	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input*4
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PG1/X0A	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PG2/X1A	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
P00/AN00	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*2, *5	- Hi-Z*6 - Input blocked*2, *5	- Previous state kept - Input blocked*2, *5	- Hi-Z*6 - Input blocked*2, *5	- Hi-Z - Input blocked*2
P01/AN01							
P02/INT02/ AN02/SCK							
P03/INT03/ AN03/SOT							
P04/INT04/ AN04/SIN/ EC0							
P05/INT05/ AN05/TO00							

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P06/INT06/ TO01 P07/INT07/ TO10	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2, *5	- Hi-Z*6 - Input blocked*2, *5	- Previous state kept - Input blocked*2, *5	- Hi-Z*6 - Input blocked*2, *5	- Hi-Z - Input blocked*2
P14/SDA0 P15/SCL0 P16/SDA1/ UO0 P17/SCL1/ UI0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2, *7	- Hi-Z - Input blocked*2, *7	- Previous state kept - Input blocked*2, *7	- Hi-Z - Input blocked*2, *7	- Hi-Z - Input enabled*3 (However, it does not function.)
P12/DBG/ EC0 P62/TO10/ UCK0 P63/TO11 P64/EC1	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z - Input blocked*2	- Hi-Z - Input enabled*3 (However, it does not function.)

SPL: Pin state setting bit in the standby control register (STBC:SPL)
Hi-Z: High impedance

*1: The pin stays at the state shown when configured as a general-purpose I/O port.

*2: “Input blocked” means direct input gate operation from the pin is disabled.

*3: “Input enabled” means that the input function is enabled. While the input function is enabled, perform a pull-up or pull-down operation in order to prevent leaks due to external input. If a pin is used as an output port, its pin state is the same as that of other ports.

*4: The PF2/$\overline{\text{RST}}$ pin stays at the state shown when configured as a reset pin.

*5: Though input is blocked, an external interrupt can be input when the external interrupt request is enabled.

*6: The pull-up control setting is still effective.

*7: The I^2C bus interface can wake up the MCU in stop mode or watch mode when its MCU standby mode wakeup function is enabled. For details of the MCU standby mode wakeup function, refer to “Chapter 19 I^2c Bus Interface” in “New 8FX MB95650L Series Hardware Manual”.

18. Electrical Characteristics

18.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	−2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL}	—	15	mA	
"L" level average current	I_{OLAV1}	—	4	mA	Other than P05 to P07, P62 and P63 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05 to P07, P62 and P63 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	37	mA	Total average output current = operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH}	—	−15	mA	
"H" level average current	I_{OHAV1}	—	−4	mA	Other than P05 to P07, P62 and P63 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		−8		P05 to P07, P62 and P63 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	−100	mA	
"H" level total average output current	ΣI_{OHAV}	—	−47	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	T_{stg}	−55	+150	°C	

*1: These parameters are based on the condition that V_{SS} is 0.0 V.

*2: V_1 and V_0 must not exceed V_{CC} + 0.3 V. V_1 must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

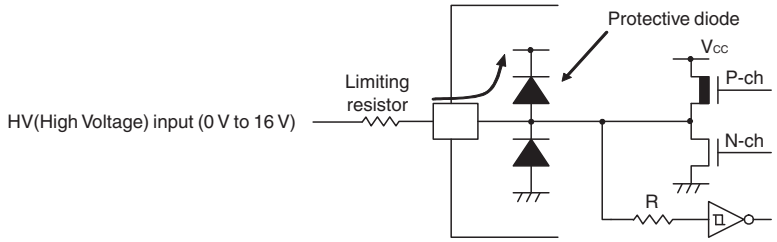
(Continued)

(Continued)

*3: Specific pins: P00 to P07, P14, P15, P62 to P64, PF0, PF1, PG1, PG2

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:

Input/Output equivalent circuit



WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

18.2 Recommended Operating Conditions

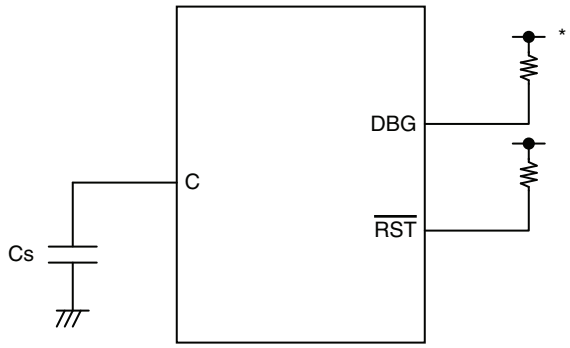
(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	1.8*1	5.5	V	In normal operation
Decoupling capacitor	C_S	0.2	10	µF	A capacitor of about 1.0 µF is recommended. *2
Operating temperature	T_A	−40	+85	°C	Other than on-chip debug mode
		+5	+35		On-chip debug mode

*1: The minimum power supply voltage becomes 2.18 V when a product with the low-voltage detection reset is used or when the on-chip debug mode is used.

*2: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

DBG / $\overline{\text{RST}}$ / C pins connection diagram



*: Connect the DBG pin to an external pull-up resistor of 2 kΩ or above. After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released. The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

18.3 DC Characteristics

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI1}	P04, P16, P17	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input level
	V_{IHI2}	P14, P15	*1	0.7 V_{CC}	—	V_{CC} + 5.5	V	CMOS input level
	V_{IHS}	P00 to P03, P05 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{ILI}	P04, P14 to P17	*1	V_{SS} − 0.3	—	0.3 V_{CC}	V	CMOS input level
	V_{ILS}	P00 to P03, P05 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2	*1	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_{D1}	P12, PF2	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
	V_{D2}	P14, P15	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
	V_{D3}	P16, P17	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	In I^2C mode
"H" level output voltage	V_{OH1}	Output pins other than P05 to P07, P12, P62, P63	I_{OH} = −4 mA*2	V_{CC} − 0.5	—	—	V	
	V_{OH2}	P05 to P07, P62, P63	I_{OH} = −8 mA*3	V_{CC} − 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P05 to P07, P62, P63	I_{OL} = 4 mA*4	—	—	0.4	V	
	V_{OL2}	P05 to P07, P62, P63	I_{OL} = 12 mA*5	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	−5	—	+5	µA	When the internal pull-up resistor is disabled
Internal pull-up resistor	R_{PULL}	P00 to P07, P62 to P64, PG1, PG2	V_I = 0 V	75	100	150	kΩ	When the internal pull-up resistor is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

(Continued)

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*6		
Power supply current*7	I_{CC}	V_{CC} (External clock operation)	F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	4.2	6.8	mA	Except during Flash memory programming and erasing
				—	9.3	14.7	mA	During Flash memory programming and erasing
				—	6	10	mA	At A/D conversion
	I_{CCS}		F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	1.7	3	mA	
	I_{CCL}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25 °C	—	35	60	µA	
	I_{CCLS}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25 °C	—	2	7	µA	
	I_{CCT}		F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25 °C	—	1	6	µA	
	$I_{CCMCRPLL}$	V_{CC}	F_{MCRPLL} = 16 MHz F_{MP} = 16 MHz Main CR PLL clock mode (multiplied by 4)	—	4.3	7.7	mA	
	I_{CCMPLL}		F_{MPLL} = 16 MHz F_{MP} = 16 MHz Main PLL clock mode (multiplied by 4)	—	4.1	7	mA	
	I_{CCMCR}		F_{CRH} = 4 MHz F_{MP} = 4 MHz Main CR clock mode	—	1.5	3	mA	
	I_{CCSCR}		Sub-CR clock mode (divided by 2) T_A = +25 °C	—	50	100	µA	

(Continued)

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*6		
Power supply current*7	I_{CCTS}	V_{CC} (External clock operation)	F_{CH} = 32 MHz Time-base timer mode T_A = +25 °C	—	450	500	µA	
	I_{CCH}		Substop mode T_A = +25 °C	—	0.7	5	µA	
	I_{PLVD}	V_{CC}	Current consumption of the low-voltage detection reset circuit in operation	—	6	26	µA	
	I_{ILVD}		Current consumption of the low-voltage detection interrupt circuit operating in normal mode	—	6	14	µA	
	I_{ILVDL}		Current consumption of the low-voltage detection interrupt circuit operating in low power consumption mode	—	3	10	µA	
	I_{CRH}		Current consumption of the main CR oscillator	—	270	320	µA	
	I_{CRL}		Current consumption of the sub-CR oscillator oscillating at 100 kHz	—	5	20	µA	
	I_{SOSC}		Current consumption of the suboscillator	—	0.8	7	µA	

*1: V_{CC} = 3.0 V, T_A = +25 °C

*2: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OH} = –2 mA.

*3: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OH} = –4 mA.

*4: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OL} = 2 mA.

*5: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OH} = 6 mA.

*6: V_{CC} = 3.3 V, T_A = +85 °C (unless otherwise specified)

*7:
- The power supply current is determined by the external clock. When the low-voltage detection reset circuit is selected, the power supply current is the sum of adding the current consumption of the low-voltage detection reset circuit (I_{PLVD}) to one of the values from I_{CC} to I_{CCH}. In addition, when the low-voltage detection reset circuit and a CR oscillator are selected, the power supply current is the sum of adding up the current consumption of the low-voltage detection reset circuit (I_{PLVD}), the current consumption of the CR oscillator (I_{CRH} or I_{CRL}) and one of the values from I_{CC} to I_{CCH}. In on-chip debug mode, the main CR oscillator (I_{CRH}) and the low-voltage detection reset circuit are always in operation, and current consumption therefore increases accordingly.
- See “18.4. AC Characteristics 18.4.1. Clock Timing” for F_{CH}, F_{CL}, F_{CRH}, F_{MCRPLL} and F_{MPLL}.
- See “18.4. AC Characteristics 18.4.2. Source Clock/Machine Clock” for F_{MP} and F_{MPL}.
- The power supply current in subclock mode is determined by the external clock. In subclock mode, current consumption in using the crystal oscillator is higher than that in using the external clock. When the crystal oscillator is used, the power supply current is the sum of adding I_{SOSC} (current consumption of the suboscillator) to the power supply current in using the external clock. For details of controlling the subclock, refer to “Chapter 3 Clock Controller” And “chapter 24 System Configuration Register” in “New 8FX MB95650L Series Hardware Manual”.

18.4 AC Characteristics

18.4.1 Clock Timing

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	—	1	—	32.5	MHz	When the main external clock is used
		X0, X1	—	—	4	—	MHz	When the main PLL clock is used
	F_{CRH}	—	—	3.92	4	4.08	MHz	Operating conditions • The main CR clock is used. • 0 °C ≤ T_A ≤ +70 °C
				3.8	4	4.2	MHz	Operating conditions • The main CR clock is used. • –40 °C ≤ T_A < 0 °C, +70 °C < T_A ≤ +85 °C
	F_{MCRPLL}	—	—	7.84	8	8.16	MHz	Operating conditions • PLL multiplication rate: 2 • 0 °C ≤ T_A ≤ +70 °C
				7.6	8	8.4	MHz	Operating conditions • PLL multiplication rate: 2 • –40 °C ≤ T_A < 0 °C, +70 °C < T_A ≤ +85 °C
				9.8	10	10.2	MHz	Operating conditions • PLL multiplication rate: 2.5 • 0 °C ≤ T_A ≤ +70 °C
				9.5	10	10.5	MHz	Operating conditions • PLL multiplication rate: 2.5 • –40 °C ≤ T_A < 0 °C, +70 °C < T_A ≤ +85 °C
				11.76	12	12.24	MHz	Operating conditions • PLL multiplication rate: 3 • 0 °C ≤ T_A ≤ +70 °C
				11.4	12	12.6	MHz	Operating conditions • PLL multiplication rate: 3 • –40 °C ≤ T_A < 0 °C, +70 °C < T_A ≤ +85 °C
				15.68	16	16.32	MHz	Operating conditions • PLL multiplication rate: 4 • 0 °C ≤ T_A ≤ +70 °C
				15.2	16	16.8	MHz	Operating conditions • PLL multiplication rate: 4 • –40 °C ≤ T_A < 0 °C, +70 °C < T_A ≤ +85 °C
	F_{MPLL}	—	—	8	—	16	MHz	When the main PLL clock is used

(Continued)

(Continued)

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the suboscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	150	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	—	30.8	—	1000	ns	When an external clock is used
		X0, X1	—	—	250	—	ns	When the main PLL clock is used
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1}, t_{WL1}	X0	—	12.4	—	—	ns	When an external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	—	—	125	—	ns	When the main PLL clock is used
	t_{WH2}, t_{WL2}	X0A	—	—	15.2	—	µs	When an external clock is used, the duty ratio should range between 40% and 60%.
Input clock rising time and falling time	t_{CR}, t_{CF}	X0, X0A	—	—	—	5	ns	When an external clock is used
CR oscillation start time	t_{CRHWK}	—	—	—	—	50	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	30	µs	When the sub-CR clock is used
PLL oscillation start time	$t_{MCRPLLWK}$	—	—	—	—	100	µs	When the main CR PLL clock is used

Input waveform generated when an external clock (main clock) is used

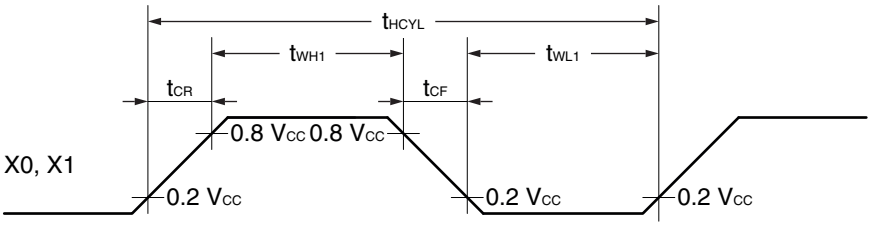
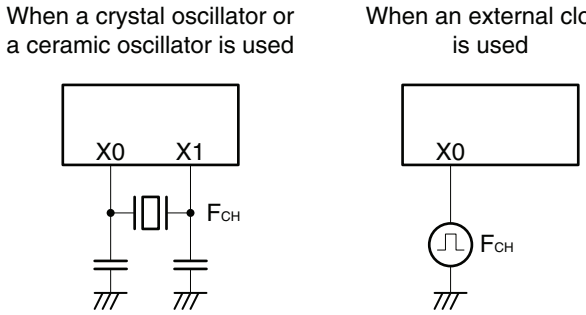


Figure of main clock input port external connection



Input waveform generated when an external clock (subclock) is used

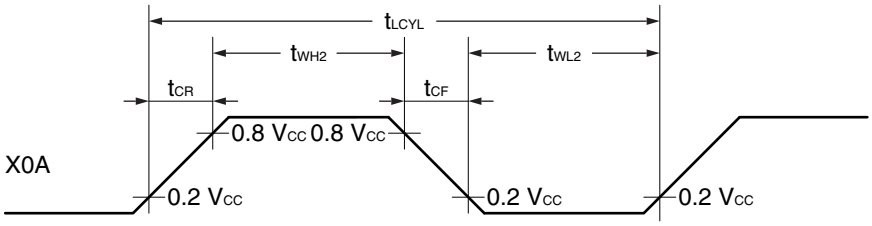
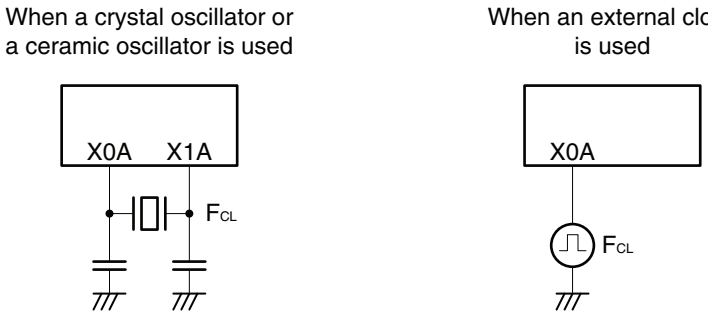
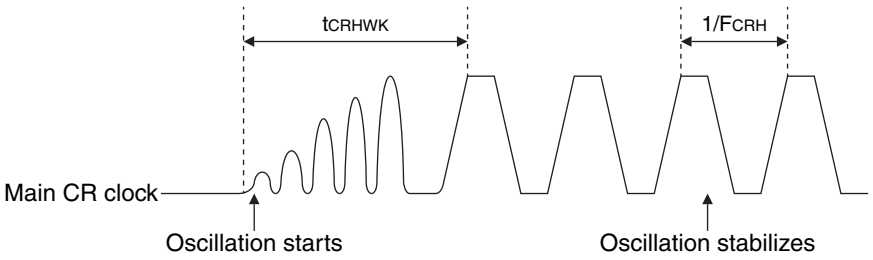


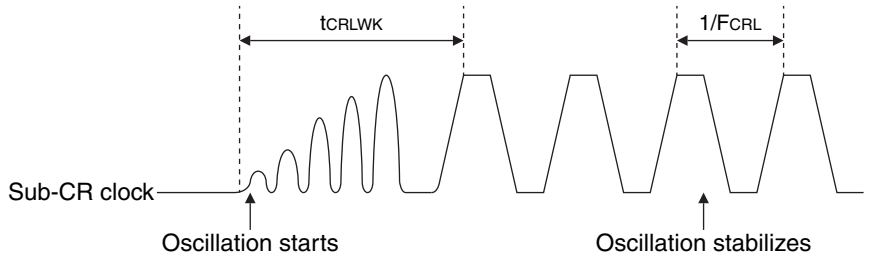
Figure of subclock input port external connection



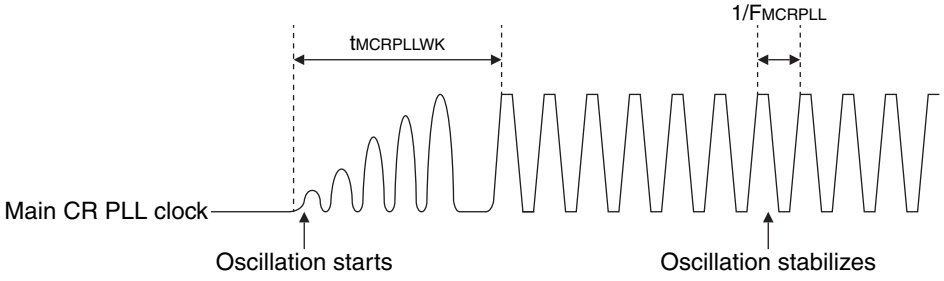
Input waveform generated when an internal clock (main CR clock) is used



Input waveform generated when an internal clock (sub-CR clock) is used



Input waveform generated when an internal clock (main CR PLL clock) is used



18.4.2 Source Clock/Machine Clock

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			—	250	—	ns	When the main CR clock is used
			62.5	—	250	ns	When the main PLL clock is used Min: F_{CH} = 4 MHz, multiplied by 4 Max: F_{CH} = 4 MHz, no division
			62.5	—	250	ns	When the main CR PLL clock is used Min: F_{CRH} = 4 MHz, multiplied by 4 Max: F_{CRH} = 4 MHz, no division
			—	61	—	µs	When the suboscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			—	4	—	MHz	When the main CR clock is used
			4	—	16	MHz	When the main PLL clock is used
			4	—	16	MHz	When the main CR PLL clock is used
	F_{SPL}		—	16.384	—	kHz	When the suboscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			250	—	4000	ns	When the main CR clock is used Min: F_{SP} = 4 MHz, no division Max: F_{SP} = 4 MHz, divided by 16
			62.5	—	4000	ns	When the main PLL clock is used Min: F_{SP} = 4 MHz, multiplied by 4 Max: F_{SP} = 4 MHz, divided by 16
			62.5	—	4000	ns	When the main CR PLL clock is used Min: F_{SP} = 4 MHz, multiplied by 4 Max: F_{SP} = 4 MHz, divided by 16
			61	—	976.5	µs	When the suboscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16

(Continued)

(Continued)

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.25	—	4	MHz	When the main CR clock is used
			0.25	—	16	MHz	When the main PLL clock is used
			0.25	—	16	MHz	When the main CR PLL clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the suboscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

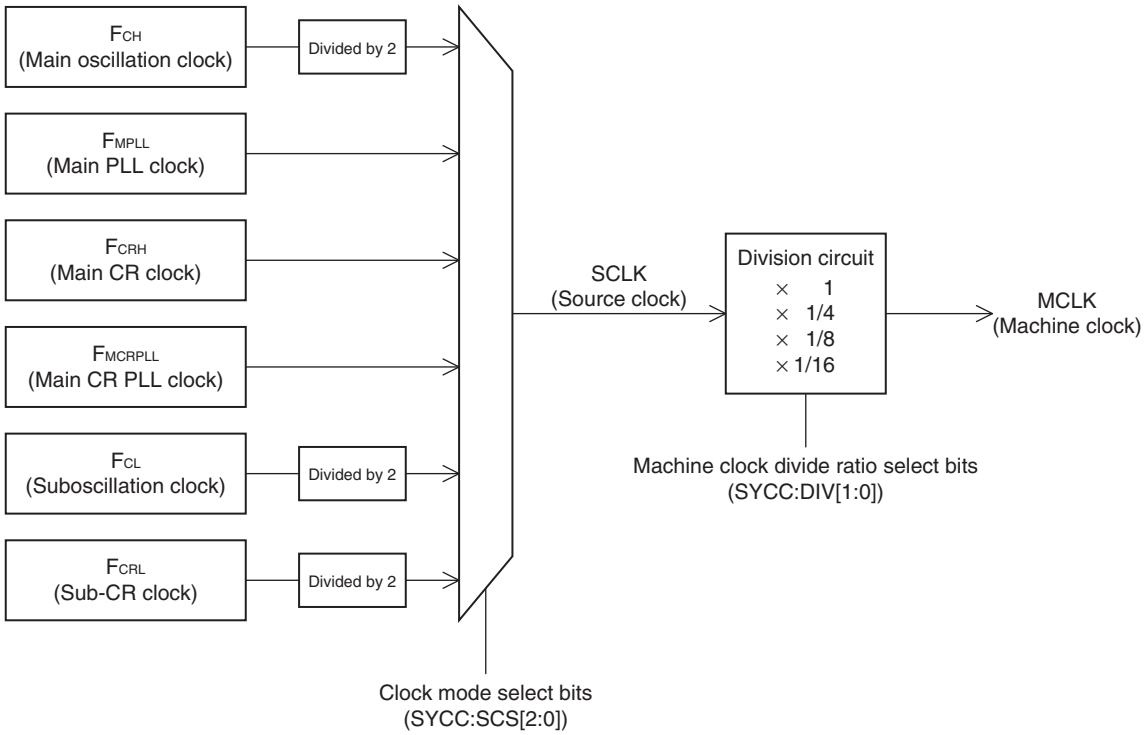
*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- PLL multiplication of main clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Main CR clock
- PLL multiplication of main CR clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Subclock divided by 2
- Sub-CR clock divided by 2

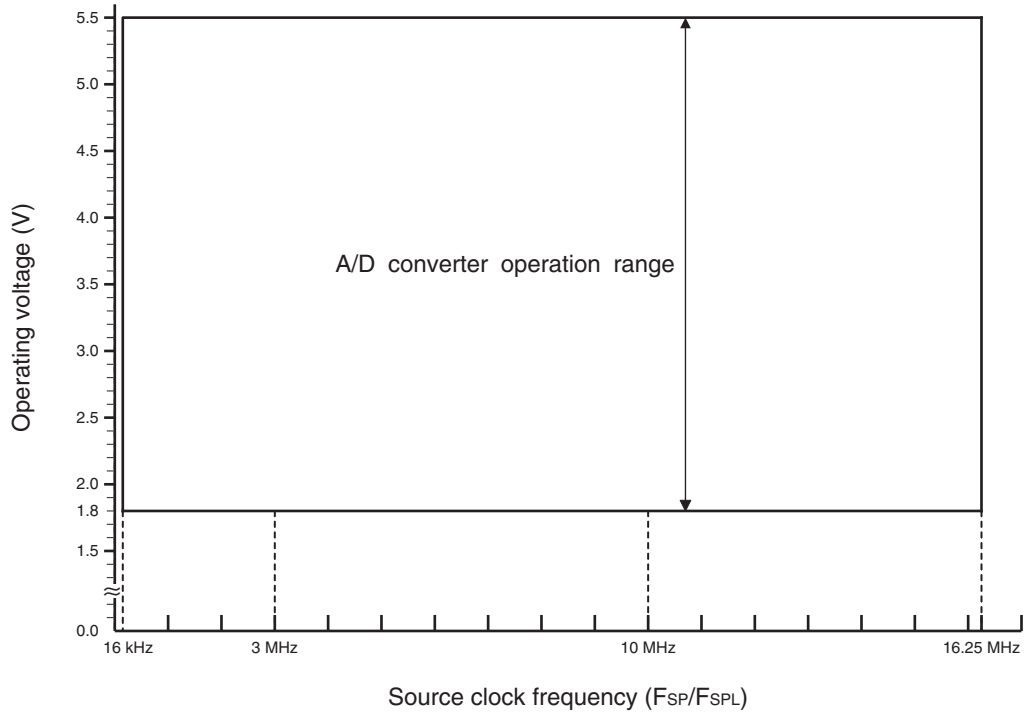
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

Schematic diagram of the clock generation block



Operating voltage - Operating frequency (T_A = −40 °C to +85 °C)

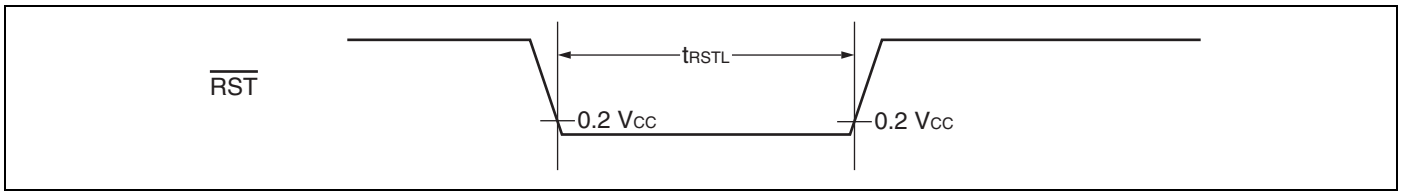


18.4.3 External Reset

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*	—	ns	

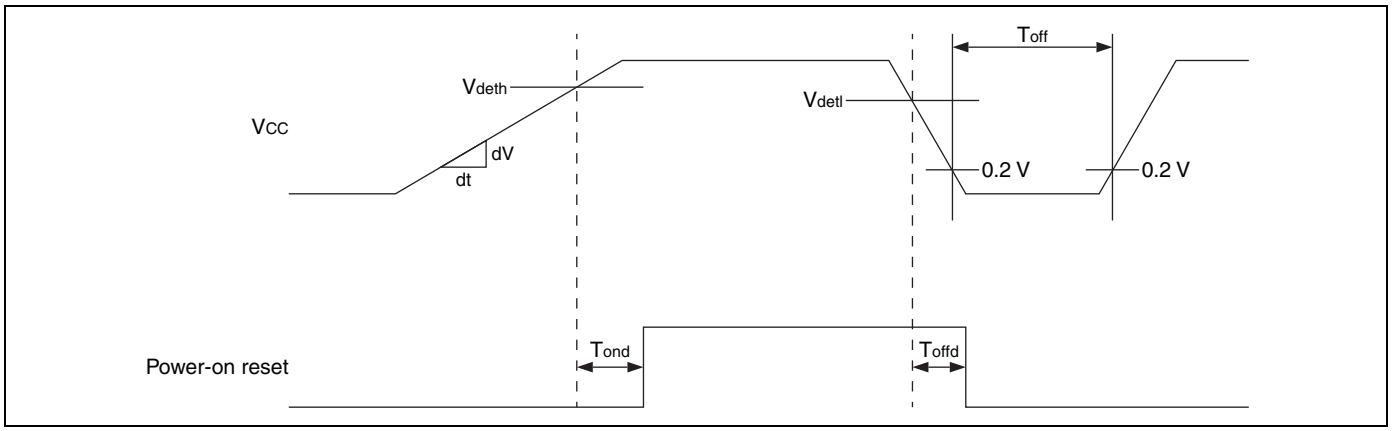
*: See "18.4.2. Source Clock/Machine Clock" for t_{MCLK}.



18.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply rising time	dV/dt	V_{CC}	0.1	—	—	V/ms	
Power supply cutoff time	T_{off}		1	—	—	ms	
Reset release voltage	V_{deth}		1.44	1.60	1.76	V	At voltage rise
Reset detection voltage	V_{detl}		1.39	1.55	1.71	V	At voltage fall
Reset release delay time	T_{ond}		—	—	10	ms	dV/dt ≥ 0.1 mV/µs
Reset detection delay time	T_{offd}		—	—	0.4	ms	dV/dt ≥ –0.04 mV/µs

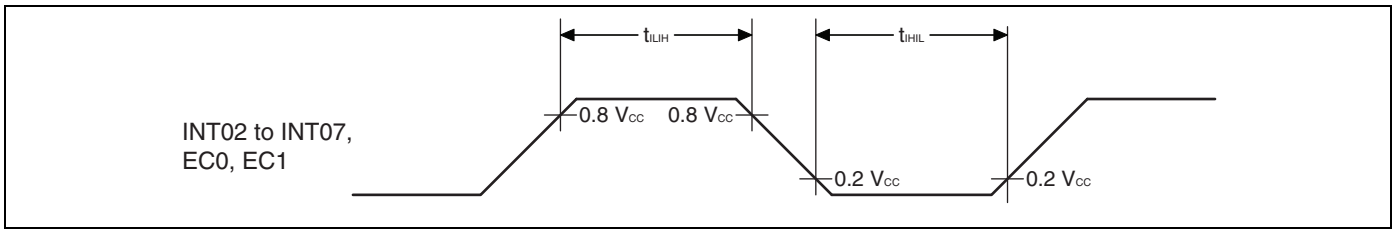


18.4.5 Peripheral Input Timing

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT02 to INT07, EC0, EC1	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.



18.4.6 LIN-UART Timing

*Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

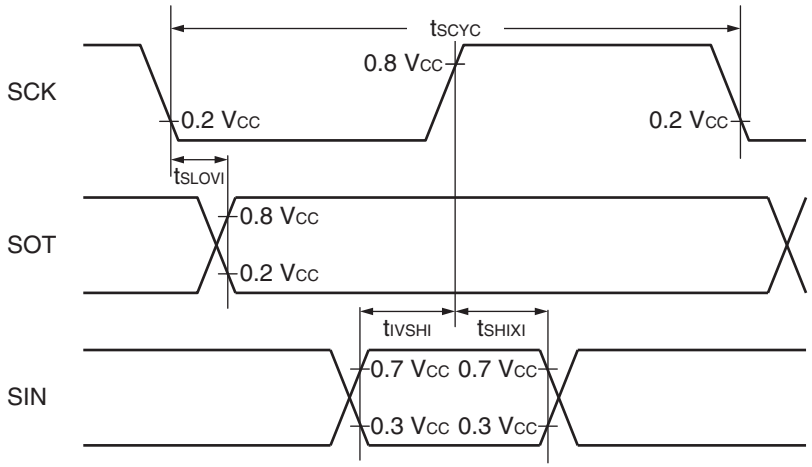
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3–t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 10	—	ns
SCK↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK↑	t_{IVSHE}	SCK, SIN		30	—	ns
SCK↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

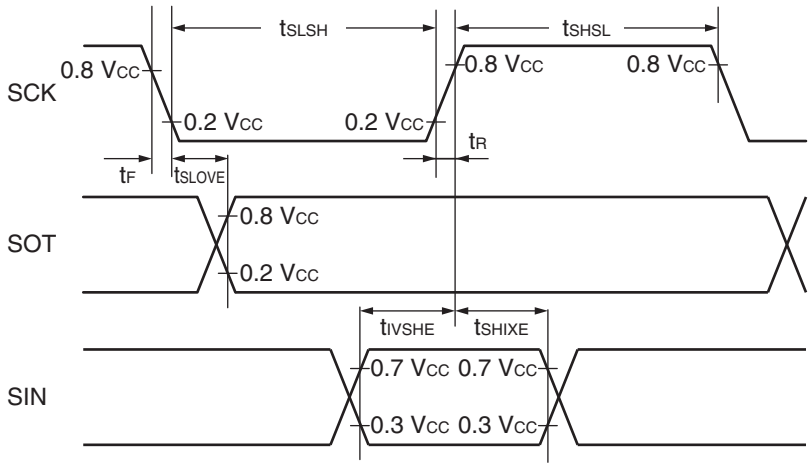
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

Internal shift clock mode



External shift clock mode



*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

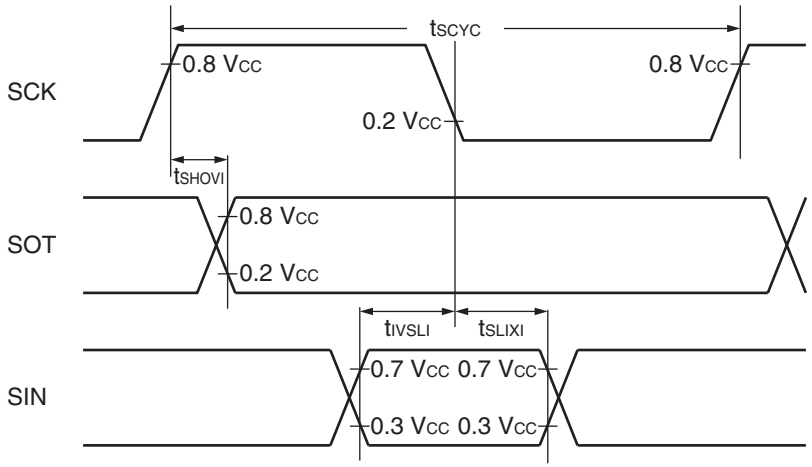
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 – t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 10	—	ns
SCK↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK↓	t_{IVSLE}	SCK, SIN		30	—	ns
SCK↓→ valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

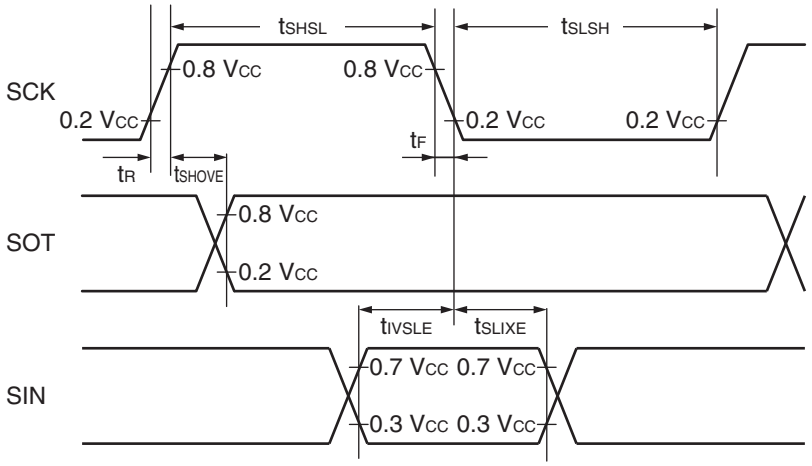
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

Internal shift clock mode



External shift clock mode



*Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2.*
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)

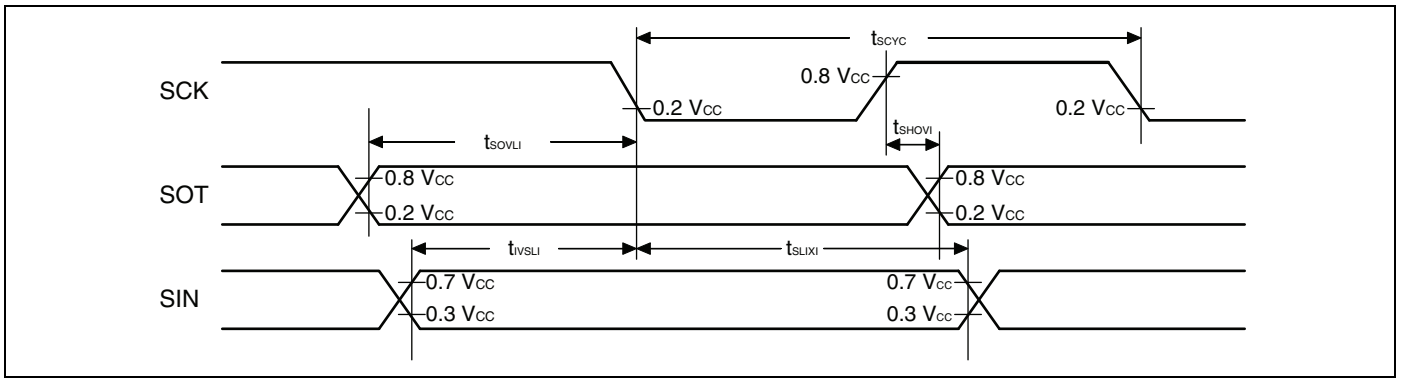
(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK↓delay time	t_{SOVLI}	SCK, SOT		3t_{MCLK}*3 – 70	—	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.



*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2.*
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

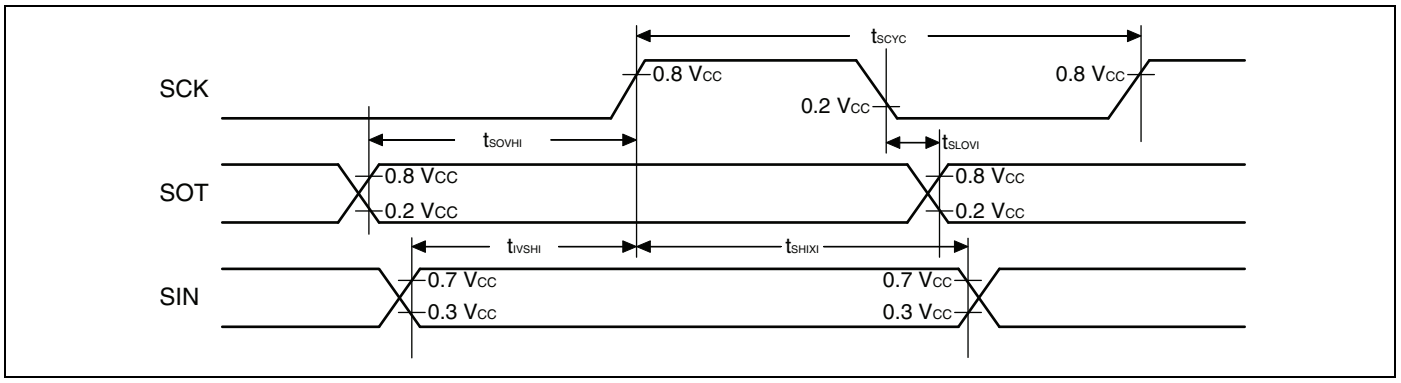
(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK↑delay time	t_{SOVHI}	SCK, SOT		3t_{MCLK}*3 – 70	—	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.



18.4.7 Low-vo ltage Detection

Normal mode

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

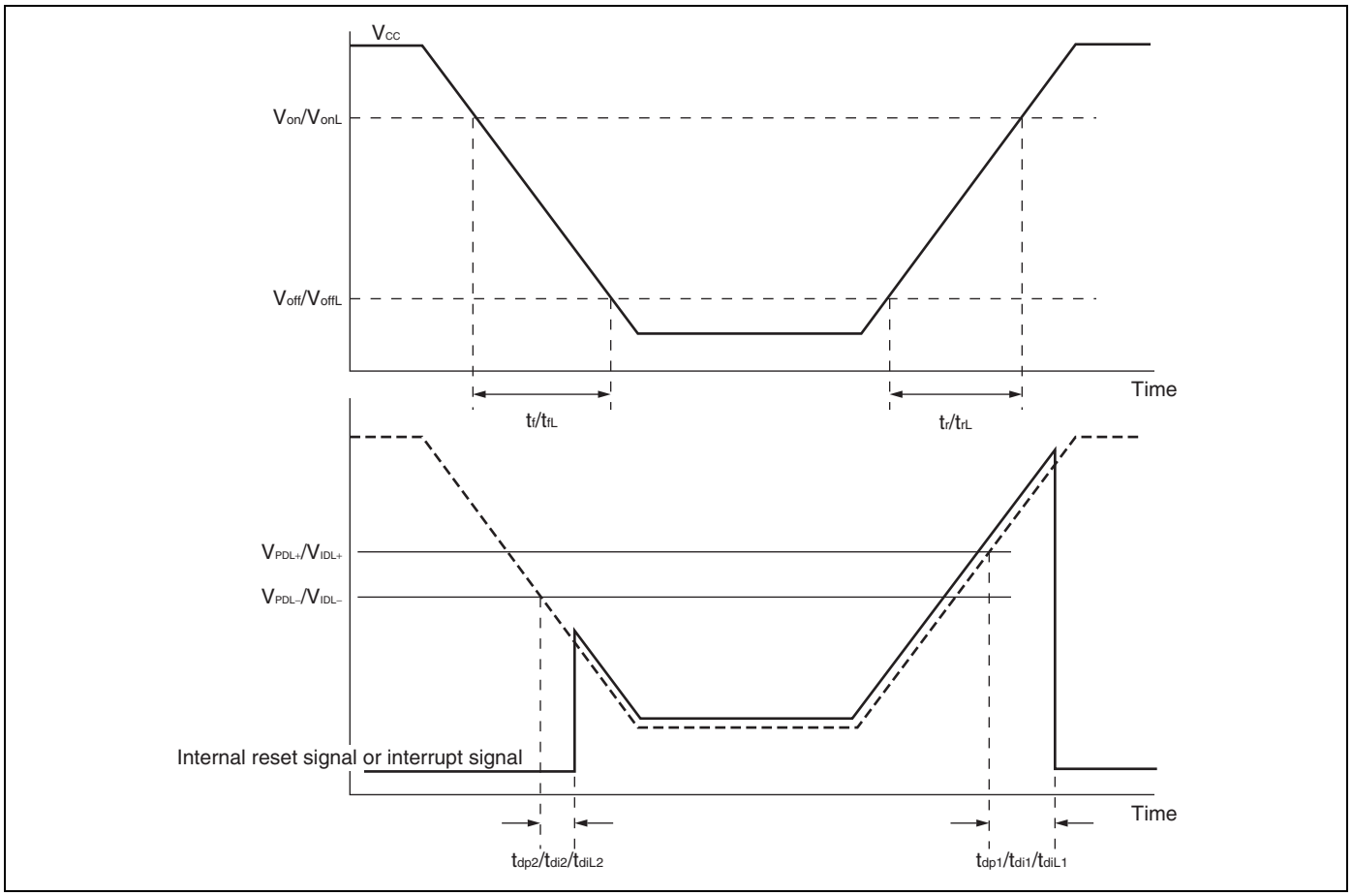
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Reset release voltage	V_{PDL+}	1.88	2.03	2.18	V	At power supply rise
Reset detection voltage	$V_{PDL–}$	1.8	1.93	2.06	V	At power supply fall
Interrupt release voltage 0	V_{IDL0+}	2.13	2.3	2.47	V	At power supply rise
Interrupt detection voltage 0	$V_{IDL0–}$	2.05	2.2	2.35	V	At power supply fall
Interrupt release voltage 1	V_{IDL1+}	2.41	2.6	2.79	V	At power supply rise
Interrupt detection voltage 1	$V_{IDL1–}$	2.33	2.5	2.67	V	At power supply fall
Interrupt release voltage 2	V_{IDL2+}	2.69	2.9	3.11	V	At power supply rise
Interrupt detection voltage 2	$V_{IDL2–}$	2.61	2.8	2.99	V	At power supply fall
Interrupt release voltage 3	V_{IDL3+}	3.06	3.3	3.54	V	At power supply rise
Interrupt detection voltage 3	$V_{IDL3–}$	2.98	3.2	3.42	V	At power supply fall
Interrupt release voltage 4	V_{IDL4+}	3.43	3.7	3.97	V	At power supply rise
Interrupt detection voltage 4	$V_{IDL4–}$	3.35	3.6	3.85	V	At power supply fall
Interrupt release voltage 5	V_{IDL5+}	3.81	4.1	4.39	V	At power supply rise
Interrupt detection voltage 5	$V_{IDL5–}$	3.73	4	4.27	V	At power supply fall
Power supply start voltage	V_{off}	—	—	1.6	V	
Power supply end voltage	V_{on}	4.39	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	697.5	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{PDL+}/V_{IDL+})
Power supply voltage change time (at power supply fall)	t_f	697.5	—	—	µs	Slope of power supply that the reset release signal generates within the rating ($V_{PDL–}$/$V_{IDL–}$)
Reset release delay time	t_{dp1}	—	—	30	µs	
Reset detection delay time	t_{dp2}	—	—	30	µs	
Interrupt release delay time	t_{di1}	—	—	30	µs	
Interrupt detection delay time	t_{di2}	—	—	30	µs	
LVD reset threshold voltage transition stabilization time	t_{stb}	—	—	30	µs	

Low power consumption mode

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Interrupt release voltage 0	V_{IDLL0+}	2.06	2.3	2.54	V	At power supply rise
Interrupt detection voltage 0	$V_{IDLL0–}$	1.98	2.2	2.42	V	At power supply fall
Interrupt release voltage 1	V_{IDLL1+}	2.33	2.6	2.87	V	At power supply rise
Interrupt detection voltage 1	$V_{IDLL1–}$	2.25	2.5	2.75	V	At power supply fall
Interrupt release voltage 2	V_{IDLL2+}	2.6	2.9	3.2	V	At power supply rise
Interrupt detection voltage 2	$V_{IDLL2–}$	2.52	2.8	3.08	V	At power supply fall
Interrupt release voltage 3	V_{IDLL3+}	2.96	3.3	3.64	V	At power supply rise
Interrupt detection voltage 3	$V_{IDLL3–}$	2.88	3.2	3.52	V	At power supply fall
Interrupt release voltage 4	V_{IDLL4+}	3.32	3.7	4.08	V	At power supply rise
Interrupt detection voltage 4	$V_{IDLL4–}$	3.24	3.6	3.96	V	At power supply fall
Interrupt release voltage 5	V_{IDLL5+}	3.68	4.1	4.52	V	At power supply rise
Interrupt detection voltage 5	$V_{IDLL5–}$	3.6	4	4.4	V	At power supply fall
Power supply start voltage	V_{offL}	—	—	1.6	V	
Power supply end voltage	V_{onL}	4.52	—	—	V	
Power supply voltage change time (at power supply rise)	t_{rL}	7300	—	—	µs	Slope of power supply that the interrupt release signal generates within the rating (V_{IDLL+})
Power supply voltage change time (at power supply fall)	t_{fL}	7300	—	—	µs	Slope of power supply that the interrupt detection signal generates within the rating ($V_{IDLL–}$)
Interrupt release delay time	t_{diL1}	—	—	400	µs	
Interrupt detection delay time	t_{diL2}	—	—	400	µs	
Interrupt threshold voltage transition stabilization time	t_{stbL}	—	—	400	µs	
Interrupt low-voltage detection mode switch time	t_{mdsw}	—	—	400	µs	Normal mode ⇔ Low power consumption mode

Note: When used for interrupt, the low-voltage detection circuit can be switched between the normal mode and the low power consumption mode. Compared with the normal mode, while the low power consumption mode has lower detection voltage accuracy and lower release voltage accuracy, it has the lower power consumption. See “18.3 DC Characteristics” for the difference in current consumption between the normal mode and the low power consumption mode. For details of the method for switching between the normal mode and the low power consumption mode, refer to “Chapter 17 Low-voltage Detection Circuit” in “New 8FX MB95650L Series Hardware Manual”.


V_{CC}
V_{on}/V_{onL}
V_{off}/V_{offL}
Time
t_f/t_{fL}
t_r/t_{rL}
V_{PDL+}/V_{IDL+}
V_{PDL-}/V_{IDL-}
Internal reset signal or interrupt signal
Time
$t_{dp2}/t_{di2}/t_{diL2}$
$t_{dp1}/t_{di1}/t_{diL1}$

18.4.8 I^2C Bus Interface Timing

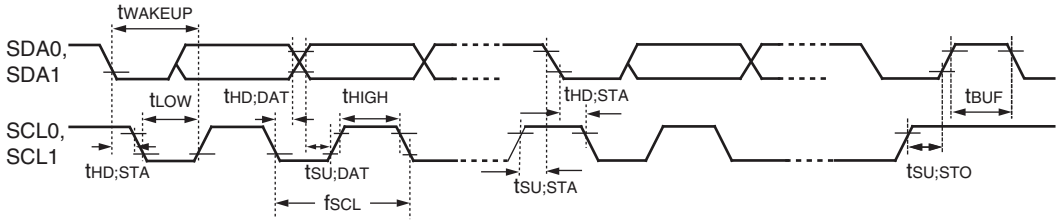
(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL0, SCL1	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL0, SCL1, SDA0, SDA1		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL0, SCL1		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL0, SCL1		4.0	—	0.6	—	µs
(Repeated) START condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL0, SCL1, SDA0, SDA1		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓↑	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓↑ → SCL ↑	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1		0.25	—	0.1	—	µs
STOP condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL0, SCL1, SDA0, SDA1		4	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUF}	SCL0, SCL1, SDA0, SDA1		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL0/1 and SDA0/1 lines, and C the load capacitor of the SCL0/1 and SDA0/1 lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” (t_{LOW}) does not extend.

*3: A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, provided that the condition of $t_{SU;DAT} \geq 250$ ns is fulfilled.



(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL0, SCL1	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm/2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL0, SCL1		$(nm/2)t_{MCLK} - 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL0, SCL1, SDA0, SDA1		$(-1 + nm/2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL0, SCL1, SDA0, SDA1		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL0, SCL1, SDA0, SDA1		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	t_{BUF}	SCL0, SCL1, SDA0, SDA1		$(2\ nm + 4)\ t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		$3\ t_{MCLK} - 20$	—	ns	Master mode

(Continued)

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
Data setup time	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1	R = 1.7 kΩ, C = 50 pF*1	(-2 + nm/2) t_{MCLK} – 20	(-1 + nm/2) t_{MCLK} + 20	ns	Master mode It is assumed that “L” of SCL is not extended. The minimum value is applied to the first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL0, SCL1		(nm/2) t_{MCLK} – 20	(1 + nm/2) t_{MCLK} + 20	ns	The minimum value is applied to the interrupt at the ninth SCL↓. The maximum value is applied to the interrupt at the eighth SCL↓.
SCL clock “L” width	t_{LOW}	SCL0, SCL1		4 t_{MCLK} – 20	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL0, SCL1		4 t_{MCLK} – 20	—	ns	At reception
START condition detection	$t_{HD;STA}$	SCL0, SCL1, SDA0, SDA1		2 t_{MCLK} – 20	—	ns	No START condition is detected when 1 t_{MCLK} is used at reception.
STOP condition detection	$t_{SU;STO}$	SCL0, SCL1, SDA0, SDA1		2 t_{MCLK} – 20	—	ns	No STOP condition is detected when 1 t_{MCLK} is used at reception.
RESTART condition detection condition	$t_{SU;STA}$	SCL0, SCL1, SDA0, SDA1		2 t_{MCLK} – 20	—	ns	No RESTART condition is detected when 1 t_{MCLK} is used at reception.

(Continued)

(Continued)

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
Bus free time	t_{BUF}	SCL0, SCL1, SDA0, SDA1	R = 1.7 kΩ, C = 50 pF*1	2 t_{MCLK} – 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		2 t_{MCLK} – 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1		t_{LOW} – 3 t_{MCLK} – 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1		t_{MCLK} – 20	—	ns	At reception
SDA↓ → SCL↑ (with wakeup function in use)	t_{WAKEUP}	SCL0, SCL1, SDA0, SDA1		Oscillation stabilization wait time +2 t_{MCLK} – 20	—	ns	

*1: R represents the pull-up resistor of the SCL0/SCL1 and SDA0/SDA1 lines, and C the load capacitor of the SCL0/SCL1 and SDA0/SDA1 lines.

*2: • See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.
- m represents the CS[4:3] bits in the I^2C clock control register ch. 0/ch. 1 (ICCR0/ICCR1).
- n represents the CS[2:0] bits in the I^2C clock control register ch. 0/ch. 1 (ICCR0/ICCR1).
- The actual timing of the I^2C bus interface is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS[4:0] bits in the ICCR0/ICCR1 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98), (5, 22), (6, 22), (7, 22) : 0.9 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (8, 22) : 0.9 MHz < t_{MCLK} ≤ 16.25 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22), (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (1, 38), (6, 4), (7, 4), (8, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (5, 8) : 3.3 MHz < t_{MCLK} ≤ 16.25 MHz

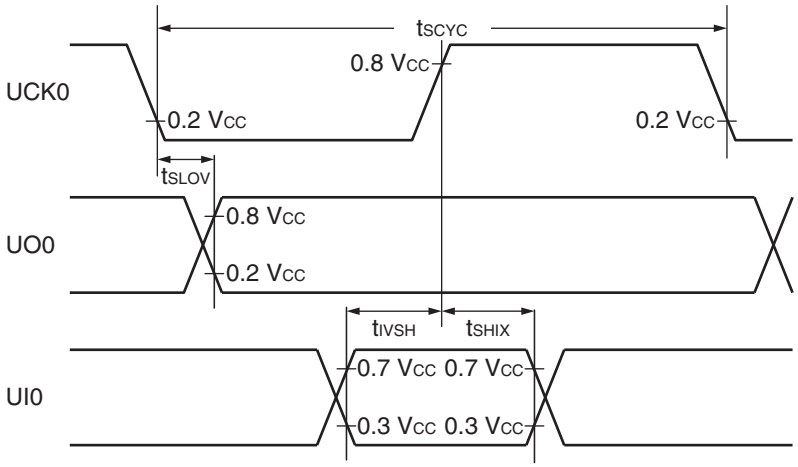
18.4.9 UART/SIO, Serial I/O Timing

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

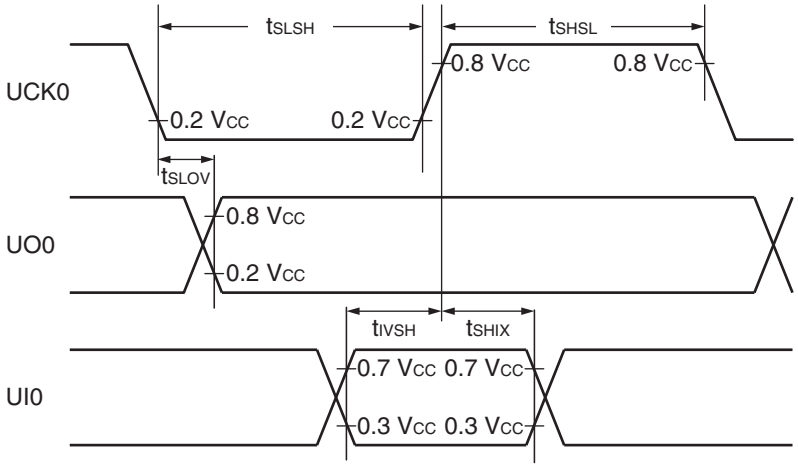
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		–190	+190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0	External clock operation	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns

*: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

Internal shift clock mode



External shift clock mode



18.5 A/D Converter

18.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	12	bit	
Total error		–6	—	+6	LSB	$V_{CC} \geq 2.7$ V
		–10	—	+10	LSB	$V_{CC} < 2.7$ V
Linearity error		–3	—	+3	LSB	$V_{CC} \geq 2.7$ V
		–5	—	+5	LSB	$V_{CC} < 2.7$ V
Differential linearity error		–1.9	—	+1.9	LSB	$V_{CC} \geq 2.7$ V
		–2.9	—	+2.9	LSB	$V_{CC} < 2.7$ V
Zero transition voltage	V_{0T}	V_{SS} – 6 LSB	—	V_{SS} + 8.2 LSB	mV	
Full-scale transition voltage	V_{FST}	V_{CC} – 6.2 LSB	—	V_{CC} + 9.2 LSB	mV	
Sampling time	T_S	*	—	10	µs	
Compare time	T_{cck}	0.861	—	14	µs	$V_{CC} \geq 2.7$ V
		2.8	—	14	µs	$V_{CC} < 2.7$ V
Time of transiting to operation enabled state	T_{stt}	1	—	—	µs	
Analog input current	I_{AIN}	–0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

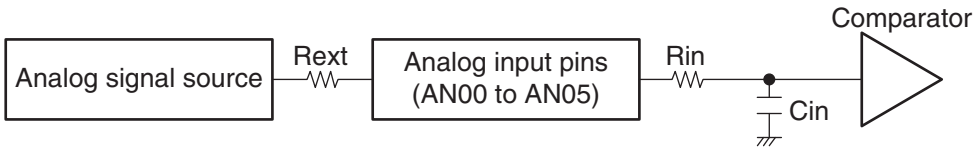
*: See “18.4.2. Notes on Using A/D Converter” for details of the minimum sampling time.

18.5.2 Notes on Using A/D Converter

External impedance of analog input and its sampling time

The A/D converter of the MB95650L Series has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

Analog input equivalent circuit



V_{CC}	Rin	Cin
4.5 V ≤ V_{CC} ≤ 5.5 V	0.9 kΩ (Max)	13 pF (Max)
2.7 V ≤ V_{CC} < 4.5 V	1.6 kΩ (Max)	13 pF (Max)
1.8 V ≤ V_{CC} < 2.7 V	4.0 kΩ (Max)	13 pF (Max)

Note: The values are reference values.

Relationship between external impedance and minimum sampling time

The sampling required varies according to external impedance. Ensure that the following condition is met when setting the sampling time.

$$Ts \geq (Rin + Rext) \times Cin \times 9$$

Ts : Sampling time
Rin : Input resistance of A/D converter
Cin : Input capacitance of A/D converter
Rext : Output impedance of external circuit

A/D conversion error

As $|V_{CC} - V_{SS}|$ decreases, the A/D conversion error increases proportionately.

18.5.3 Definitions of A/D Converter Terms

Resolution

It indicates the level of analog variation that can be distinguished by the A/D converter.

When the number of bits is 12, analog voltage can be divided into 2^{12} = 4096.

Linearity error (unit: LSB)

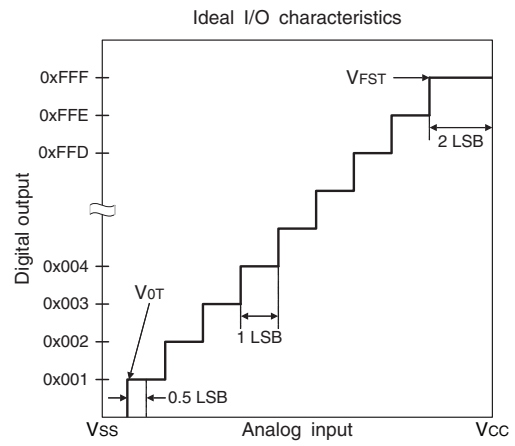
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“000000000000” ← → “000000000001”) of a device to the full-scale transition point (“111111111111” ← → “111111111110”) of the same device.

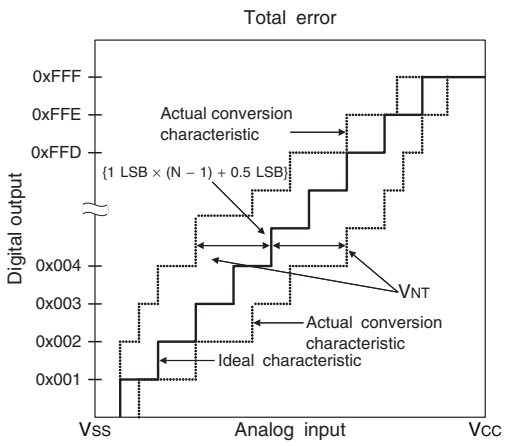
Differential linear error (unit: LSB)

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

Total error (unit: LSB)

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.





$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{4096}\ \text{V}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{LSB}$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

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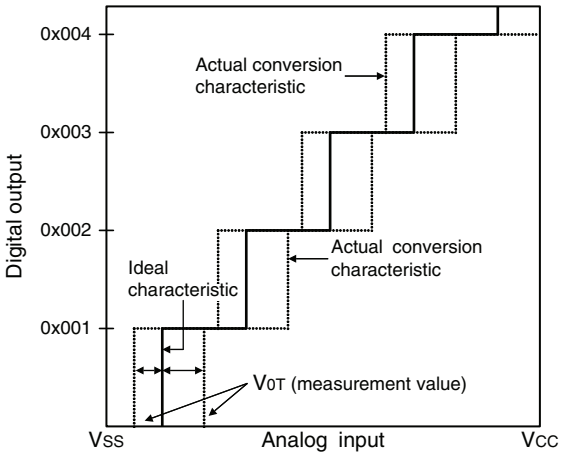
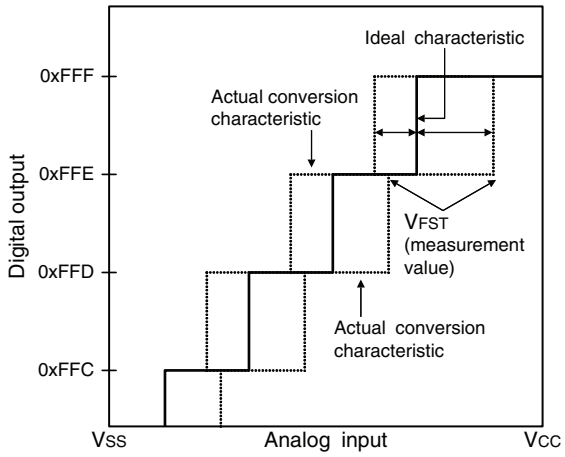
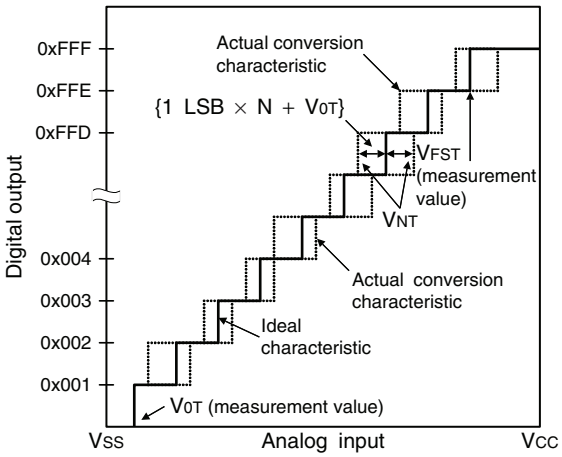
Zero transition error



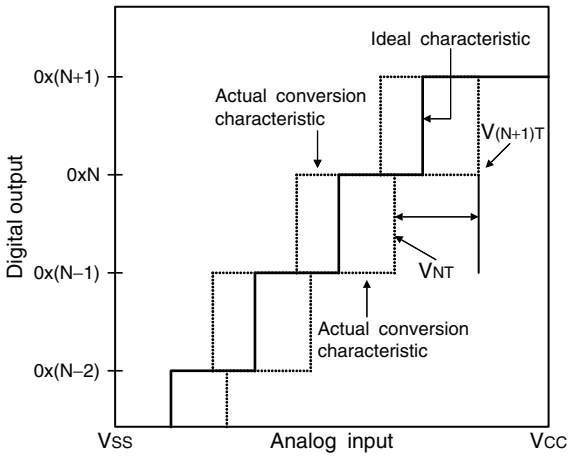
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} – 2 LSB [V]

18.6 Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.3*1	1.6*2	s	The time of writing “0x00” prior to erasure is excluded.
Sector erase time (32 Kbyte sector)	—	0.6*1	3.1*2	s	The time of writing “0x00” prior to erasure is excluded.
Byte writing time	—	17	272	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	1.8	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85 °C Number of program/erase cycles: 1000 or below
	10*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 1001 to 10000 inclusive
	5*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 10001 or above

*1: V_{CC} = 5.5 V, T_A = +25 °C, 0 cycle

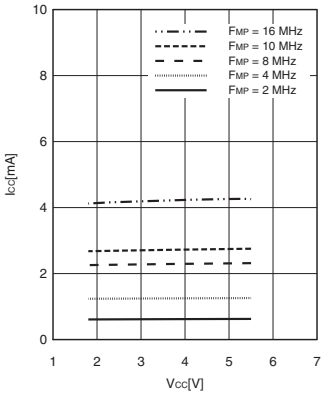
*2: V_{CC} = 1.8 V, T_A = +85 °C, 100000 cycles

*3: These values were converted from the result of a technology reliability assessment. (These values were converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85 °C.)

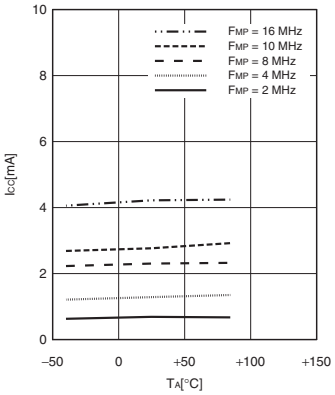
19. Sample Characteristics

Power supply current temperature characteristics

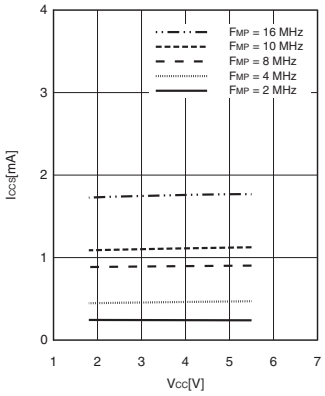
I_{CC} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



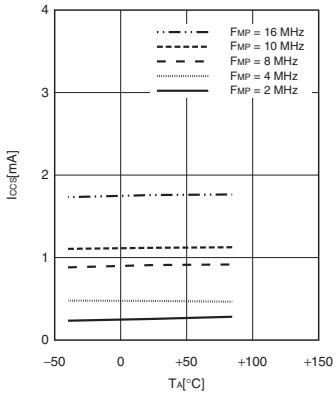
I_{CC} – T_A
V_{CC} = 3.3V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



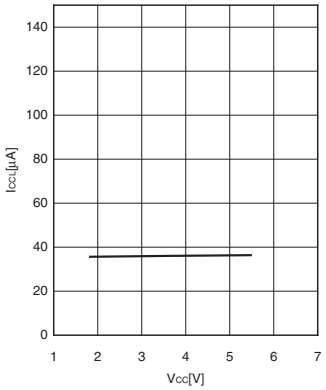
I_{CCS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



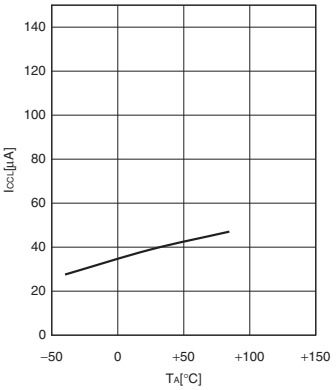
I_{CCS} – T_A
V_{CC} = 3.3 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



I_{CCL} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



I_{CCL} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



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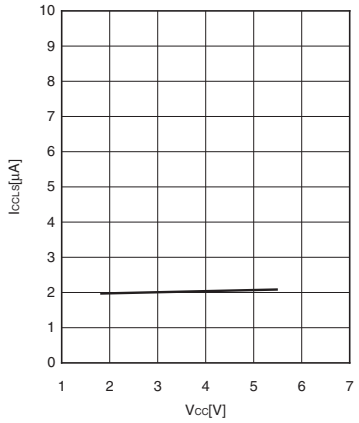
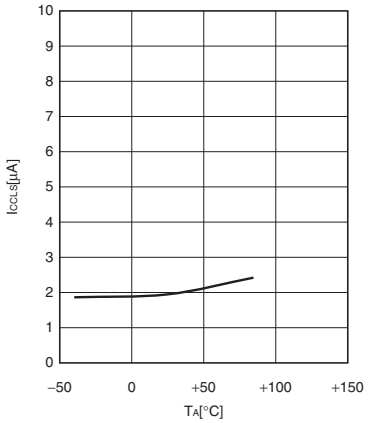
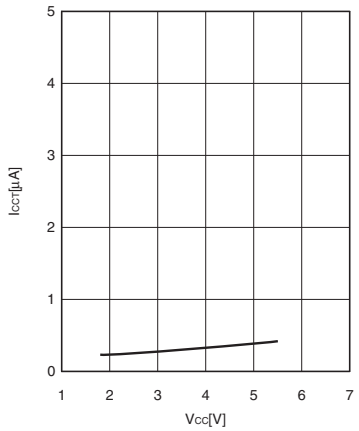
I_{CCLS} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



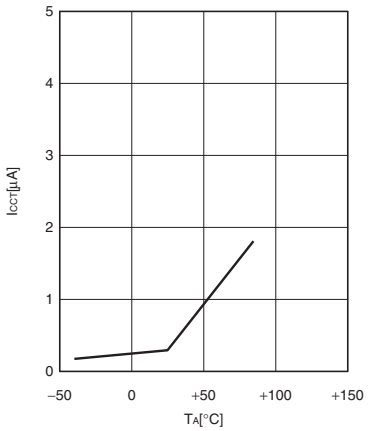
I_{CCLS} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



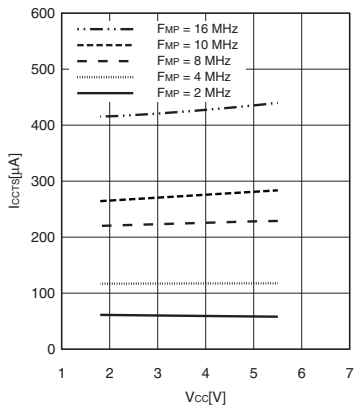
I_{CCT} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



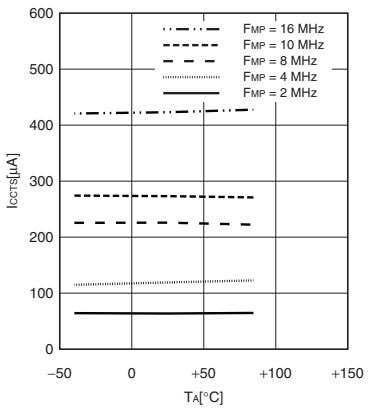
I_{CCT} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



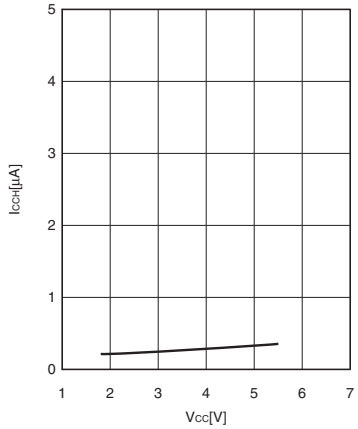
I_{CCTS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



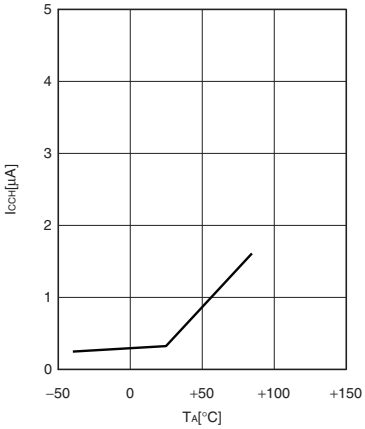
I_{CCTS} – T_A
V_{CC} = 3.3 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



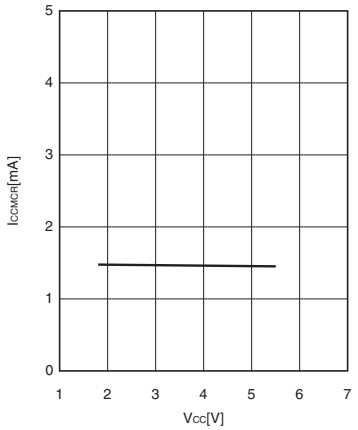
$I_{CCH} - V_{CC}$
T_A = +25 °C, F_{MPL} = (stop)
Substop mode with the external clock stopping



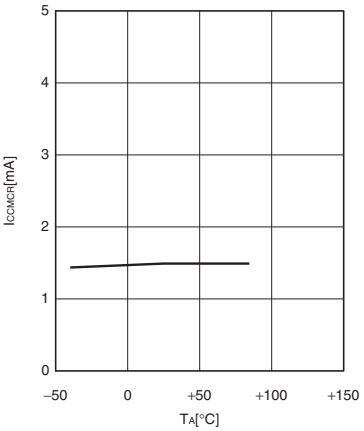
$I_{CCH} - T_A$
V_{CC} = 3.3 V, F_{MPL} = (stop)
Substop mode with the external clock stopping



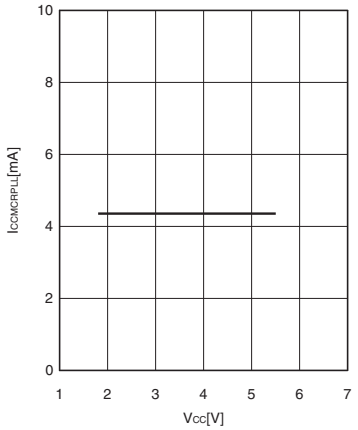
$I_{CCMCR} - V_{CC}$
T_A = +25 °C, F_{MP} = 4 MHz (no division)
Main CR clock mode



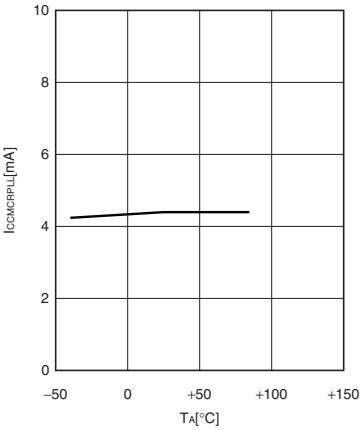
$I_{CCMCR} - T_A$
V_{CC} = 3.3 V, F_{MP} = 4 MHz (no division)
Main CR clock mode



$I_{CCMCRPLL} - V_{CC}$
T_A = +25 °C, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main CR PLL clock mode



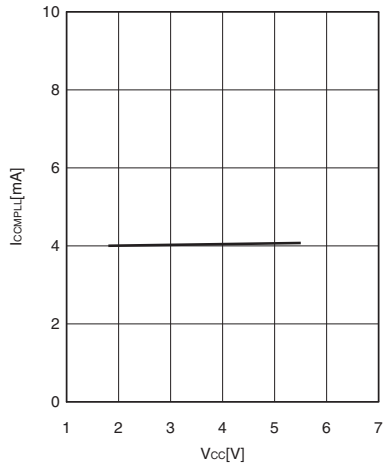
$I_{CCMCRPLL} - T_A$
V_{CC} = 3.3 V, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main CR PLL clock mode



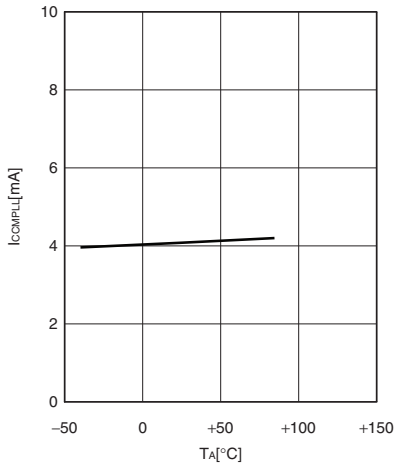
(Continued)

(Continued)

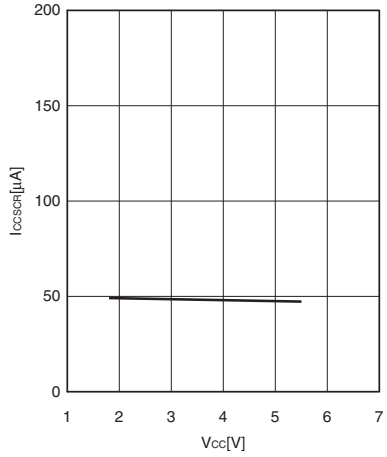
$I_{CCMPLL} - V_{CC}$
T_A = +25 °C, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main PLL clock mode



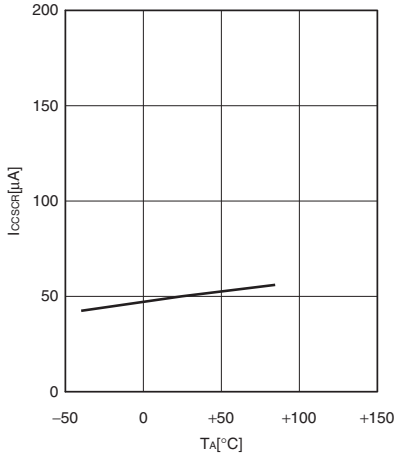
$I_{CCMPLL} - T_A$
V_{CC} = 3.3 V, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main PLL clock mode



$I_{CCSCR} - V_{CC}$
T_A = +25 °C, F_{MPL} = 50 kHz (divided by 2)
Sub-CR clock mode

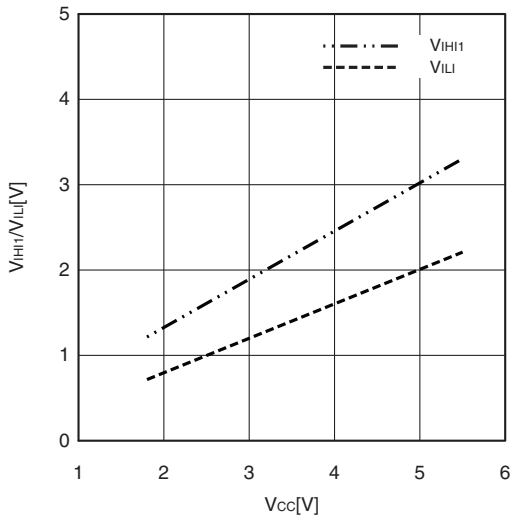


$I_{CCSCR} - T_A$
V_{CC} = 3.3 V, F_{MPL} = 50 kHz (divided by 2)
Sub-CR clock mode

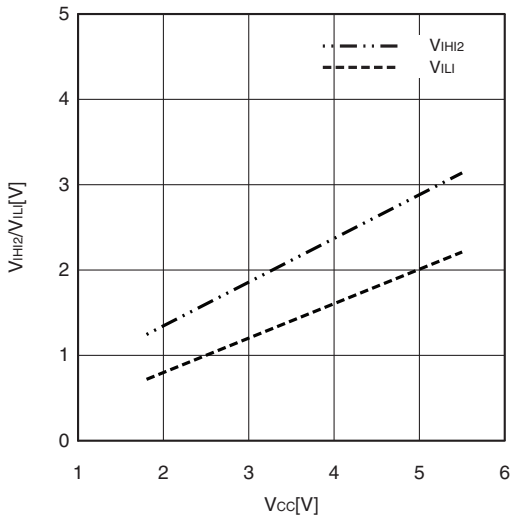


Input voltage characteristics

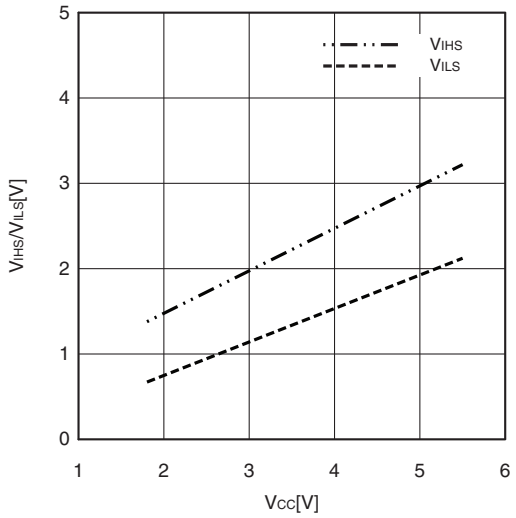
V_{IHI1} – V_{CC} and V_{ILI} – V_{CC}
T_A = +25 °C



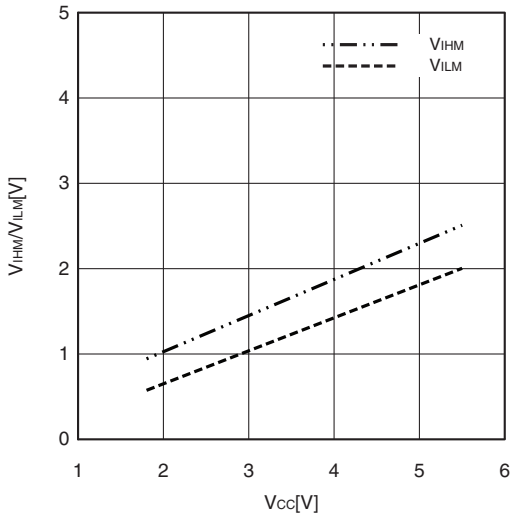
V_{IHI2} – V_{CC} and V_{ILI} – V_{CC}
T_A = +25 °C



V_{IHS} – V_{CC} and V_{ILS} – V_{CC}
T_A = +25 °C

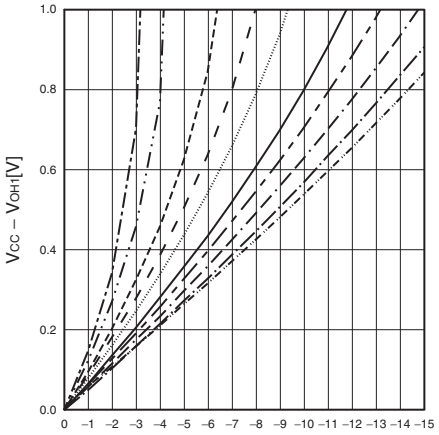


V_{IHM} – V_{CC} and V_{ILM} – V_{CC}
T_A = +25 °C



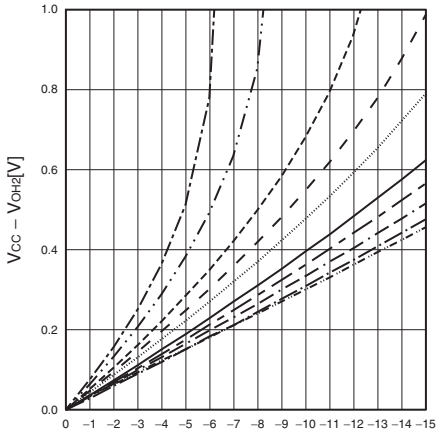
Output voltage characteristics

$(V_{CC} - V_{OH1}) - I_{OH}$
$T_A = +25\ °C$



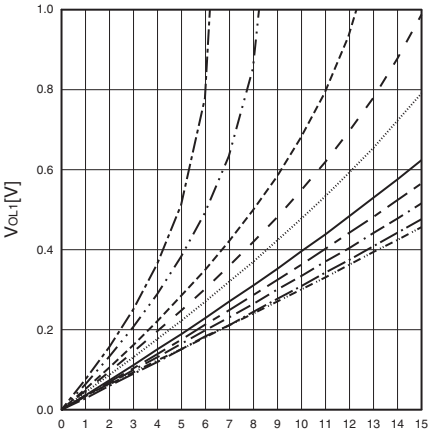
VCC = 1.8 V
VCC = 2.0 V
VCC = 2.4 V
VCC = 2.7 V
VCC = 3.0 V
VCC = 3.6 V
VCC = 4.0 V
VCC = 4.5 V
VCC = 5.0 V
VCC = 5.5 V

$(V_{CC} - V_{OH2}) - I_{OH}$
$T_A = +25\ °C$



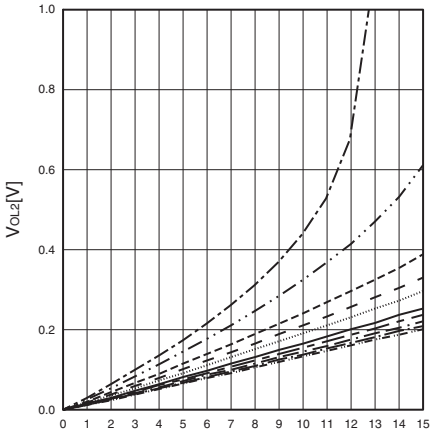
VCC = 1.8 V
VCC = 2.0 V
VCC = 2.4 V
VCC = 2.7 V
VCC = 3.0 V
VCC = 3.6 V
VCC = 4.0 V
VCC = 4.5 V
VCC = 5.0 V
VCC = 5.5 V

$V_{OL1} - I_{OL}$
$T_A = +25\ °C$



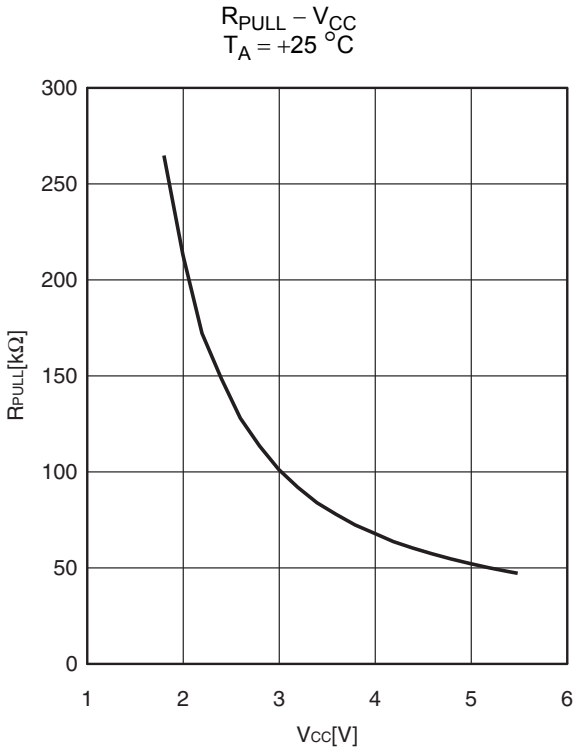
VCC = 1.8 V
VCC = 2.0 V
VCC = 2.4 V
VCC = 2.7 V
VCC = 3.0 V
VCC = 3.6 V
VCC = 4.0 V
VCC = 4.5 V
VCC = 5.0 V
VCC = 5.5 V

$V_{OL2} - I_{OL}$
$T_A = +25\ °C$



VCC = 1.8 V
VCC = 2.0 V
VCC = 2.4 V
VCC = 2.7 V
VCC = 3.0 V
VCC = 3.6 V
VCC = 4.0 V
VCC = 4.5 V
VCC = 5.0 V
VCC = 5.5 V

Pull-up characteristics



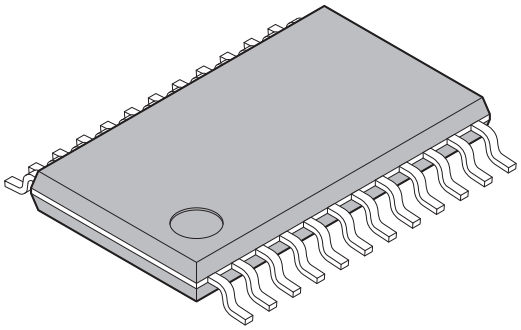
20. Mask Options

No.	Part number	MB95F652E MB95F653E MB95F654E MB95F656E	MB95F652L MB95F653L MB95F654L MB95F656L
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset/interrupt	With low-voltage detection reset/interrupt	Without low-voltage detection reset/interrupt
2	Reset	Without dedicated reset input	With dedicated reset input

21. Ordering Information

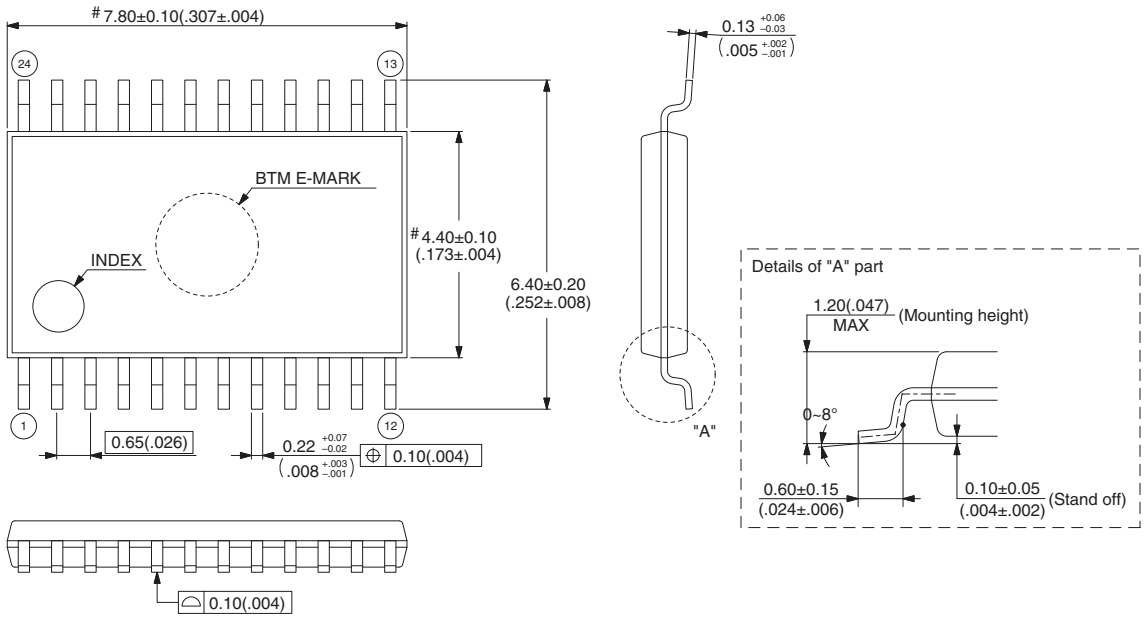
Part number	Package
MB95F652EPFT-G-SNE2 MB95F652LPFT-G-SNE2 MB95F653EPFT-G-SNE2 MB95F653LPFT-G-SNE2 MB95F654EPFT-G-SNE2 MB95F654LPFT-G-SNE2 MB95F656EPFT-G-SNE2 MB95F656LPFT-G-SNE2	24-pin plastic TSSOP (FPT-24P-M10)
MB95F652EPF-G-SNE2 MB95F652LPF-G-SNE2 MB95F653EPF-G-SNE2 MB95F653LPF-G-SNE2 MB95F654EPF-G-SNE2 MB95F654LPF-G-SNE2 MB95F656EPF-G-SNE2 MB95F656LPF-G-SNE2	24-pin plastic SOP (FPT-24P-M34)
MB95F652EWQN-G-SNE1 MB95F652EWQN-G-SNERE1 MB95F652LWQN-G-SNE1 MB95F652LWQN-G-SNERE1 MB95F653EWQN-G-SNE1 MB95F653EWQN-G-SNERE1 MB95F653LWQN-G-SNE1 MB95F653LWQN-G-SNERE1 MB95F654EWQN-G-SNE1 MB95F654EWQN-G-SNERE1 MB95F654LWQN-G-SNE1 MB95F654LWQN-G-SNERE1 MB95F656EWQN-G-SNE1 MB95F656EWQN-G-SNERE1 MB95F656LWQN-G-SNE1 MB95F656LWQN-G-SNERE1	32-pin plastic QFN (LCC-32P-M19)

22. Package Dimension

24-pin plastic TSSOP		
	Lead pitch	0.65 mm
	Package width × package length	4.40 mm × 7.80 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.10 g
(FPT-24P-M10)		

24-pin plastic TSSOP
(FPT-24P-M10)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) #: These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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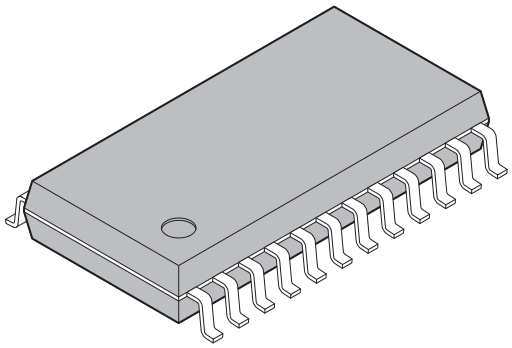
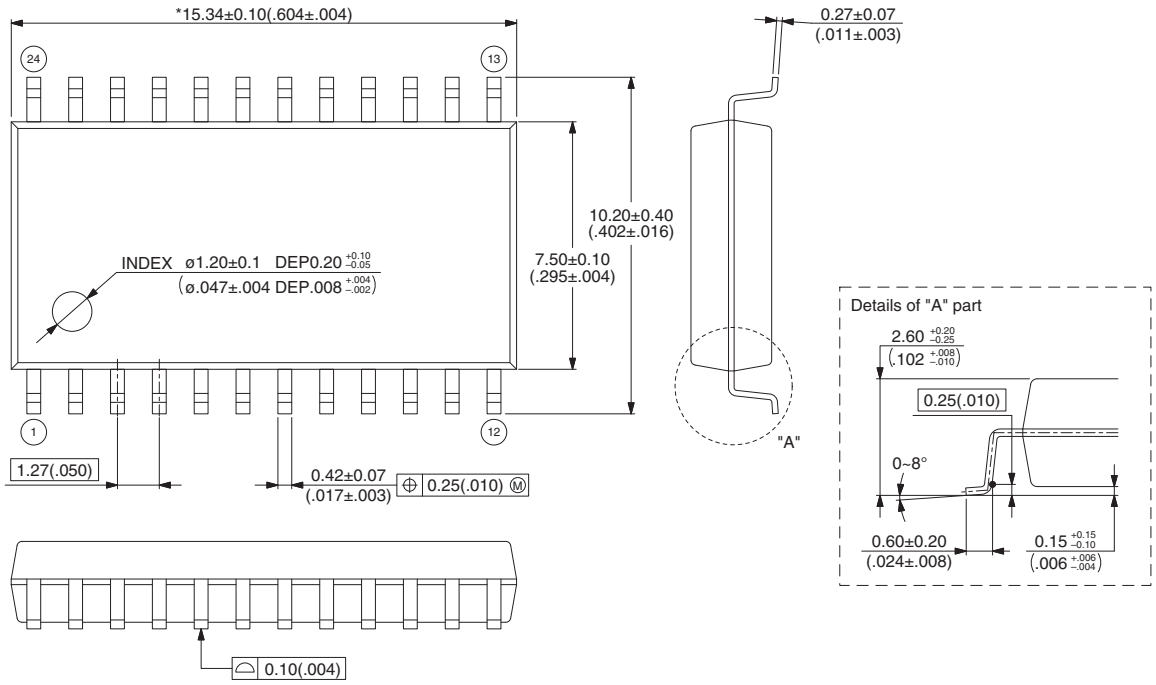
24-pin plastic SOP		
	Lead pitch	1.27 mm
	Package width × package length	7.50 mm × 15.34 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	2.80 mm MAX
(FPT-24P-M34)	Weight	0.44 g

24-pin plastic SOP
(FPT-24P-M34)

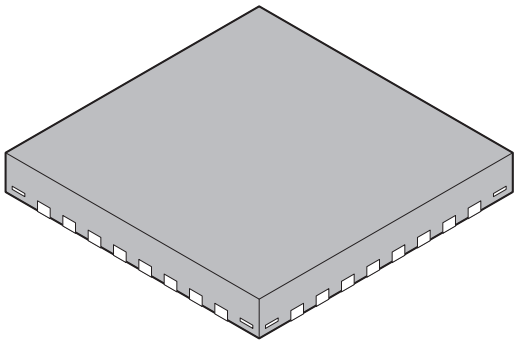
Note 1) * : These dimensions do not include resin protrusion.



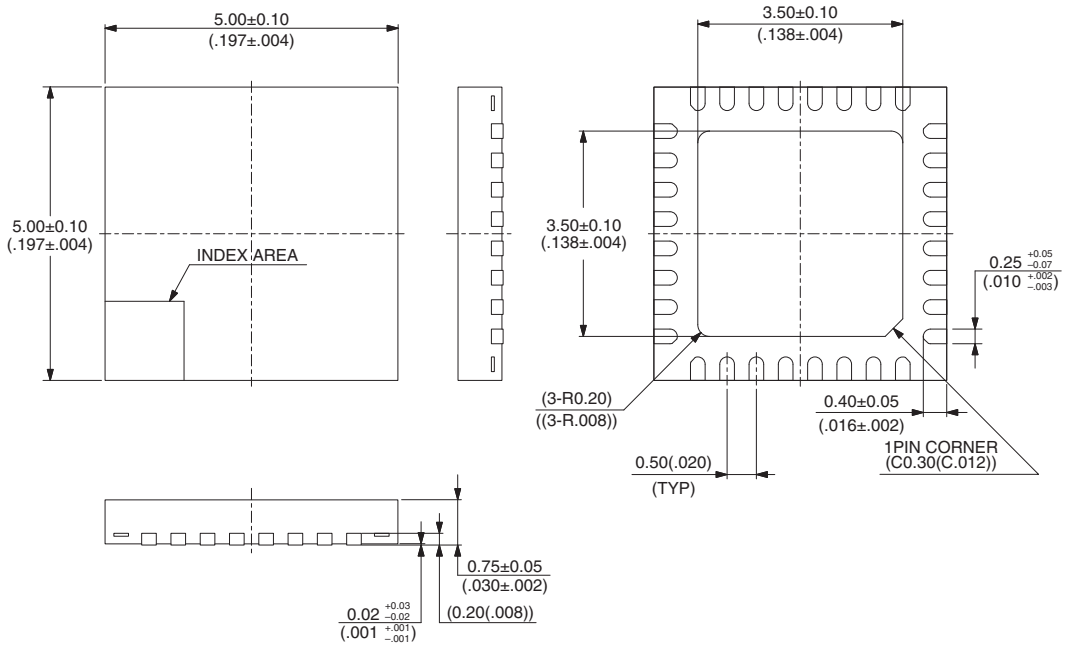
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

(Continued)

32-pin plastic QFN  (LCC-32P-M19)	Lead pitch	0.50 mm
	Package width × package length	5.00 mm × 5.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.06 g

32-pin plastic QFN
(LCC-32P-M19)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

23. Major Changes

Spansion Publication Number: DS702–00016–3v0-E

Page	Section	Details
19	Pin Connection • C pin	Corrected the following statement. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. → The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S.
64	Electrical Characteristics 4. AC Characteristics (1) Clock Timing	Corrected the pin name of the parameter “Input clock rising time and falling time”. X0 → X0, X0A

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB95650L Series New 8FX 8-bit Microcontrollers Document Number: 002-04696				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	06/14/2013	Migrated to Cypress and assigned document number 002-04696. No change to document contents or format.
*A	5216808	AKIH	04/12/2016	Updated to Cypress format.
*B	5846146	YSAT	08/07/2017	Adapted new Cypress logo

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