IS6608A

3.3V to 16V Input, 35A Stackable Multi-Phase Sync Step-Down Converter W/ PMBus1.3 supporting telemetry

Rev2.4 2021/09/04

Part Number	Input Voltage	Output Voltage	Current Rating
IS6608A	3.3V~16V	0.5V~5.5V	30A

Description

The IS6608A is a fully integrated synchronous buck converter with advanced non-linear current mode control. It has the highest power density in industry. With its wide input voltage range, it can support up to 30A continuous output current at defined conditions. A maximum 8 converters can be paralleled to form multi-phase operation and support up to 280A load current. During multi-phase operation, the converter can support dynamic auto-phase dropping and adding to achieve the highest efficiency.

The IS6608A enables single input operation due to built-in analog bias LDO. External bias can be used to further improve efficiency. An accurate differential sensing scheme together with a precision internal 0.6V, ±1% reference voltage helps to achieve excellent line and load regulation over temperature range.

The IS6608A has fully integrated protection features including OCP, NOCP, OVP, UVP and over temperature protection (OTP). In addition, 4 Switching frequencies, 400kHz, 600kHz, 800kHz and 1MHz can be easily programmed.

The IS6608A utilizes PMBus 1.3 interface for device operating settings and telemetry functions.

The IS6608A is available in a 25-pin FCQFN 4mm x 5mm package.

Applications

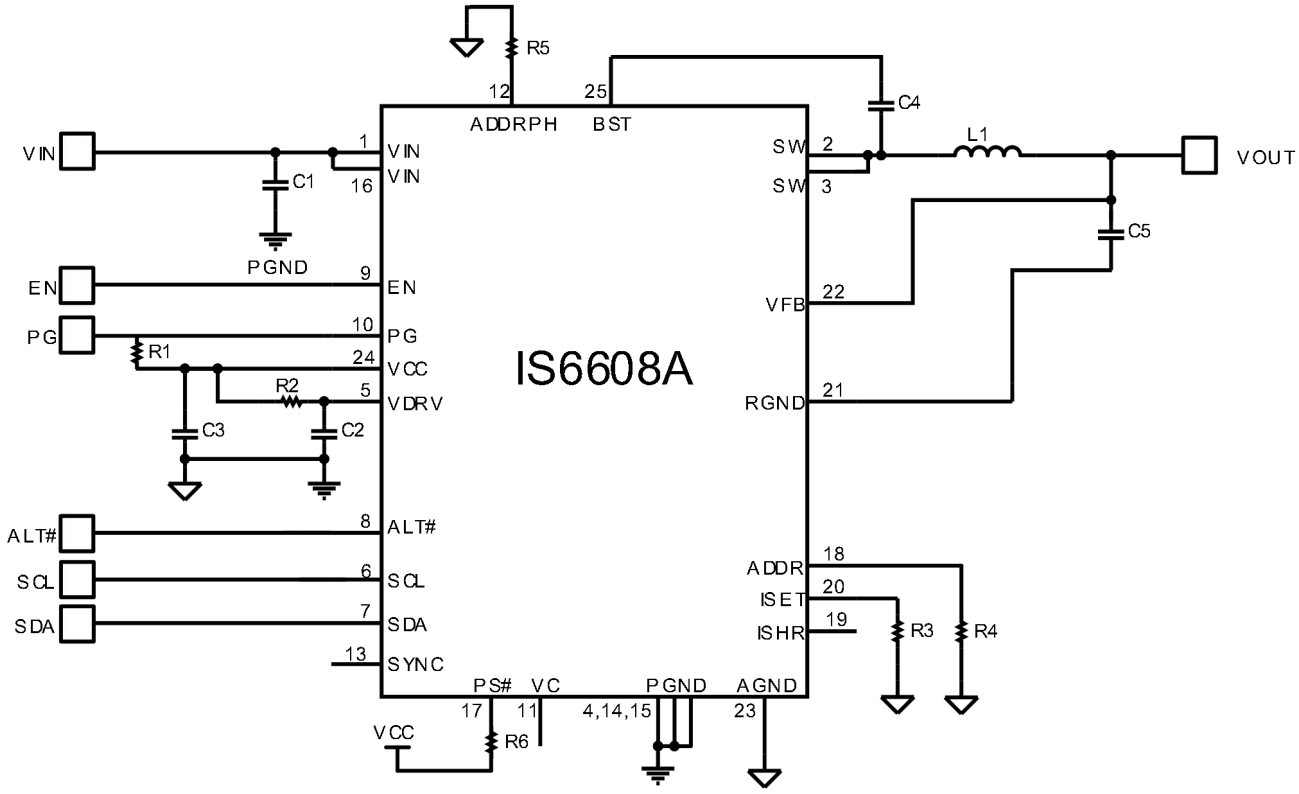
Telecom/Datacom

Computers and Servers

Features

- Advanced non-linear with Fast Transient Response.
- With External Bias: Input Voltage Range: 3.3 V to 16V.
- With Internal Bias: Input Voltage Range: 4.5V to 16V.
- Output Voltage Range: 0.5V to 5.5V, and 90% Max Duty Cycle.
- 30A Continuous Output Current and 35A peak current.
- Excellent Load and Line Regulations with 0.5% Voltage Accuracy.
- Up to 90% Efficiency at V_{IN}=12V, V_{OUT}=1.2V
- Differential Remote Sense
- Pre-bias Start-up
- Junction Temperature Range from -40ºC to 125ºC
- 10μA Current into VIN Pin during Shutdown
- Adjustable Switching Frequency: 400kHz, 600kHz, 800kHz and 1MHz
- OCP, NOCP, OVP, UVLO and OTP
- PMbus 1.3 supporting telemetry functions
- QFN 4mm x 5mm Package with 25-Pin

Typical Application Circuit



Order Information

Part Number	Package	Shipping Method	Package Marking
IS6608A-XXXX	QFN-25(4mm x 5mm)	3000u Tape & Reel	IS6608A

The correct part number to order is “IS6608A-XXXX”. The numeric suffix XXXX represents unique configuration setting for the device. Each X could have a HEX value between 0 and F. Please work with the company FAE to create this set of numbers.

TOP MARKING (IS6608A)

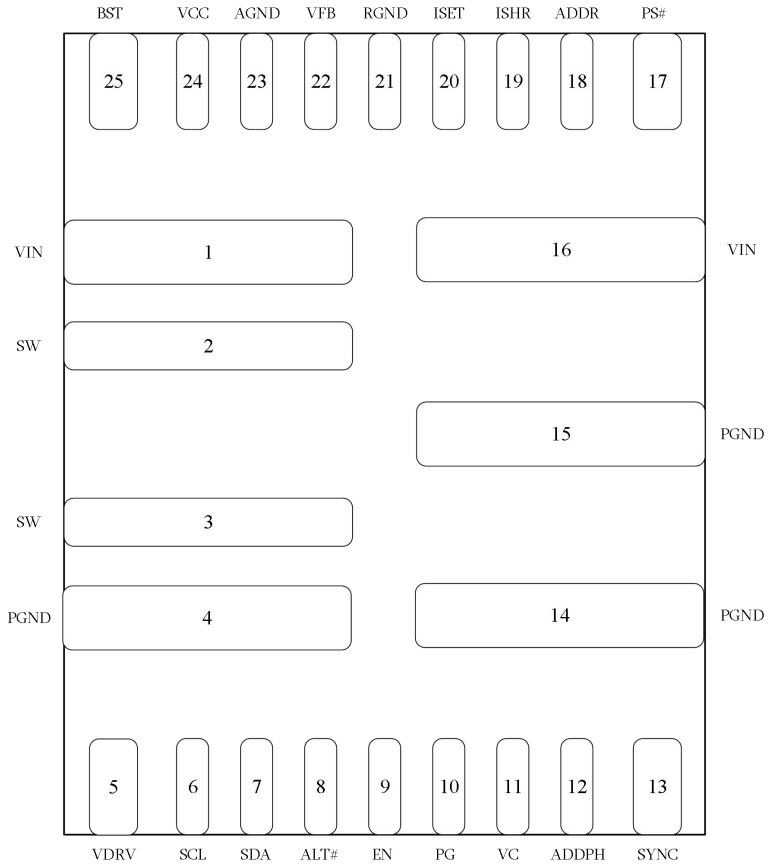
IS6608A

C12TC8

YYWW

IS: Innovision Semiconductor prefix
6608A: Part number
C12TC8: Lot ID
YYWW : Year code and Week code

Package Reference



Top View

Absolute Maximum Ratings

Supply Voltage (V_{in})	-0.3V to 20V
V_{cc} Voltage (V_{cc})	-0.3V to 5.5V
Switch Node Voltage (V_{SW}) DC	-0.3V to 20V
Switch Node Voltage (V_{SW}) 25ns	-5V to 25V
BST Pin (V_{bst}) DC	-0.3V to 23.5V
BST Pin (V_{bst}) 25ns	-5V to 29V
All other pins	-0.3V to 5.5V
Junction Temperature (T_j)	150°C
Storage Temperature	-65°C to 150°C

Recommended Operating Conditions

Supply Voltage (V_{in})	3.3V to 16V
V_{cc} Voltage (V_{cc})	3.0V to 5V
Output Voltage (V_o)	0.4V to 5.5V
Max Output Current (I_{o_max})	35A
Junction Temperature (T_j)	-40°C to 125°C

Thermal Ratings

Θ_{JC} Max	6°C/W
Θ_{JB} Typ (Still Air, No Heat sink)	1.8°C/W

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

Electrostatic Discharge	Standard	Value
Human Body Mode (HBM)	JEDEC EIA/JESD22-A114	±2000V
Charge Device Mode (CDM)	JEDEC EIA/JESD22-C101F	±2000V

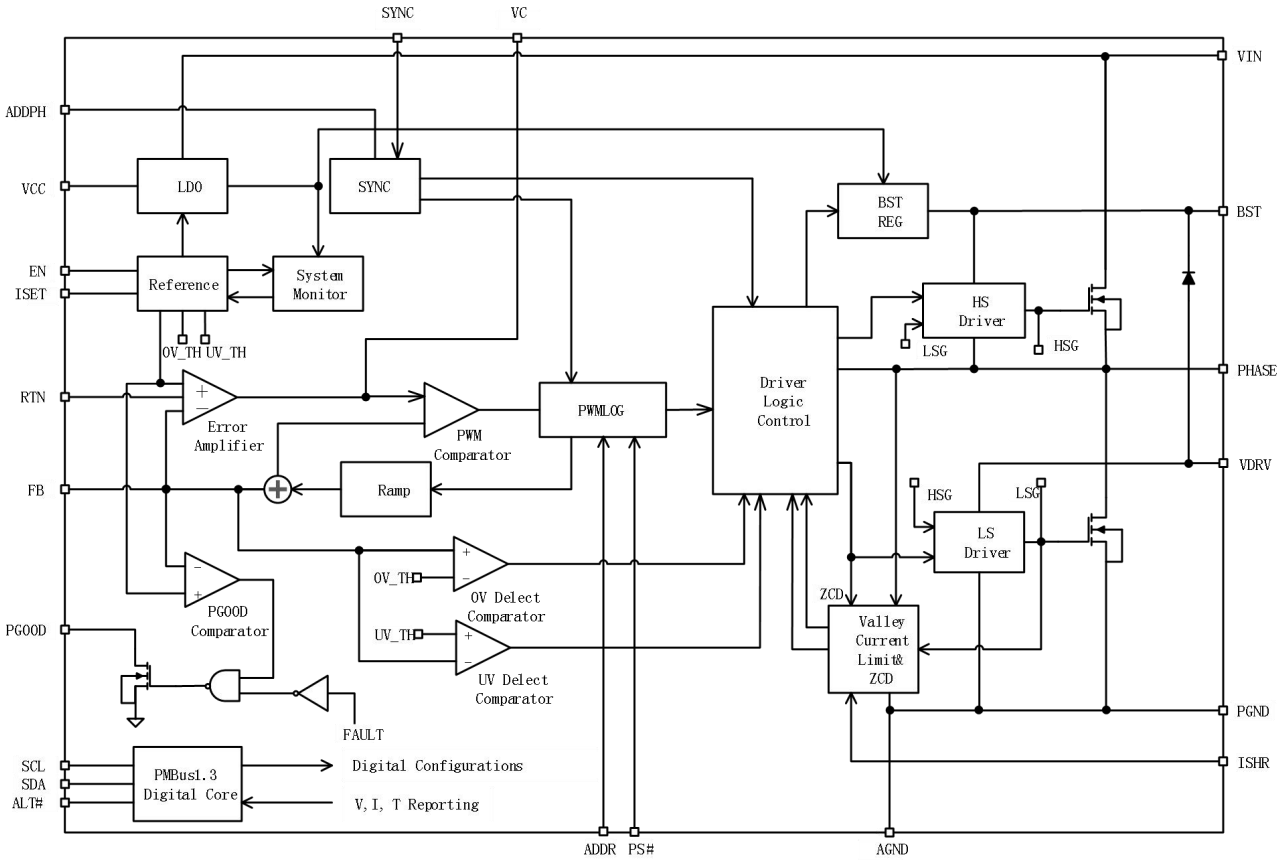
1). JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2). JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Pin Out and Package

IS6608A(QFN-25)

Pin Number	Name	Description
1, 16	VIN	Supply voltage. Input to the power stage and internal LDO. Make the connection with wide PCB traces.
2, 3	SW	Switch output. Switch node of power stage. Connect PH to the inductor and bootstrap capacitor. Make the connection with wide PCB traces
4, 14, 15	PGND	System ground. PGND is power ground of the power stage. Make the connection with wide PCB traces.
5	VDRV	Supply power for the drive and control circuits
6	SCL	PMBus Clock pin
7	SDA	PMBus Data pin
8	ALT#	PMBus Alert pin
9	EN	Enable pin. An input signal which turns the regulator on or off. Connect EN pin to VIN through a pull-dowm and pull-up resistor divider. Do not float this pin
10	PG	Power good output with open drain. If the output voltage is within regulation, the pull-up resistor is required to indicate high
11	VC	Voltage loop control signal
12	ADDPH	Phase address setting. A resistor to ground to set the PWM phase
13	SYNC	Synchronization pin. Connect all devices together for PWM timing synchronization
17	PS#	Phase shedding pin. High voltage is to enable the phase shedding. Low voltage is to disable it. Suggest adding a pull-up resistor to VCC
18	ADDR	PMBus address setting pin.
19	ISHR	Current sharing pin. Connect all devices together for current sharing
20	ISET	A reference current setting. Connect a resistor to AGND to set the internal reference current
21	RGND	Output remote sense feedback. Connect the pin to the negative side of the voltage sense point.
22	VFB	Output remote sense return. An external resistor divider from the output to RTN (tapped to FB) sets the output voltage.
23	AGND	Signal logic ground. A Kelvin connection to PGND is required.
24	VCC	Internal 5V LDO output. Supply power for the control circuits.
25	BST	Bootstrap connection. Connect a capacitor between PHASE and BST, which is required to form a floating supply across the high-side switch driver.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VIN Supply Current						
Supply current (quiescent)	I_{IN}	VCTRL = 0V		2	4	mA
MOSFET						
RDS(ON)	$R_{on\ HS}$	TJ = 25°C		4.2		mΩ
	$R_{on\ LS}$	TJ = 25°C		1.4		
Switch leakage	I_{SWLKG_HS}	SW = 0V			10	μA
	$I_{SW\ LKG\_LS}$	SW = 12V			20	
Output Current Limit						
Output current limit (inductor valley)	I_{LIM_VALLEY}	D7h = 0x14	27	30	33	A
Min output current limit(inductor valley) programmable value	$I_{LIM\_VALLEY\_MIN}$			1.5		A
Max output current limit (inductor valley) programmable value	$I_{LIM\_VALLEY\_MAX}$		36	40	44	A
Output current limit (DC)	I_{LIM_DC}	46h = 0x007C (per-phase)		30		A
Min output over-current programmable value	$I_{LIM\_DC\_MIN}$			3		A
Max output over-current warning programmable value	$I_{LIM\_DC\_MAX}$	46h = 0x00BA (per-phase)		45		A
Output over-current warning (DC)	I_{WARN}	4Ah = 0x0074 (per-phase)	25	28	31	A

Min output over-current warning programmable value				3		A
Max output over-current warning programmable value		4Ah = 0x00BA (per-phase)		45		A
Low-side negative current limit in OVP	$I_{LIM\_NEG\_OVP}$	D5h[2] = 1b'0		-13		A
		D5h[2] = 1b'1		-20		
Low-side negative current limit in OSM	$I_{LIM\_NEG\_OSM}$			-10		A
Frequency and Timer						
Switching frequency	f_{SW}	Vo = 1V, Io = 0A, T A = 25°C, (D2h[2:1] = 2b'00)		400		kHz
		Vo = 1V, Io = 0A, T A = 25°C, (D2h[2:1] = 2b'01)		600		kHz
		Vo = 1V, Io = 0A, T A = 25°C, (D2h[2:1] = 2b'10)		800		kHz
		Vo = 1V, Io = 0A, T A = 25°C, (D2h[2:1] = 2b'11)		1000		kHz
Minimum on time	T_{ON_MIN}	Fs = 1000kHz, Vo = 0.6V			50	ns
Minimum off time	T_{OFF_MIN}	VFB = 580mV			150	ns
Output Over-Voltage and Under-Voltage Protection (OVP, UVP)						
OVP threshold	V_{OVP}	Default setting (D4h[1:0] = 2b'00)		1.15		VREF
UVP threshold	V_{UVP}	Default setting (D9h[3:2] = 2b'10)		0.8		VREF
Max programmable OVP threshold	V_{OVP_max}	D4h[1:0] = 2b'11		1.3		VREF
Min programmable OVP threshold	V_{OVP_min}	D4h[1:0] = 2b'00		1.15		VREF

OVP threshold resolution		Per LSB		0.05		VREF
Max programmable UVP threshold	V_{UVP_max}	D9h[3:2] = 2b'11		0.85		VREF
Min programmable UVP threshold	V_{UVP_min}	D9h[3:2] = 2b'00		0.7		VREF
UVP threshold resolution		Per LSB		0.05		VREF
OSM threshold rising	V_{OSM_RISE}	EAh[9] = 1b'0		1.05		VREF
OSM threshold falling	V_{OSM_FALL}			1.025		VREF
EN						
Input high voltage	V_{IH_EN}		2.8			V
Input low voltage	V_{IL_EN}				1.3	V
ADC						
Input voltage range			0		1.28	V
ADC resolution				10		Bits
DNL				1.5		LSB
Sample rate				3		kHz
DAC (Feedback Voltage)						
Range			512	600	672	mV
Feedback accuracy	V_{FB}	21h = 0x012C, D1h[1:0] = 2b'00	594	600	606	mV
Resolution		Per LSB		2		mV
Output voltage slew rate		Default setting (DAh[3:0] = 4b'0000)		20		µs/2mV
Minimum output voltage slew rate		DAh[3:0] = 4b'1111	30	40	50	µs/2mV
Maximum output voltage slew rate		DAh[3:0] = 4b'0000		10		µs/2mV
Maximum feedback voltage with margin	$V_{FB\_MG\_HIGH\_MAX}$			672		mV

Minimum feedback voltage with margin	$V_{FB\_MG\_LOW\_MIN}$			512		mV
Feedback voltage with margin high	$V_{FB\_MG\_HIGH}$			672		mV
Feedback voltage with margin low	$V_{FB\_MG\_LOW}$			512		mV
Soft Start and Turn-On Delay						
Soft-start time	t_{SS}	61h[2:0] = 3b'001		2		ms
Min programmable soft-start time	t_{SS_min}	61h[2:0] = 3b'000		1		ms
Max programmable soft-start time	t_{SS_max}			16		ms
Turn-on delay	t_{ON_DELAY}	60h = 0x0001		4		ms
Min turn-on delay	$t_{ON\_DELAY\_Min}$	60h = 0x0000		0		ms
Max turn-on delay	$t_{ON\_DELAY\_Max}$	60h = 0x0100		1024		ms
Error Amplifier						
Feedback current	I_{FB}	VFB = VREF		50	100	nA
Soft Shutdown						
Soft shutdown discharge MOSFET	R_{ON_DISCH}	TJ = 25°C		60	120	Ω
Under-Voltage Lockout (UVLO)						
VCC under-voltage lockout threshold rising	$V_{VCCUVLO\_Rise}$		2.9	3	3.1	V
VCC under-voltage lockout threshold falling	$V_{VCCUVLO\_Fall}$			2.7		V
VCC output voltage	V_{VCC}		4.85	5	5.15	V
Min input programmable turn-on voltage	$V_{IN\_ON\_MIN}$	VCC = 5V		2.9		V
Max input programmable turn-on voltage	$V_{IN\_ON\_MAX}$			16.5		V

Min input programmable turn-off voltage	$V_{IN\_OFF\_MIN}$	VCC = 5V		2.75		V
Max input programmable turn-off voltage	$V_{IN\_OFF\_MAX}$			15.75		V
VDRV under-voltage lockout threshold rising	$V_{DRVUVLO\_Rise}$			2.95		V
VDRV under-voltage lockout threshold falling	$V_{DRVUVLO\_Fall}$			2.6		V
Power Good (PG)						
Power good high threshold	$PG_{Vth\_Hi\_Rise}$	FB from low to high, default setting (D9h[1:0] = 2b'01)		0.95		VREF
Power good low threshold	$PG_{Vth\_Lo\_Rise}$	FB from low to high, default setting (D4h[1:0] = 2b'00)		1.15		VREF
	$PG_{Vth\_Lo\_Fall}$	FB from high to low, default setting (D9h[3:2] = 2'b10)		0.8		VREF
Power good low-to-high delay	P_{GTd}	Default setting (D1h[5:2] = 4b'0001)	1.6	2	2.4	ms
Power good sink current capability	V_{PG}	I PG = 10mA			0.3	V
Power good leakage current	I_{PG_LEAK}	VPG = 3V			2.6	μA
Power good low-level output voltage	V_{OL_100}	VIN = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor, TJ = 25°C			820	mV
	V_{OL_10}	VIN = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor, TJ = 25°C			920	
Thermal Protection (TP)						

TP fault rising threshold	T_{SD_Rise}	Default setting (4Fh = 0x0091)		145		℃
TP fault falling threshold	T_{SD_Fall}	Default setting (4Fh = 0x007D and D6h[2:1] = 2b'00)		125		℃
Min TP Fault Temp	$T_{SD\_WARN\_MIN}$			35		℃
Max TP Fault Temp	$T_{SD\_WARN\_MAX}$			165		℃
TP warning rising threshold	T_{WARN_Rise}	Default setting (4Ah = 0x0078)		120		℃
TP warning falling threshold	T_{WARN_Fall}	Default setting (4Ah = 0x0078, D6h[2:1] = 2b'00)		100		℃
Min TP warning temp	$T_{SD\_WARN\_MIN}$			35		℃
Max TP warning temp	$T_{SD\_WARN\_MAX}$			160		℃
Monitoring Parameters						
Min output voltage monitor range	V_{MVOUT_RANGE}			0		V
Max output voltage monitor range	V_{MVOUT_RANGE}			5.5		V
Output voltage monitor accuracy	V_{MVOUT_ACC}	Vo = 0.6V	-0.02	0.6	0.02	V
Output voltage bit resolution				1.25		mV
Output current monitor accuracy	I_{MIOUT_ACC}	Vo = 1.2V, fs = 800kHz, Io = 30A	-3		3	A
Output current bit resolution				62.5		mA
Min input voltage monitor	V_{MIN_RANGE}			2.5		V
Max input voltage monitor	V_{MIN_RANGE}			18		V
Input voltage monitor accuracy	V_{MIN_ACC}		-0.02	12	0.02	V

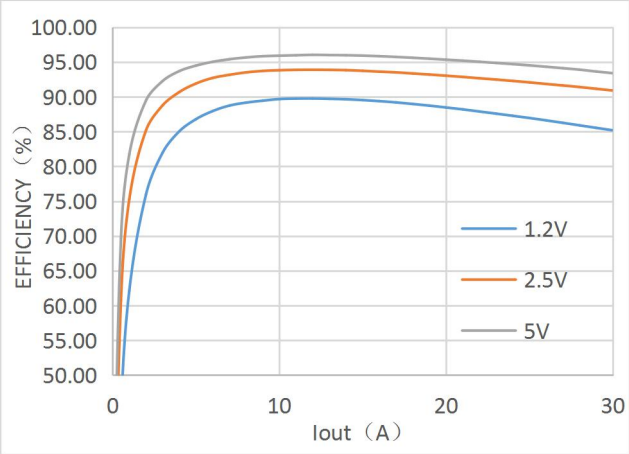
Input voltage bit resolution				25		mV
PMBus TM DC Characteristics (SDA, SCL, ALT#, EN)						
Input high voltage	V_{IH}				VCC-0.8V	V
Input low voltage	V_{IL}		0.8			V
Output low voltage	V_{OL}	I_{OL} = 1mA			0.4	V
Input leakage current	I_{LEAK}	SDA, SCL, ALT# = 3.3V	-10		10	μA
Maximum voltage (SDA, SCL, ALT#, EN)	V_{MAX}	Transient voltage including ringing	-0.3	3.3	5.5	V
Pin capacitance on SDA,SCL	C_{PIN}				10	pF
PMBus TM Timing Characteristics						
Min operating frequency				10		kHz
Max operating frequency				1000		kHz
Bus free time		Between stop and start condition	4.7			μs
Holding time			4			μs
Repeated start condition set-up time			4.7			μs
Stop condition set-up time			4			μs
Data hold time			300			ns
Data set-up time			250			ns
Clock low time out			25		35	ms
Clock low period			4.7			μs
Clock high period			4		50	μs
Clock/data fall time					300	ns
Clock/data rise time					1000	ns

TYPICAL PERFORMANCE

V_{IN} =12 V, T_A= 25˚C, V_{OUT}= 1.2 V, F_S = 800 kHz , L=0.22uH unless otherwise noted.

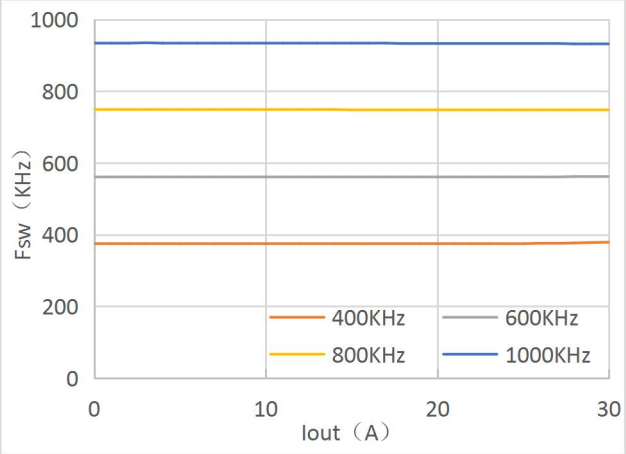
Efficiency

Forced CCM, 800kHz , 0.47uH/0.8mΩ



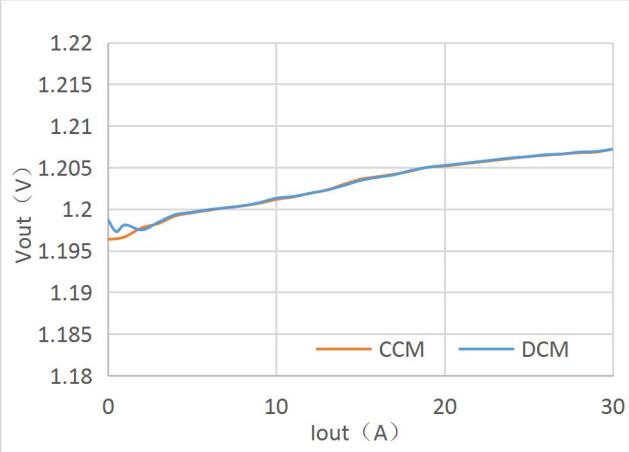
Switching Frequency

Forced CCM



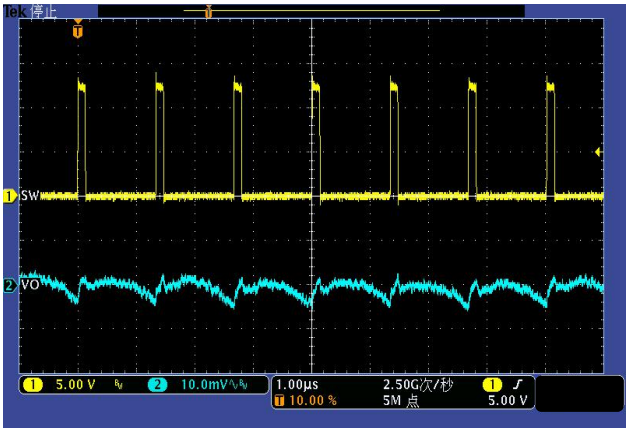
Load Regulation

Forced CCM,800kHz

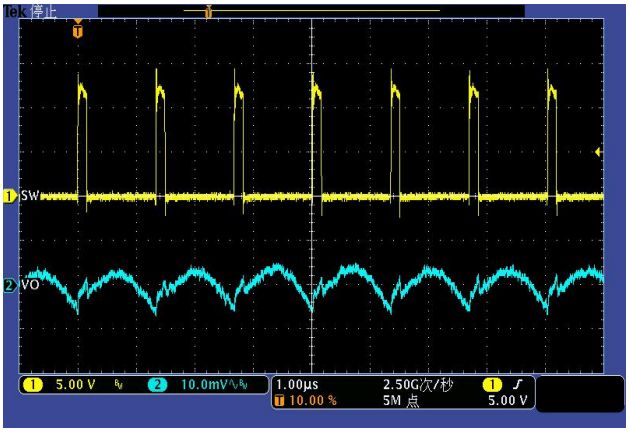


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

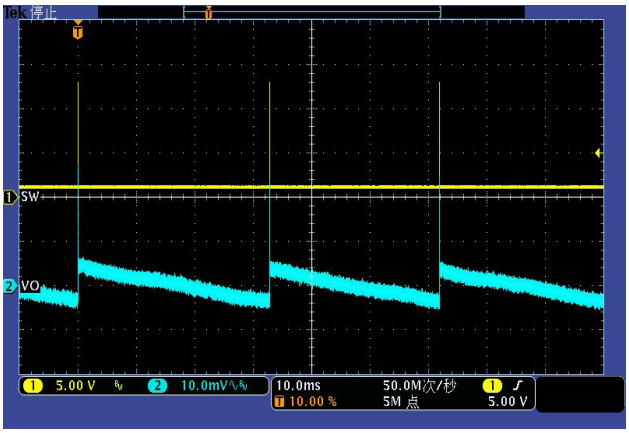
IOUT=0A，CCM，800kHz，1-Phase



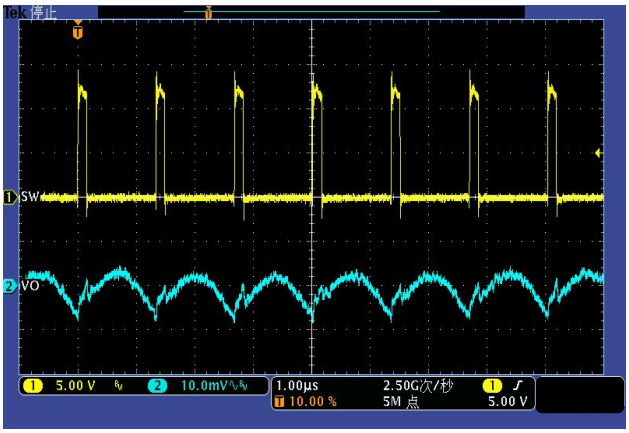
IOUT=30A，CCM，800kHz，1-Phase



IOUT=0A，DCM，800kHz，1-Phase

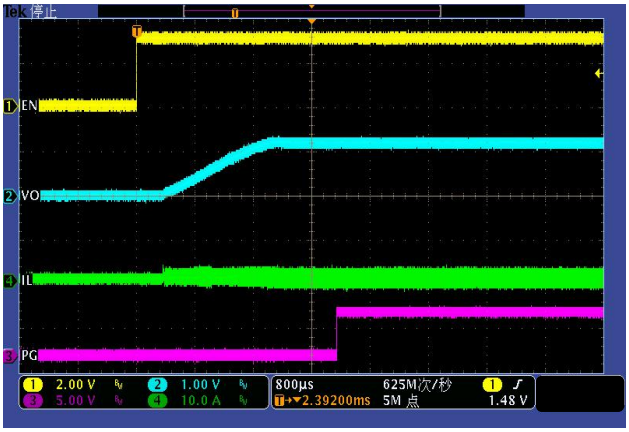


IOUT=30A，DCM，800kHz，1-Phase



Power On through EN，CCM

IOUT=0A, 1-Phase

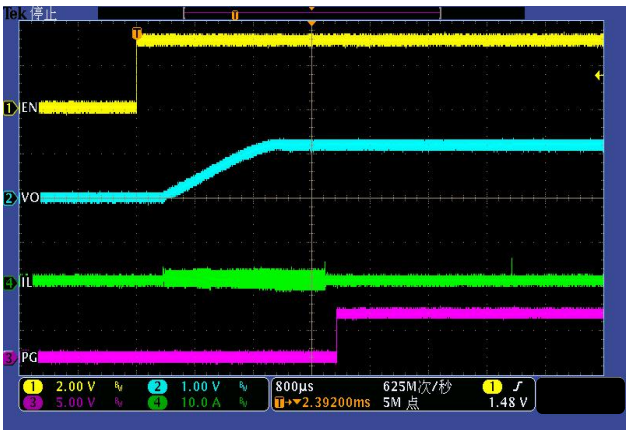


Power On through EN，CCM

IOUT=30A, 1-Phase

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power On through EN，DCM
I_{OUT}=0A, 1-Phase



Power On through EN，DCM
I_{OUT}=30A, 1-Phase

Power Off through EN，CCM
I_{OUT}=0A, 1-Phase

Power Off through EN，CCM
I_{OUT}=30A, 1-Phase

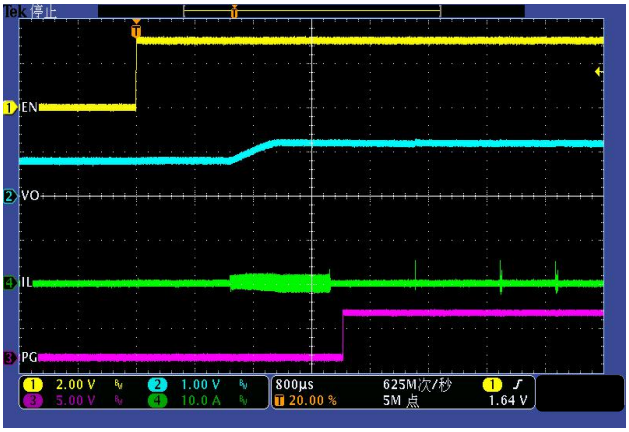
Power Off through EN，DCM
I_{OUT}=0A, 1-Phase

Power Off through EN，DCM
I_{OUT}=30A, 1-Phase

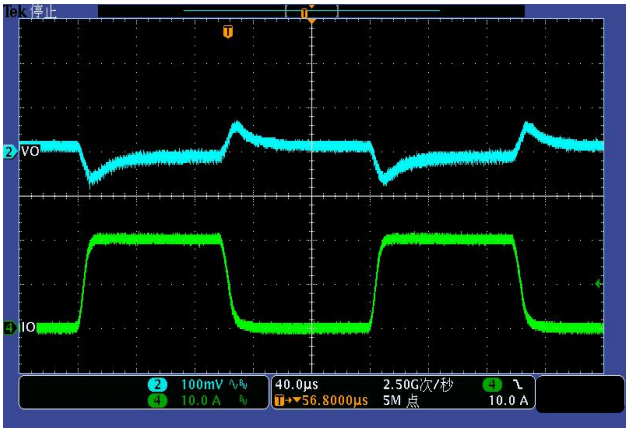
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Pre-Bias Start-Up
CCM, 1-Phase

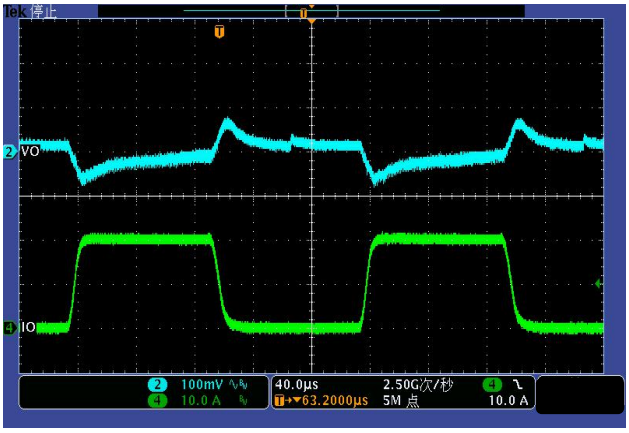
Pre-Bias Start-Up
DCM, 1-Phase



Load Transient， IOUT=0A~20A
1MHz, CCM

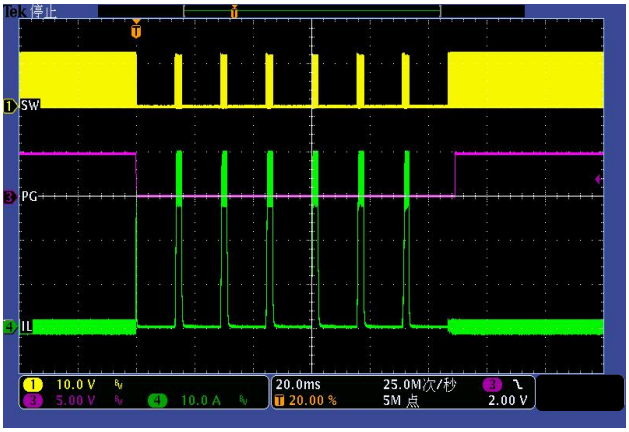


Load Transient， IOUT=0A~20A
1MHz, DCM



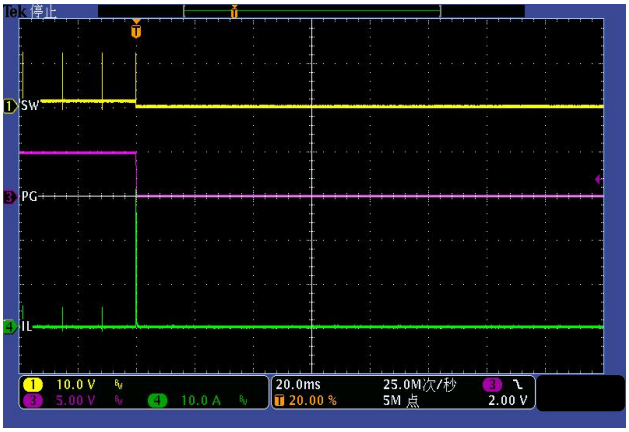
OCP, Latch-Off Option
CCM, 1-Phase

OCP, HICCUP Option
CCM, 1-Phase

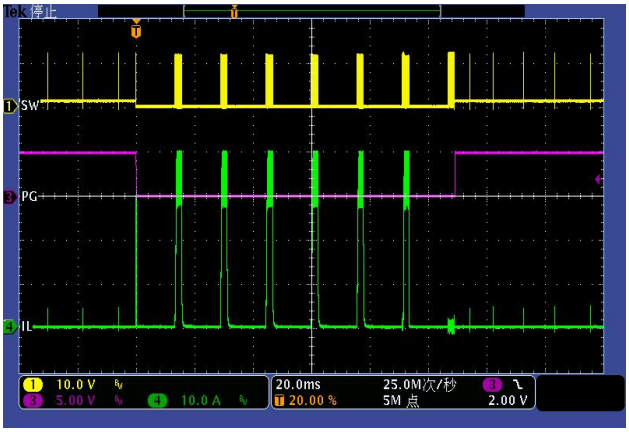


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

OCP, Latch-Off Option
DCM, 1-Phase



OCP, HICCUP Option
DCM, 1-Phase



OVP, HICCUP Option
DCM, 1-Phase

OVP, HICCUP Option
CCM, 1-Phase

OVP, Latch-Off Option
DCM, 1-Phase

OVP, HICCUP Option
CCM, 1-Phase

MULTI-PHASE OPERATION

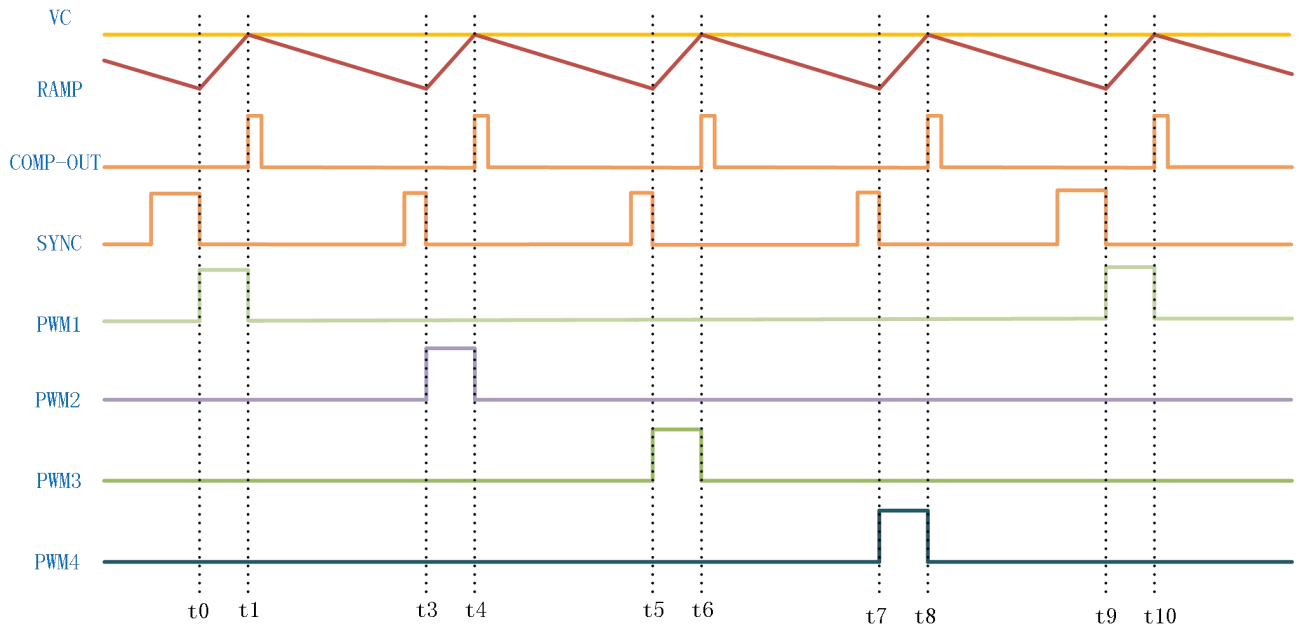


Figure 1: multi-phase PWM interleaved operation(steady state)

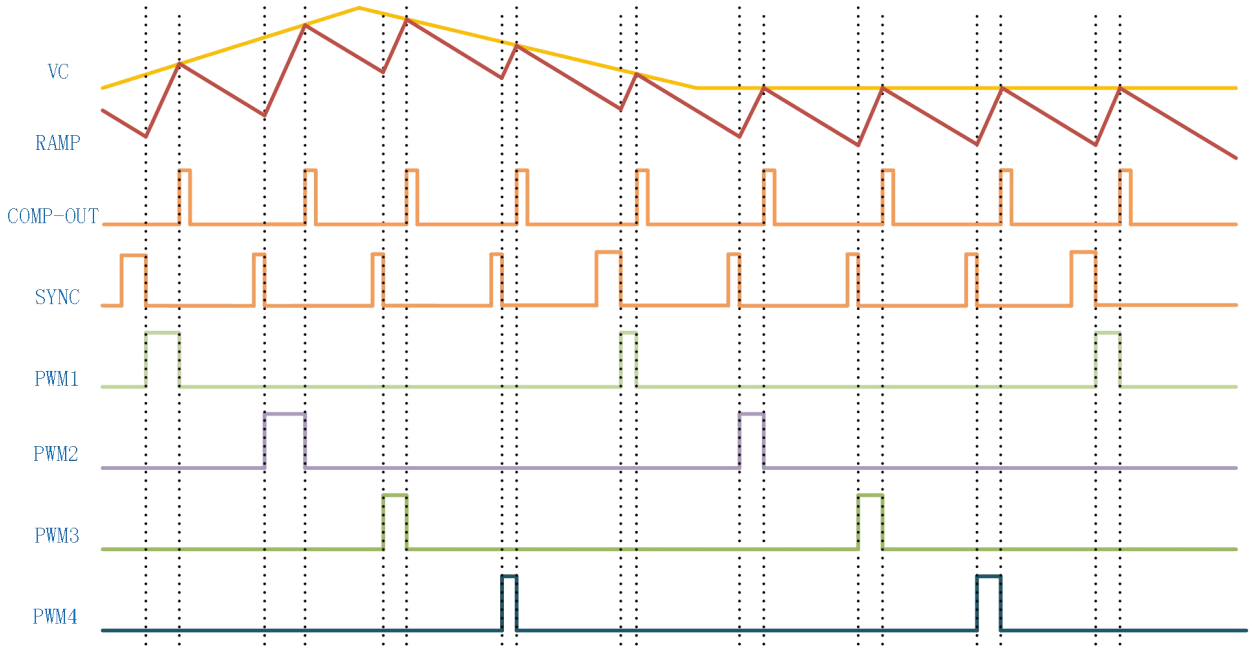


Figure 1: multi-phase PWM interleaved operation(load transition

FUNCTIONAL INFORMATION

Feedback (FB)

FB and RTN pins are used for remote sensing purpose. Where feedback resistors are required for output voltage programming, the FB pin must be connected to the mid-point of the resistor divider, and the RTN pin must always be connected to the load return. FB and RTN pins are high-impedance input terminals of the differential remote sense amplifier. The feedback resistor divider should use resistor values much less than 100 kΩ. The output voltage of IS6608A can be adjusted by changing the resistor divider, R_{top} and R_{bot}. Calculate output voltage from R_{top} and R_{bot} using the formula below:

$$V_{OUT} = \frac{R_{top} + R_{bot}}{R_{bot}} \times 0.6V$$

Resistor Selection for Common Output Voltages is listed in the following table. The accuracy should be 1% or better to ensure voltage setpoint accuracy is satisfied.

V_{OUT}(V)	R_{top}(kΩ)	R_{bot}(kΩ)
0.9	1	2
1.2	2	
1.8	4	
2.5	6.33	
3.3	9	
5	14.67	

Inductor Selection

To calculate the value of the output inductor, use the following equation.

$$\text{Lout} = \frac{\text{Vout}}{(\text{Vin}_{\max} \times \text{fsw})} \times \frac{\text{Vin}_{\max} - \text{Vout}}{\text{Iout}_{\max} \times \text{Kind}}$$

The coefficient K_{ind} represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing a high inductor ripple current impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, maintain a K_{ind} coefficient between 0.10 and 0.50 for balanced performance. Using this target ripple current, the required inductor size can be calculated using the equation provided above.

Selecting a K_{ind} of 0.25, the target inductance L_{out} = 390 nH. Using the standard value, the 390 nH is chosen in this application for its high current rating, low DCR, and small size. The inductor ripple current, RMS current, and peak current can be calculated using the following 3 equations. These values should be used to select an inductor with approximately the target inductance value, and current ratings that allow normal operation with some margin.

$$I_{RIPPLE} = \frac{\text{Vout}}{(\text{Vin}_{\max} \times \text{fsw})} \times \frac{\text{Vin}_{\max} - \text{Vout}}{L_{OUT}}$$

$$IL_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{1}{12} \times {I_{RIPPLE}}^2}$$

$$IL_{PEAK} = I_{OUT} + \frac{1}{2} \times I_{RIPPLE}$$

Choose an inductor that does not saturate under the maximum peak inductor current. Also, choose an inductor that gives the best thermal performance under the above calculated RMS current.

Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor affects three criteria:

- Stability
- Regulator response to a change in load current or load transient
- Output voltage ripple

These three considerations are important when designing regulators that must operate where

the electrical conditions are unpredictable. The output capacitance needs to be selected based on the most stringent of these three criteria.

Minimum Output Capacitance to Ensure Stability

To prevent sub-harmonic multiple pulsing behavior, IS6608A application designs must strictly follow the small signal stability considerations describe in the following equation.

$$C_{OUT\_\min} > \frac{t_{ON}}{2} \times \frac{8\tau}{L_{OUT}} \times \frac{V_{REF}}{V_{out}}$$

where

- $C_{OUT(min)}$ is the minimum output capacitance needed to meet the stability requirement of the design
- t_{ON} is the on-time information based on the switching frequency and duty cycle (in this design, 100 ns)
- τ is the ramp compensation time constant of the design based on the switching frequency and duty cycle (in this design, 1 μsec)
- L_{OUT} is the output inductance (in the design, 0.39 μH)
- V_{REF} is the reference voltage level (in this design, 0.6 V)
- V_{OUT} is the output voltage (1 V)

The stability is ensured when the amount of the output capacitance is greater than the minimum required value. And when all MLCCs (multi-layer ceramic capacitors) are used, both DC and AC derating effects must be considered to ensure that the minimum output capacitance requirement is met with sufficient margin.

the minimum capacitance required by the stability is much smaller than that is required by the load transient.

Response to a Load Transient

The output capacitance must supply the load with the required current when current is not immediately provided by the regulator. When the output capacitor supplies load current, the impedance of the capacitor greatly affects the magnitude of voltage deviation (such as undershoot and overshoot) during the transient.

For normal applications with less than 10% duty cycle, the output voltage deviation during a dynamic load release determines how much output capacitance is needed.

Use the next equation to estimate the amount of capacitance needed for a given dynamic load release.

$$C_{OUT\_\text{LoadRelease}} = \frac{L_{OUT} \times \Delta I_{LOAD}{}^2}{2 \times \Delta V_{Load\_Release} \times V_{OUT}}$$

In general applications where the overall output voltage tolerance is +/-5%, the allowed transient voltage deviation during the worst case load release can be set at around 3% depending on how much output voltage setpoint accuracy (1% in this design) and the ripple voltage requirement (1% in this design). The minimum output capacitance to meet the overshoot requirement can be calculated using the above equation. This example uses a combination of POSCAP and MLCC capacitors to meet the overshoot requirement.

- POSCAP bank #1: 2 x 470 μF, 2.5 V, 6 mΩ per capacitor
- MLCC bank #2: 4 × 100 μF, 2.5 V, 1 mΩ per capacitor with DC+AC derating factor of 50%

Recalculating the worst case overshoot using the described capacitor bank design, the overshoot needs to be 30 mV or less which meets the 3% overshoot transient specification requirement.

Output Voltage Ripple

The output voltage ripple is another important design consideration. The following equation calculates the minimum output capacitance required to meet the output voltage ripple specification. This criterion is the requirement when the impedance of the output capacitance is dominated by ESR.

$$Cout_{\min\_Ripple} = \frac{I_{RIPPLE}}{8 \times F_{SW} \times V_{OUT\_RIPPLE}}$$

In this example, the maximum output voltage ripple is 5.5 mV. Because this capacitance value is significantly lower compared to that of transient load release, determining the output capacitance bank using the worst case load release requirement is generally adequate. Because the output capacitor bank consists of both POSCAP and MLCC type capacitors, it is important to consider the ripple effect at the switching frequency due to effective ESR.

For detailed calculations, please contact the factory to obtain a user-friendly Excel based design tool.

Input Capacitor Selection

The IS6608A devices require a high-quality, ceramic, type X5R or X7R, input decoupling capacitor with a value of at least 1 μF of effective capacitance on the VCC pin, relative to AGND. The power stage input decoupling capacitance (effective capacitance at the VIN and PGND pins) must be sufficient to supply the high switching currents demanded when the high-side MOSFET switches on, while providing minimal input voltage ripple as a result. This effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple to the device during full load. The input ripple current can be calculated using the equation below.

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with the DC bias taken into consideration. For this design example, a ceramic capacitor with at least a 25 V voltage rating is required to support the maximum input voltage. For this design, allow 0.1 V input ripple for $V_{RIPPLE(cap)}$, and 0.3 V input ripple for $V_{RIPPLE(esr)}$. the minimum input capacitance for this design is 38.5 μF, and the maximum ESR is 9.4 mΩ. For this example, four 22 μF, 25 V low-ESR polymer capacitors in parallel were selected for the power stage.

Bootstrap Capacitor Selection

A ceramic capacitor with a value of 0.1 μF must be connected between the BOOT and SW pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. Use a capacitor with a voltage rating of 25 V or higher.

R-C Snubber and VIN Pin High-Frequency Bypass

Though it is possible to operate the IS6608A within absolute maximum ratings without ringing reduction techniques, some designs may require external components to further reduce ringing levels. This example uses two approaches: a high frequency power stage bypass capacitor on the VIN pins, and an R-C snubber between the PHASE area and GND.

The high-frequency VIN bypass capacitor is a lossless ringing reduction technique which helps minimizes the outboard parasitic inductances in the power stage, which store energy during the low-side MOSFET on-time, and discharge once the high-side MOSFET is turned on. For this design twin 1uF, 25 V, 0603 sized high-frequency capacitors are used. The placement of these capacitors is critical to its effectiveness. It's ideal placement is shown in PCB layout guidelines.

PMBUS™ INTERFACE

The Power Management Bus (“PMBus™”) is an open standard protocol that defines a means of communicating with power conversion and other devices. Its top speed is 1MHZ

Slave Address

The user can set the address through PMBus. Of course, the user can also set the address through R_ADDR and R_ISET. The detailed configuration is shown in the table 1.

Table 1 Address Setting

R_ADDR(kΩ)	Slave Address (R_ISET=60.4kΩ)	Slave Address (R_ISET=180kΩ)
5	30h	40h
15	31h	41h
25	32h	42h
37	33h	43h
52	34h	44h
70	35h	45h
95	36h	46h
125	37h	47h
160>	3Fh	3Fh

Alert Response Address(ARA)

The Alert Response Address is 0x0C. The ALERT# signal remains asserted until is cleared. It is cleared when the device successfully transmits its address in response to receiving the Alert Response Address. It is also cleared by a CLEAR_FAULTS command.

Multiple-Time Programming(MTP)

The IS6608A supports multiple-time programming cells to store user configurations. During this process, the voltage of VCC increases to 5V.

Table 2. Bit And Byte Symbols Used In This Specification

Symbol	Meaning
DATA BYTE	A shaded rectangle with a number over it represents one or more bits, as indicated by the number, sent from the host(a slave device). The name of the data or bit field may be included within the rectangle. If the data has a specific value, as might be shown in an example of a command, the value is written below the data or bit field name.
S	The START condition sent from a bus master device. The START condition is not a bit and does not have a number 1 over it.
Sr	A REPEATED START condition sent from a bus master device. The REPEATED START condition is not a bit and does not have a number 1 over it
A	An ACKnowledge condition sent the host(a slave device).
N	A NOT ACKnowledge condition sent the host(a slave device).
P	A STOP condition sent by a bus master device. The STOP condition is not a bit and does not have a number 1 over it.
SLAVE ADDRESS	The first seven bits of the address byte, generally corresponding to the physical address of the device.
R	The bit [0] of the address byte with a value of 1, indicating the device is being addressed with a read.
W	The bit [0] of the address byte with a value of 0, indicating the device is being addressed with a write.
COMMAND CODE	A one byte value that indicates a command the slave device is to execute
LOW DATA BYTE	In a two byte value, the lower order byte (bits [7:0]).
HIGH DATA BYTE	In a two byte value, the higher order byte (bits [15:8]).
PEC	A byte with the Packet Error Check (PEC) value, if used.
…	The bit/byte/packet diagram is continued on the next line.

NOTE:

The gray：sent from the host.

The white：sent from a slave device.

PMBus™ Message Format

a) Send Byte and Send Byte with PEC

1	7	1	1	8	1	1
S	SLAVE	W	A	DATA BYTE	A	P

1	7	1	1	8	1	8	1	1
S	SLAVE	W	A	DATA BYTE	A	PEC	A	P

b) Receive Byte and Receive Byte with PEC

1	7	1	1	8	1	1
S	SLAVE	R	A	DATA BYTE	N	P

1	7	1	1	8	1	8	1	1
S	SLAVE	R	A	DATA BYTE	A	PEC	N	P

c) Write Byte and Write Byte with PEC

1	7	1	1	8	1	8	1	1
S	SLAVE	W	A	COMMAND	A	DATA BYTE	A	P

1	7	1	1	8	1	8	1	8	1	1
S	SLAVE	W	A	COMMAND	A	DATA BYTE	A	PEC	A	P

d) Write Word and Write Word with PEC

1	7	1	1	8	1	8	1	8	1	1
S	SLAVE	W	A	COMMAND	A	LOW DATA	A	HIGH DATA	A	P

1	7	1	1	8	1	8	1	8	1	8	1	1
S	SLAVE	W	A	COMMAND	A	LOW DATA	A	HIGH DATA	A	PEC	A	P

e) Read Byte and Read Byte with PEC

1	7	1	1	8	1	1	7	1	1	8	1	1
S	SLAVE	W	A	COMMAND	A	Sr	SLAVE	R	A	DATA BYTE	N	P

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	SLAVE	W	A	COMMAND	A	Sr	SLAVE	R	A	DATA BYTE	A	PEC	N	P

f) Read Word and Read Word with PEC

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	SLAVE	W	A	COMMAND	A	Sr	SLAVE	R	A	LOW DATA	A	HIGH DATA	N	P

1	7	1	1	8	1	1	7	1	1	8	1	8	1
S	SLAVE	W	A	COMMAND	A	Sr	SLAVE	R	A	LOW DATA	A	HIGH DATA	A

8	1	1
PEC	N	P

g) Block Read with PEC

1	7	1	1	8	1	1	7	1	1	8	1	8	1
S	SLAVE	W	A	COMMAND	A	Sr	SLAVE	R	A	Byte Count = N	A	DATA BYTE 1	A

8	1	…	8	1	1
DATA BYTE 2	A	…	DATA BYTE N	N	P

1	7	1	1	8	1	1	7	1	1	8	1	8	1
S	SLAVE	W	A	COMMAND	A	Sr	SLAVE	R	A	Byte Count = N	A	DATA BYTE 1	A

8	1	…	8	1	8	1	1
DATA BYTE 2	A	…	DATA BYTE N	A	PEC	N	P

REGISTER MAP

Name	Code	Type	Bytes	Default Value	MTP?
OPERATION	01h	r/w w/PEC	1	0x80	YES
ON_OFF_CONFIG	02h	r/w w/PEC	1	0x16	YES
CLEAR_FAULTS	03h	Send byte	0	-	
WRITE_PROTECT	10h	r/w w/PEC	1	0x00	YES
STORE_USER_ALL	15h	Send byte	0	-	
RESTORE_USER_ALL	16h	Send byte	0	-	
CAPABILITY	19h	r w/PEC	1	0xB0	
VOUT_MODE	20h	r w/PEC	1	0x40	
VOUT_COMMAND	21h	r/w w/PEC	2	0x0258 (1.2V)	YES
VOUT_MAX	24h	r/w w/PEC	2	0x0ABE (5.5V)	YES
VOUT_MARGIN_HIGH	25h	r/w w/PEC	2	0x02A0 (1.344V)	YES
VOUT_MARGIN_LOW	26h	r/w w/PEC	2	0x0200 (1.024V)	YES
VOUT_SCALE_LOOP	29h	r/w w/PEC	2	0x01F4 (0.5)	YES
VOUT_MIN	2Bh	r/w w/PEC	2	0x00FA (0.5V)	YES
VIN_ON	35h	r/w w/PEC	2	0x0020 (8V)	YES
VIN_OFF	36h	r/w w/PEC	2	0x00014 (5V)	YES
IOUT_OC_FAULT_LIMIT	46h	r/w w/PEC	2	0x00A1 (39A)	YES
IOUT_OC_WARN_LIMIT	4Ah	r/w w/PEC	2	0x0091 (35A)	YES
OT_FAULT_LIMIT	4Fh	r/w w/PEC	2	0x0046(140℃)	YES
OT_WARN_LIMIT	51h	r/w w/PEC	2	0x0041 (130℃)	YES
VIN_OV_FAULT_LIMIT	55h	r/w w/PEC	2	0x0021 (16.5V)	YES
VIN_OV_WARN_LIMIT	57h	r/w w/PEC	2	0x0021 (16.5V)	YES
VIN_UV_WARN_LIMIT	58h	r/w w/PEC	2	0x0010 (4V)	YES
TON_DELAY	60h	r/w w/PEC	2	0x0000 (0ms)	YES
TON_RISE	61h	r/w w/PEC	2	0x0001 (2ms)	YES
STATUS_BYTE	78h	r w/PEC	1		
STATUS_WORD	79h	r w/PEC	2		
STATUS_VOUT	7Ah	r w/PEC	1		
STATUS_IOUT	7Bh	r w/PEC	1		
STATUS_INPUT	7Ch	r w/PEC	1		
STATUS_TEMPERATURE	7Dh	r w/PEC	1		
STATUS_CML	7Eh	r w/PEC	1		
READ_VIN	88h	r w/PEC	2		
READ_VOUT	8Bh	r w/PEC	2		
READ_IOUT	8Ch	r w/PEC	2		
READ_TEMPERATURE_1	8Dh	r w/PEC	2		
PMBUS_REVISION	98h	r w/PEC	1	0x33h, ASCII “13” (PMBusTM	
MFR_ID	99h	Block read w/PEC	1(byte)+ 3(data)	0x49 0x53 0x00, ASCII"IS "	
MFR_MODEL	9Ah	Block read w/PEC	1(byte)+ 8(data)	0x49 0x53 0x36 0x36 0x30 0x38 0x00 0x00 ASCII"IS6608 "	
MFR_REVISION	9Bh	Block read w/PEC	1(byte)+ 1(data)	0x31 ASCII”1” (REV 1)	YES
MFR_4_DIGIT	9Dh	Block read w/PEC	1(byte)+	0x30 0x30(00)	YES
			6(data)	0x31 0x36 0x30 0x30 (1600)	

REGISTER MAP *(continued)*

Name	Code	Type	Bytes	Default Value	MTP?
MFR_CTRL_COMP	D0h	r/w w/PEC	1	0x0D	YES
MFR_CTRL_VOUT	D1h	r/w w/PEC	1	0x40	YES
MFR_CTRL_OPS	D2h	r/w w/PEC	1	0x05	YES
MFR_ADDR_PMBUS	D3h	r/w w/PEC	1	0x00	YES
MFR_VOUT_OVP_FAULT_LIMIT	D4h	r/w w/PEC	1	0x00	YES
MFR_OVP_NOCP_SET	D5h	r/w w/PEC	1	0x00	YES
MFR_OT_OC_SET	D6h	r/w w/PEC	1	0x00	YES
MFR_OC_PHASE_LIMIT	D7h	r/w w/PEC	1	0x14 (30A)	YES
MFR_HICCUP_ITV_SET	D8h	r/w w/PEC	1	0x00	YES
MFR_PGOOD_ON_OFF	D9h	r/w w/PEC	1	0x00	YES
MFR_FB_STEP	DAh	r/w w/PEC	1	0x00	YES
MFR_LOW_POWER	E5h	r/w w/PEC	1	0x03	YES
MFR_CTRL	EAh	r/w w/PEC	2	0x0108	YES

OPERATION (01h)

The OPERATION command is used to configure the operational state of the converter, in conjunction with input from the EN pin. The command default value is 0x80.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r	r
Function	On/off state	Turn off	Voltage source		Margin fault response		Reserved	
Default value	1	0	00		00		00	

OPERATION Command Data Byte Contents

Bit[7:6]	Bit[5:4]	Bit[3:2]	Bit[1:0]	On/off	Margin state	01h
00	xx	xx	xx	Immediate off	N/A	0x00
01	xx	xx	xx	Immediate off	N/A	0x60
10	00	xx	xx	On	Off	0x80
10	01	01	xx	On	Margin low (ignore fault)	0x94
10	01	10	xx	On	Margin low (act on fault)	0x98
10	10	01	xx	On	Margin high (ignore fault)	0xA4
10	10	10	xx	On	Margin high (act on fault)	0xA8

ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of EN pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied. The default response for any PMBus device is specified by the device manufacturer. The command default value is 0x16.

Bits	Name	Access	Behavior	Default	Description
[7:5]	Reserved	r		000	Always read as 000.
[4]	on	r/w	Live	1	0:powers up any time power is present. 1:by the en pin and OPERATION command.
[3]	op	r/w	Live	0	0:ignores the on/off portion of the OPERATION command 1:depending on bit [2].
[2]	en	r/w	Live	1	0:ignores the EN pin. 1:requires the EN pin.
[1]	pol_en	r/w	Live	1	0:Active low. 1:Active high.
[0]	delay	r		1	Use the programmed turn off delay and fall time.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its ALERT# signal output if the device is asserting the ALERT# signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit shall immediately be set again and the host notified by the usual means. This command is write only. There is no data byte for this command.

WRITE PROTECT (10h)

This command reads only. The default value is 0x00(Enable writes to all commands.).

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the Operating Memory to the matching locations in the non-volatile User Store memory. Any items in Operating Memory that do not have matching locations in the User Store are ignored. It is permitted to use the STORE_USER_ALL command while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable, undesirable or even catastrophic results. PMBus device users are urged to contact the PMBus device manufacturer about the consequences of using the STORE_USER_ALL command while the device is operating and providing output power. This command has no data bytes. This command is write only.

• OPERATION (01h)	• TON_RISE (61h)
• ON_OFF_CONFIG (02h)	• TOFF_DELAY (64h)
• VOUT_COMMAND (21h)	• MFR_REVISION (9Bh)
• VOUT_MAX (24h)	• MFR_4_DIGIT (9Dh)
• VOUT_MARGIN_HIGH (25h)	• MFR_CTRL_COMP (D0h)
• VOUT_MARGIN_LOW (26h)	• MFR_CTRL_VOUT (D1h)
• VOUT_SCALE_LOOP (29h)	• MFR_CTRL_OPS (D2h)
• VOUT_MIN (2Bh)	• MFR_ADDR_PMBUS (D3h)
• VIN_ON (35h)	• MFR_VOUT_OVP_FAULT_LIMIT (D4h)
• VIN_OFF (36h)	• MFR_OVP_NOCP_SET (D5h)
• IOUT_OC_FAULT_LIMIT (46h)	• MFR_OT_OC_SET (D6h)
• IOUT_OC_WARN_LIMIT (4Ah)	• MFR_OC_PHASE_LIMIT (D7h)
• OT_FAULT_LIMIT (4Fh)	• MFR_HICCUP_ITV_SET (D8h)
• OT_WARN_LIMIT (51h)	• MFR_PGOOD_ON_OFF (D9h)
• VIN_OV_FAULT_LIMIT (55h)	• MFR_VOUT_STEP (DAh)
• VIN_OV_WARN_LIMIT (57h)	• MFR_LOW_POWER (E5h)
• VIN_UV_WARN_LIMIT (58h)	• MFR_CTRL (EAh)
• TON_DELAY (60h)	• MFR_SLAVE_RESPONSE (F8h)

CAPABILITY (19h)

This command provides a way for a host system to determine some key capabilities of a PMBus device. This command is read only. The command default value is 0xB0.

Bits	Name	Access	Behavior	Default	Description
[7]	Packet Error Checking	r/w	Live	1	0:Packet Error Checking not supported 1:Packet Error Checking is supported
[6:5]	Maximum Bus Speed	r/w	Live	01	00:Maximum supported bus speed is 100kHz. 01:Maximum supported bus speed is 1MHz. 10:Maximum supported bus speed is 400kHz. 11:Reserved.
[4]	ALERT#	r/w	Live	1	0:The device does not have an ALERT# pin and does not support the PMBus Alert Response protocol . 1:The device does have an ALERT# pin and does support the PMBus Alert Response protocol
[3:0]	Reserved	r		0000	Always read as 0000.

VOUT_MODE (20h)

The data byte for the VOUT_MODE command is one byte that consists of a three bit Mode and a five bit Parameter. The three bit Mode sets whether the device uses the LINEAR, Half-precision IEEE 754 floating point, VID or DIRECT modes for output voltage related commands. This command is read only. The command default value is 0x40. (only direct format is supported in IS6608A)

VOUT_COMMAND (21h)

The VOUT_COMMAND command is used to sets the output voltage of IS6608A.The value is unsigned, and 1LSB = 2mV. The default value is 0x0258(1.2V).

Command	VOUT_COMMAND															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				2mV/LSB											
Default value	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0

VOUT_MAX (24h)

The VOUT_ MAX command sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output over voltage protection. The value is unsigned, and 1LSB = 2mV. The default value is 0x0ABE(5.5V).

Command	VOUT_MAX															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				2mV/LSB											
Default value	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0

VOUT_MARGIN_HIGH (25h)

This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”. The value is unsigned, and 1LSB = 2mV. The default value is 0x02A0(1.344V).

Command	VOUT_MARGIN_HIGH															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				2mV/LSB											
Default value	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0

VOUT_MARGIN_LOW (26h)

This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”. The value is unsigned, and 1LSB = 2mV. The default value is 0x0200(1.024V).

Command	VOUT_MARGIN_LOW															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				2mV/LSB											
Default value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP command sets the feedback resistance voltage divider ratio. The value is dimensionless., and 1LSB = 0.001. The default value is 0x01F4(0.5).

Command	VOUT_SCALE_LOOP															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				0.001/LSB											
Default value	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

VOUT_MIN (2Bh)

The VOUT_ MIN command sets a lower limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output under voltage protection. If a PMBus device supports this command, it must be able to detect that an attempt has been made to program the output to a voltage less than the value set by the VOUT_MIN command. This will be treated as a warning condition and not a fault condition. The value is unsigned, and 1LSB = 2mV. The default value is 0x00FA(0.5V).

Command	VOUT_MN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				2mV/LSB											
Default value	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0

VIN_ON (35h)

The VIN_ON command sets the value of the input voltage, in Volts, at which the unit should start power conversion. .The value is unsigned, and 1LSB = 250mV. The default value is 0x0020(8V).

Command	VIN_ON															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				250mV/LSB											
Default value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage, in Volts, at which the unit, once operation has started, should stop power conversion. The value is unsigned, and 1LSB = 250mV. The default value is 0x0014(5V).

Command	VIN_OFF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				250mV/LSB											
Default value	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

IOUT_OC_FAULT_LIMIT (46h)

The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in Amperes, that causes the Overcurrent detector to indicate an Overcurrent fault condition. The value is unsigned, and 1LSB = 250mA. The default value is 0x008C(35A).

Command	IOUT_OC_FAULT_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				250mA/LSB											
Default value	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0

IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OV_WARN_LIMIT command sets the value of the output current that causes an output Overcurrent warning. The value is unsigned, and 1LSB = 250mA. The default value is 0x0078(30A).

Command	IOUT_OC_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				250mA/LSB											
Default value	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT command sets the temperature of the unit, in degrees Celsius, at which it should indicate an Overtemperature Fault. The value is unsigned, and 1LSB = 2°C. The default value is 0x0046(140°C).

Command	OT_FAULT_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				2°C/LSB											
Default value	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1

OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT command sets the temperature of the unit, in degrees Celsius, at which it should indicate an Overtemperature Warning alarm. The value is unsigned, and 1LSB = 1°C. The default value is 0x0041(130°C).

Command	OT_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				2°C/LSB											
Default value	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1

VIN_OV_FAULT_LIMIT (55h)

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage that causes an Input Overvoltage Fault. The value is unsigned, and 1LSB = 500mV. The default value is 0x0021(16.5V). The VIN_OV_FAULT_LIMIT setting value should not be higher than 18V.

Command	VIN_OV_FAULT_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				500mV/LSB											
Default value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT command sets the value of the input voltage that causes an input voltage high warning. This value is typically less than the Input Overvoltage Fault threshold. The value is unsigned, and 1LSB = 500mV. The default value is 0x0021(16.5V). The maximum value is 18V.

Command	VIN_OV_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				500mV/LSB											
Default value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

VIN_UV_WARN_LIMIT (58h)

The VIN_UV_WARN_LIMIT command sets the value of the input voltage that causes an input voltage low warning. This value is typically greater than the Input Undervoltage Fault threshold. The value is unsigned, and 1LSB = 250mV. The default value is 0x0010(4V). The minimum value is 3.3V.

Command	VIN_UV_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved				250mV/LSB											
Default value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

TON_DELAY (60h)

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. This command reads only. The default value is 0x0000(0ms).

TON_RISE (61h)

The TON_RISE command sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. A value of 0 milliseconds instructs the unit to bring its output voltage to the programmed regulation value as quickly as possible. The value is unsigned, and 1LSB = 1ms. The default value is 0x0001(1ms).The maximum value is 0x0007(16ms).

Command	TON_RISE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved													1ms/LSB		
Default value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

STATUS_BYTE (78h)

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults.

Bits	Name	Behavior	Default	Description
[7]	Reserved		0	Always read as 0.
[6]	OFF	Live	0	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
[5]	VOUT_OV		0	An output overvoltage fault has occurred.
[4]	IOUT_OC_FAULT	Latched	0	An output overcurrent fault has occurred.
[3]	VIN_UV_FAULT		0	An input undervoltage fault has occurred.
[2]	TEMPERATURE	Live	0	A temperature fault or warning has occurred.
[1]	CML	Latched	0	A communications, memory or logic fault has occurred.
[0]	NONE_OF_THE_ABOVE	Live	0	A fault or warning not listed in bits [7:1] has occurred.

STATUS_WORD (79h)

The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE command.

Bits	Name	Behavior	Default	Description
[15]	VOUT	Live	0	An output voltage fault or warning has occurred.
[14]	IOUT	Live	0	An output current fault or warning has occurred.
[13]	INPUT	Live	0	An input voltage, input current, or input power fault or warning has occurred.
[12]	Reserved		0	Always read as 0.
[11]	PG_STATUS#	Live	0	The POWER_GOOD signal, if present, is negated.
[10:9]	Reserved		00	Always read as 00.
[8]	UNKNOWN	Latched	0	A fault type not given in bits [15:1] of the SATUS_WORD has been detected
[7]	Reserved		0	Always read as 0.
[6]	OFF	Live	0	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
[5]	VOUT_OV		0	An output overvoltage fault has occurred.
[4]	IOUT_OC_FAULT	Latched	0	An output overcurrent fault has occurred.
[3]	VIN_UV_FAULT		0	An input undervoltage fault has occurred.
[2]	TEMPERATURE	Live	0	A temperature fault or warning has occurred.
[1]	CML	Latched	0	A communications, memory or logic fault has occurred.
[0]	NONE_OF_THE_ABOVE	Live	0	A fault or warning not listed in bits [7:1] has occurred.

STATUS_VOUT (7Ah)

The STATUS_VOUT command returns one data byte with contents.

Bits	Name	Behavior	Default	Description
[7]	VOUT_OV_FAULT	Live	0	Output Overvoltage Fault.
[6:5]	Reserved		00	Always read as 00.
[4]	VOUT_UV_FAULT	Live	0	Output Undervoltage Fault.
[3]	VOUT_MAX_MIN	Live	0	VOUT_MAX_MIN Warning (An attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command or lower than the limited allowed by the VOUT_MIN command.
[2:1]	Reserved		00	Always read as 00.
[0]	UNKNOWN	Latched	0	0: no other fault has occurred 1: a fault type not specified in bit[15:1] of STATUS_WORD has been detected

STATUS_IOUT (7Bh)

The STATUS_IOUT command returns one data byte with contents.

Bits	Name	Behavior	Default Set	Description
[7]	IOUT_OC_FAULT	latched	0	Output Overcurrent Fault.
[6]	IOUT_OC_LV_FAULT	latched	0	Output Overcurrent And Low Voltage Fault.
[5]	IOUT_OC_WARNING	latched	0	Output Overcurrent Warning.
[4:0]	Reserved		00000	Always read as 00000.

STATUS_INPUT (7Ch)

The STATUS_INPUT command returns one data byte with contents.

Bits	Name	Behavior	Default Set	Description
[7]	VIN_OV_FAULT	latched	0	Input Overvoltage Fault.
[6]	VIN_OV_WARNING	latched	0	Input Overvoltage Warning.
[5]	VIN_UV_WARNING	latched	0	Input Undervoltage Warning.
[4:0]	Reserved		00000	Always read as 0.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns one data byte with contents.

Bits	Name	Behavior	Default	Description
[7]	OT_FAULT	latched	0	Overtemperature Fault.
[6]	OT_WARNING	latched	0	Overtemperature Warning.
[5:0]	Reserved		000000	Always read as 000000.

STATUS_CML (7Eh)

The STATUS_CML command returns one data byte with contents.

Bits	Name	Behavior	Default Set	Description
[7]	Invalid or unsupported Command	latched	0	Invalid Or Unsupported Command Received.
[6]	Invalid / unsupported data	latched	0	Invalid Or Unsupported Data Received.
[5]	Reserved		0	Always read as 0.
[4]	Memory fault	latched	0	Memory Fault Detected.
[3:2]	Reserved		00	Always read as 00.
[1]	Other fault	latched	0	A communication fault other than the ones listed in this table has occurred.
[0]	Memory	latched	0	Other Memory Or Logic Fault has occurred.

READ_VIN (88h)

The READ_VIN command returns the 10-bit measured value of the input voltage. The value is unsigned, and 1LSB = 25mV.

Command	READ_VOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Reserved						25mV /LSB									
Default value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_VOUT (8Bh)

The READ_VOUT command returns the 13-bit measured value of the output voltage. The value is unsigned, and 1LSB = 1.25mV.

Command	READ_VOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Reserved			1.25mV /LSB												
Default value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_IOUT (8Ch)

The READ_IOUT command returns the 14-bit measured value of the output current. The value is unsigned, and 1LSB = 62.5mA.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x		62.5mA/LSB													
Default value	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0

READ_TEMPERATURE_1 (8Dh)

READ_TEMPERATURE_1 is a 2-byte, two's complement integer. Bit[9] is the sign bit.

Command	READ_TEMPERATURE_1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	X	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Reserved						Sign	2°C /LSB								
Default value	0	0	0	0	0	0	0	X	0	0	1	1	0	0	1	0

Direct Value vs Real-World Value

Sign	Direct Value	Real-World Value (°C)
0	0 X000 0000	0
0	0 X000 0001	2
0	1 X111 1111	+511
1	0 X000 0001	-511
1	1 X111 1111	-2

PMBUS_REVISION (98h)

PMBUS_REVISION command stores or reads the revision of the PMBus to which the device is compliant. The command has one data byte. Bits [7:4] indicate the revision of PMBus specification Part I to which the device is compliant. Bits [3:0] indicate the revision of PMBus specification Part II to which the device is compliant. this as a read only command

Bit[7:4]	Part I Revision	Bits [3:0]	Part II Revision
0000b	1.0	0000b	1.0
0001b	1.1	0001b	1.1
0010b	1.2	0010b	1.2
0011b	1.3	0011b	1.3

MFR_ID (99h)

The MFR_ID command is used to either set or read the manufacturer's ID (name, abbreviation or symbol that identifies the unit's manufacturer). Each manufacturer chooses their identifier.

Byte	Byte Name	Value	Description
0	Byte Count	0x03	Always read as 0x03. The number of data bytes that the block read command expects to read.
1	Character 1	0x4D, ASCII of "I"	Always read as 0x49.
2	Character 2	0x50, ASCII of "S"	Always read as 0x53.
3	Character 3	0x53, ASCII of " "	Always read as 0x00.

MFR_MODEL (9Ah)

The MFR_MODEL command is used to either set or read the manufacturer's model number.

Byte	Byte Name	Value	Description
0	Byte Count	0x08	Always read as 0x08, the number of data bytes that the block read command expects to read.
1	Character 1	0x4D, ASCII of "I"	Always read as 0x49.
2	Character 2	0x50, ASCII of "S"	Always read as 0x53.
3	Character 3	0x51, ASCII of "6"	Always read as 0x36.
4	Character 4	0x38, ASCII of "6"	Always read as 0x36.
5	Character 5	0x36, ASCII of "0"	Always read as 0x30.
6	Character 6	0x34, ASCII of "8"	Always read as 0x38.
7	Character 7	0x35, ASCII of " "	Always read as 0x00.
8	Character 8	0x50, ASCII of " "	Always read as 0x00.

MFR_4_DIGIT (9Dh)

The MFR_4_DIGIT sets a unique four-digit number to identify different MTP configurations.

Byte	Byte Name	Value
0	Character 0	0x31
1	Character 1	0x36~0x39
2	Character 2	0x30, 0x31
3	Character 3	0x30~0x3F
4	Character 4	0x30~0x33
5	Character 5	0x30~0x3F

MFR_CTRL_COMP (D0h)

Bits	Name	Access	Behavior	Default	Description
[7:5]	Reserved	r		0000	Always read as 0000.
[4]	Cff	r/w	Live	0	Sets the feed-forward capacitance when the internal feedback resistor divider is selected. 0: 20pF 1: 50pF
[3:1]	RAMP Level	r/w	Live	110	Set the internal of RAMP compensation to stabilize the loop. 000 is the smallest，111 is the largest.
[0]	Slave Fault Detection	r/w	Live	1	Enable or disable the slave fault detection function through the PG pin. 0: slave-phase fault detection is enabled 1: slave-phase fault detection is disabled

MFR_CTRL_VOUT (D1h)

Bits	Name	Access	Behavior	Default	Description
[7]	Reserved	r		0	Always read as 0.
[6]	Vo discharge	r/w	Live	1	Enables or disables the active output voltage discharge when the IS6608A is commanded off through EN or the OPERATION command.
[5:2]	PG delay	r	Live	0000	Always read as 0000.
[1:0]	FB_RANGE	r/w	Live	00	Chooses the internal voltage divider ratio. 00: Vref/FB = 1, FB = 0.3 ~ 0.672V, LSB = 2mV 01: Vref/FB = 0.5, FB = 0.5 ~ 1.344V, LSB = 4mV 10: Vref/FB = 0.25, FB = 0.7 ~2.688V, LSB = 8mV 11: Vref/FB = 0.125, FB = 1.3 ~ 5.5V, LSB =16mV

MFR_CTRL_OPS (D2h)

Bits	Name	Access	Behavior	Default	Description
[7:3]	Reserved	r		00000	Always read as 00000.
[2:1]	SWITCHING_ FREQUENCY	r/w	Live	10	00: set fs to 400kHz 01: set fs to 600kHz 10: set fs to 800kHz 11: set fs to 1000kHz
[0]	SKIP_CCM	r/w	Live	1	0: pulse-skip mode at light load 1: forced CCM at light load

MFR_ADDR_PMBUS (D3h)

Command	MFR_ADDR_PMBUS							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	enable	ADDR						
Default value	0	0	0	0	0	0	0	0

MFR_VOUT_OVP_FAULT_LIMIT (D4h)

Bits	Name	Access	Behavior	Default	Description
[7:4]	Reserved	r		0000	Always read as 0000.
[3:2]	OV_EXIT_ TH	r/w	Live	00	Sets the OVP exit threshold. 00: 10% * VREF 01: 50% * VREF 10: 80% * VREF 11: 102.5% * VREF
[1:0]	OV_ENTRY_ TH	r/w	Live	00	Sets the OVP entry threshold. 00: 115% * VREF 01: 120% * VREF 10: 125% * VREF 11: 130% * VREF

MFR_OVP_NOCP_SET (D5h)

Bits	Name	Access	Behavior	Default	Description
[7:4]	Reserved	r		0000	Always read as 0000.
[3]	DELAY_NOCP (D400)	r/w	Live	0	0: 100ns delay after NOCP 1: 200ns delay after NOCP
[2]	NOCP	r/w	Live	0	0: set NOCP to -10A. 1: set NOCP to -15A.
[1:0]	VOUT_OV _Response	r/w	Live	00	00: latch-off with output voltage discharge 01: latch-off without output voltage discharge in DCM 10: hiccup with output voltage discharge 11: hiccup without output voltage discharge in DCM

MFR_OT_OC_SET (D6h)

Bits	Name	Access	Behavior	Default	Description
[7:4]	Reserved	r		0000	Always read as 0000.
[3]	OC_response	r/w	Live	00	0: latch-off, never retry 1: retry
[2:1]	OT_hyst	r/w	Live	00	00: 40°C 01: 50°C 10: 60°C 11: 70°C
[0]	OT_Response	r/w	Live	0	0: latch-off, never retry 1: retry after the temp drops by the value set by bit[2:1]

MFR_OC_PHASE_SET (D7h)

Bits	Name	Access	Behavior	Default	Description
[7:5]	Reserved	r		000	Always read as 000.
[4:0]	OC_limit	r/w	Live	10100	Current limit. 1.5A/LSB, [00000] = 0A.

MFR_HICCUP_ITV_SET (D8h)

Bits	Name	Access	Behavior	Default	Description
[7:6]	Reserved	r		00	Always read as 00.

[5:0]	Hiccup_itv	r/w	Live	000000	OC fault hiccup interval time. 000000: 4ms 1 LSB = 4ms

MFR_UVP_PGOOD_ON_LIMIT (D9h)

Bits	Name	Access	Behavior	Default	Description
[7:4]	Reserved	r		0000	Always read as 0000.
[3:2]	UV_TH	r/w	Live	00	Sets the UVP threshold. When FB drops below the UV_TH level, the IS6608A enters UVP. The response of UVP is the same as in OCP. 00: 69% * VREF 01: 74% * VREF 10: 79% * VREF 11: 84% * VREF
[1:0]	PG_ON	r/w	Live	00	Sets the threshold of FB at which PG is pulled high during soft start. Once FB reaches the threshold, PG is pulled high after the delay set by D1[5:2]. 00: 90% * VREF 01: 92.5% * VREF 10: 95% * VREF 11: 97.5% * VREF

MFR_FB_STEP (DAh)

Bits	Name	Access	Behavior	Default	Description
[7:4]	Reserved	r		0000	Always read as 0000.
[3:0]	FB_step	r/w	Live	0000	0000: 5μs/mV 1LSB = 1μs/mV

MFR_LOW_POWER (E5h)

Bits	Name	Access	Behavior	Default	Description
[7:2]	Reserved	r		000000	Always read as 000000.
[1:0]	LP_PS#	r/w	Live	00	11: low-power mode is enabled when PS# is low and disabled when PS# is high Others: Auto phase shedding

MFR_CTRL (EAh)

Bits	Name	Access	Behavior	Default	Description
[15:11]	Reserved	r		00000	Always read as 00000.
[10]	Total_OC_ hiccup_interval	r/w	Live	0	Chooses whether the interval during OCP HICCUP can be changed through register D8h. 0: fixed OCP hiccup interval 1: adjustable OCP hiccup interval
[9]	OSM	r/w	Live	0	Enables or disables the output sink mode (OSM) function. 0: enable output sink mode (OSM) 1: disable OSM
[8]	Reserved	r		0	Always read as 0.
[7]	Auto_phase	r/w	Live	0	0: disable 1: enable
[6:4]	Phase_count	r/w	Live	000	Set the count of phase
[3]	Phase_manage	r/w	Live	1	0: single-phase 1: multi-phase

[2:0]	Reserved	r		000	Always read as 00.

MFR_CTRL (F8h)

F8H command can be setting slave

Bits	Name	Access	Behavior	Default	Description
[7:6]	Reserved	r/w	Live	11	01:slave phase cannot be read 11:slave phase can be read Others: Reserved
[5:0]	Reserved	r		00000	Always read as 00000.

PCB Layout Guidelines

Efficient PCB layout plays an important role to achieve stable operation. For optimal performance, follow these guidelines.

1. Place the input MLCC capacitors as close to the IN and PGND pins as possible.
2. Place one 1 μF 0402 MLCC near pin1.
3. Place the major MLCC capacitors on the same layer as the IS6608A.
4. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
5. Place a VCC decoupling capacitor close to the device.
6. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
7. Place BST capacitor as close to BST and SW as possible. Routing widths should be greater than 20 mm. It is recommended to use a 0.1 μF to 1 μF bootstrap capacitor.

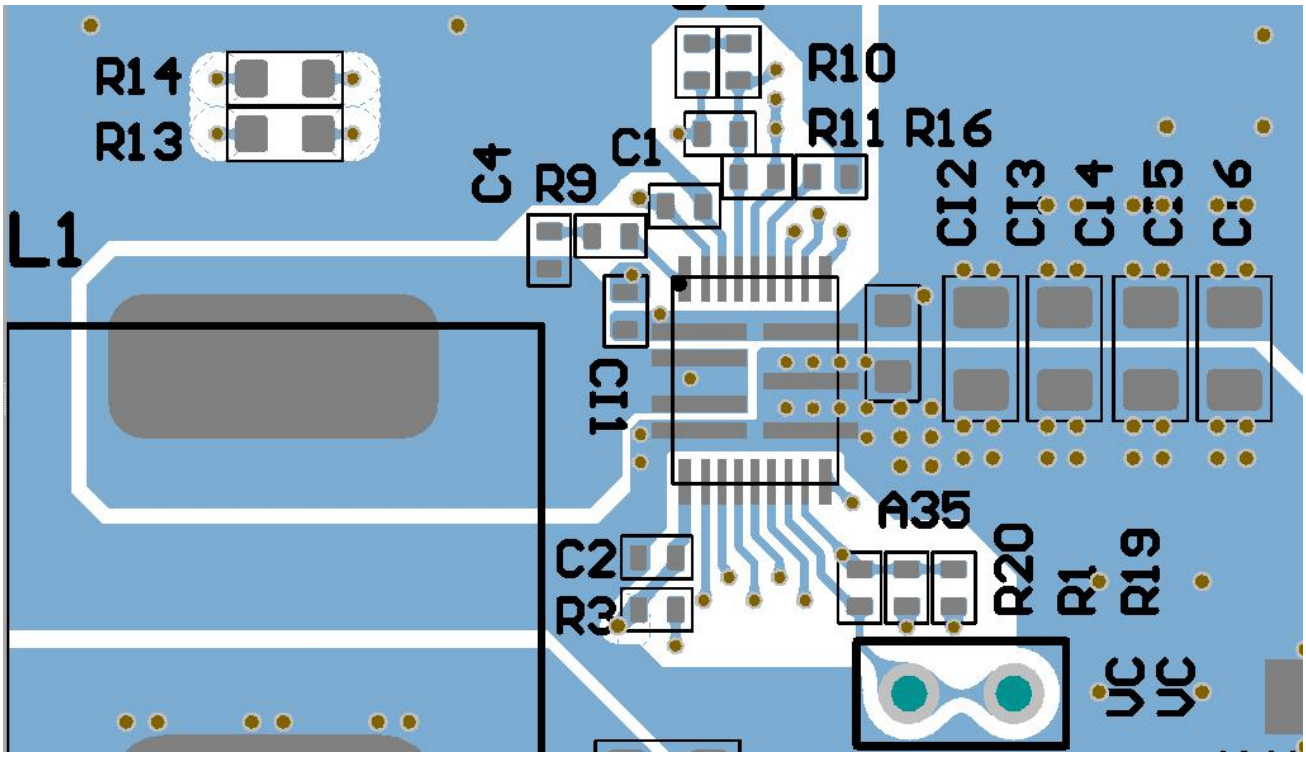
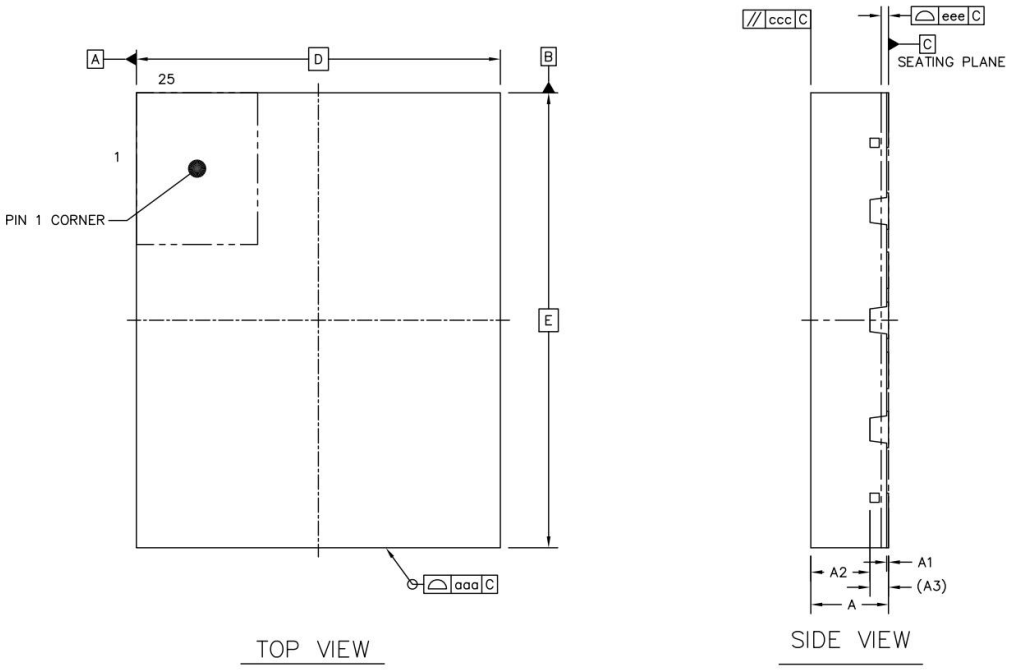
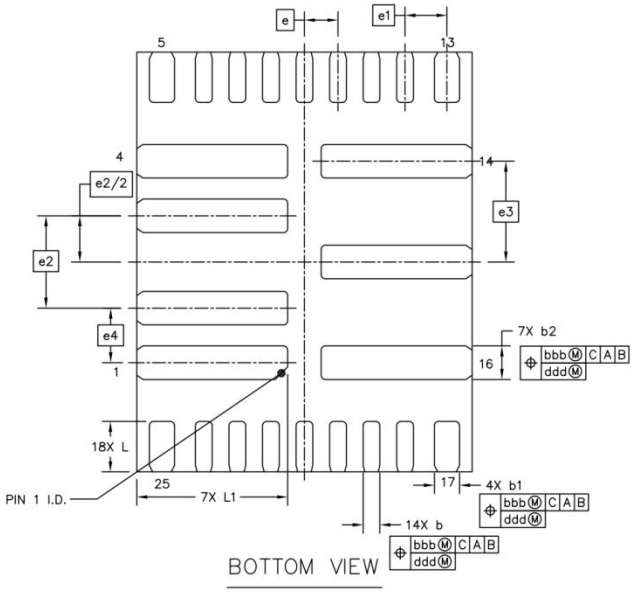


Figure 8: Example of PCB Layout (Placement and Top Layer）

Package Dimension

QFN-25(4mm X 5mm)





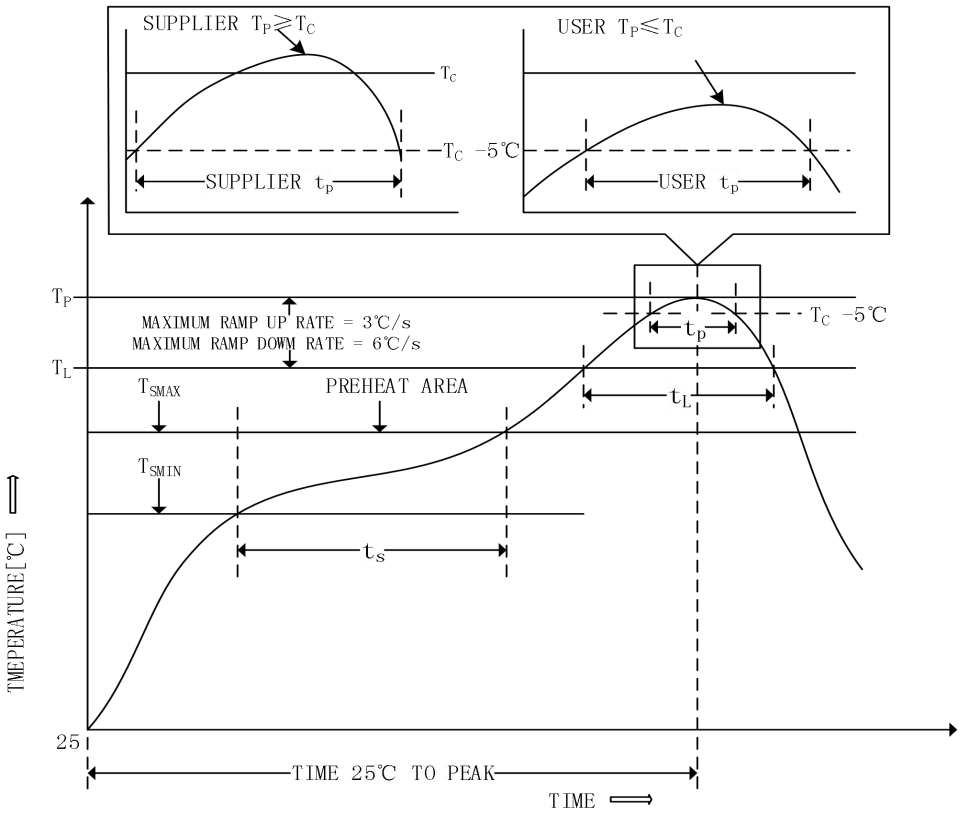
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
		b1	0.25	0.3	0.35
		b2	0.35	0.4	0.45
BODY SIZE	X	D		4 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.4 BSC	
		e1		0.5 BSC	
		e2		1.1 BSC	
		e3		1.2 BSC	
		e4		0.65 BSC	
LEAD LENGTH		L	0.5	0.6	0.7
		L1	1.7	1.8	1.9
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	

Unit：mm

Reflow Specification

Qualification Reflow: The IS6608 was qualified in accordance with IPC/JEDEC J-STD-020D.01. This standard classifies proper packaging, storage and handling in order to avoid subsequent thermal and mechanical damage during the solder reflow attachment phase of PCB assembly.

The qualification preconditioning process specifies a sequence consisting of a bake cycle, moisture soak cycle (in a temperature humidity oven), and three consecutive solder reflow cycles, followed by functional device testing.



Production Reflow:

PROFILE FEATURE	SN - PB EUTECTIC ASSEMBLY	PB-FREE ASSEMBLY
Peak package body temperature (TP)	For users, TP must not exceed TC(235℃).For suppliers, TP must equal or exceed TC(235℃).	For users, TP must not exceed TC(260℃).For suppliers, TP must equal or exceed TC(260℃).

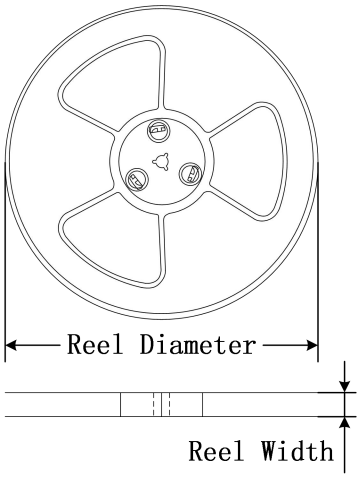
Storage Specifications

The storage specification of the IS6608 conforms to IPC/JEDEC J-STD-020D.01 Moisture Sensitivity Level (MSL) 3.

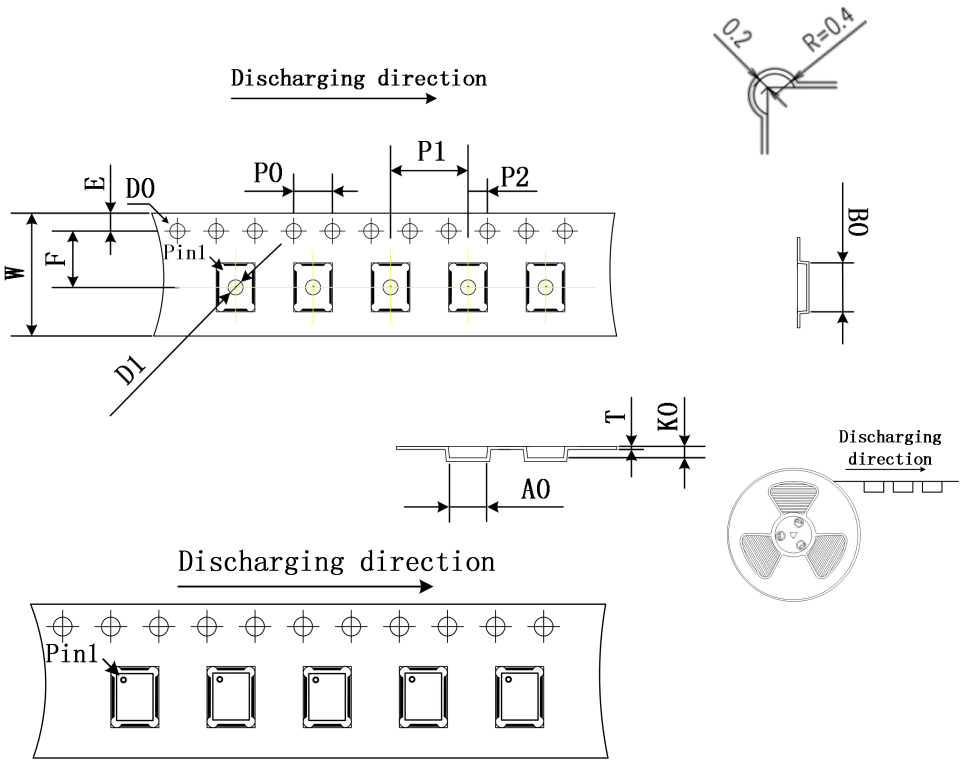
After opening moisture-sealed bag	168 hours -- Storage conditions: ambient ≤30°C at 60%RH

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter (inch)	Reel Width（mm）
QFN-25(4 x 5)	13″	

NOTE:

1) .The accumulative error of any 10 chain holes shall not exceed ± 0.2mm

2). The non-parallelism of 100mm long carrier band in the carrier band length direction shall not exceed 1mm.

3) . Material: black, PS material.

4) .All dimensions meet the requirements of EIA-481-D.

5) .This picture is for reference only. Refer to the actual product.

Unit(mm)

EIA	W	E	F	A0	B0	K0	P0	P1	P2	D0	D1	T
DIM	12 ±0.3	1.75 ±0.1	5.5 ±0.1	4.25 ±0.1	5.25 ±0.1	1.2 ±0.1	4.00 ±0.1	8.00 ±0.1	2.00 ±0.1	1.5 ±0.1	1.5 ±0.1	0.3 ±0.05

REVISION HISTORY

REV.	Date	Description
2.4	2021.9.06	Features：VCC Bias Typical Application Circuit Order Information EN Input high voltage EN Input Low voltage Figure 8: Example of PCB Layout EN pin out description PS pin out description