4-Bit Bidirectional Voltage-Level Translator with Auto Direction Sensing

Features

- Voltage level translator without direction control signal
- Wide V_{CCA},V_{CCB} operating range:1.1V to 5V
- V_{CCA} and V_{CCB} are independent: V_{CCA} may be greater than, equal to, or less than V_{CCB}
- 100 pF capacitance drive capability
- 140 Mbps date rate for V_{CCA} and V_{CCB} > 1.8 V
- VCC isolation feature – If either VCC input is at GND, all outputs are in High-Impedance state
- OE input circuit referenced to V_{CCA}
- QFN 1.8mm×1.8mm×0.55mm-12L package
  QFN 2.0mm×1.7mm×0.5mm-12L package

Applications

Portable Equipment
UART
GPIO

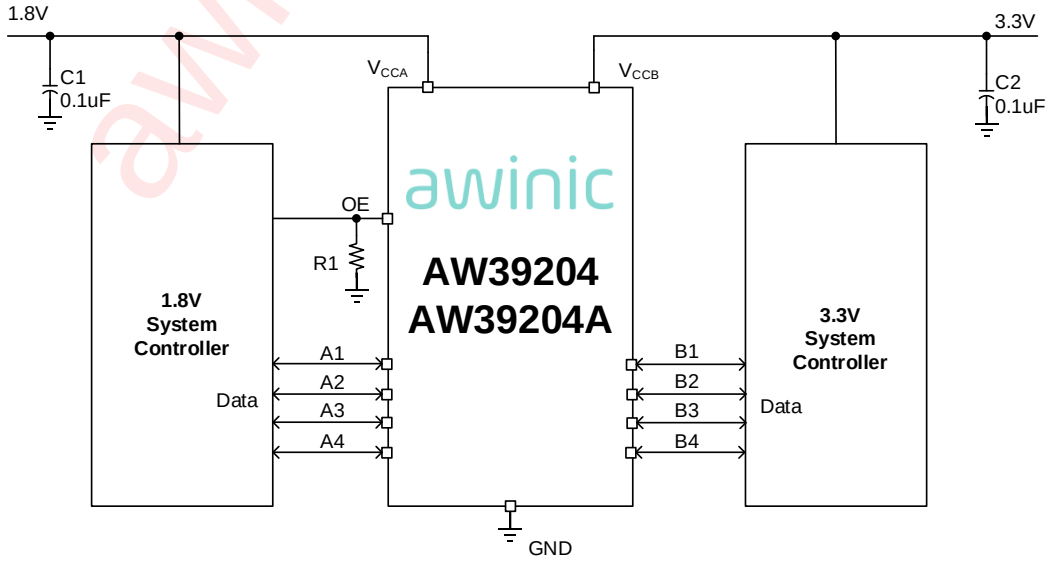
General Description

AW39204/AW39204A is a 4-bit non-inverting bidirectional voltage-level translator, it can be used to convert digital signal with mixed-voltage systems. It needs two separate power supply rails, with the A ports supporting operating voltages from 1.1 V to 5 V while it tracks the V_{CCA} supply, and the B ports supporting operating voltages from 1.1 V to 5 V while it tracks the V_{CCB} supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.2 V,1.8 V, 2.5 V, 3.3 V, and 5 V voltage nodes.

If the voltage level of output-enable (OE) pin is low, the chip works in the high-impedance state, which significantly reduces the power-supply quiescent current consumption. And the OE input circuit is supplied by V_{CCA}.

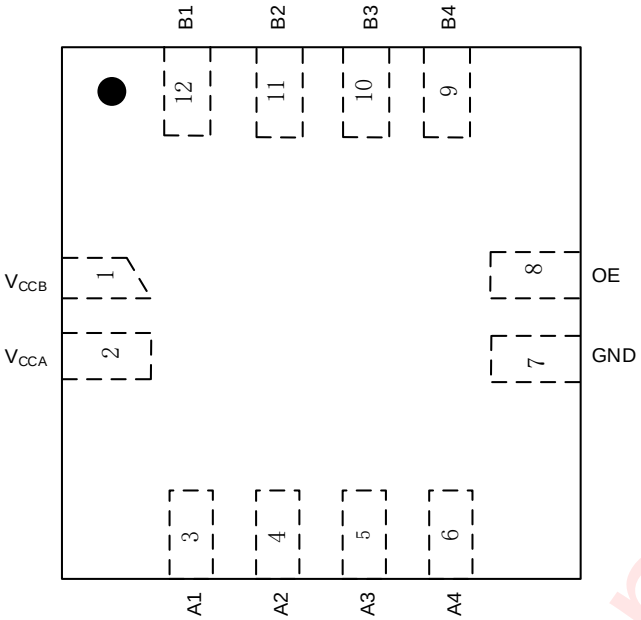
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Typical Application Circuit



Pin Configuration and Top Mark

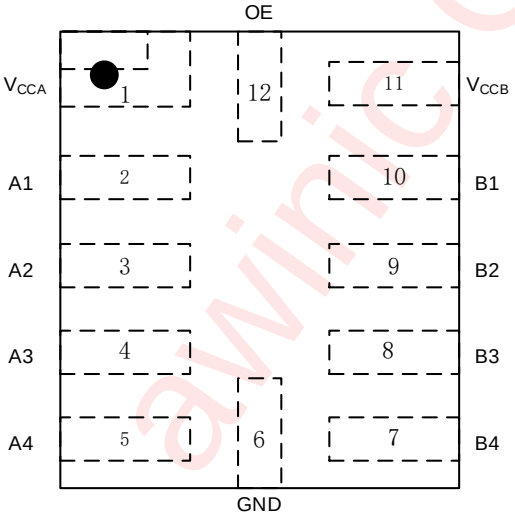
AW39204QNR
(Top View)



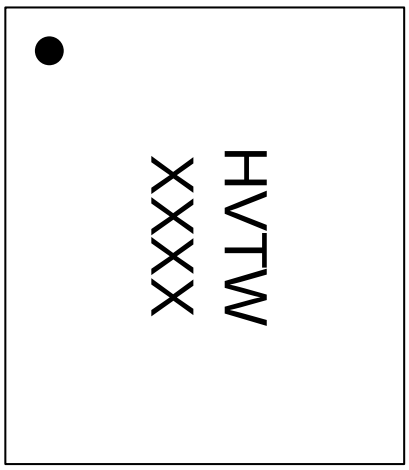
AW39204QNR Marking
(Top View)

FP6R – AW39204QNR
XXXX - Production Tracing Code

AW39204AQNR
(Top View)



AW39204AQNR Marking
(Top View)

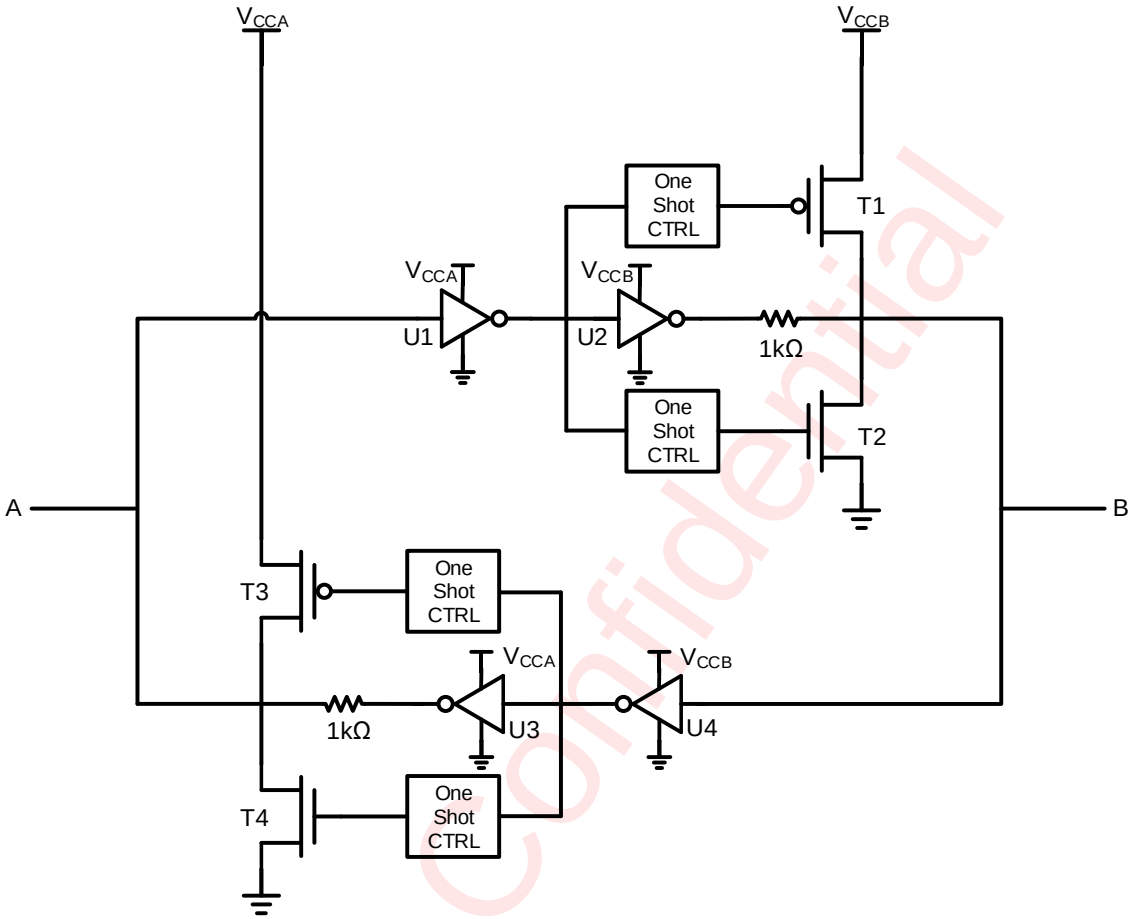


HVTW – AW39204AQNR
XXXX - Production Tracing Code

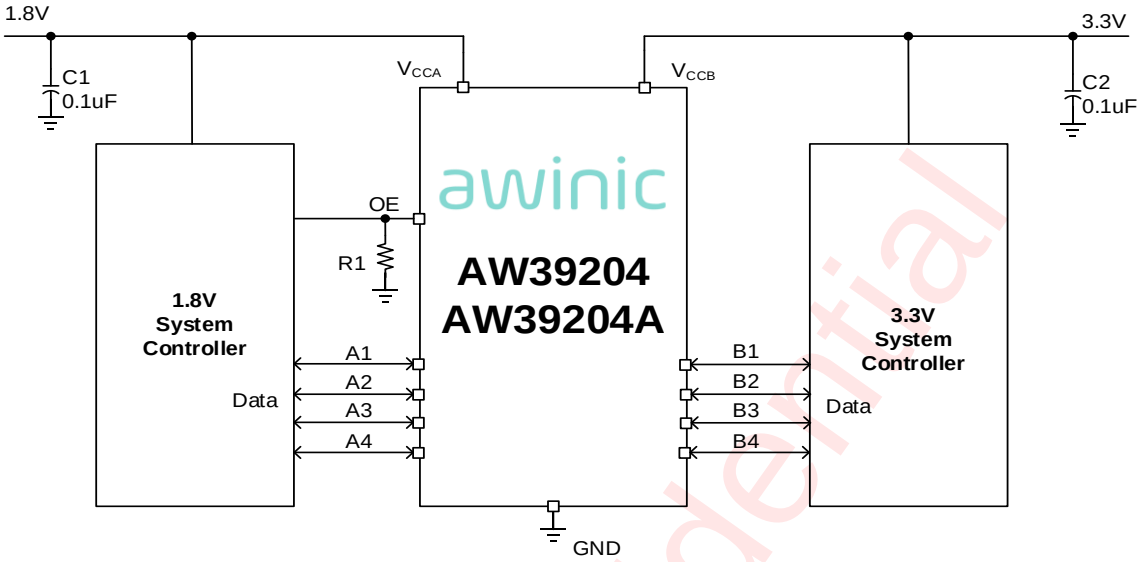
Pin Definition

No.		NAME	DESCRIPTION
AW39204QNR	AW39204AQNR		
1	11	V_{CCB}	B-port supply voltage
2	1	V_{CCA}	A-port supply voltage
3	2	A1	Input/output 1. Referenced to V_{CCA}
4	3	A2	Input/output 2. Referenced to V_{CCA}
5	4	A3	Input/output 3. Referenced to V_{CCA}
6	5	A4	Input/output 4. Referenced to V_{CCA}
7	6	GND	Ground
8	12	OE	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
9	7	B4	Input/output 4. Referenced to V_{CCB}
10	8	B3	Input/output 3. Referenced to V_{CCB}
11	9	B2	Input/output 2. Referenced to V_{CCB}
12	10	B1	Input/output 1. Referenced to V_{CCB}

Functional Block Diagram



Typical Application Circuits



AW39204/AW39204A Application Circuit

- ***Notice for typical application circuits:***

1. Capacitance of C1 and C2 should be 0.1μF or more.
2. Resistance of R1 should be 100kΩ or more for current consumption.
3. The device driving the data I/Os of the AW39204QNR/AW39204AQNR must have the drive strength of at least ±3 mA.
4. Pull-up resistors are not required on both sides for Logic I/O.
5. If pull-up or pull-down resistors are needed, the resistor value must be over 20 kΩ.
6. The AW39204QNR/AW39204AQNR should not be used in applications such as I2C or 1-Wire, please refer to the AW39104 or contact Awinic.
7. The output ports are disabled when either power supply is off (V_{CCA} or V_{CCB} = 0 V). This feature causes all of the I/O pins to be in the power saving high impedance state.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW39204QNR	-40°C～85°C	QFN 1.8mm×1.8mm-12L	FP6R	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW39204AQNR	-40°C～85°C	QFN 2.0mm×1.7mm-12L	HVTW	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage	V_{CCA}	-0.3 to 6V
	V_{CCB}	-0.3 to 6V
V_I Input voltage	A port	-0.3 to 6V
	B port	-0.3 to 6V
V_O Output voltage range in high or low state	A port	-0.3 to 6V
	B port	-0.3 to 6V
Junction-to-ambient thermal resistance θ_{JA}(NOTE2)		120°C /W
Operating free-air temperature range		-40°C -85°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C -150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
HBM(NOTE3)		±6kV
CDM(NOTE4)		±1.5kV
Latch-Up		
Test condition(NOTE5)		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE3: All pins. Test Condition: ANSI/ESDA/JEDEC JS-001 2017.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

*NOTE5: All pins. Test Condition:*JESD78E-2016

Recommended Operating Conditions

SYMBOL	PARAMETERS		RANGE
V_{CCA}	Supply voltage		1.1V to 5V
V_{CCB}			1.1V to 5V
V_{OE}	Enable control pin voltage		0V to 5V
V_{IO}	Input/Output voltage	A-port	0V to 5V
		B-port	0V to 5V
T_A	Operating free-air temperature		-40°C to 85°C
△t/△V	Input transition rise or fall rate V_I, V_{IO} from30%to70% of VCC; VCC = 3.3 V±0.3 V		0 to 40ns/V

DC Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		V_{CCA}(V)	V_{CCB}(V)	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		T_A = 25°C	1.2 – 5	1.2 – 5	0.8× V_{CC}			V
V_{OEH}	OE High-level input voltage		T_A = 25°C	1.2 – 5	1.2 – 5	0.8 ×V_{CCA}			V
V_{IL}	Low-level input voltage		T_A = 25°C	1.2 – 5	1.2 – 5			0.2 ×V_{CC}	V
V_{OEL}	OE Low-level input voltage		T_A = 25°C	1.2 – 5	1.2 – 5			0.2 ×V_{CC}	V
V_{OHA}	High-level output voltage	I_{OH}=-20μA	T_A = 25°C	1.2 – 5		0.9 × V_{CCA}			V
V_{OLA}	Low-level output voltage	I_{OL}=20μA	T_A=-40°C-85°C	1.2 – 5				0.2	V
V_{OHB}	High-level output voltage	I_{OH}=-20μA	T_A = 25°C		1.2 – 5	0.9× V_{CC}			V
V_{OLB}	Low-level output voltage	I_{OL}=20μA	T_A = -40°C - 85°C		1.2 – 5			0.2	V
I_I	OE Pin Input Current	V_I = V_{CC} or GND	T_A = 25°C	1.2 – 5	1.2 – 5			±1	μA
			T_A = -40°C - 85°C	1.2 – 5	1.2 – 5			±2	μA
I_{OFF}	A-port	V_I or V_O = 0 to 4.5 V	T_A = 25°C	0	1.2 – 5			±1	μA
			T_A = -40°C - 85°C					±2	μA
	B-port		T_A = 25°C	1.2 – 5	0			±1	μA
			T_A = -40°C-85°C					±2	μA
I_{OZ}	A or B port	OE = GND	T_A = 25°C	1.2 – 5	1.2 – 5			±1	μA
			T_A = -40°C - 85°C	1.2 – 5	1.2 – 5			±2	μA
I_{CCA}		V_I = V_{CC} or GND, I_O = 0	T_A = 25°C	1.2 – 5	1.2 – 5			3	μA
			T_A = -40°C - 85°C	1.2 – 5	1.2 – 5			5	μA
I_{CCB}		V_I = V_{CC} or GND, I_O = 0	T_A = 25°C	1.2 – 5	1.2 – 5			3	μA
			T_A = -40°C - 85°C	1.2 – 5	1.2 – 5			5	μA
I_{CCZA}	High-Z state supply current	V_I = V_{CC} or GND, I_O = 0, OE = GND	T_A = 25°C	1.2 – 5	1.2 – 5			3	μA
			T_A = -40°C - 85°C	1.2 – 5	1.2 – 5			5	μA
I_{CCZB}	High-Z state supply current	V_I = V_{CC} or GND, I_O = 0, OE = GND	T_A = 25°C	1.2 – 5	1.2 – 5			3	μA
			T_A = -40°C - 85°C	1.2 – 5	1.2 – 5			5	μA

Timing Requirements

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	LOAD	V_{CCA}(V)	V_{CCB}(V)	MIN	MAX	UNIT
Data rate	C_L=15pF	1.2-5	1.2-5		50	Mbps
	C_L=15pF	1.8-5	1.8-5		140	Mbps
	C_L=30pF	1.2-5	1.2-5		40	Mbps
	C_L=30pF	1.8-5	1.8-5		120	Mbps
	C_L=50pF	1.2-5	1.2-5		30	Mbps
	C_L=50pF	1.8-5	1.8-5		100	Mbps
	C_L=100pF	1.2-5	1.2-5		20	Mbps
	C_L=100pF	1.8-5	1.8-5		60	Mbps

Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

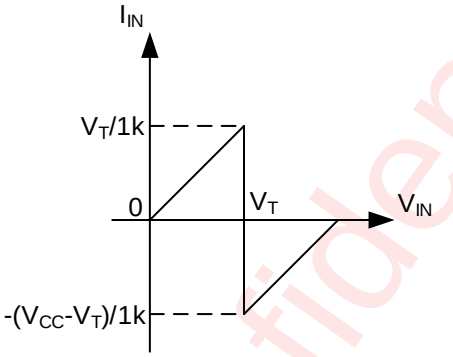
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V_{CCA}(V)	V_{CCB}(V)	MIN	TYP	MAX	UNIT
T_{PD}	A	B	C_L=15pF	1.2-5	1.2-5		18	35	ns
			C_L=15pF	1.8-5	1.8-5		9	18	
			C_L=30pF	1.2-5	1.2-5		18	35	
			C_L=30pF	1.8-5	1.8-5		8	18	
			C_L=50pF	1.2-5	1.2-5		19	35	
			C_L=50pF	1.8-5	1.8-5		9	18	
			C_L=100pF	1.2-5	1.2-5		20	35	
			C_L=100pF	1.8-5	1.8-5		10	18	
	B	A	C_L=15pF	1.2-5	1.2-5		18	35	ns
			C_L=15pF	1.8-5	1.8-5		9	18	
			C_L=30pF	1.2-5	1.2-5		18	35	
			C_L=30pF	1.8-5	1.8-5		9	18	
			C_L=50pF	1.2-5	1.2-5		19	35	
			C_L=50pF	1.8-5	1.8-5		9	18	
			C_L=100pF	1.2-5	1.2-5		19	35	
			C_L=100pF	1.8-5	1.8-5		10	18	
t_{en}	OE	A	C_L=15pF	1.2-5	1.2-5		50	150	ns
		B	C_L=15pF	1.8-5	1.8-5		50	100	ns
t_{dis}	OE	A	C_L=15pF	1.2-5	1.2-5		95	200	ns
		B	C_L=15pF	1.8-5	1.8-5		95	200	ns
t_{rB}, t_{fB}	B-port rise and fall times		C_L=15pF	1.2-5	1.2-5		1.5		ns
t_{rA}, t_{fA}	A-port rise and fall times		C_L=15pF	1.2-5	1.2-5		1.5		ns
t_{SK}	Channel-to-channel skew		C_L=15pF	1.2-5	1.2-5		0.5		ns

Typical Characteristics

AW39204/AW39204A is a 4-bit voltage-level translator without direction control signal, which is suitable for interfacing devices or systems operating at different interface voltages with one another. Port A can supports I/O voltages from 1.1 V to 5 V, while Port B is able to support I/O voltage range from 1.1 V to 5 V.

Input Driver Requirements

The figure shows the typical I_{IN} vs V_{IN} curve. For proper operation, the device driving the data I/Os of the AW39204QNR/AW39204AQNR must have the drive strength of at least ±3 mA.



(1) V_{CC} is the supply voltage.

(2) V_T is the input threshold voltage of AW39204QNR/AW39204AQNR (typically it is VCC/2).

Typical I_{IN} vs V_{IN} Curve

VCC Capacitor Selection

The device is a 4-bit high-performance voltage-level translator that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, recommend 0.1μF or larger than 0.1μF.

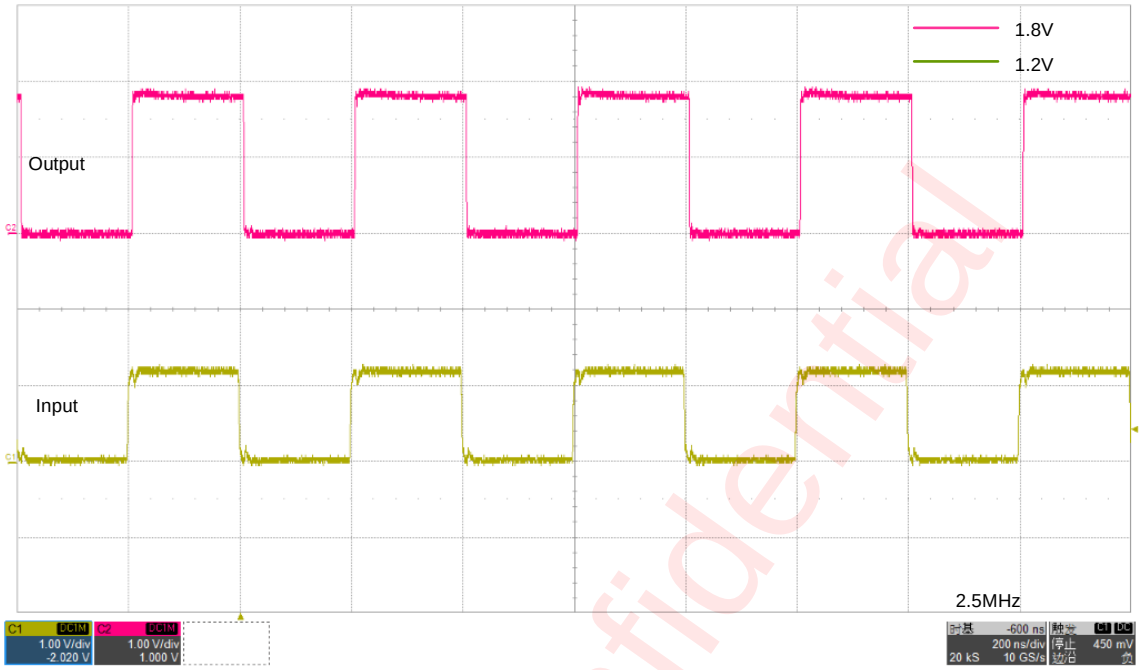
Input Voltage Range

V_{IH} is the lowest valid logic high value of the input port, V_{IL} is the highest valid logic low value of the input port, so the valid logic high value should exceed V_{IH}, the valid logic low value should less than V_{IH}.

I/O Current

Don't recommend to have the strong current on the I/O pins at the same time. Don't recommend to have the external pull-up or pull-down resistors.

Application Curve



2.5-MHz 1.2V-1.8V Signal Level-Translation @C_L=15p

2.5-MHz 1.2V-1.8V Signal Level-Translation @C_L=30p

2.5-MHz 1.8V-3.3V Signal Level-Translation @C_L=15p

2.5-MHz 1.8V-3.3V Signal Level-Translation @C_L=30p

Detailed Functional Description

AW39204/AW39204A is a 4-bit high-performance voltage-level translator without direction control signal, which is a non-inverting converter and can be used to convert digital signal with mixed-voltage systems. Port A can support I/O voltages from 1.1 V to 5 V, while Port B is able to support I/O voltage range from 1.1 V to 5 V. The chip uses a transmission gate architecture with an rising edge rate accelerator (one-shot), to increase overall data rate.

One-Shot Accelerator

The One-Shot rising edge accelerator circuit speeds up the rising edge to help increasing the chip's data rate. Once the chip has detected the rising edge of the input signal from low to high, which enables the internal pull-up PMOS transistor between power supply and output, thereby accelerating the output port from low to high. While detecting the output has been turned up, the one-shot pulse signal is finished and pull-up PMOS transistor is quickly turned off. This architecture reduces the average dynamic power consumption of the chip while allowing it to meet different drive requirements.

Enable and Disable

The AW39204/AW39204A has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs are actually disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pull-up or Pull-down Resistor on I/O Lines

The AW39204QNR/AW39204AQNR is designed to drive capacitive loads of up to 100 pF. The output drivers of the AW39204QNR/AW39204AQNR have low dc drive strength. If pull-up or pull-down resistors are connected externally to the data I/Os, their values must be kept higher than 20 kΩ to ensure that they do not contend with the output drivers of the AW39204QNR/AW39204AQNR. But if the receiver is integrated with the smaller pull down or pull up resistor, below formula can be used for estimation to evaluate the V_{OH} and V_{OL}.

$$V_{OL} = V_{CCout} * \frac{1.5k\Omega}{1.5k\Omega + R_{pu}}$$

$$V_{OH} = V_{CCout} * \frac{R_{pd}}{1.5k\Omega + R_{pd}}$$

where

- V_{CCout} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{pd} is the value of the external pull down resistor
- R_{pu} is the value of the external pull up resistor
- 1.5 kΩ is the counting the variation of the serial resistor 1kΩ in the I/O line.

Because of this restriction on external resistors, the AW39204QNR/AW39204AQNR should not be used in applications such as I2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the Awinic AW39104QNR series of level translators.

Power Up

During operation,AW39204/AW39204A can work at both $V_{CCA} \leqslant V_{CCB}$ and $V_{CCA} \geqslant V_{CCB}$. During power-up sequencing, any power supply can be ramped up first. The AW39204/AW39204A has circuitry that disables all output ports when either VCC is switched off ($V_{CCA/B}$ = 0 V).

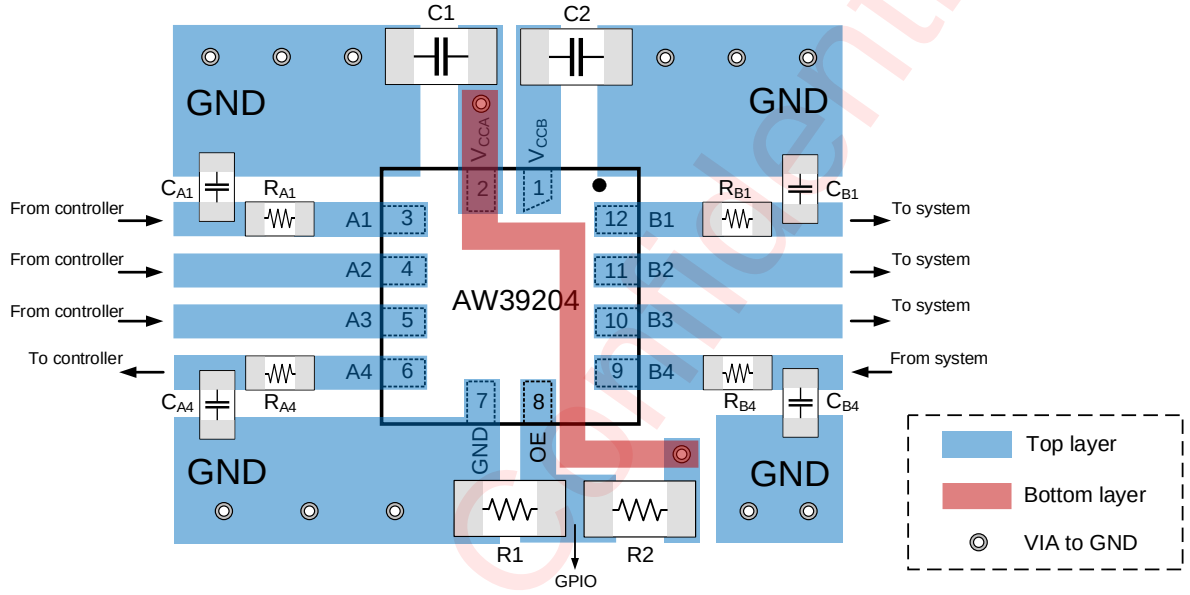
Power Off Protection

The AW39204/AW39204A has power protection function. When the chip is powered off but the signal input source on the port is not turned off, the port does not sink current to the chip when there is still signal input.

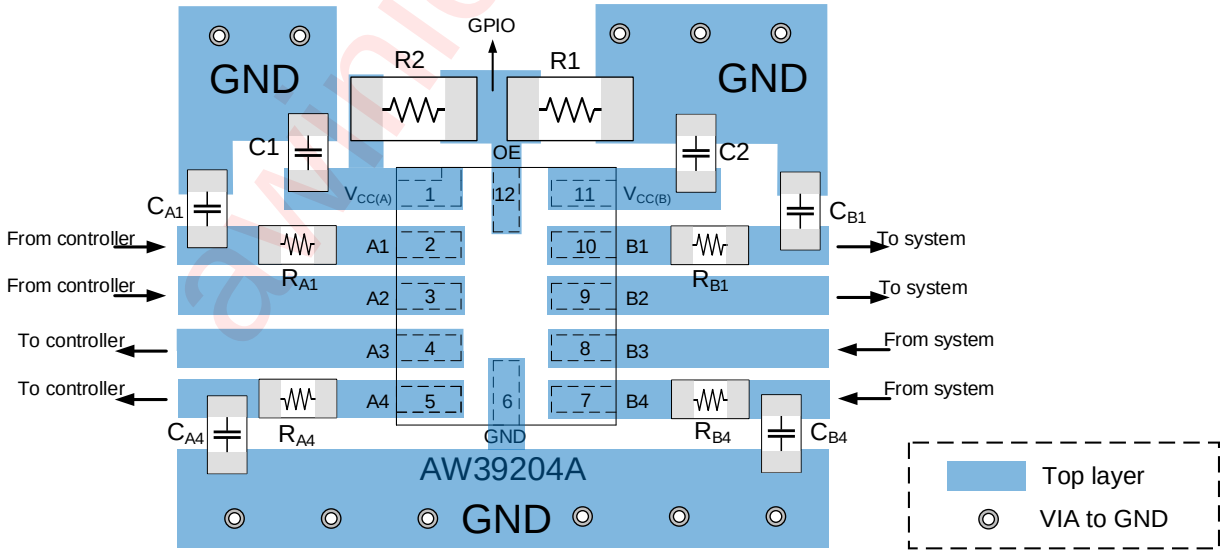
PCB Layout Consideration

To make full use of the performance of AW39204/AW39204A, the printed-circuit board layout guidelines below should be followed.

1. C1 and C2 should be placed on the top layer as close as possible to the V_{CCA} and V_{CCB} pin.
2. The trace of signals should be short enough to avoid any reflection when transmitted.
3. For long transmission lines, place a series resistor equivalent to the impedance of the transmission lines to avoid signal integrity issues.



AW39204 PCB Layout

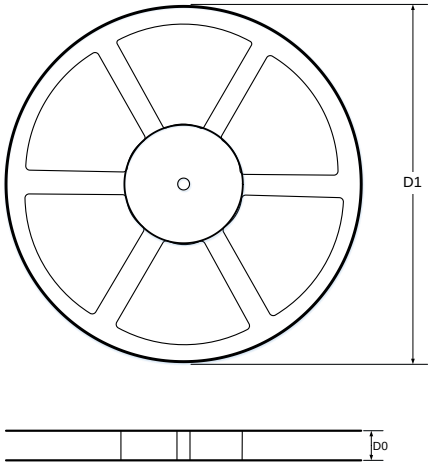


AW39204A PCB Layout

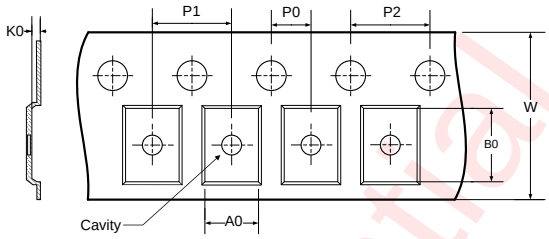
Tape And Reel Information

QFN 1.8mmX1.8mm-12L

REEL DIMENSIONS

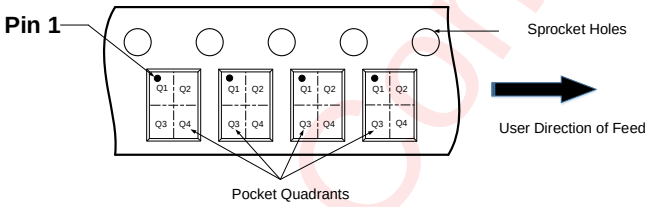


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



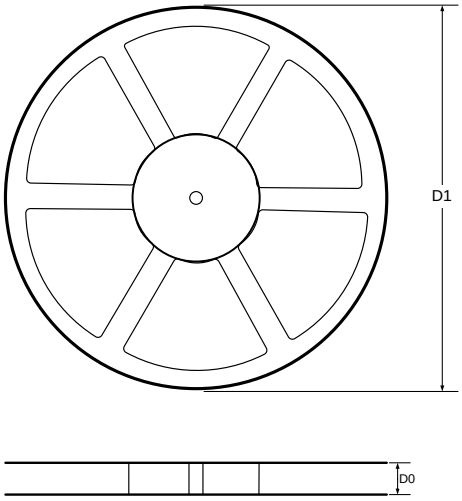
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.06	2.06	0.73	2	4	4	8	Q1

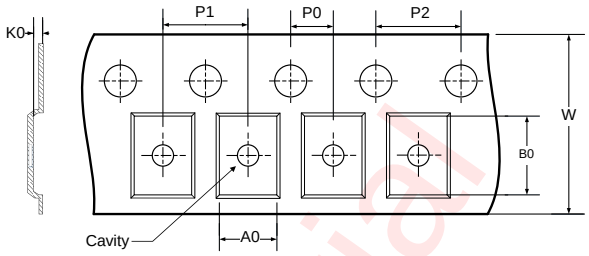
All dimensions are nominal

QFN 2.0mmX1.7mm-12L

REEL DIMENSIONS

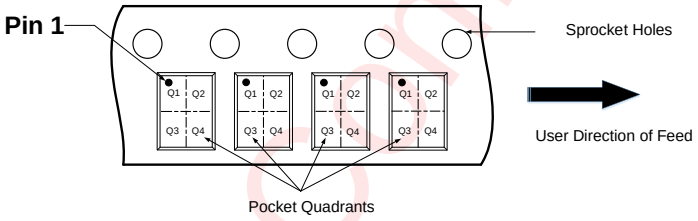


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

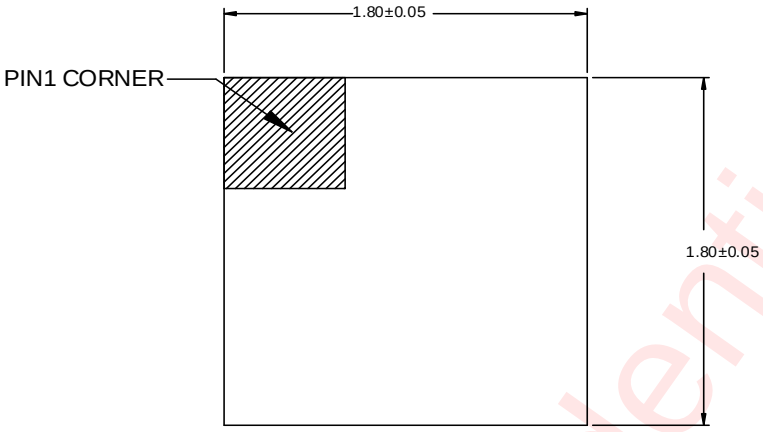
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180	9.5	1.9	2.3	0.75	2	4	4	8	Q1

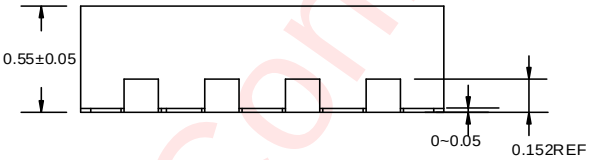
All dimensions are nominal

Package Description

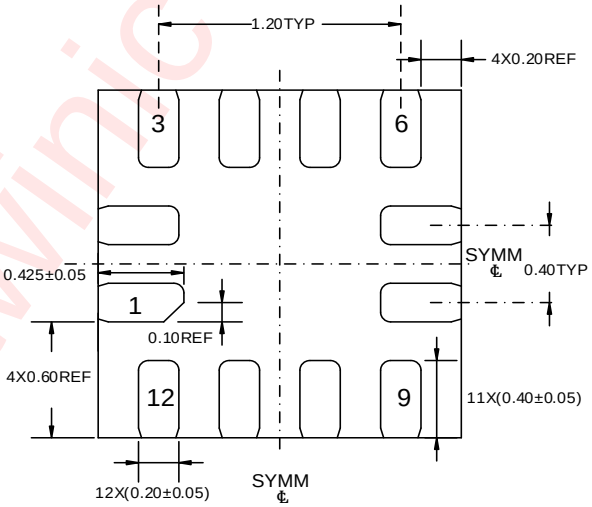
QFN 1.8mmX1.8mm-12L



TOP VIEW



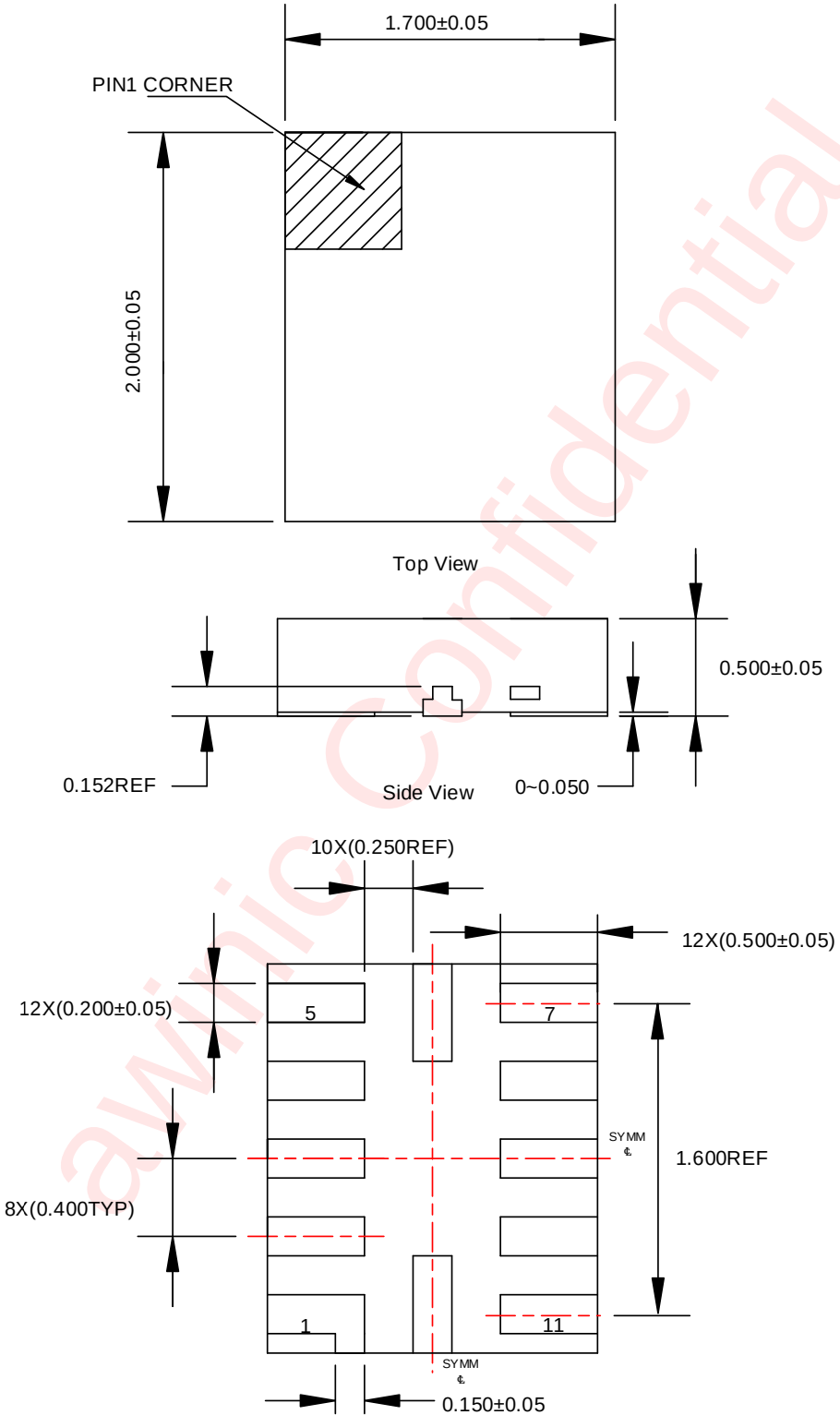
SIDE VIEW



BOTTOM VIEW

Unit：mm

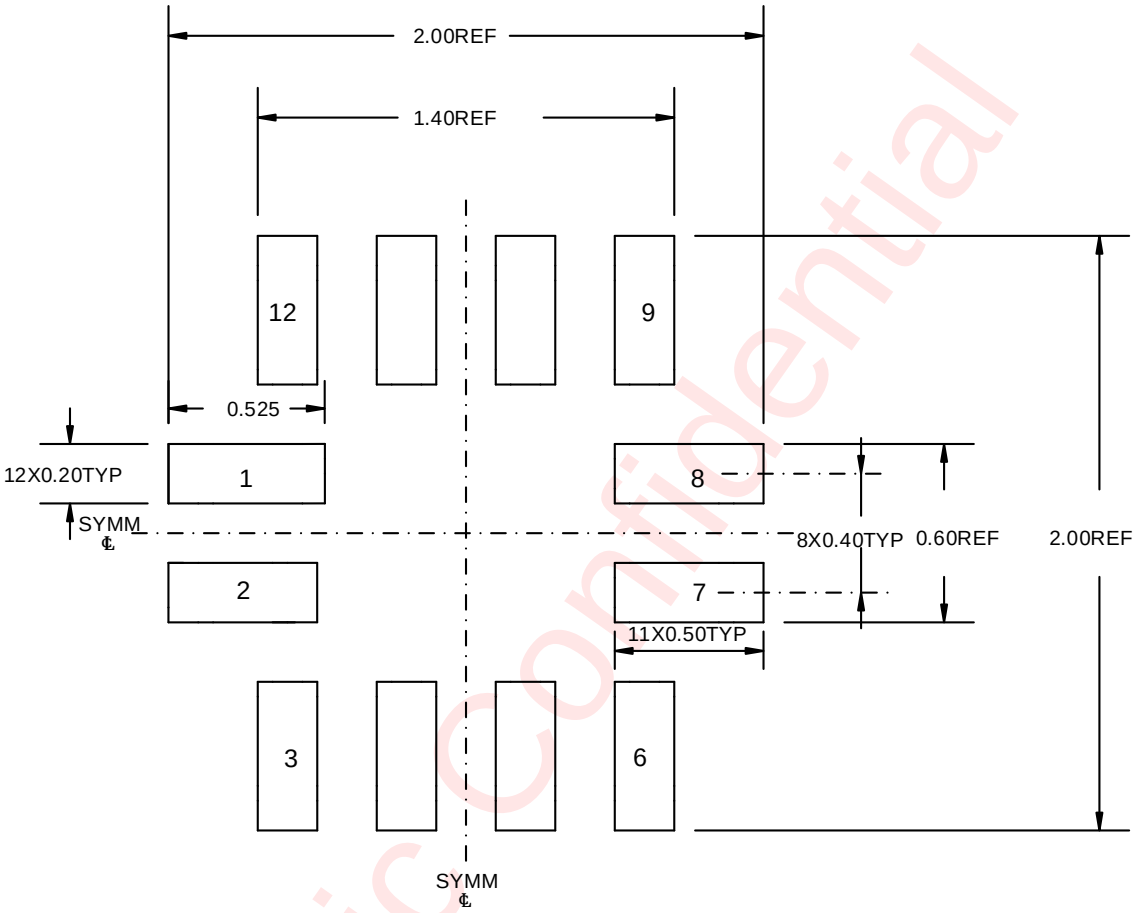
QFN 2.0mmX1.7mm-12L

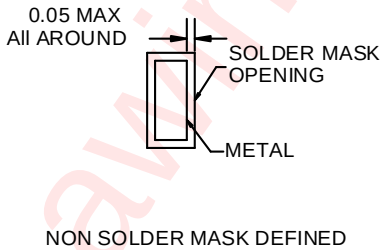


Unit: mm

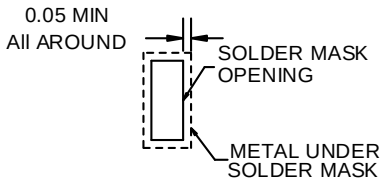
Land Pattern Data

QFN 1.8mmX1.8mm-12L





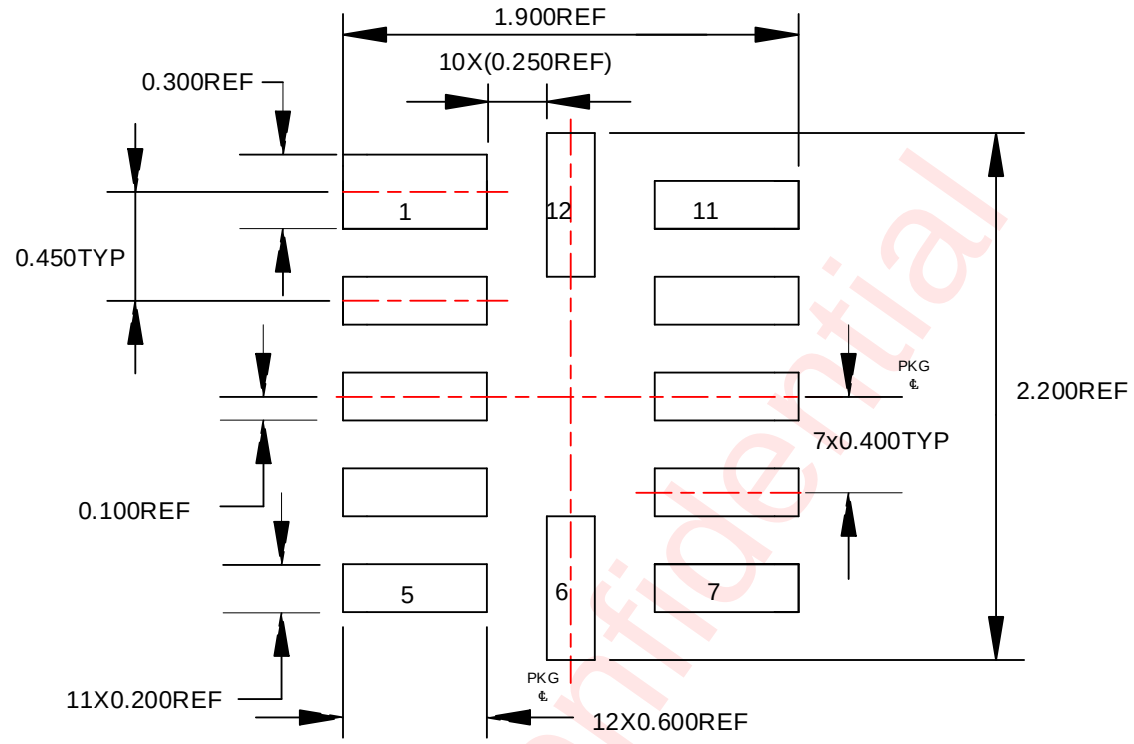
NON SOLDER MASK DEFINED

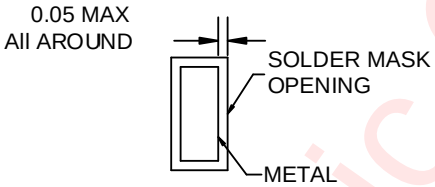


SOLDER MASK DEFINED

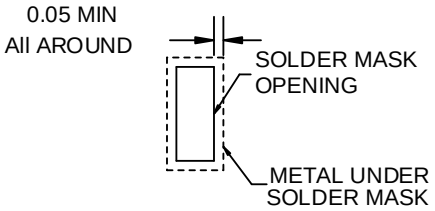
Unit: mm

QFN 2.0mmX1.7mm-12L





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit：mm

Revision History

Version	Date	Change Record
V1.0	December 2019	Officially released.
V1.1	March 2021	Add chapter input driver requirements and pull-up or pull-down resistor on I/O lines, update the application curve.
V1.2	May 2022	Add AW39204AQNR and Update the t_{dis}, HBM Characteristic
V1.3	May 2023	Revise ordering information format

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.