Low Noise Amplifier with Bypass Switch for LTE Middle Band

FEATURES

- Operating frequency 1805MHz to 2200MHz
- Noise figure(NF) =0.9dB
- High power gain =13.5dB
- Insertion Loss in bypass mode =3dB
- Gain mode IIP3ib=+7dBm
- Gain mode input 1dB-compression point=
 -1.2dBm
- Bypass mode input 1dB-compression point= +4dBm
- Supply voltage: 1.5V to 3.3V
- Gain mode current 8.0mA
- Bypass mode current <1uA
- Input and output DC decoupled
- Requires only one input matching inductor
- Integrated matching for the output
- FCDFN 1.1mmX0.7mmX0.37mm -6L package
- 2kV HBM ESD protection (including RFIN and RFOUT pin)

GENERAL DESCRIPTION

- The AW15208MFDR is a Low Noise Amplifier with bypass designed for LTE receiver applications. The AW15208MFDR requires only one external input matching inductor, reduces assembly complexity and the PCB area, enabling a cost-effective solution.
- The AW15208MFDR achieves low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5V up to 3.3V. All these features make AW15208MFDR an excellent choice for LTE LNA as it improves sensitivity with low noise figure and high gain, provides better immunity against jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost.
- The AW15208MFDR is available in a small lead-free, RoHS-Compliant, FCDFN 1.1mmX0.7mmX0.37 mm -6L package.

APPLICATIONS

- Cell phones
- Tablets
- Other RF front-end modules

TYPICAL APPLICATION CIRCUIT

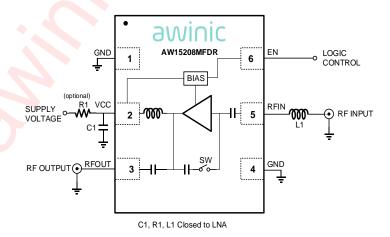


Figure 1 Typical Application Circuit of AW15208MFDR

1

PIN CONFIGURATION AND TOP MARK

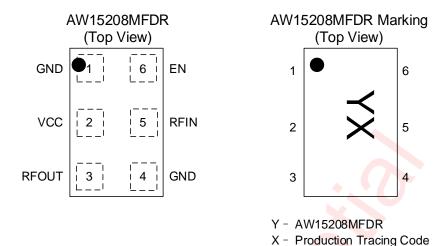


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

| No. | NAME | DESCRIPTION |
|-----|-------|--|
| 1 | GND | Ground |
| 2 | VCC | Supply connection |
| 3 | RFOUT | RF output |
| 4 | GND | Ground |
| 5 | RFIN | RF input |
| 6 | EN | EN (high level) supports 1.8V/2.8V IO with internal 150Kohm pull-down resistor |



FUNCTIONAL BLOCK DIAGRAM

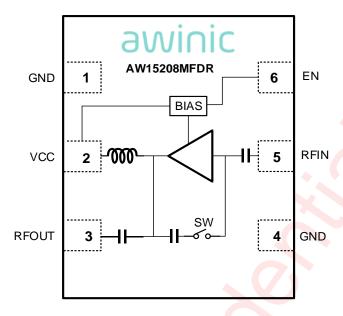


Figure 3 Functional Block Diagram

ORDERING INFORMATION

| Part Number | Temperature | Package | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form |
|-------------|-------------|------------------------------|---------|----------------------------------|------------------------------|------------------------------|
| AW15208MFDR | -40℃~85℃ | FCDFN 1.1mmX 0.7mm -6L | Y | MSL1 | ROHS+HF | 3000 units/Tape & Reel |

ABSOLUTE MAXIMUM RATINGS[1]

| PARAMETERS | RANGE | | |
|--|----------------------------|--|--|
| Supply voltage VCC | -0.3V to 3.6V | | |
| EN pin voltage | -0.3V to 3.6V | | |
| Supply maximum current ICC | 30mA | | |
| RF input power Pin | 25dBm | | |
| Maximum Junction temperature T _{JMAX} | 150°C | | |
| Storage temperature T _{STG} | -65℃ to 150℃ | | |
| Operating free-air temperature range | -40°C to 85°C | | |
| Lead temperature (Soldering 10 Seconds) | 260°C | | |
| ESD ^[2] | | | |
| НВМ | ±2kV | | |
| CDM | ±1kV | | |
| Latch-up | | | |
| Standard: JEDEC EIA/JESD78E | +IT: +200mA -IT: -200mA | | |

^[1] Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

^[2] The human body model is a 100pF capacitor discharged through a 1.5k Ω resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001-2017. The CDM test method: ANSI/ESDA/JEDEC JS-002-2018.

ELECTRICAL CHARACTERISTICS

TA=+25°C , V_{CC}=2.8V, EN=2.8V, frequency=1805MHz to 2200MHz. Input matched to 50Ω using a $3.3nH^{[3]}$ inductor in series. (unless otherwise noted).

| Symbol | Parameter | Test Condition | Min | Тур | Max | Units | | | |
|----------|--|--|-----|------|------|-------|--|--|--|
| DC Elect | DC Electrical Characteristic | | | | | | | | |
| VCC | Supply Voltage | | 1.5 | - | 3.3 | ٧ | | | |
| | Digital Input-Logic High | | 0.8 | | 3.3 | V | | | |
| VEN | Digital Input-Logic Low | | , (| | 0.45 | V | | | |
| IEN | Control current | | | | 10 | uA | | | |
| ISD | Leakage current | VDD=3.4V | | | 3 | uA | | | |
| Gain Mod | de | 4 | | • | • | | | | |
| ICC | Supply Current | VEN>0.8V | | 8 | 11 | mA | | | |
| Gp | Power Gain | 1805MHz-2200MHz [4] [5] | 12 | 13.5 | 15 | dB | | | |
| RLin | Input Return Loss | 1805MHz-2200MHz [4] [5] | 6 | 11.0 | | dB | | | |
| RLout | Output Return Loss | 1805MHz-2200MHz [4] [5] | 6 | 12.0 | | dB | | | |
| ISL | Reverse Isolation | 1805MHz-2200MHz [4] [5] | 17 | 25.0 | | dB | | | |
| NF | Noise Figure | 1805MHz-2200MHz [4] [5] | | 0.9 | 1.4 | dB | | | |
| IP1dB | In-band input 1dB-compression point | 1805MHz-2200MHz [4] [5] | -6 | -4.5 | | dBm | | | |
| IIP3ib | In-band input 3rd-order intercept point | 1805MHz-2200MHz [4] [5] | 0 | 6.7 | | dBm | | | |
| ton | turn-on time | time from V _{EN} ON to 90% of the gain | | 2 | 4 | μs | | | |
| toff | turn-off time | time from V _{EN} OFF to 10% of the gain | | 1 | 2 | μs | | | |
| K | Stability Factor | 0.2MHz-10GHz | 1 | | | | | | |
| Bypass N | Mode | | | | | | | | |
| ICC | Supply Current | VEN<0.45V | | | 1 | uA | | | |
| Gp | Power Gain | 1805MHz-2200MHz [4] [5] | -4 | -2.5 | | dB | | | |
| RLin | Input Return Loss | 1805MHz-2200MHz [4] [5] | 6 | 12.0 | | dB | | | |
| RLout | Output Return Loss | 1805MHz-2200MHz [4] [5] | 6 | 13.0 | | dB | | | |
| NF | Noise Figure | 1805MHz-2200MHz [4] [5] | | 2.5 | 4 | dB | | | |
| IP1dB | In-band input 1dB-compression point | 1805MHz-2200MHz [4] [5] | 1 | 4 | | dBm | | | |
| IIP3 | In-band input 3rd-order intercept point | 1805MHz-2200MHz [4] [5] | 6 | 11 | | dBm | | | |

^[3] High quality-factor 3.3nH inductor.

^[4] Input power is -25dBm.

^[5] PCB losses are subtracted.



TA=+25°C , Vcc=1.8V, EN=1.8V, frequency=1805MHz to 2200MHz. Input matched to 50Ω using a $3.3nH^{[3]}$ inductor in series. (unless otherwise noted).

| Symbol | Parameter | Test Condition | Min | Тур | Max | Units |
|--------|---|--------------------------------------|-----|------|------|-------|
| | | DC Electrical Characteristic | | l | | |
| VCC | Supply Voltage | | 1.5 | - | 3.3 | V |
| | Digital Input-Logic High | | 0.8 | | 3.3 | ٧ |
| VEN | Digital Input-Logic Low | | | | 0.45 | V |
| IEN | Control current | 4 | | | 10 | uA |
| ISD | Leakage current | VDD=3.4V | | | 3 | uA |
| | | Gain Mode | | | | |
| ICC | Supply Current | VEN>0.8V | | 8.0 | 10 | mA |
| Gp | Power Gain | 1805MHz-2200MHz [4] [5] | 12 | 13.1 | 15 | dB |
| RLin | Input Return Loss | 1805MHz-2200MHz [4] [5] | 6 | 8.0 | | dB |
| RLout | Output Return Loss | 1805MHz-2200MHz [4] [5] | 6 | 12.0 | | dB |
| ISL | Reverse Isolation | 1805MHz-2200MHz [4] [5] | 17 | 25.0 | | dB |
| NF | Noise Figure | 1805MHz-2200MHz [4] [5] | | 0.9 | 1.4 | dB |
| IP1dB | In-band input 1dB-compression point | 1805MHz-2200MHz [4] [5] | -8 | -6.7 | | dBm |
| IIP3ib | In-band input 3rd-order intercept point | 1805MHz-2200MHz [4] [5] | 0 | 6.7 | | dBm |
| ton | turn-on time | time from VEN ON to 90% of the gain | | 2 | 4 | μs |
| toff | turn-off time | time from VEN OFF to 10% of the gain | | 1 | 2 | μs |
| K | Stability Factor | 0.2MHz-10GHz | 1 | | | |
| | | Bypass Mode | | | | |
| ICC | Supply Current | VEN<0.45V | | | 1 | uA |
| Gp | Power Gain | 1805MHz-2200MHz [4] [5] | -4 | -3.0 | | dB |
| RLin | Input Return Loss | 1805MHz-2200MHz [4] [5] | 6 | 11.5 | | dB |
| RLout | Output Return Loss | 1805MHz-2200MHz [4] [5] | 6 | 13.0 | | dB |
| NF | Noise Figure | 1805MHz-2200MHz [4] [5] | | 3 | 4 | dB |
| IP1dB | In-band input 1dB-compression point | 1805MHz-2200MHz [4] [5] | 1 | 4 | | dBm |
| IIP3 | In-band input 3 rd -order intercept point | 1805MHz-2200MHz [4] [5] | 6 | 11 | | dBm |

^[3] High quality-factor 3.3nH inductor.

^[4] Input power is -25dBm.[5] PCB losses are subtracted.

二海艾万电子技术股份有限公司

Aug. 2021 V1.5

MEASUREMENT DIAGRAM

Test DC Characteristics(Current & Power Consumption)

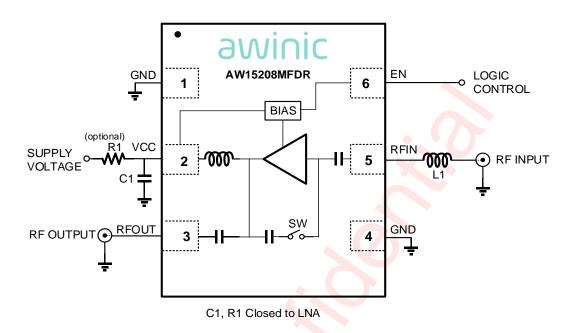


Figure 4 AW15208MFDR DC Test Diagram

Test S-Parameter

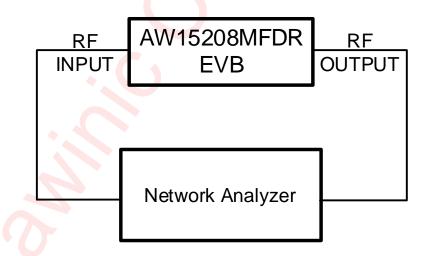


Figure 5 AW15208MFDR S-parameter Measurement Diagram

上海艾为电子技术股份有眼公司
Shanghai awinic technology co., ltd.

Aug. 2021 V1.5

Test Noise Figure

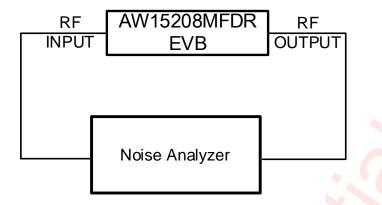


Figure 6 AW15208MFDR Noise Figure Measurement Diagram

Test IIP3

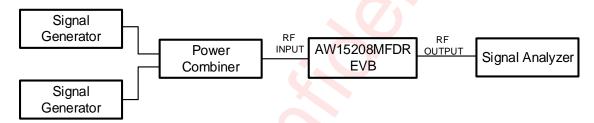


Figure 7 AW15208MFDR IIP3 Measurement Diagram

APPLICATION INFORMATION

Choice of components

- The AW15208MFDR requires only one external inductor for input matching. If the device/phone manufacturers implement very good power supply filtering on their boards, the bypass capacitor mentioned in this application circuit may be optional. With the power supply decoupling capacitor, better performance would be received, like a little higher gain, etc. The value is optimized for the key performance, such as higher power gain, lower noise figure, and better return loss. Typical value of inductor is 3.3nH with high quality factor, and capacitor is 1nF. The typical application circuit can refer to Figure1.
- The output of AW15208MFDR is internally matched to 50 ohm and a DC blocking capacitor is integrated on-chip, thus no external component is required at the output.
- The AW15208MFDR should be placed close to the diversity antenna with the inputmatching inductor. Use 50 ohm micro-strip lines to connect RF INPUT and RF OUTPUT. Bypass capacitor need be located close to the device. For long Vcc lines, it may be necessary to add more decoupling capacitors. Proper grounding of the GND pins is very important.

Following tables show recommended inductor and capacitor values.

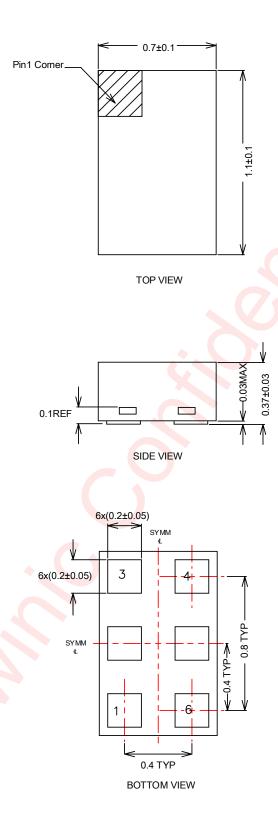
Inductor Selection Table

| Compon | ent | Part | Typical(nH) | | Q(min) | Q(min) Frequency(MHz) | | Size |
|--------|-----|-----------|-------------|--|--------|-----------------------|---------|------|
| L1 | | SDCL1005C | 3.3 | | 25 | 250 | Sunlord | 0402 |

Capacitor Selection Table

| Component | Part | Typical(pF) | Voltage(V) | MFR | Size |
|-----------|--------|-------------|------------|--------|------|
| C1 | GRM155 | 1000 | 50 | Murata | 0402 |

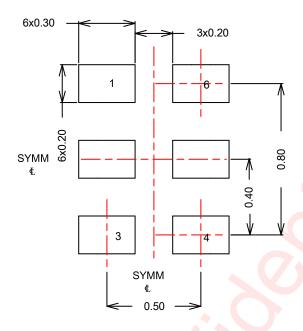
PACKAGE DESCRIPTION

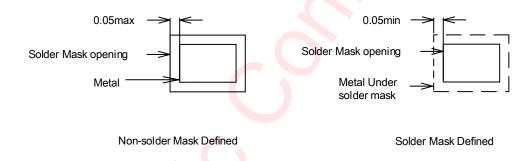


Unit : mm

Figure 8 Package Outline

LAND PATTERN



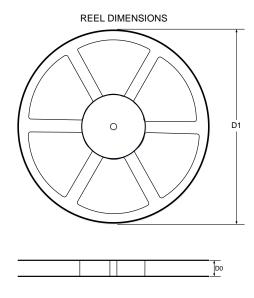


Unit: mm

Figure 9 Land Pattern



TAPE & REEL DESCRIPTION

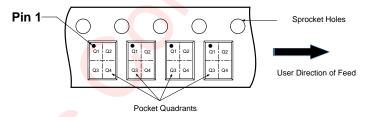


TAPE DIMENSIONS K0+

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness W: Overall width of the carrier tape
- P0: Pitch between successive cavity centers and sprocket hole
- P1: Pitch between successive cavity centers
- P2: Pitch between sprocket hole
- D1: Reel Diameter
- D0: Reel Width

Cavity

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

| D1 (mm) | D0 (mm) | A0 (mm) | B0 (mm) | | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|------------|------------|------------|------------|------|------------|------------|------------|-----------|---------------|
| 178 | 8.4 | 0.8 | 1.2 | 0.55 | 2 | 2 | 4 | 8 | Q1 |

All dimensions are nominal

Figure 10 **Tape & Reel Description**



| Version | Date | Change Record |
|---------|-----------|--|
| V1.0 | Mar. 2019 | Officially Released |
| V1.1 | Oct. 2019 | Update electrical characteristics |
| V1.2 | Oct. 2020 | Update electrical characteristics |
| V1.3 | Feb. 2021 | Update stability factor Add noise figure under bypass mode |
| V1.4 | Jul. 2021 | Add IEN,ISD,IIP3 in bypass mode |
| V1.5 | Aug. 2021 | Add logic for gain mode, change test condition of ISD |

DISCLAIMER

Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.