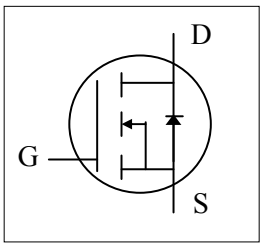
AP6NA3R2MT

Halogen-Free Product

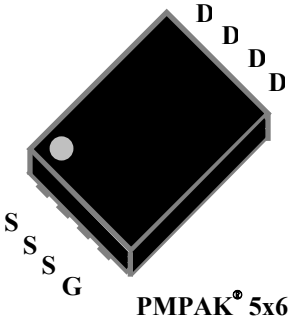
Advanced Power Electronics Corp.

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **100% R_g & UIS Test**
- ▼ **Simple Drive Requirement**
- ▼ **Lower On-resistance**
- ▼ **RoHS Compliant & Halogen-Free**



BV_{DSS}	60V
$R_{DS(ON)}$	3.28mΩ



PMPAK® 5x6

Description

AP6NA3R2 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK ® 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[4](Silicon Limited)	112	A
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[4]	100	A
I_D@T_A=25℃	Drain Current, V_{GS} @ 10V[3]	30	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 10V[3]	24	A
I_{DM}	Pulsed Drain Current[1]	350	A
P_D@T_C=25℃	Total Power Dissipation	69.4	W
P_D@T_A=25℃	Total Power Dissipation[3]	5	W
E_{AS}	Single Pulse Avalanche Energy[5]	125	mJ
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	1.8	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	25	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	60	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=20A	-	-	3.28	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2	-	4	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=20A	-	60	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=48V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}= ±20V, V_{DS}=0V	-	-	±0.1	uA
Q_g	Total Gate Charge	I_D=20A	-	62	99.2	nC
Q_{gs}	Gate-Source Charge	V_{DS}=30V	-	18	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=10V	-	17	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=30V	-	18	-	ns
t_r	Rise Time	I_D=20A	-	52	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=6Ω	-	42	-	ns
t_f	Fall Time	V_{GS}=10V	-	63	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	3400	5440	pF
C_{oss}	Output Capacitance	V_{DS}=50V	-	560	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	30	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1	2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=20A, V_{GS}=0V	-	-	1.3	V
t_{rr}	Reverse Recovery Time	I_S=20A, V_{GS}=0V,	-	42	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	37	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec; 60°C/W at steady state.

4.Package limitation current is 100A .

5.Starting T_j=25°C , V_{DD}=30V , L=0.1mH , R_G=25Ω, V_{GS}=10V

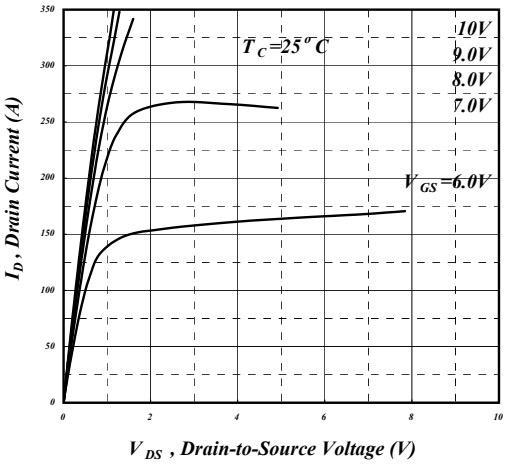


Fig 1. Typical Output Characteristics

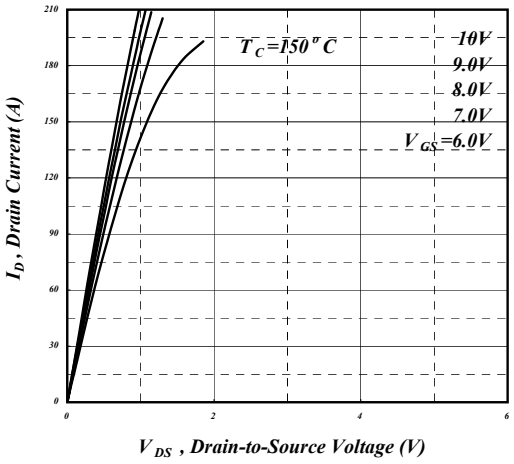


Fig 2. Typical Output Characteristics

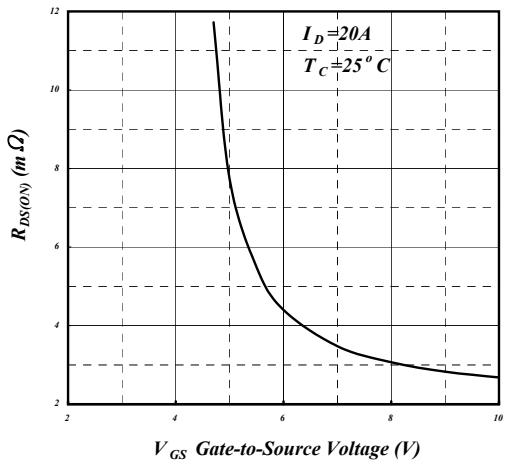


Fig 3. On-Resistance v.s. Gate Voltage

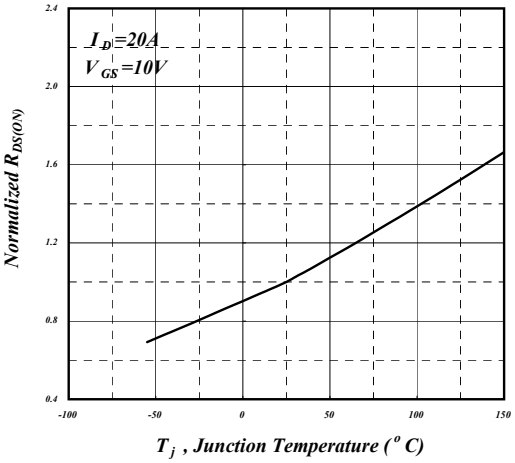


Fig 4. Normalized On-Resistance v.s. Junction Temperature

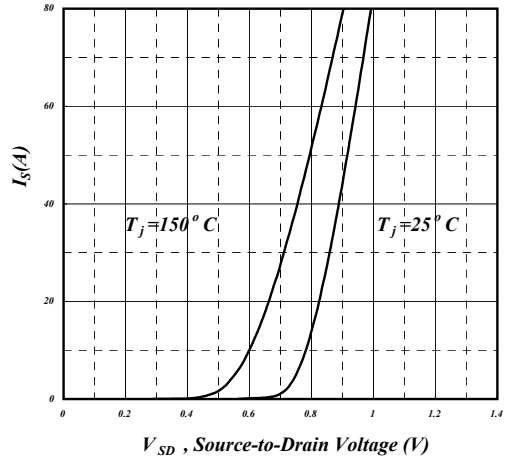


Fig 5. Forward Characteristic of Reverse Diode

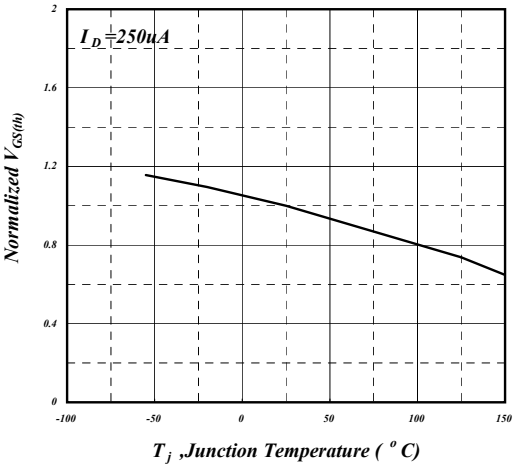


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

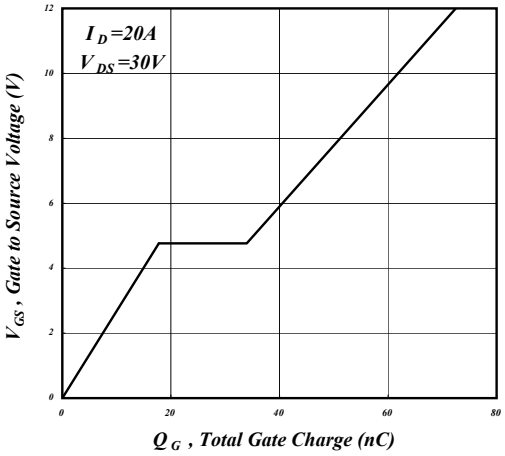


Fig 7. Gate Charge Characteristics

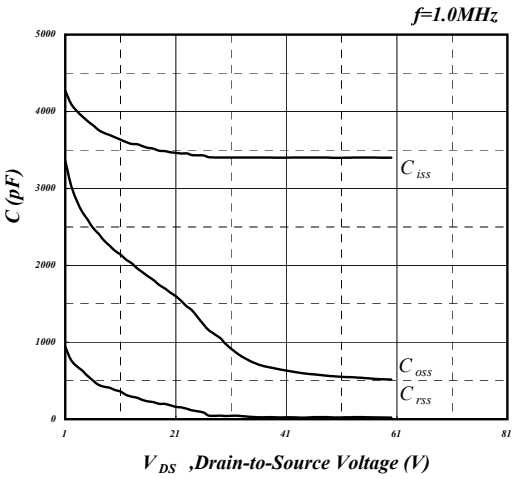


Fig 8. Typical Capacitance Characteristics

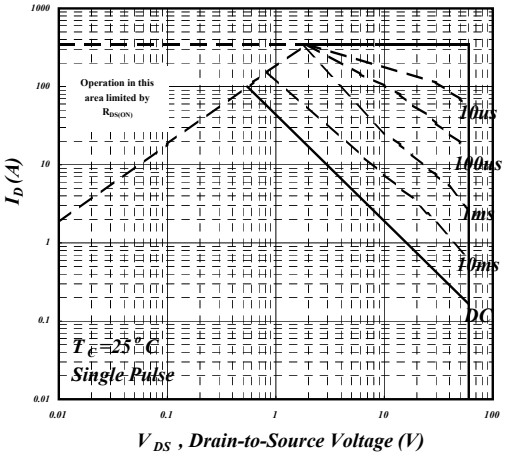


Fig 9. Maximum Safe Operating Area

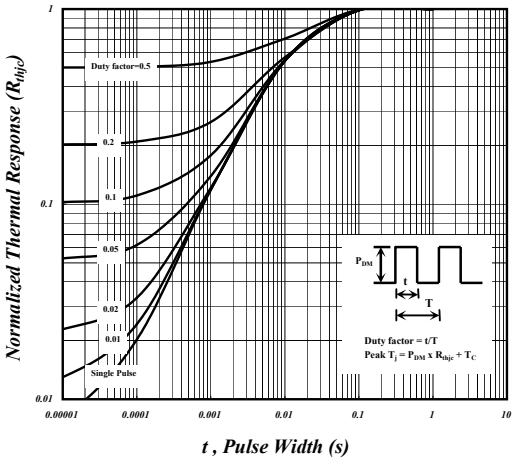


Fig 10. Effective Transient Thermal Impedance

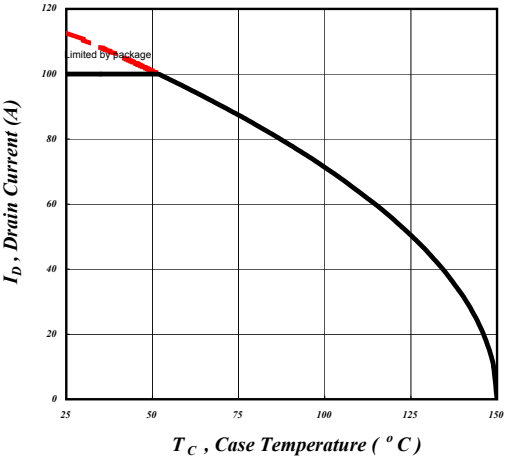


Fig 11. Drain Current v.s. Case Temperature

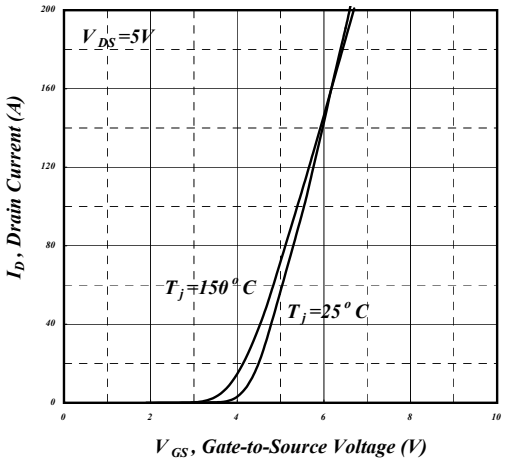


Fig 12. Transfer Characteristics

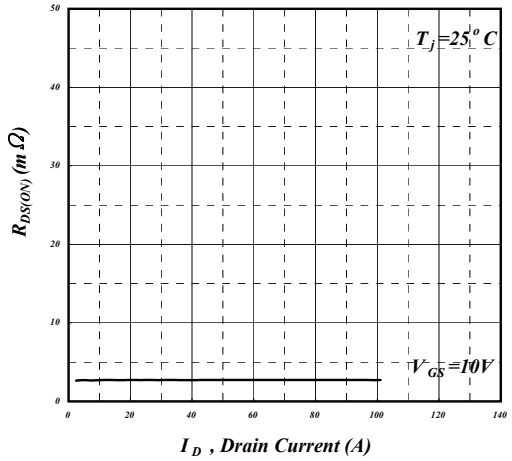


Fig 13. Typ. Drain-Source on State Resistance

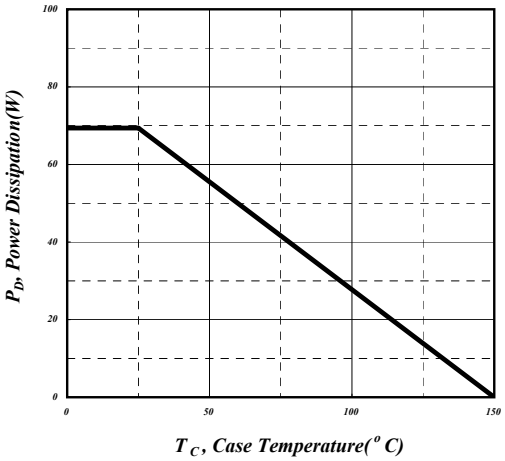


Fig 14. Total Power Dissipation

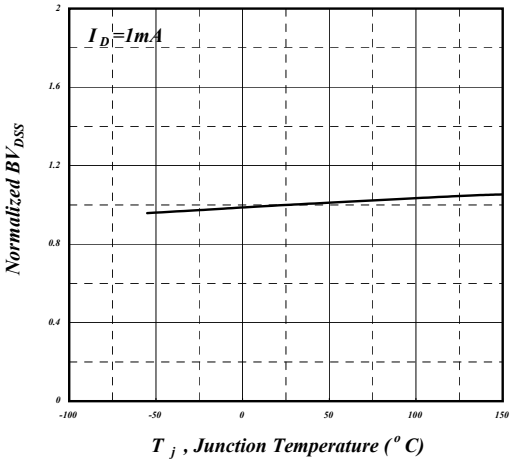
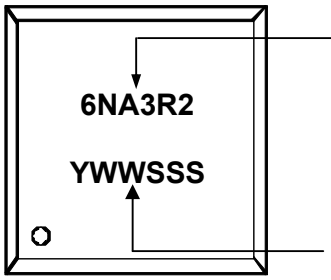


Fig 15. Normalized BV_{DSS} v.s. Junction Temperature

MARKING INFORMATION



Part Number

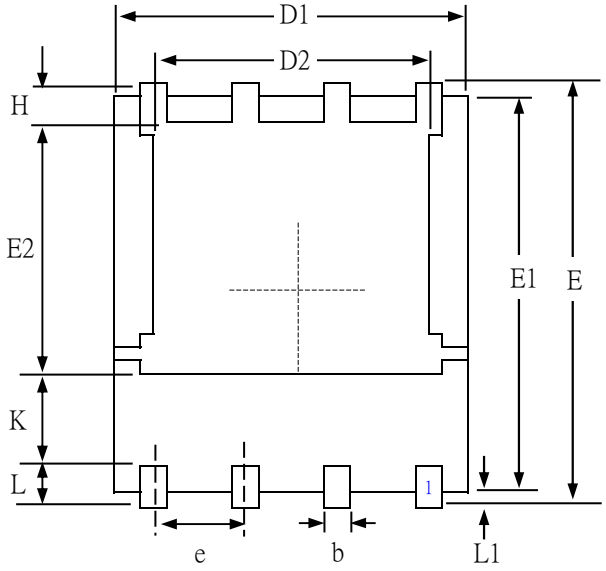
Date Code (YWWSSS)

Y：Last Digit Of The Year

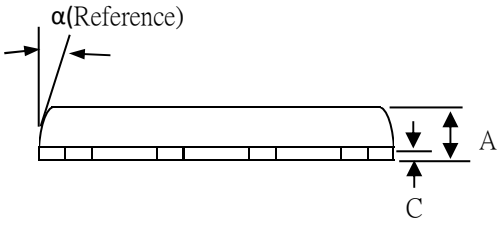
WW：Week

SSS：Sequence

Package Outline : PMPAK 5x6



BACKSIDE VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.10	1.30
b	0.33	0.41	0.51
C		0.254(Ref.)	
D1	4.80	4.90	5.10
D2	3.61	4.00	4.40
E	5.80	6.03	6.25
E1 (Ref.)	5.60	5.75	5.90
E2 (Ref.)	3.30	3.55	3.80
e		1.27 BSC	
H	0.35	—	0.90
K (Ref.)	1.00	1.275	—
L	0.35	0.55	0.75
L1	0.06	0.13	0.20
α(Ref.)	0°	—	12°

1.All dimension are in millimeters.

2.Dimension does not include burrs and mold flash/protrusions.

3.The outline schematic is not to scale and slightly different from the actual product appearance.

PMPAK 5X6(E-TYPE) FOOTPRINT：