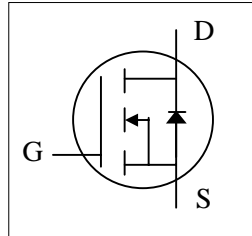
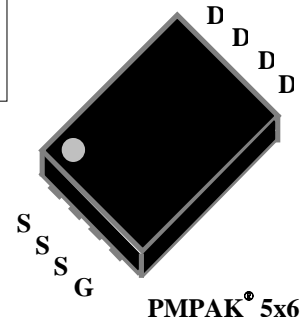




- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ RoHS Compliant & Halogen-Free



BV _{DSS}	30V
R _{DS(ON)}	5mΩ



Description

AP3N5R0 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK[®] 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.

Absolute Maximum Ratings @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V	61	A
I _D @T _A =25°C	Drain Current, V _{GS} @ 10V ³	24.7	A
I _D @T _A =70°C	Drain Current, V _{GS} @ 10V ³	19.7	A
I _{DM}	Pulsed Drain Current ¹	200	A
P _D @T _C =25°C	Total Power Dissipation	31.2	W
P _D @T _A =25°C	Total Power Dissipation ³	5	W
E _{AS}	Single Pulse Avalanche Energy ⁴	61.2	mJ
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Unit
R _{thj-c}	Maximum Thermal Resistance, Junction-case	4	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	25	°C/W



AP3N5R0MT

Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =1mA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =19A	-	-	5	mΩ
		V _{GS} =4.5V, I _D =16A	-	-	8	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1.3	-	2.3	V
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =19A	-	69	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =16A	-	22	35.2	nC
Q _{gs}	Gate-Source Charge	V _{DS} =15V	-	7	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	10.5	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V	-	11	-	ns
t _r	Rise Time	I _D =19A	-	59	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	29	-	ns
t _f	Fall Time	V _{GS} =10V	-	13	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1900	3040	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	305	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	245	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.5	3	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =19A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time	I _S =20A, V _{GS} =0V,	-	15	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	-	6	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec ; 60°C/W at steady state.
- 4.Starting T_j=25°C , V_{DD}=30V , L=0.1mH , R_G=25Ω , V_{GS}=10V

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

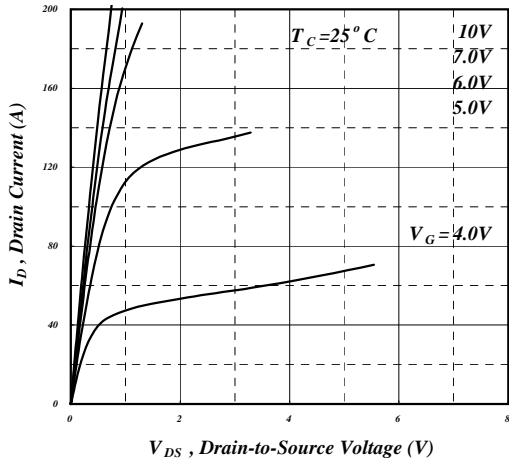


Fig 1. Typical Output Characteristics

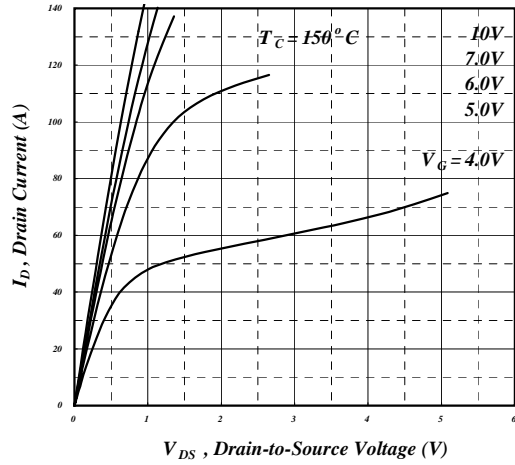


Fig 2. Typical Output Characteristics

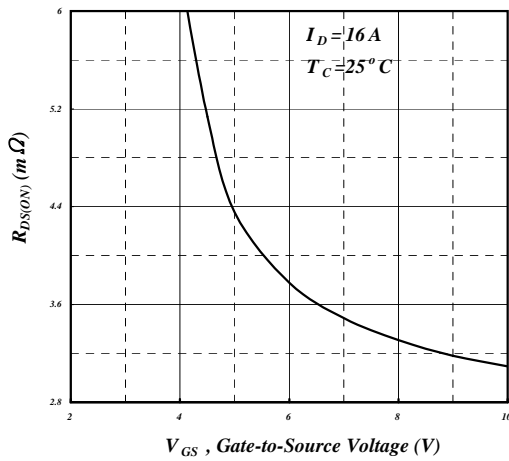


Fig 3. On-Resistance v.s. Gate Voltage

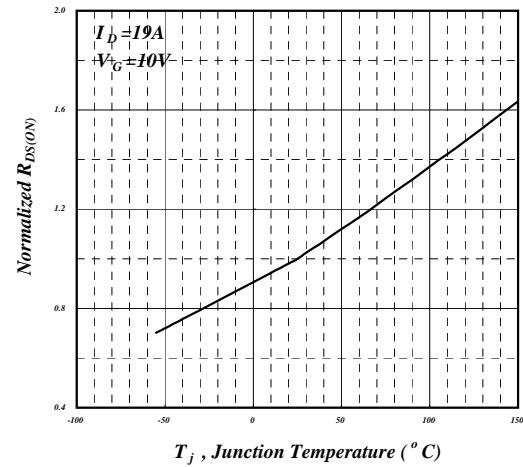


Fig 4. Normalized On-Resistance v.s. Junction Temperature

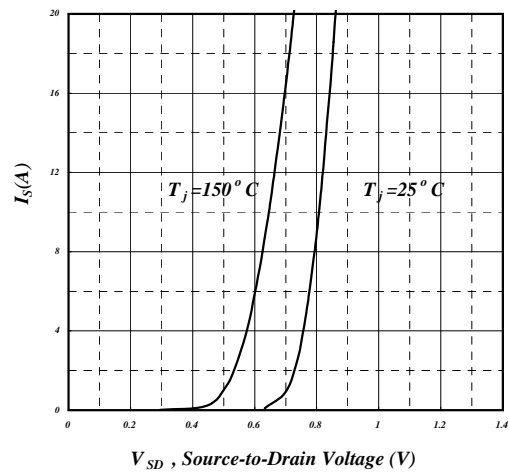


Fig 5. Forward Characteristic of Reverse Diode

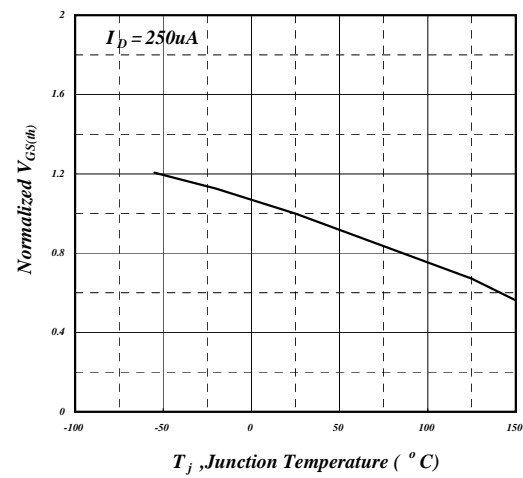


Fig 6. Transfer Characteristics

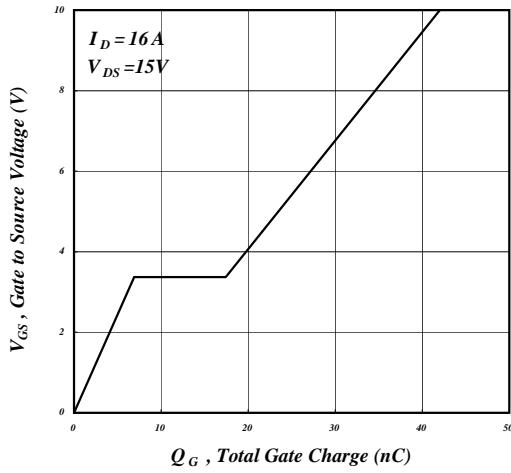


Fig 7. Gate Charge Characteristics

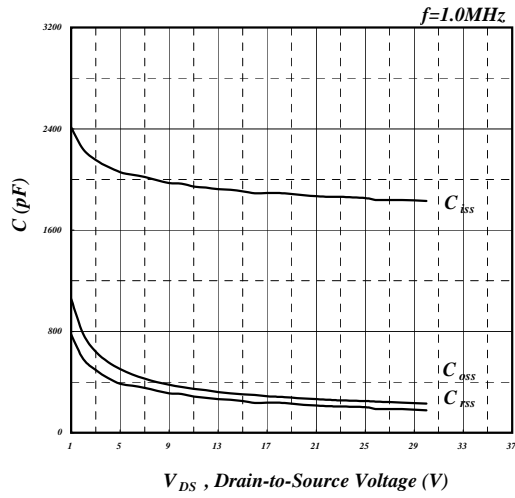


Fig 8. Typical Capacitance Characteristics

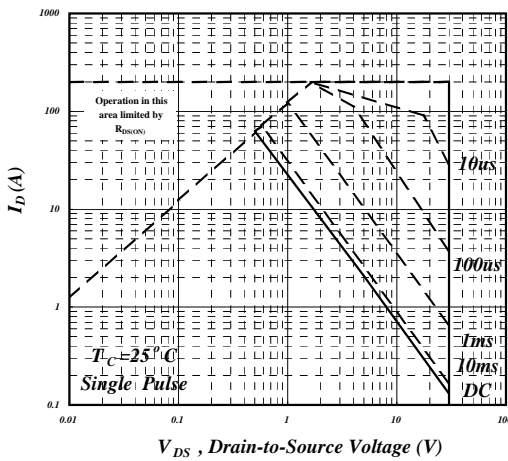


Fig 9. Maximum Safe Operating Area

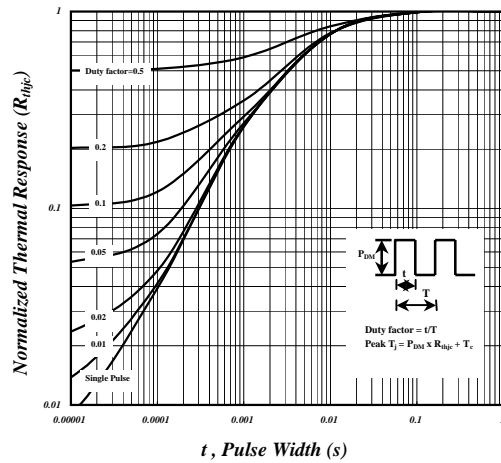


Fig 10. Effective Transient Thermal Impedance

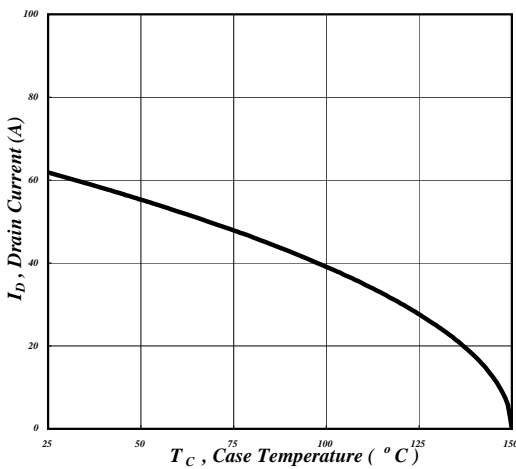


Fig 11. Drain Current v.s. Case Temperature

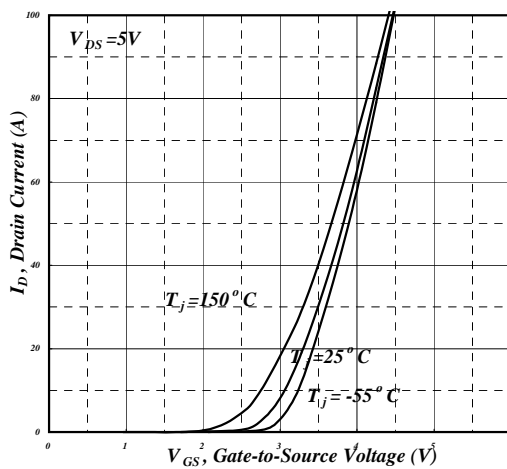


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

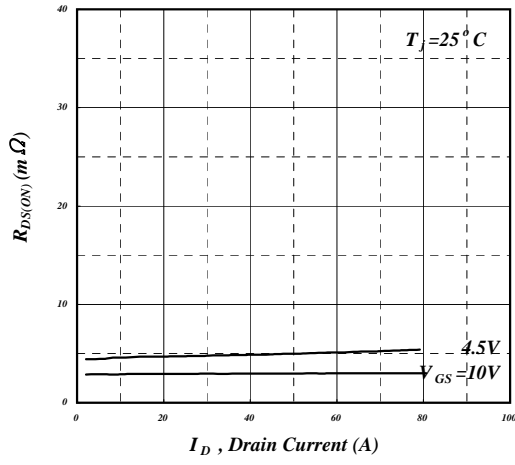


Fig 13. Typ. Drain-Source on State Resistance

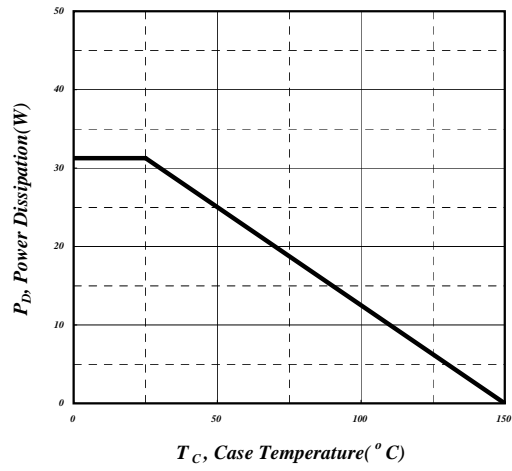
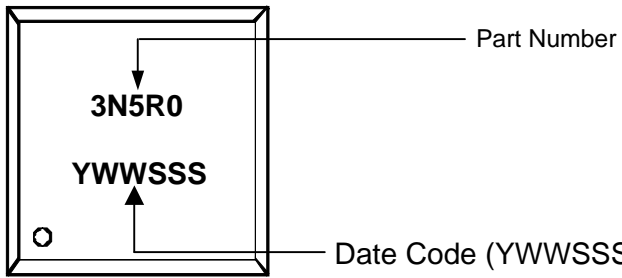


Fig 14. Total Power Dissipation



MARKING INFORMATION



Date Code (YWWSSS)

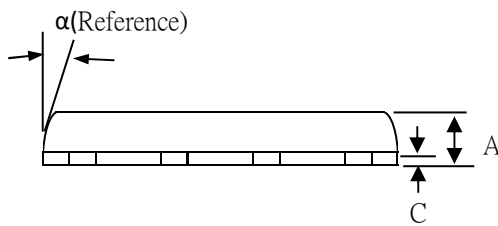
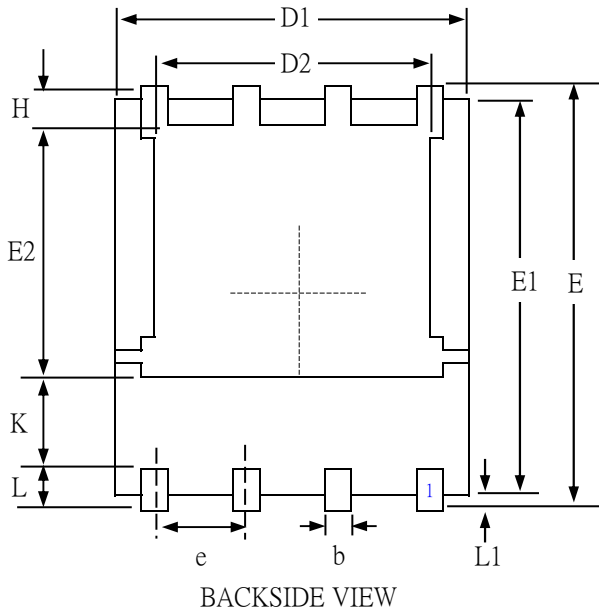
Y : Last Digit Of The Year

WW : Week

SSS : Sequence



Package Outline : PMPAK 5x6

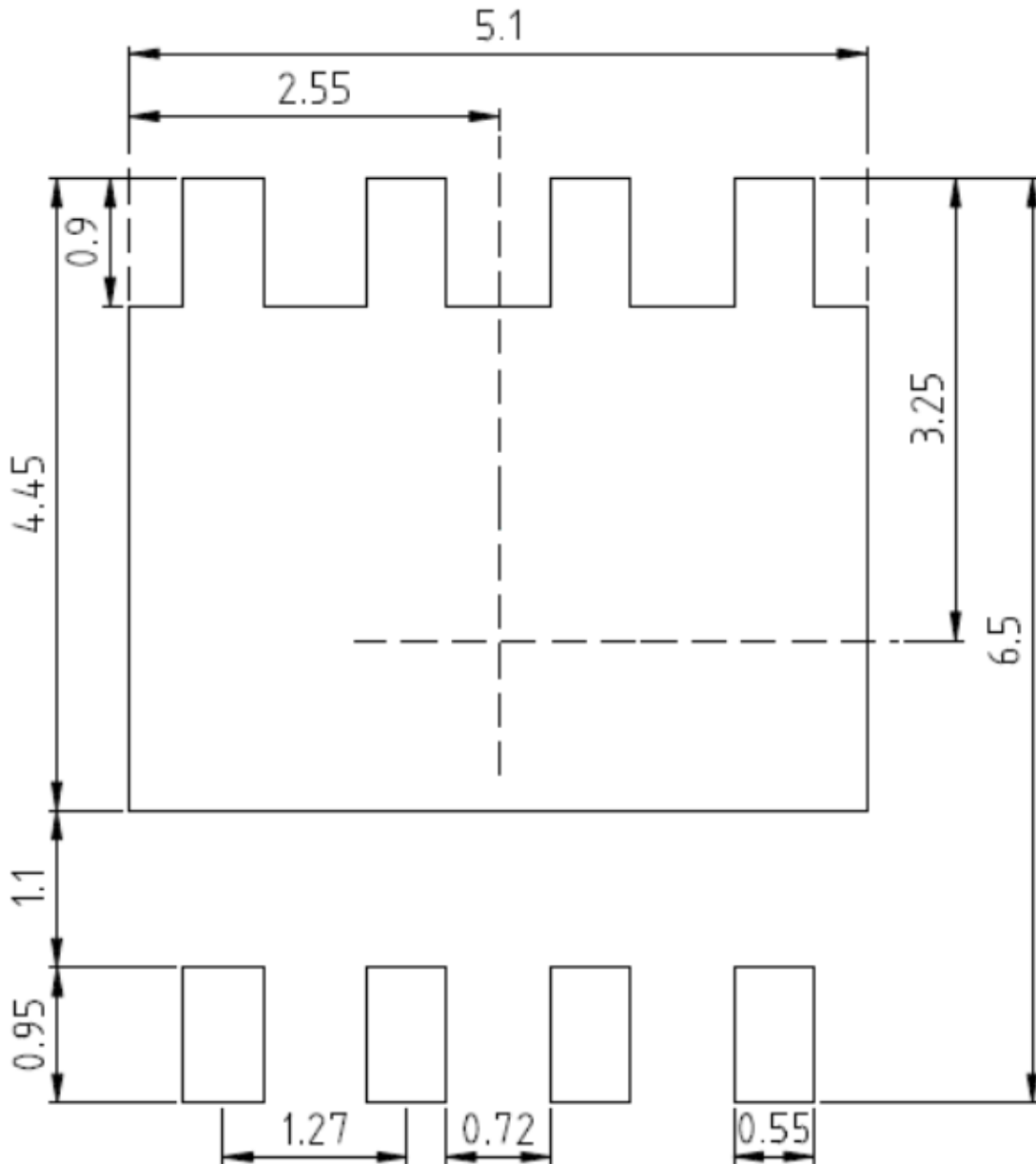


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.10	1.30
b	0.33	0.41	0.51
C	0.254(Ref.)		
D1	4.80	4.90	5.10
D2	3.61	4.00	4.40
E	5.80	6.03	6.25
E1 (Ref.)	5.60	5.75	5.90
E2 (Ref.)	3.30	3.55	3.80
e	1.27 BSC		
H	0.35	—	0.90
K (Ref.)	1.00	1.275	—
L	0.35	0.55	0.75
L1	0.06	0.13	0.20
α (Ref.)	0°	—	12°

1. All dimension are in millimeters.
2. Dimension does not include burrs and mold flash/protrusions.
3. The outline schematic is not to scale and slightly different from the actual product appearance.



PMPAK 5X6(E-TYPE) FOOTPRINT :



UNIT: mm