Section 1A Overview of RH850/F1KH-D8

1A.1 RH850/F1KH Outline

This RH850/F1KH-D8 is a 32-bit single-chip microcontroller with dual core CPUs, Code Flash, Data Flash, RAM modules, DMA controllers, A/D converters, timer units and many communication interfaces that are used in the automotive applications. This microcontroller has been developed as a Safety Element out of Context (SEooC) in accordance with ISO26262.

RH850/F1KH-D8 main features are as follows:

(1) RH850 dual core CPU

This microcontroller contains dual RH850G3KH2.0 cores support RISC-type instruction sets and have significantly improved the instruction execution speed with basic instructions (one clock cycle per instruction) and the optimized 5-stage pipeline configurations. Furthermore, this product also supports bit manipulation instructions as instructions best suited for various fields.

Two-byte basic instructions and high-level language instructions improve object code efficiency for the C compiler and reduce the program size. Furthermore, this product is suited for advanced real-time control applications by offering a high-speed response time including the processing time of the on-chip interrupt controller.

(2) On-Chip Code Flash and Data Flash

This microcontroller has high-speed Code Flash from which CPU can fetch the instructions and the constant data. Code Flash with a capacity of up to 8 MB can be reprogrammed when the chip is implemented in the application system.

This chip also has Data Flash with a capacity of 256 KB.

(3) Rich peripheral functionality

This microcontroller supports common communication interfaces such as CSI as well as automotive-oriented communication interfaces such as Ethernet, FlexRay, CAN-FD, LIN and SENT. As internal peripheral modules, this microcontroller incorporates A/D Converter and Timer module.

(4) Low power consumption

This microcontroller provides some function for low power consumption. Low Power Sampler (LPS) polls signal inputs without CPU core interaction. DeepSTOP mode disables power to select circuits within the chip.

(5) Functional Safety support

This microcontroller includes several dedicated functionalities such as the memory protection with ECC on data and clock monitors to support the functional safety standard (ISO26262) required in the automotive applications.

(6) Security support

This microcontroller supports various security features. The Intelligent Cryptographic Unit -Master (ICUMD) has a dedicated secure CPU (RH850 G3K) and some secure peripherals such as AES engines Random Number Generator (RNG). This microcontroller also realizes the HW-level domain separation between non-secure and secure domains. The internal resources such as Code and Data Flash can be assigned to either a non-secure or secure domain, and the secure domain is protected against non-secure accesses by the HW mechanism. This microcontroller also has the protection scheme for debug and test functionality.

1A.2 RH850/F1KH Functions

Table 1A.1 Overview of Product

Product Name			RH850/F1KH-D8		
			176 Pins	233 Pins	324 Pins
Memory			See **Table 1A.2, Product Lineup**.		
External Memory Access Controller (MEMC)			23 bit Address Bus		24 bit Address Bus
Serial Flash Memory I/F (SFMA)		Bus width	4 bit		
		Mode	SDR		
		Max. clock	40 MHz		
Memory Card I/F (MMCA)		Bus width	Not provided		8 bit
		Mode			Backward-compatible
		Max. clock			20 MHz
CPU	CPU System		G3KH (Dual Core)		
	CPU frequency		240 MHz max.		
	FPU		Single-precision		
	Protection Function	Memory Protection Unit (MPU)	Provided		
		Internal Peripheral-device Guard (IPG)	Provided		
		Processor Element Guard (PEG)	Provided		
DMA			64 channels		
Operating clock	Main Oscillator (MainOSC)		8/16/20/24 MHz		
	Low Speed Internal Oscillator (LS IntOSC)		240 kHz (typ.)		
	High Speed Internal Oscillator (HS IntOSC)		8 MHz (typ.)		
	PLL	PLL0 (for CPU, with SSCG)	Provided		
		PLL1 (for CPU/Peripheral)	Provided		
	Sub Oscillator (SubOSC)		32.768 kHz		
I/O port			144	174	246
A/D converter	ADCA0	Physical input channels	Total 34 ch (12 bit resolution: 16 ch + 10 bit resolution: 18 ch)		
		External multiplexer support for channel number extension	Provided		
		Channels with T&H	Provided		
	ADCA1	Physical input channels	Total 24 ch (12 bit resolution: 16 ch + 10 bit resolution: 8 ch)	Total 36 ch (12 bit resolution: 16 ch + 10 bit resolution: 20 ch)	
		External multiplexer support for channel number extension	Not provided		
		Channels with T&H	Not provided		

Table 1A.1 Overview of Product

Product Name		RH850/F1KH-D8		
		176 Pins	233 Pins	324 Pins
Timer	Timer Array Unit D (TAUD)	1 unit (16 bit resolution timers × 16 channels /unit)		
	Timer Array Unit B (TAUB)	2 units (16 bit resolution timers × 16 channels /unit)		
	Timer Array Unit J (TAUJ)	4 units (32 bit resolution timers × 4 channels /unit)		
	Operating System Timer (OSTM)	10 units		
	Real-Time Clock (RTCA)	1 unit		
	Encoder Timer (ENCA)	1 unit		
	Window Watchdog Timer A (WDTA)	3 units		
Serial interfaces	Clocked Serial Interface G (CSIG)	5 channels		
	Clocked Serial Interface H (CSIH)	5 channels		
	CAN Interface (RS-CANFD)	8 channels		12 channels
	LIN/UART Interface (RLIN3)	8 channels		
	LIN Master Interface (RLIN2)	10 channels	12 channels	16 channels
	I^2C Interface (RIIC)	2 channels		
	Clock Extension Peripheral Interface (CXP1)	Not provided		
	Single Edge Nibble Transmission (RSENT)	2 channels		
	FlexRay Interface (FLXA)	2 channel (A ch, B ch)		
	Ethernet AVB (ETNB)	1 channel (MII)		2 channels (MII)
External Interrupts	Maskable	24		
	Non-maskable (NMI)	1		
Other functions	Clock Monitors (CLMA)	For PLL0, PLL1, HS IntOSC, MainOSC		
	Data CRC (DCRA)	4 channels		
	Low-Voltage Indicator (LVI)	Provided		
	Power-On Clear (POC)	Provided		
	Core Voltage Monitors (CVM)	Provided		
	Error Correction Coding (ECC)	For Code flash, Data flash, Local RAM, Retention RAM, Global RAM, CSIH, RS-CANFD, FLXA, ETNB		For Code flash, Data flash, Local RAM, Retention RAM, Global RAM, CSIH, RS-CANFD, FLXA, ETNB, MMCA
	Low Power Sampler (LPS)	Provided		
	PWM Output/Diagnostic (PWM-Diag)	72 channels	80 channels	96 channels
	Motor Control	1 unit		
	Key Return (KR)	8 channels		
	CLOCK OUTPUT (FOUT)	Provided		
	RESET OUTPUT ($\overline{\text{RESETOUT}}$)	Provided		
	Intelligent Cryptographic Unit Master D (ICUMD)	Provided		
	On-Chip debug (OCD)	Provided		
	Boundary Scan	Provided		

Table 1A.1 Overview of Product

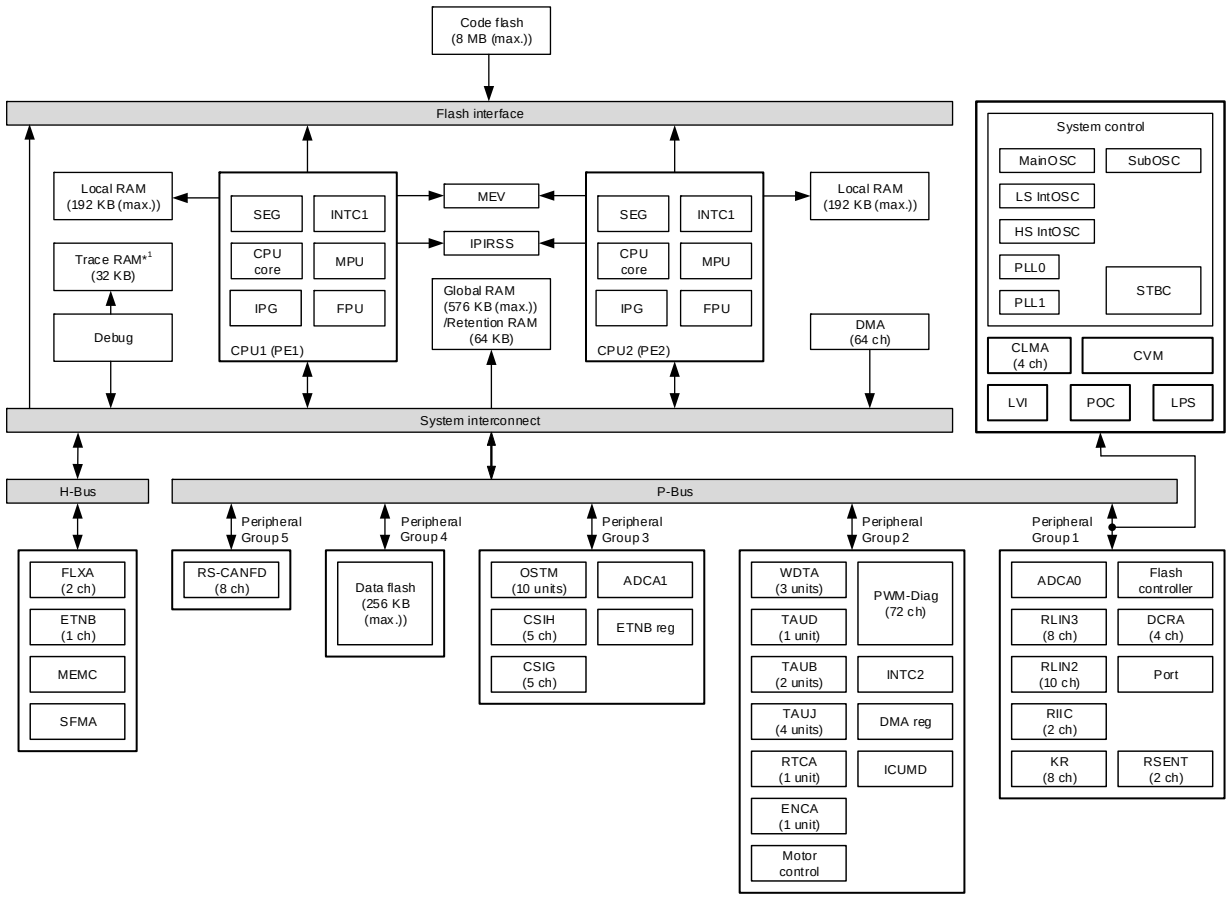
Product Name			RH850/F1KH-D8		
			176 Pins	233 Pins	324 Pins
Voltage supply	Internal supply	REG0VCC (for AWO)	VPOC to 5.5 V		
		REG1VCC (for ISO)	VPOC to 3.6 V		
	Input/output buffer supplies		VPOC to 5.5 V		
	A/D Converter supplies		3.0 to 5.5 V		
Package			176-pin LQFP	233-pin FPBGA	324-pin FPBGA

1A.3 RH850/F1KH Product Lineup

Table 1A.2 Product Lineup

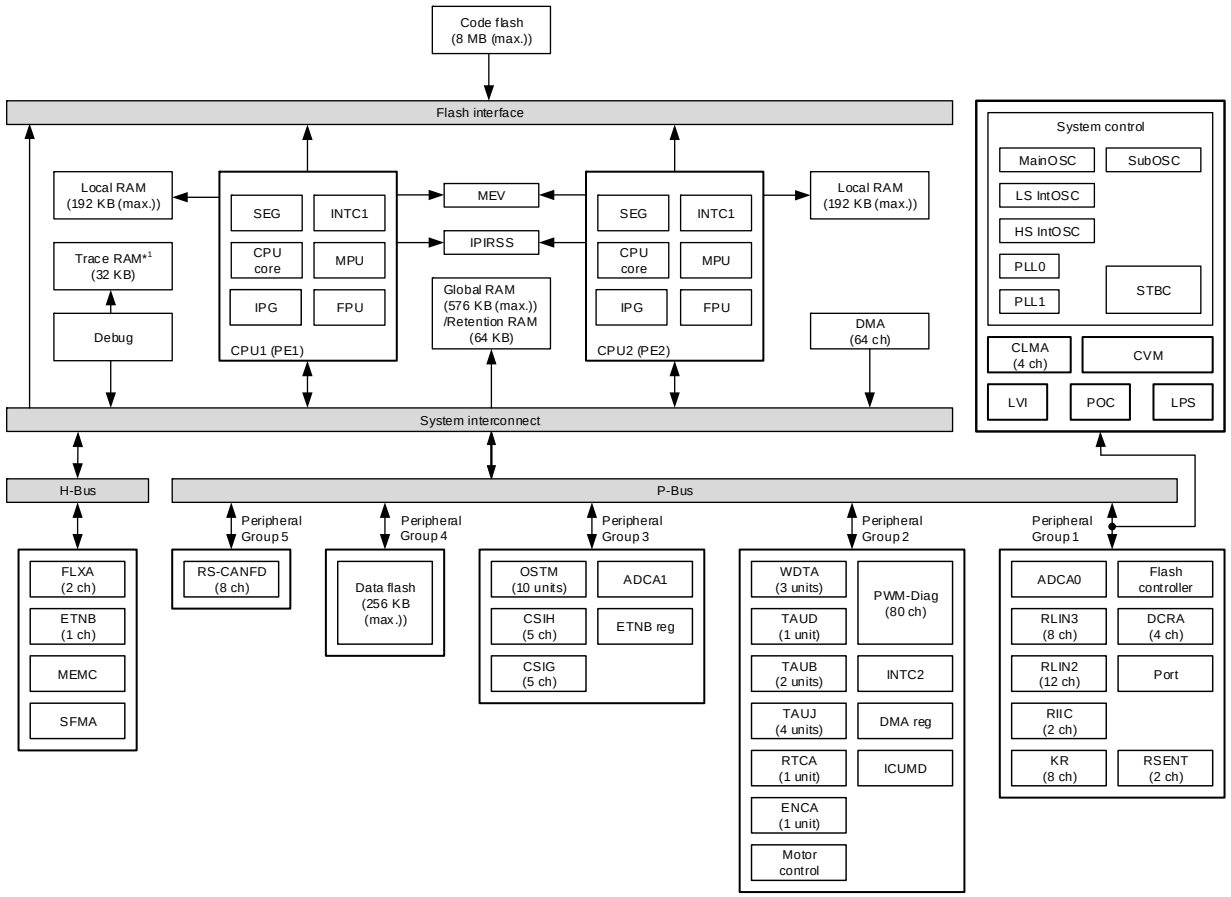
F1KH-D8		Memory							Part Name	
				Local RAM (LRAM)		Global RAM (GRAM)	Retention RAM (RRAM)	Trace RAM	Operating Temperature (Ta)	
Pin Count	CPU Frequency	Code Flash	Data Flash	CPU1	CPU2				–40°C to +105°C Package	–40°C to +125°C Package
176 pins	240 MHz max.	6 MB	256 KB	160 KB	160 KB	512 KB	64 KB	Not available	R7F7017083AFP-C LQFP	–
		8 MB		192 KB	192 KB	576 KB		32 KB	R7F7017093AFP-C LQFP	–
233 pins	240 MHz max.	6 MB	256 KB	160 KB	160 KB	512 KB	64 KB	Not available	R7F7017103ABG-C FPBGA	R7F7017104ABG-C FPBGA
		8 MB		192 KB	192 KB	576 KB		32 KB	R7F7017113ABG-C FPBGA	R7F7017114ABG-C FPBGA
324 pins	240 MHz max.	6 MB	256 KB	160 KB	160 KB	512 KB	64 KB	Not available	R7F7017143ABG-C FPBGA	R7F7017144ABG-C FPBGA
		8 MB		192 KB	192 KB	576 KB		32 KB	R7F7017153ABG-C FPBGA	R7F7017154ABG-C FPBGA

1A.4 RH850/F1KH Product Block Diagrams



Note 1. The trace RAM is only supported by products with 8 MB code flash memory.

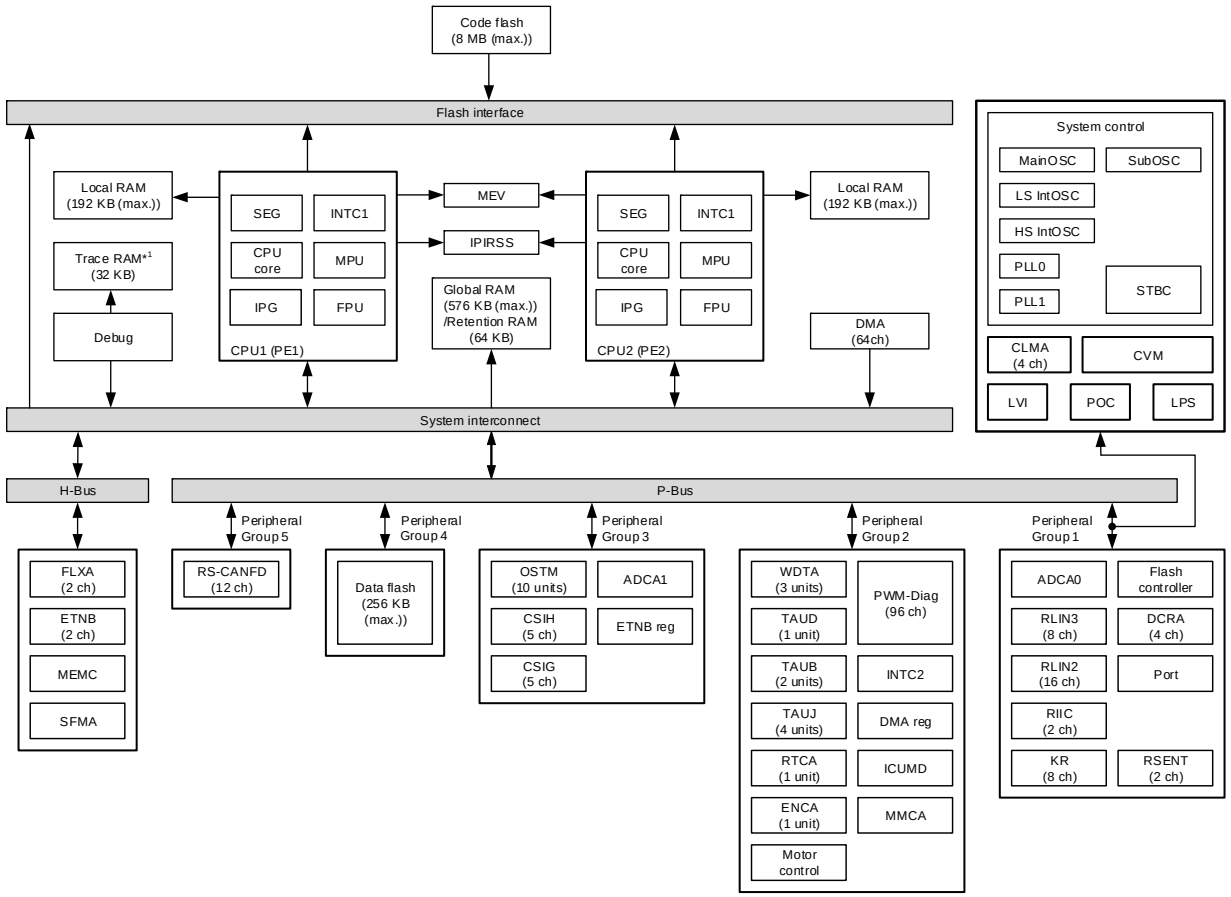
Figure 1A.1 Internal Block Diagram (RH850/F1KH-D8 176-Pin Version)



Note 1. The trace RAM is only supported by products with 8 MB code flash memory.

Figure 1A.2 Internal Block Diagram (RH850/F1KH-D8 233-Pin Version)

Figure 1A.3 Reserved



Note 1. The trace RAM is only supported by products with 8 MB code flash memory.

Figure 1A.4 Internal Block Diagram (RH850/F1KH-D8 324-Pin Version)

Section 1B Overview of RH850/F1KM-S4, RH850/F1KM-S2

1B.1 RH850/F1KM-S4, RH850/F1KM-S2 Outline

This RH850/F1KM-S4, F1KM-S2 is a 32-bit single-chip microcontroller with single CPU, Code Flash, Data Flash, RAM modules, DMA controllers, A/D converters, timer units and many communication interfaces that are used in the automotive applications. This microcontroller has been developed as a Safety Element out of Context (SEooC) in accordance with ISO26262.

RH850/F1KM-S4, F1KM-S2 main features are as follows:

(1) RH850 single core CPU

This microcontroller contains single RH850G3KH2.0 core support RISC-type instruction sets and have significantly improved the instruction execution speed with basic instructions (one clock cycle per instruction) and the optimized 5-stage pipeline configurations. Furthermore, this product also supports bit manipulation instructions as instructions best suited for various fields.

Two-byte basic instructions and high-level language instructions improve object code efficiency for the C compiler and reduce the program size. Furthermore, this product is suited for advanced real-time control applications by offering a high-speed response time including the processing time of the on-chip interrupt controller.

(2) On-Chip Code Flash and Data Flash

This microcontroller has high-speed Code Flash from which CPU can fetch the instructions and the constant data. Code Flash with a capacity of up to 4 MB can be reprogrammed when the chip is implemented in the application system.

This chip also has Data Flash with a capacity of 128 KB.

(3) Rich peripheral functionality

This microcontroller supports common communication interfaces such as CSI as well as automotive-oriented communication interfaces such as Ethernet (some pkg products of S4) FlexRay (only S4), CAN-FD, LIN and SENT. As internal peripheral modules, this microcontroller incorporates A/D Converter and Timer module.

(4) Low power consumption

This microcontroller provides some function for low power consumption. Low Power Sampler (LPS) polls signal inputs without CPU core interaction. DeepSTOP mode disables power to select circuits within the chip.

(5) Functional Safety support

This microcontroller includes several dedicated functionalities such as the memory protection with ECC on data and clock monitors to support the functional safety standard (ISO26262) required in the automotive applications.

(6) Security support

This microcontroller supports various security features. The Intelligent Cryptographic Unit -Master (ICUMD) has a dedicated secure CPU (RH850 G3K) and some secure peripherals such as AES engines Random Number Generator (RNG). This microcontroller also realizes the HW-level domain separation between non-secure and secure domains. The internal resources such as Code and Data Flash can be assigned to either a non-secure or secure domain, and the secure domain is protected against non-secure accesses by the HW mechanism. This microcontroller also has the protection scheme for debug and test functionality.

1B.2 RH850/F1KM Functions

Table 1B.1 Overview of Product

Product Name			RH850/F1KM-S4				
			100 Pins	144 Pins	176 Pins	233 Pins	272 Pins
Memory			See **Table 1B.3, Product Lineup**.				
External Memory Access Controller (MEMC)			Not provided		23 bit Address Bus		24 bit Address Bus
Serial Flash Memory I/F (SFMA)		Bus width	Not provided	4 bit			
		Mode		SDR			
		Max. clock		40 MHz			
CPU	CPU System		G3KH				
	CPU frequency		240 MHz max.				
	FPU		Single-precision				
	Protection Function	Memory Protection Unit (MPU)	Provided				
		Internal Peripheral-device Guard (IPG)	Provided				
		Processor Element Guard (PEG)	Provided				
DMA			32 channels				
Operating clock	Main Oscillator (MainOSC)		8/16/20/24 MHz				
	Low Speed Internal Oscillator (LS IntOSC)		240 kHz (typ.)				
	High Speed Internal Oscillator (HS IntOSC)		8 MHz (typ.)				
	PLL	PLL0 (for CPU, with SSCG)	Provided				
		PLL1 (for CPU/Peripheral)	Provided				
	Sub Oscillator (SubOSC)		Not provided	32.768 kHz			
I/O port			75	114	144	174	214
A/D converter	ADCA0	Physical input channels	Total 32 ch (12 bit resolution: 16 ch + 10 bit resolution: 16 ch)	Total 34 ch (12 bit resolution: 16 ch + 10 bit resolution: 18 ch)			
		External multiplexer support for channel number extension	Provided				
		Channels with T&H	Provided				

Table 1B.1 Overview of Product

Product Name			RH850/F1KM-S4				
			100 Pins	144 Pins	176 Pins	233 Pins	272 Pins
A/D converter	ADCA1	Physical input channels	Not provided	Total 12 ch (12 bit resolution: 8 ch + 10 bit resolution: 4 ch)	Total 24 ch (12 bit resolution: 16 ch + 10 bit resolution: 8 ch)	Total 36 ch (12 bit resolution: 16 ch + 10 bit resolution: 20 ch)	
		External multiplexer support for channel number extension	Not provided				
		Channels with T&H	Not provided				
Timer	Timer Array Unit D (TAUD)		1 unit (16 bit resolution timers × 16 channels /unit)				
	Timer Array Unit B (TAUB)		1 unit (16 bit resolution timers × 16 channels /unit)		2 units (16 bit resolution timers × 16 channels /unit)		
	Timer Array Unit J (TAUJ)		4 units (32 bit resolution timers × 4 channels /unit)				
	Operating System Timer (OSTM)		5 units				
	Real-Time Clock (RTCA)		1 unit				
	Encoder Timer (ENCA)		1 unit				
	Window Watchdog Timer A (WDTA)		2 units				
Serial interfaces	Clocked Serial Interface G (CSIG)		1 channel	2 channels	4 channels		
	Clocked Serial Interface H (CSIH)		4 channels				
	CAN Interface (RS-CANFD)		8 channels				
	LIN/UART Interface (RLIN3)		3 channels	6 channels	8 channels		
	LIN Master Interface (RLIN2)		3 channels	6 channels	10 channels	12 channels	
	I^2C Bus Interface (RIIC)		2 channels				
	Clock Extension Peripheral Interface (CXP1)		Not provided				
	Single Edge Nibble Transmission (RSENT)		1 channel	2 channels			
	FlexRay Interface (FLXA)		2 channel (A ch, B ch)				
	Ethernet AVB (ETNB)		Not provided		1 channel (MII)		
External Interrupts	Maskable		14	24			
	Non-maskable (NMI)		1				
Other functions	Clock Monitors (CLMA)		For PLL0, PLL1, HS IntOSC, MainOSC				
	Data CRC (DCRA)		4 channels				
	Low-Voltage Indicator (LVI)		Provided				
	Power-On Clear (POC)		Provided				
	Core Voltage Monitors (CVM)		Provided				
	Error Correction Coding (ECC)		For Code flash, Data flash, Local RAM, Retention RAM, Global RAM, CSIH, RS-CANFD, FLXA		For Code flash, Data flash, Local RAM, Retention RAM, Global RAM, CSIH, RS-CANFD, FLXA, ETNB		

Table 1B.1 Overview of Product

Product Name		RH850/F1KM-S4				
		100 Pins	144 Pins	176 Pins	233 Pins	272 Pins
Other functions	Low Power Sampler (LPS)	Provided				
	PWM Output/Diagnostic (PWM-Diag)	44 channels	64 channels	72 channels	80 channels	96 channels
	Motor Control	1 unit				
	Key Return (KR)	8 channels				
	CLOCK OUTPUT (FOUT)	Provided				
	RESET OUTPUT ($\overline{\text{RESETOUT}}$)	Provided				
	Intelligent Cryptographic Unit Master D (ICUMD)	Provided				
	On-Chip debug (OCD)	Provided				
	Boundary Scan	Provided				
Voltage supply	Internal supply	VPOC to 5.5 V				
	Input/output buffer supplies	VPOC to 5.5 V				
	A/D Converter supplies	3.0 to 5.5 V				
Package		100-pin LQFP	144-pin LQFP	176-pin LQFP	233-pin FPBGA	272-pin FPBGA

Table 1B.2 Overview of Product

Product Name			RH850/F1KM-S2		
			100 Pins	144 Pins	176 Pins
Memory			See **Table 1B.4, Product Lineup**.		
External Memory Access Controller (MEMC)			Not provided		
Serial Flash Memory I/F (SFMA)		Bus width	Not provided	4 bit	
		Mode		SDR	
		Max. clock		40 MHz	
CPU	CPU System		G3KH		
	CPU frequency		240 MHz max.		
	FPU		Single-precision		
	Protection Function	Memory Protection Unit (MPU)	Provided		
		Internal Peripheral-device Guard (IPG)	Provided		
		Processor Element Guard (PEG)	Provided		
DMA			32 channels		
Operating clock	Main Oscillator (MainOSC)		8/16/20/24 MHz		
	Low Speed Internal Oscillator (LS IntOSC)		240 kHz (typ.)		
	High Speed Internal Oscillator (HS IntOSC)		8 MHz (typ.)		
	PLL	PLL0 (for CPU, with SSCG)	Provided		
		PLL1 (for CPU/Peripheral)	Provided		
	Sub Oscillator (SubOSC)		Not provided	32.768 kHz	
I/O port			75	114	144
A/D converter	ADCA0	Physical input channels	Total 32 ch (12 bit resolution: 16 ch + 10 bit resolution: 16 ch)	Total 34 ch (12 bit resolution: 16 ch + 10 bit resolution: 18 ch)	
		External multiplexer support for channel number extension	Provided		
		Channels with T&H	Provided		

Table 1B.2 Overview of Product

Product Name			RH850/F1KM-S2		
			100 Pins	144 Pins	176 Pins
A/D converter	ADCA1	Physical input channels	Not provided	Total 12 ch (12 bit resolution: 8 ch + 10 bit resolution: 4 ch)	Total 24 ch (12 bit resolution: 16 ch + 10 bit resolution: 8 ch)
		External multiplexer support for channel number extension	Not provided		
		Channels with T&H	Not provided		
Timer	Timer Array Unit D (TAUD)		1 unit (16 bit resolution timers × 16 channels /unit)		
	Timer Array Unit B (TAUB)		1 unit (16 bit resolution timers × 16 channels /unit)		2 units (16 bit resolution timers × 16 channels /unit)
	Timer Array Unit J (TAUJ)		4 units (32 bit resolution timers × 4 channels /unit)		
	Operating System Timer (OSTM)		5 units		
	Real-Time Clock (RTCA)		1 unit		
	Encoder Timer (ENCA)		1 unit		
	Window Watchdog Timer A (WDTA)		2 units		
Serial interfaces	Clocked Serial Interface G (CSIG)		1 channel	2 channels	4 channels
	Clocked Serial Interface H (CSIH)		4 channels		
	CAN Interface (RS-CANFD)		8 channels		
	LIN/UART Interface (RLIN3)		3 channels	6 channels	8 channels
	LIN Master Interface (RLIN2)		3 channels	6 channels	10 channels
	I^2C Bus Interface (RIIC)		2 channels		
	Clock Extension Peripheral Interface (CXP1)		Not provided		
	Single Edge Nibble Transmission (RSENT)		1 channel	2 channels	
	FlexRay Interface (FLXA)		Not provided		
	Ethernet AVB (ETNB)		Not provided		
External Interrupts	Maskable		14	24	
	Non-maskable (NMI)		1		
Other functions	Clock Monitors (CLMA)		For PLL0, PLL1, HS IntOSC, MainOSC		
	Data CRC (DCRA)		4 channels		
	Low-Voltage Indicator (LVI)		Provided		
	Power-On Clear (POC)		Provided		
	Core Voltage Monitors (CVM)		Provided		
	Error Correction Coding (ECC)		For Code flash, Data flash, Local RAM, Retention RAM, Global RAM, CSIH, RS-CANFD		

Table 1B.2 Overview of Product

Product Name		RH850/F1KM-S2		
		100 Pins	144 Pins	176 Pins
Other functions	Low Power Sampler (LPS)	Provided		
	PWM Output/Diagnostic (PWM-Diag)	44 channels	64 channels	72 channels
	Motor Control	1 unit		
	Key Return (KR)	8 channels		
	CLOCK OUTPUT (FOUT)	Provided		
	RESET OUTPUT ($\overline{\text{RESETOUT}}$)	Provided		
	Intelligent Cryptographic Unit Master D (ICUMD)	Provided		
	On-Chip debug (OCD)	Provided		
	Boundary Scan	Provided		
Voltage supply	Internal supply	VPOC to 5.5 V		
	Input/output buffer supplies	VPOC to 5.5 V		
	A/D Converter supplies	3.0 to 5.5 V		
Package		100-pin LQFP	144-pin LQFP	176-pin LQFP

1B.3 RH850/F1KM Product Lineup

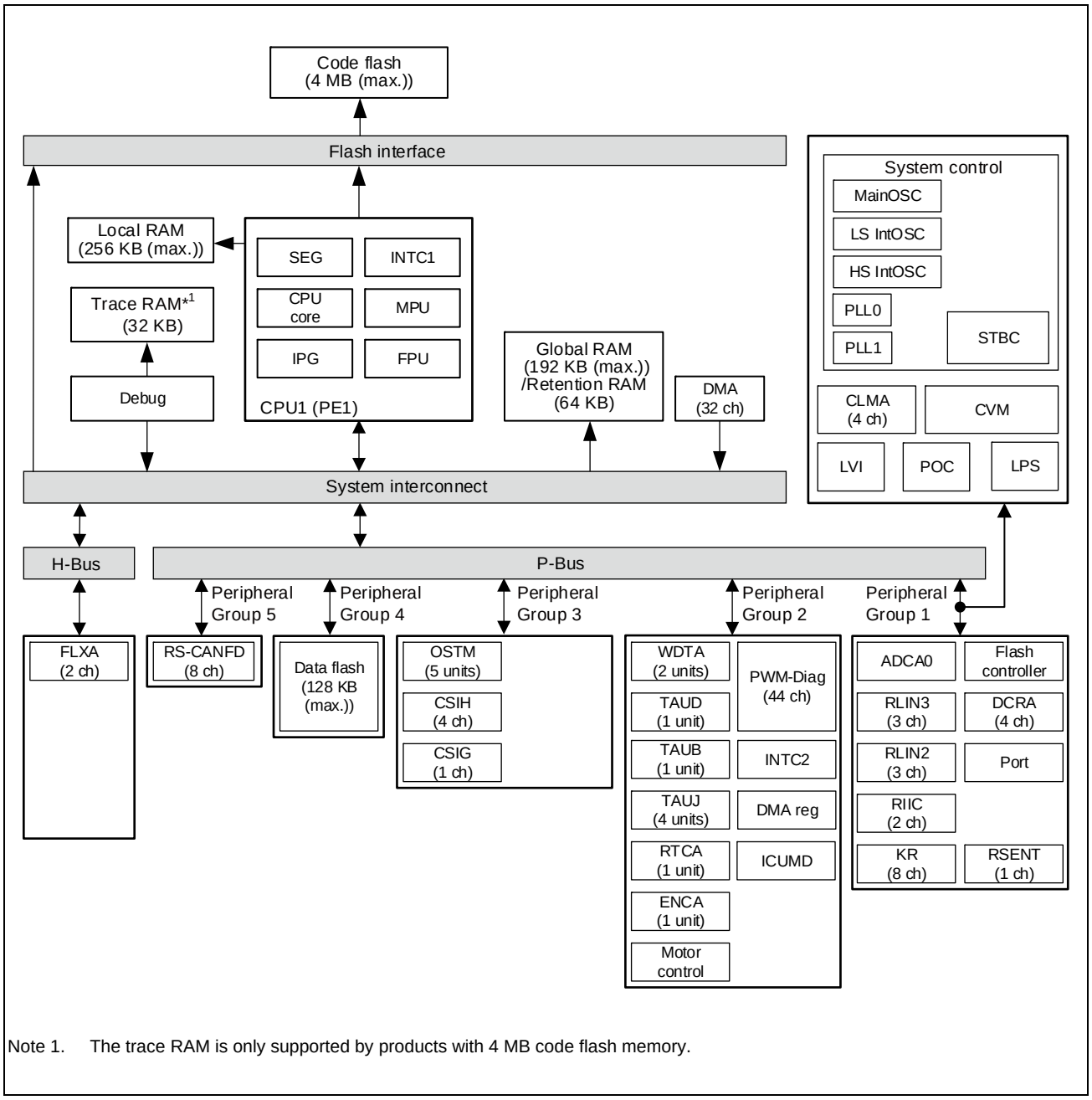
Table 1B.3 Product Lineup

F1KM-S4		Memory						Part Name	
								Operating Temperature (Ta)	
Pin Count	CPU Frequency	Code Flash	Data Flash	Local RAM (LRAM)	Global RAM (GRAM)	Retention RAM (RRAM)	Trace RAM	–40°C to +105°C Package	–40°C to +125°C Package
100 pins	240 MHz max.	3 MB	128 KB	192 KB	128 KB	64 KB	Not available	R7F7016443AFP-C LQFP	—
		4 MB		256 KB	192KB		32 KB	R7F7016453AFP-C LQFP	—
144 pins	240 MHz max.	3 MB	128 KB	192 KB	128 KB	64 KB	Not available	R7F7016463AFP-C LQFP	—
		4 MB		256 KB	192KB		32 KB	R7F7016473AFP-C LQFP	—
176 pins	240 MHz max.	3 MB	128 KB	192 KB	128 KB	64 KB	Not available	R7F7016483AFP-C LQFP	—
		4 MB		256 KB	192KB		32 KB	R7F7016493AFP-C LQFP	—
233 pins	240 MHz max.	3 MB	128 KB	192 KB	128 KB	64 KB	Not available	R7F7016503ABG-C FPBGA	R7F7016504ABG-C FPBGA
		4 MB		256 KB	192KB		32 KB	R7F7016513ABG-C FPBGA	R7F7016514ABG-C FPBGA
272 pins	240 MHz max.	3 MB	128 KB	192 KB	128 KB	64 KB	Not available	R7F7016523ABG-C FPBGA	R7F7016524ABG-C FPBGA
		4 MB		256 KB	192KB		32 KB	R7F7016533ABG-C FPBGA	R7F7016534ABG-C FPBGA

Table 1B.4 Product Lineup

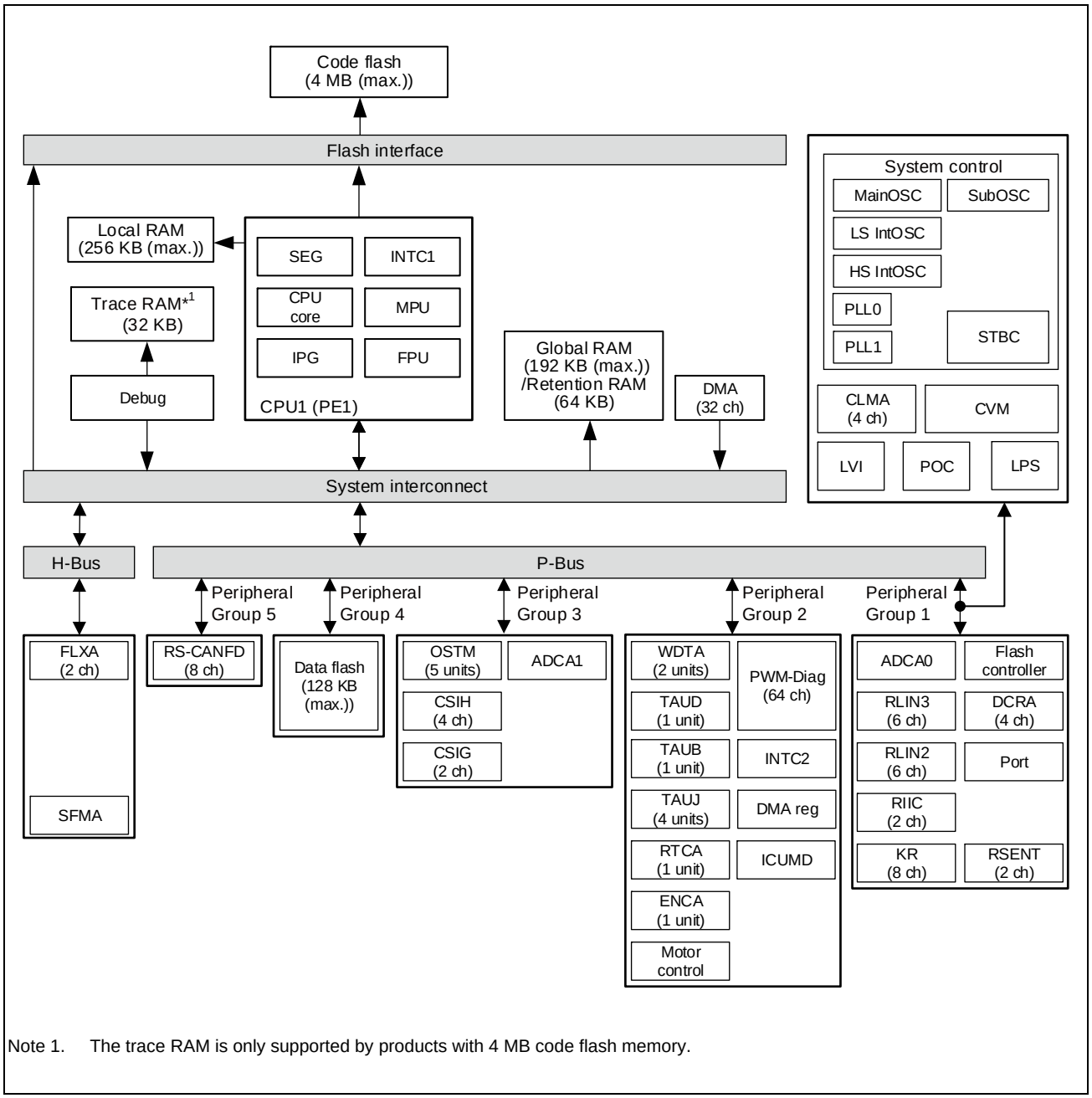
F1KM-S2		Memory						Part Name	
								Operating Temperature (Ta)	
Pin Count	CPU Frequency	Code Flash	Data Flash	Local RAM (LRAM)	Global RAM (GRAM)	Retention RAM (RRAM)	Trace RAM	–40°C to +105°C Package	–40°C to +125°C Package
100 pins	240 MHz max.	2 MB	128 KB	128 KB	96 KB	32 KB	Not available	R7F7017603AFP-C LQFP	—
144 pins	240 MHz max.	2 MB	128 KB	128 KB	96 KB	32 KB	Not available	R7F7017623AFP-C LQFP	—
176 pins	240 MHz max.	2 MB	128 KB	128 KB	96 KB	32 KB	Not available	R7F7017643AFP-C LQFP	—

1B.4 RH850/F1KM Product Block Diagrams



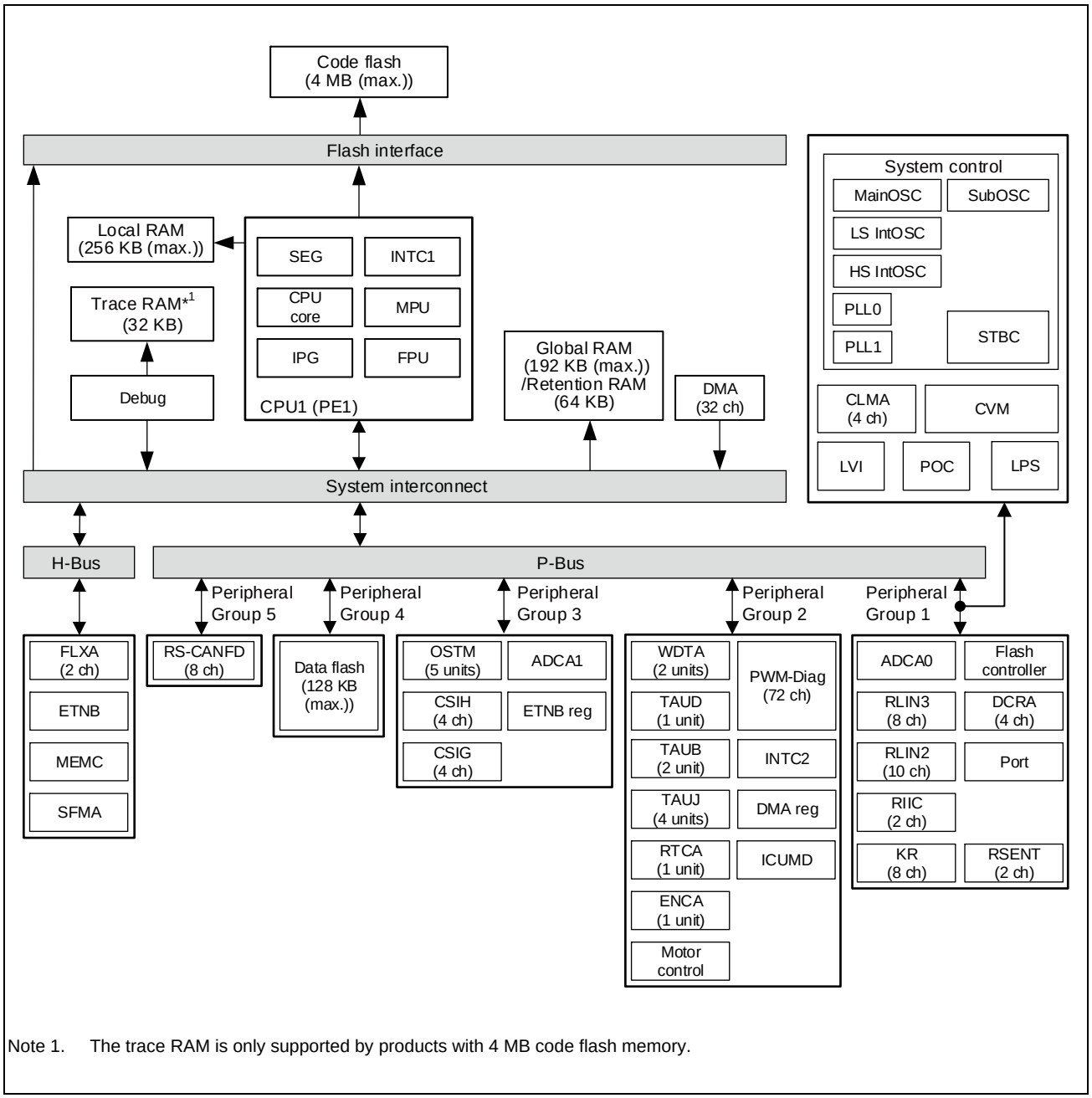
Note 1. The trace RAM is only supported by products with 4 MB code flash memory.

Figure 1B.1 Internal Block Diagram (RH850/F1KM-S4 100-Pin Version)



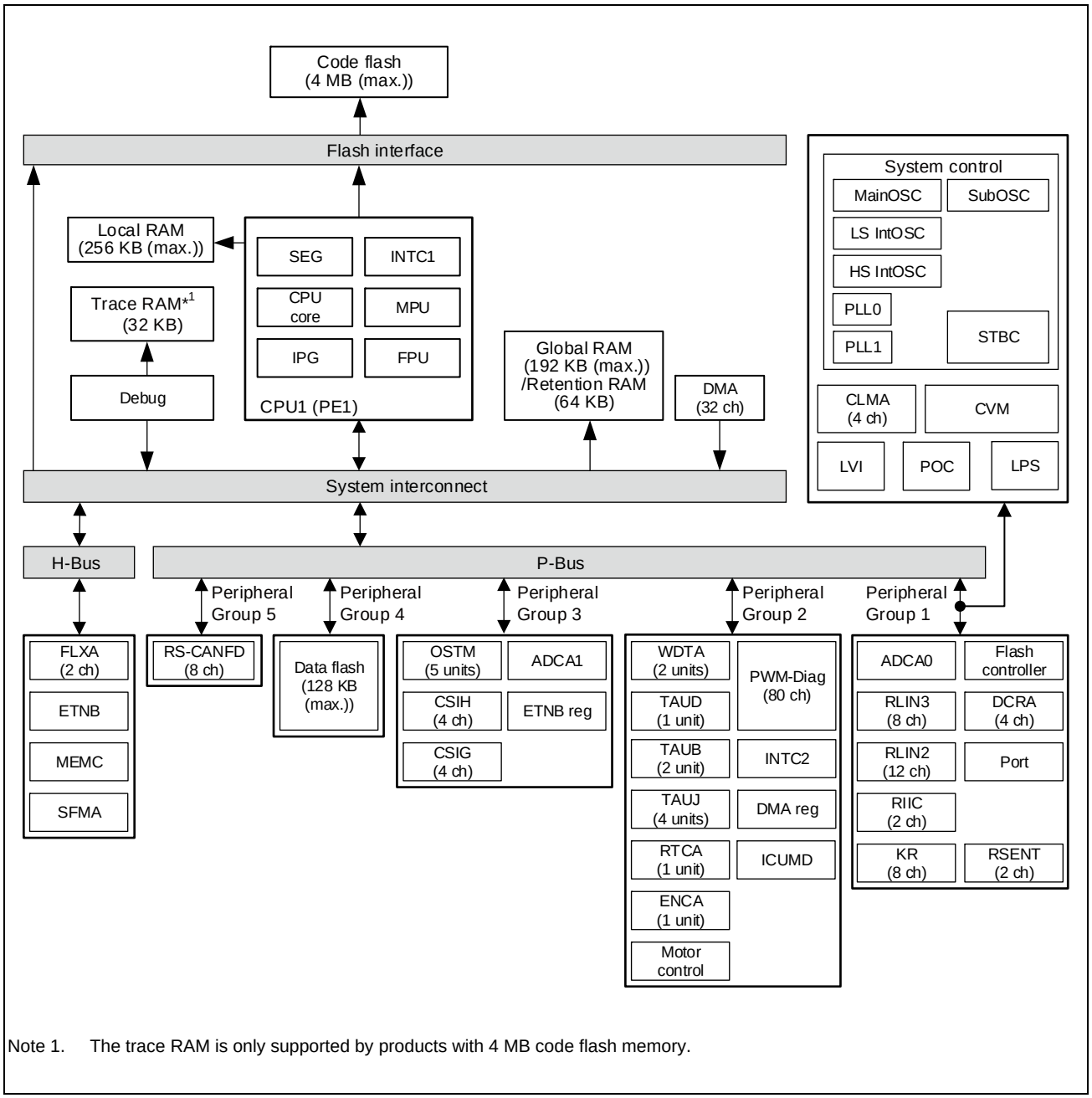
Note 1. The trace RAM is only supported by products with 4 MB code flash memory.

Figure 1B.2 Internal Block Diagram (RH850/F1KM-S4 144-Pin Version)



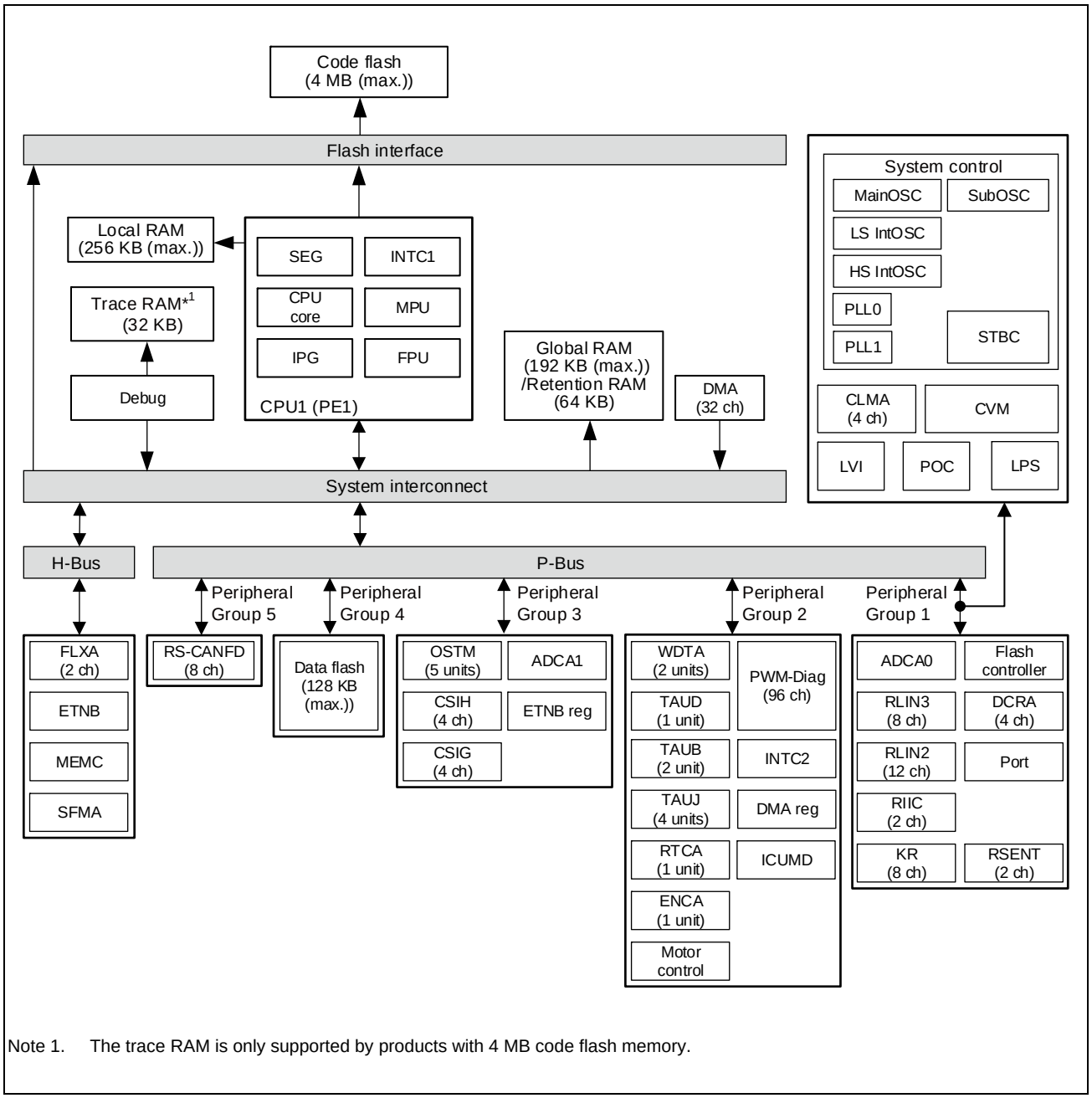
Note 1. The trace RAM is only supported by products with 4 MB code flash memory.

Figure 1B.3 Internal Block Diagram (RH850/F1KM-S4 176-Pin Version)



Note 1. The trace RAM is only supported by products with 4 MB code flash memory.

Figure 1B.4 Internal Block Diagram (RH850/F1KM-S4 233-Pin Version)



Note 1. The trace RAM is only supported by products with 4 MB code flash memory.

Figure 1B.5 Internal Block Diagram (RH850/F1KM-S4 272-Pin Version)

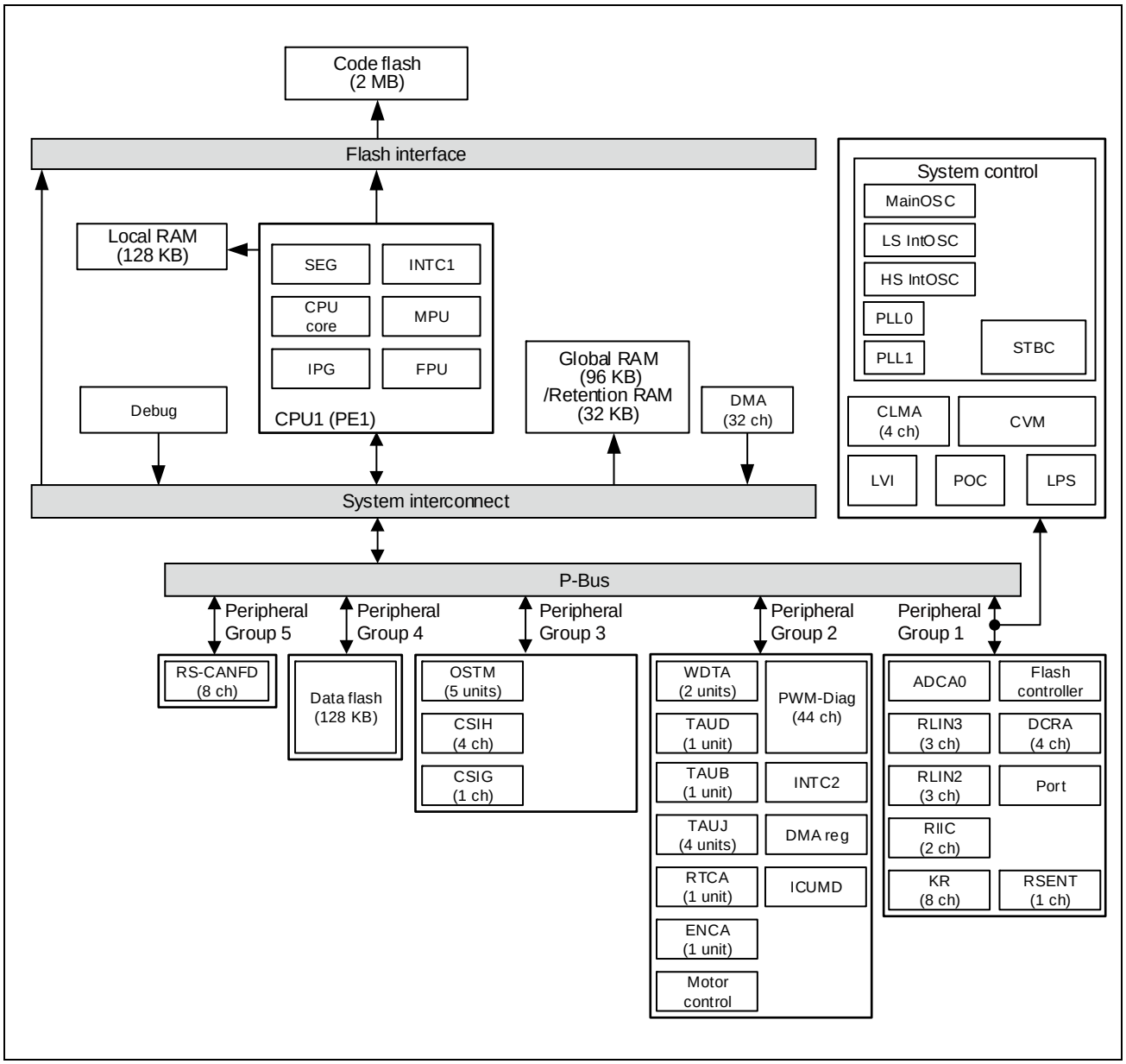


Figure 1B.6 Internal Block Diagram (RH850/F1KM-S2 100-Pin Version)

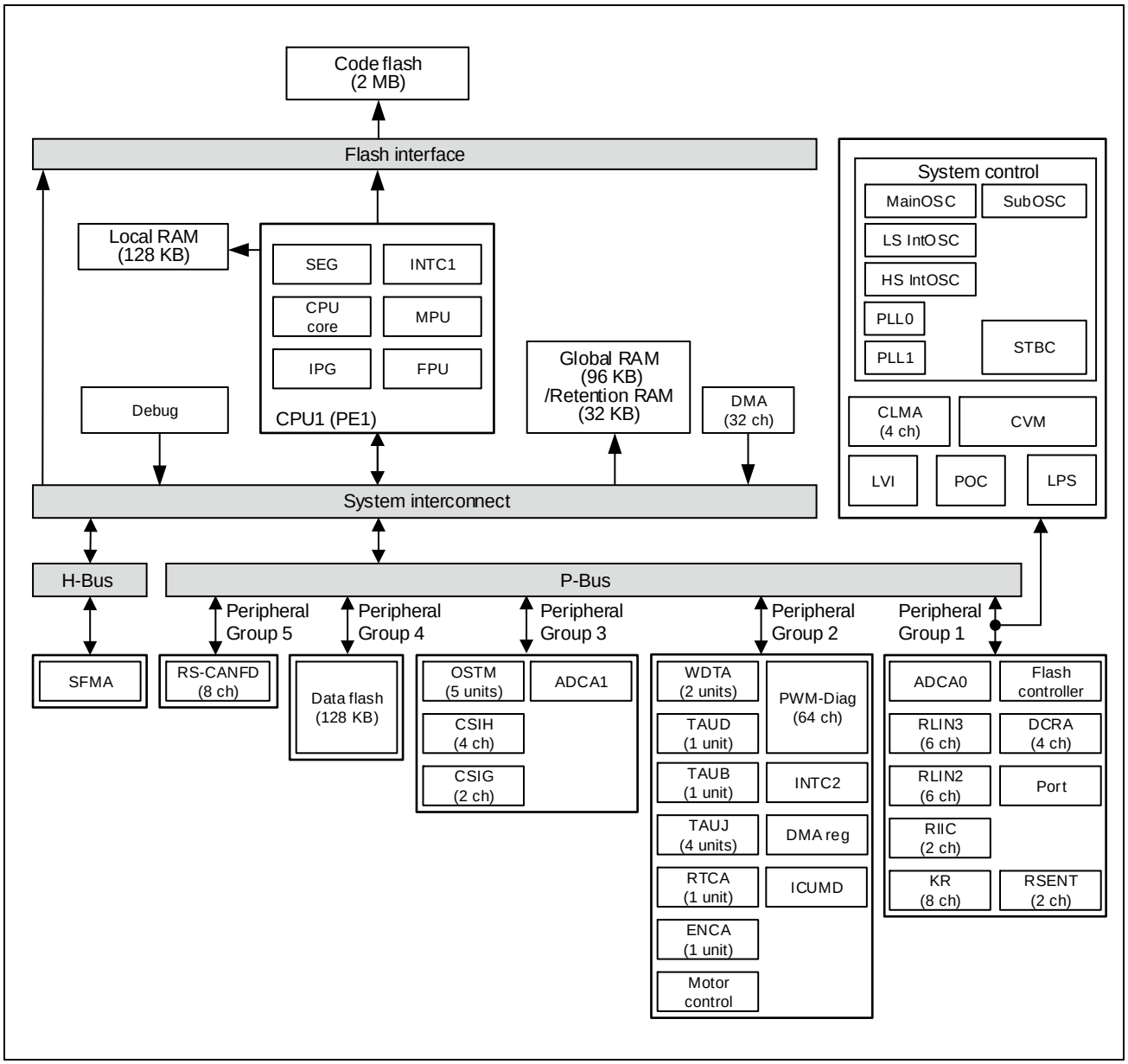


Figure 1B.7 Internal Block Diagram (RH850/F1KM-S2 144-Pin Version)

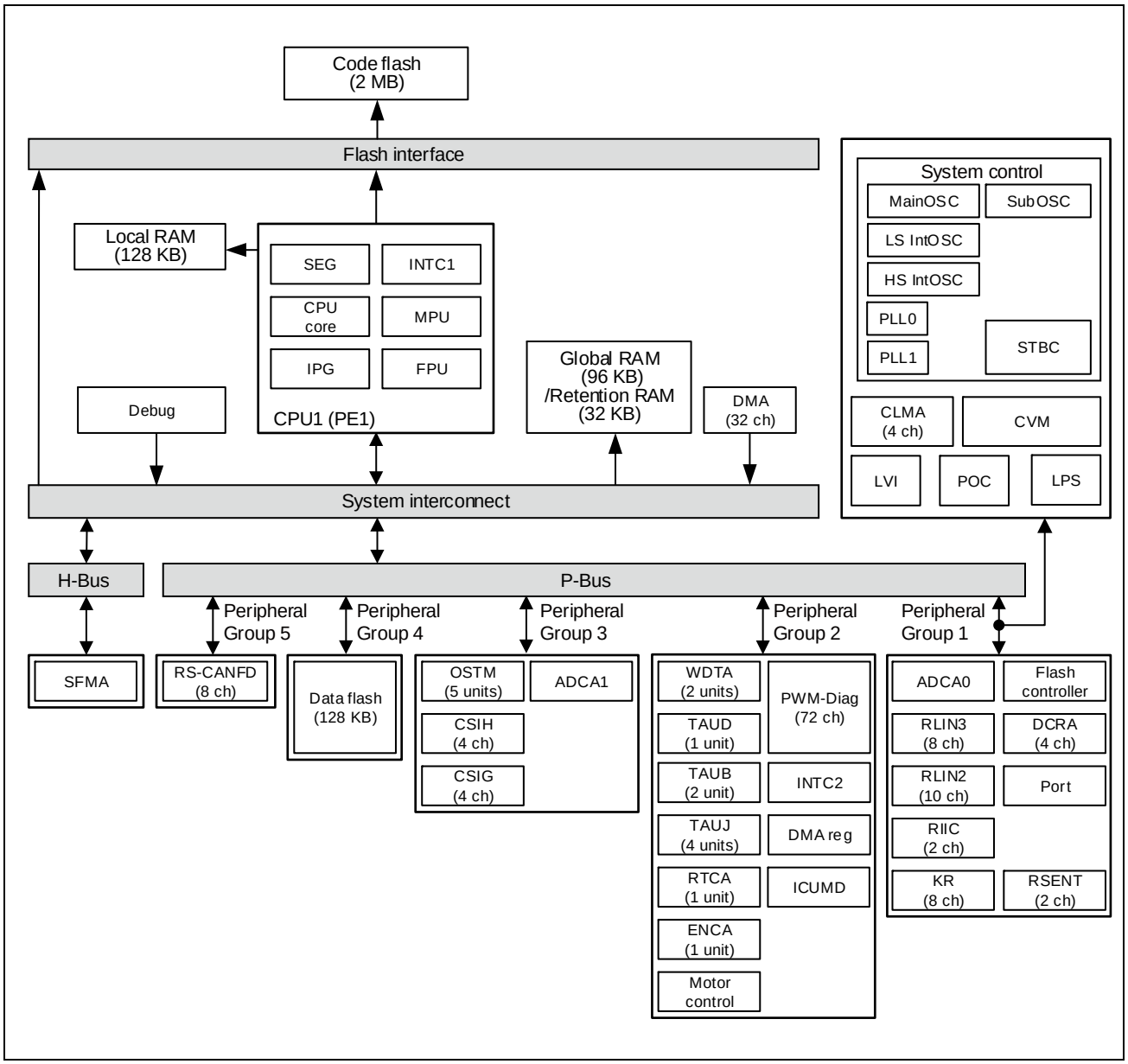


Figure 1B.8 Internal Block Diagram (RH850/F1KM-S2 176-Pin Version)

Section 1C Overview of RH850/F1KM-S1

1C.1 RH850/F1KM-S1 Outline

This RH850/F1KM-S1 is a 32-bit single-chip microcontroller with single CPU, Code Flash, Data Flash, RAM modules, DMA controllers, A/D converters, timer units and many communication interfaces that are used in the automotive applications. This microcontroller has been developed as a Safety Element out of Context (SEooC) in accordance with ISO26262.

RH850/F1KM-S1 main features are as follows:

(1) RH850 single core CPU

This microcontroller contains single RH850G3KH2.0 core support RISC-type instruction sets and have significantly improved the instruction execution speed with basic instructions (one clock cycle per instruction) and the optimized 5-stage pipeline configurations. Furthermore, this product also supports bit manipulation instructions as instructions best suited for various fields.

Two-byte basic instructions and high-level language instructions improve object code efficiency for the C compiler and reduce the program size. Furthermore, this product is suited for advanced real-time control applications by offering a high-speed response time including the processing time of the onchip interrupt controller.

(2) On-Chip Code Flash and Data Flash

This microcontroller has high-speed Code Flash from which CPU can fetch the instructions and the constant data. Code Flash with a capacity of up to 1024 KB can be reprogrammed when the chip is implemented in the application system.

This chip also has Data Flash with a capacity of 64 KB.

(3) Rich peripheral functionality

This microcontroller supports common communication interfaces such as CSI as well as automotive-oriented communication interfaces such as CAN-FD, LIN and SENT. As internal peripheral modules, this microcontroller incorporates A/D Converter and Timer module.

(4) Low power consumption

This microcontroller provides some function for low power consumption. Low Power Sampler (LPS) polls signal inputs without CPU core interaction. DeepSTOP mode disables power to select circuits within the chip.

(5) Functional Safety support

This microcontroller includes several dedicated functionalities such as the memory protection with ECC on data and clock monitors to support the functional safety standard (ISO26262) required in the automotive applications.

(6) Security support

This microcontroller supports various security features. The Intelligent Cryptographic Unit -Slave (ICUSE) has some secure peripherals such as AES engines Random Number Generator (RNG). This microcontroller also realizes the HW-level domain separation between non-secure and secure domains. The internal resources such as Data Flash can be assigned to either a non-secure or secure domain, and the secure domain is protected against non-secure accesses by the HW mechanism. This microcontroller also has the protection scheme for debug and test functionality.

1C.2 RH850/F1KM Functions

Table 1C.1 Overview of Product

Product Name			RH850/F1KM-S1			
			48 Pins	64 Pins	80 Pins	100 Pins
Memory			See **Table 1C.2, Product Lineup**.			
External Memory Access Controller (MEMC)			Not provided			
CPU	CPU System		G3KH			
	CPU frequency		120 MHz max			
	FPU		Single-Precision			
	Protection Function	Memory Protection Unit (MPU)	Provided			
		Internal Peripheral Guard (IPG)	Provided			
		Processor Element Guard (PEG)	Provided			
DMA			16 channels			
Operating clock	Main Oscillator (MainOSC)		8/16/20/24 MHz			
	Low Speed Internal Oscillator (LS IntOSC)		240 kHz(typ.)			
	High Speed Internal Oscillator (HS IntOSC)		8 MHz(typ.)			
	PLL	PLL0 (for CPU, with SSCG)	Not provided			
		PLL1 (for CPU/Peripheral)	Provided			
	Sub Oscillator (SubOSC)		Not provided			
I/O port			33	49	65	81
A/D converter	ADCA0	Physical input channels	Total 12 ch	Total 21 ch	Total 25 ch	Total 36 ch
			(12 bit resolution: 8 ch + 10 bit resolution: 4 ch)	(12 bit resolution: 10 ch + 10 bit resolution: 11 ch)	(12 bit resolution: 11 ch + 10 bit resolution: 14 ch)	(12 bit resolution: 16 ch + 10 bit resolution: 20 ch)
		External multiplexer support for channel number extension	Provided			
		Channels with T&H	3			6
	ADCA1	Physical input channels	Not provided			
		External multiplexer support for channel number extension	Not provided			
		Channels with T&H	Not provided			
Timer	Timer Array Unit D (TAUD)		1 unit (16 bit resolution timers × 16 channels /unit)			
	Timer Array Unit B (TAUB)		Not provided		1 unit (16 bit resolution timers × 16 channels /unit)	
	Timer Array Unit J (TAUJ)		4 units (32 bit resolution timers × 4 channels /unit)			
	Operating System Timer (OSTM)		1 unit			
	Real-Time Clock (RTCA)		1 unit			
	Encoder Timer (ENCA)		1 unit			
	Window Watchdog Timer A (WDTA)		2 units			

Table 1C.1 Overview of Product

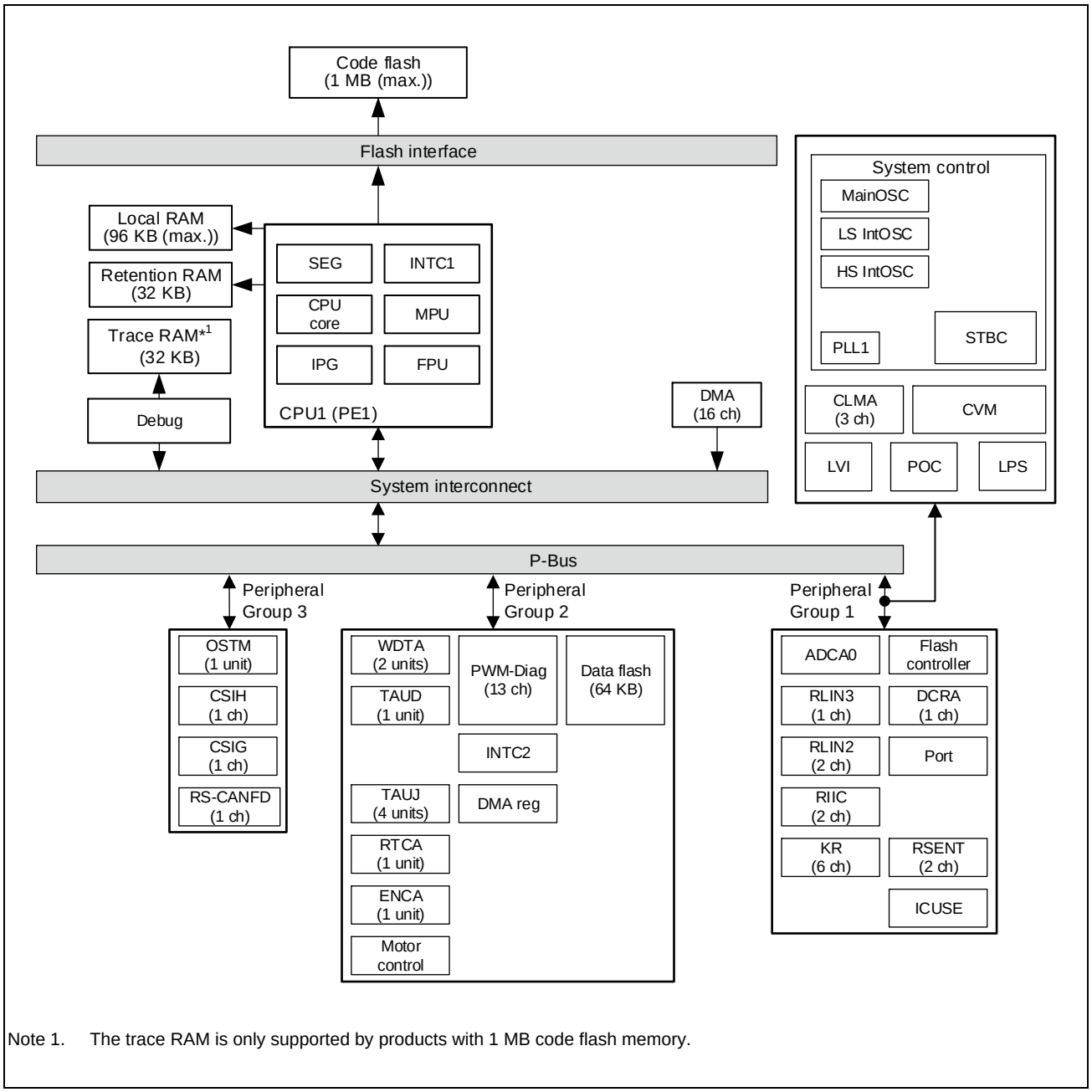
Product Name		RH850/F1KM-S1			
		48 Pins	64 Pins	80 Pins	100 Pins
Serial interfaces	Clocked Serial Interface G (CSIG)	1 channel			
	Clocked Serial Interface H (CSIH)	1 channel		3 channels	4 channels
	CAN Interface (RS-CANFD)	1 channel	3 channels		6 channels
	LIN/UART Interface (RLIN3)	1 channel	2 channels	3 channels	4 channels
	LIN Master Interface (RLIN2)	2 channels			3 channels
	I^2C Bus Interface (RIIC)	2 channels			
	Clock Extension Peripheral Interface (CXP1)	Not provided			
	Single Edge Nibble Transmission (RSENT)	2 channels			
External Interrupts	Maskable	8		12	13
	Non-maskable (NMI)	1			
Other functions	Clock Monitors (CLMA)	For PLL1, HS IntOSC, MainOSC			
	Data CRC (DCRA)	1 channel		4 channels	
	Low-Voltage Indicator (LVI)	Provided			
	Power-On Clear (POC)	Provided			
	Core Voltage Monitors (CVM)	Provided			
	Error Correction Coding (ECC)	For Code Flash, Data Flash, Local RAM, Retention RAM, CSIH, RS-CANFD			
	Low Power Sampler (LPS)	Provided			
	PWM Output/Diagnostic (PWM-Diag)	13 channels	24 channels		48 channels
	Motor Control	1 unit			
	Key Return (KR)	6 channels	8 channels		
	CLOCK OUTPUT (FOUT)	Provided			
	RESET OUTPUT ($\overline{\text{RESETOUT}}$)	Not Provided	Provided		
	Intelligent Cryptographic Unit E (ICUSE)	Provided			
	Secure WDT (SWDT)	Provided			
	On-Chip debug (OCD)	Provided			
	Boundary Scan	Provided			
Voltage supply	Internal supply	VPOC to 5.5 V			
	Input/output buffer supplies	VPOC to 5.5 V			
	A/D Converter supplies	3.0 V to 5.5 V			
Package		48-pin LQFP	64-pin LQFP	80-pin LQFP	100-pin LQFP

1C.3 RH850/F1KM Product Lineup

Table 1C.2 Product Lineup

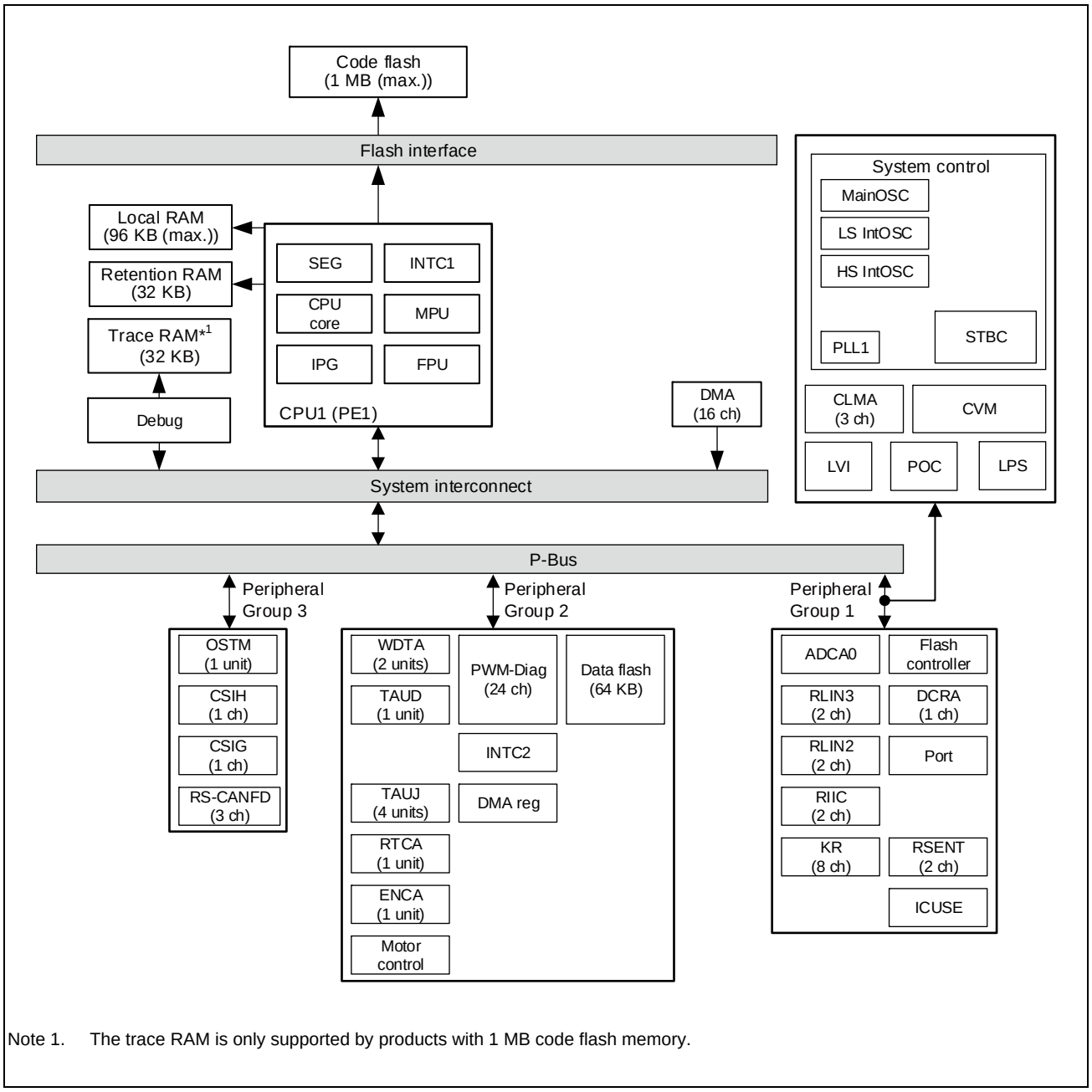
F1KM-S1		Memory					Part Name	
							Operating Temperature (Ta)	
Pin Count	CPU Frequency	Code Flash	Data Flash	Local RAM (LRAM)	Retention RAM (RRAM)	Trace RAM	–40°C to +105°C Package	–40°C to +125°C Package
100 pins	120 MHz max.	1024 KB	64 KB	96 KB	32 KB	32 KB	R7F7016843AFP-C LQFP	R7F7016844AFP-C LQFP
		768 KB		64 KB		Not available	R7F7016853AFP-C LQFP	R7F7016854AFP-C LQFP
		512 KB		32 KB		Not available	R7F7016863AFP-C LQFP	R7F7016864AFP-C LQFP
80 pins	120 MHz max.	1024 KB	64 KB	96 KB	32 KB	32 KB	R7F7016873AFP-C LQFP	R7F7016874AFP-C LQFP
		768 KB		64 KB		Not available	R7F7016883AFP-C LQFP	R7F7016884AFP-C LQFP
		512 KB		32 KB		Not available	R7F7016893AFP-C LQFP	R7F7016894AFP-C LQFP
64 pins	120 MHz max.	1024 KB	64 KB	96 KB	32 KB	32 KB	R7F7016903AFP-C LQFP	R7F7016904AFP-C LQFP
		768 KB		64 KB		Not available	R7F7016913AFP-C LQFP	R7F7016914AFP-C LQFP
		512 KB		32 KB		Not available	R7F7016923AFP-C LQFP	R7F7016924AFP-C LQFP
48 pins	120 MHz max.	1024 KB	64 KB	96 KB	32 KB	32 KB	R7F7016933AFP-C LQFP	R7F7016934AFP-C LQFP
		768 KB		64 KB		Not available	R7F7016943AFP-C LQFP	R7F7016944AFP-C LQFP
		512 KB		32 KB		Not available	R7F7016953AFP-C LQFP	R7F7016954AFP-C LQFP

1C.4 RH850/F1KM Product Block Diagrams



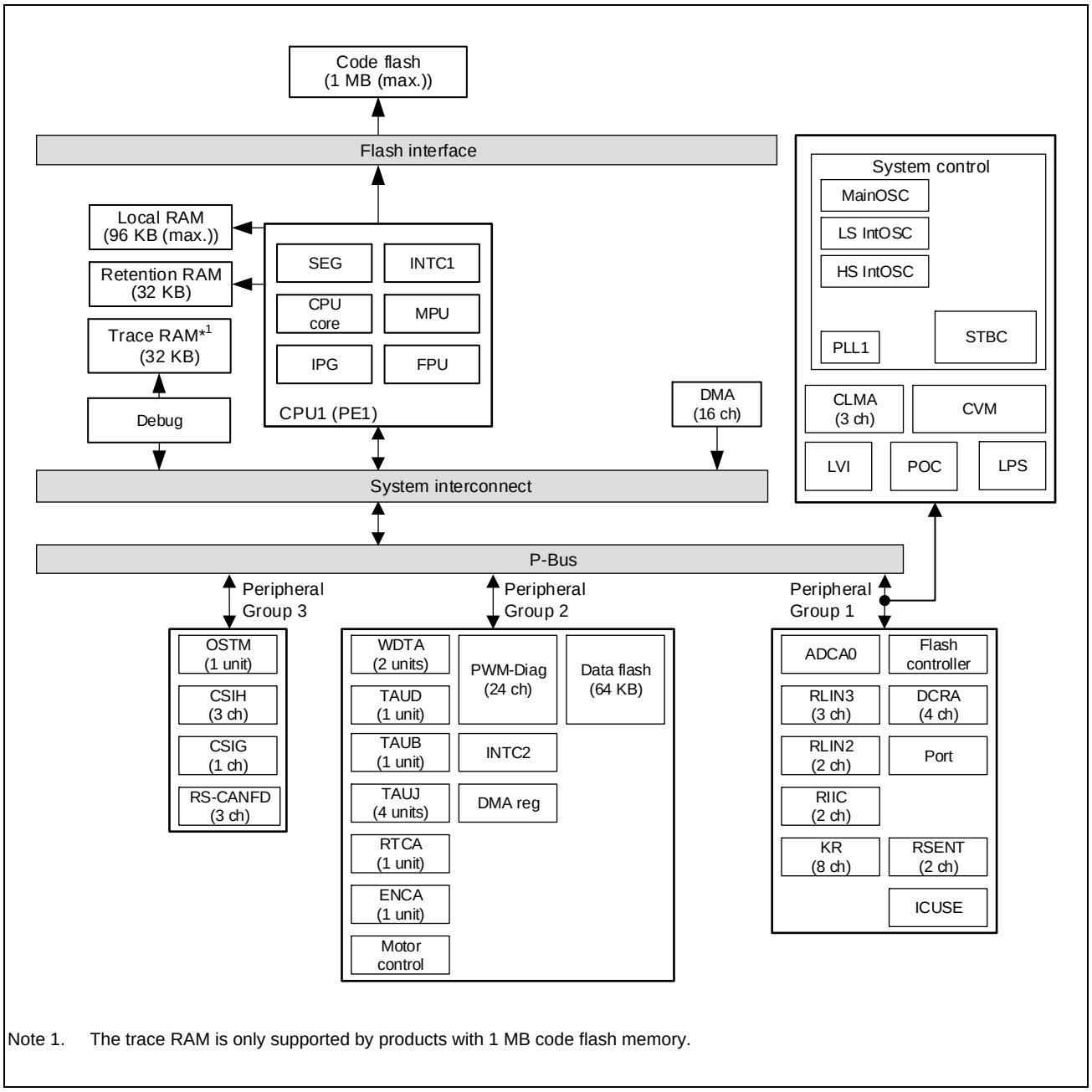
Note 1. The trace RAM is only supported by products with 1 MB code flash memory.

Figure 1C.1 Internal Block Diagram (RH850/F1KM-S1 48-Pin Version)



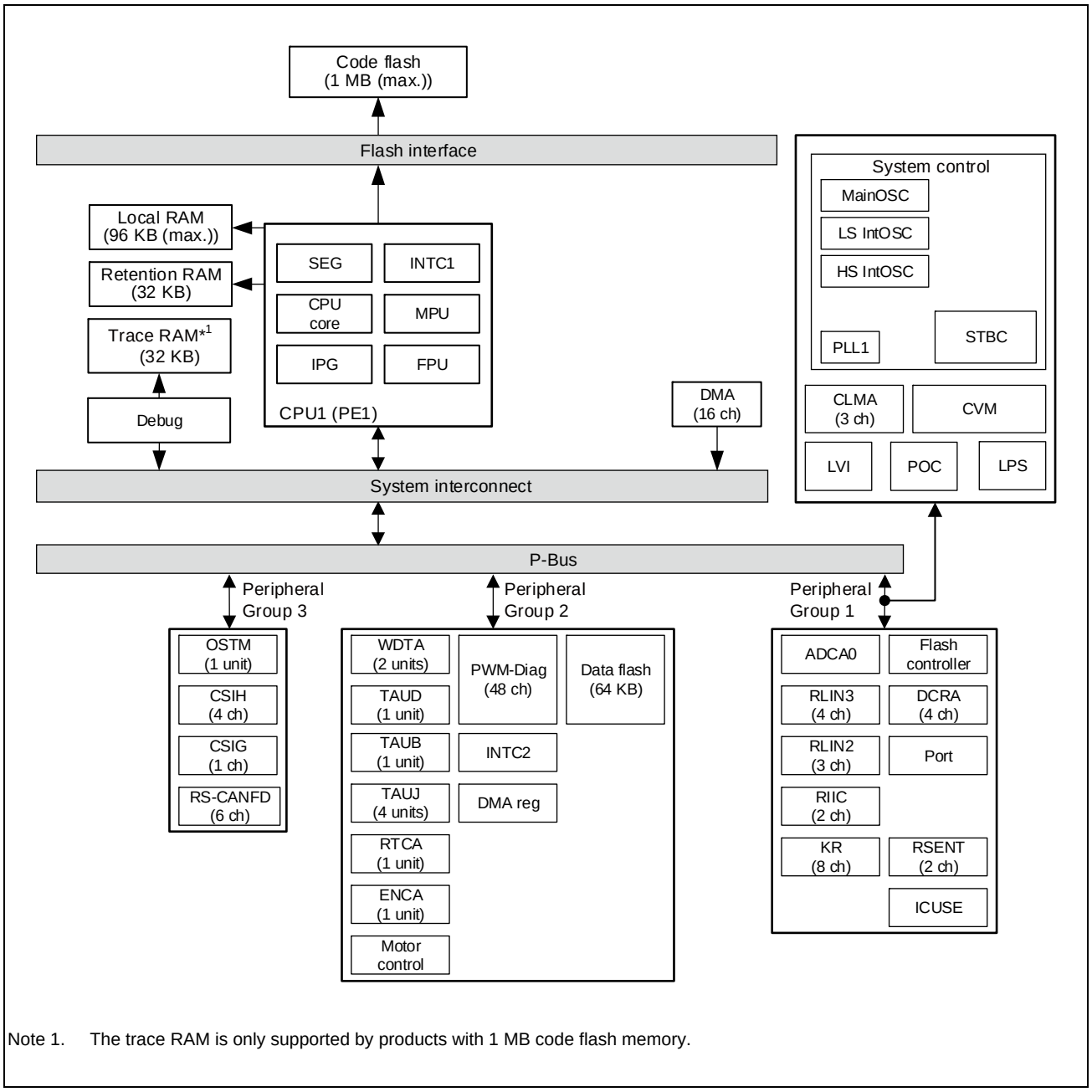
Note 1. The trace RAM is only supported by products with 1 MB code flash memory.

Figure 1C.2 Internal Block Diagram (RH850/F1KM-S1 64-Pin Version)



Note 1. The trace RAM is only supported by products with 1 MB code flash memory.

Figure 1C.3 Internal Block Diagram (RH850/F1KM-S1 80-Pin Version)



Note 1. The trace RAM is only supported by products with 1 MB code flash memory.

Figure 1C.4 Internal Block Diagram (RH850/F1KM-S1 100-Pin Version)

Section 2A Pin Function of RH850/F1KH-D8

This section describes the pin and port functions.

2A.1 Pin Connection Diagram

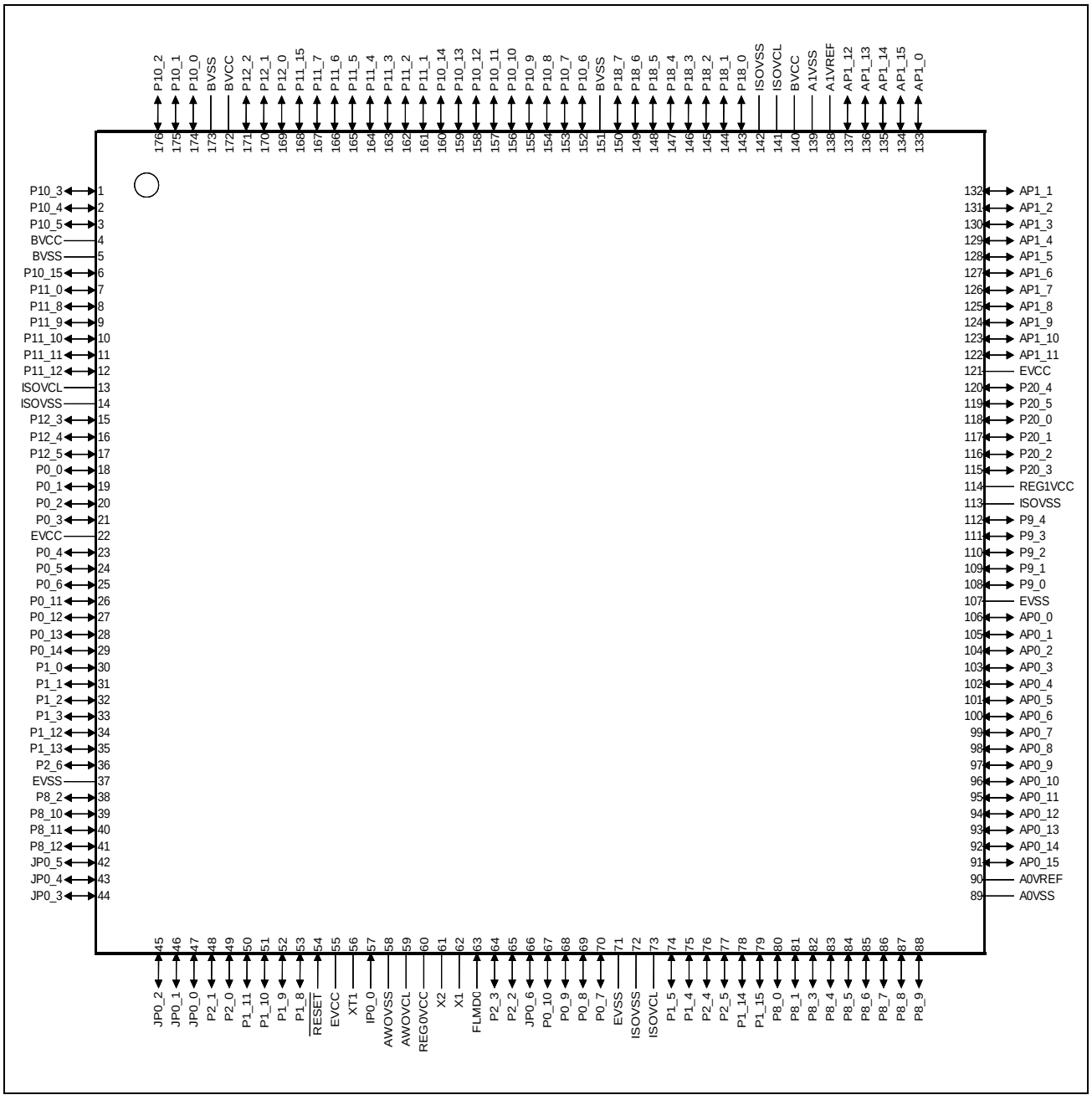
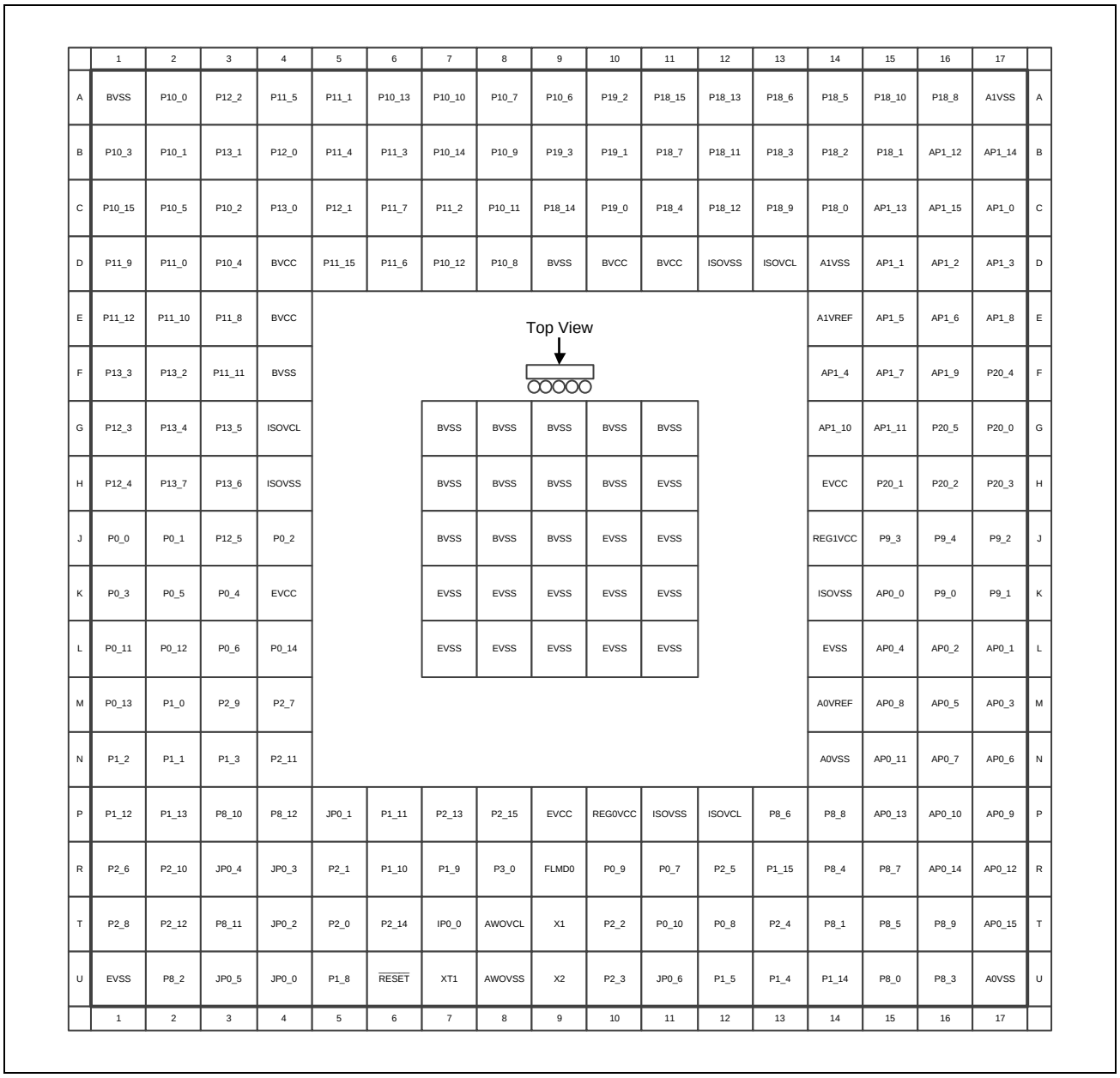


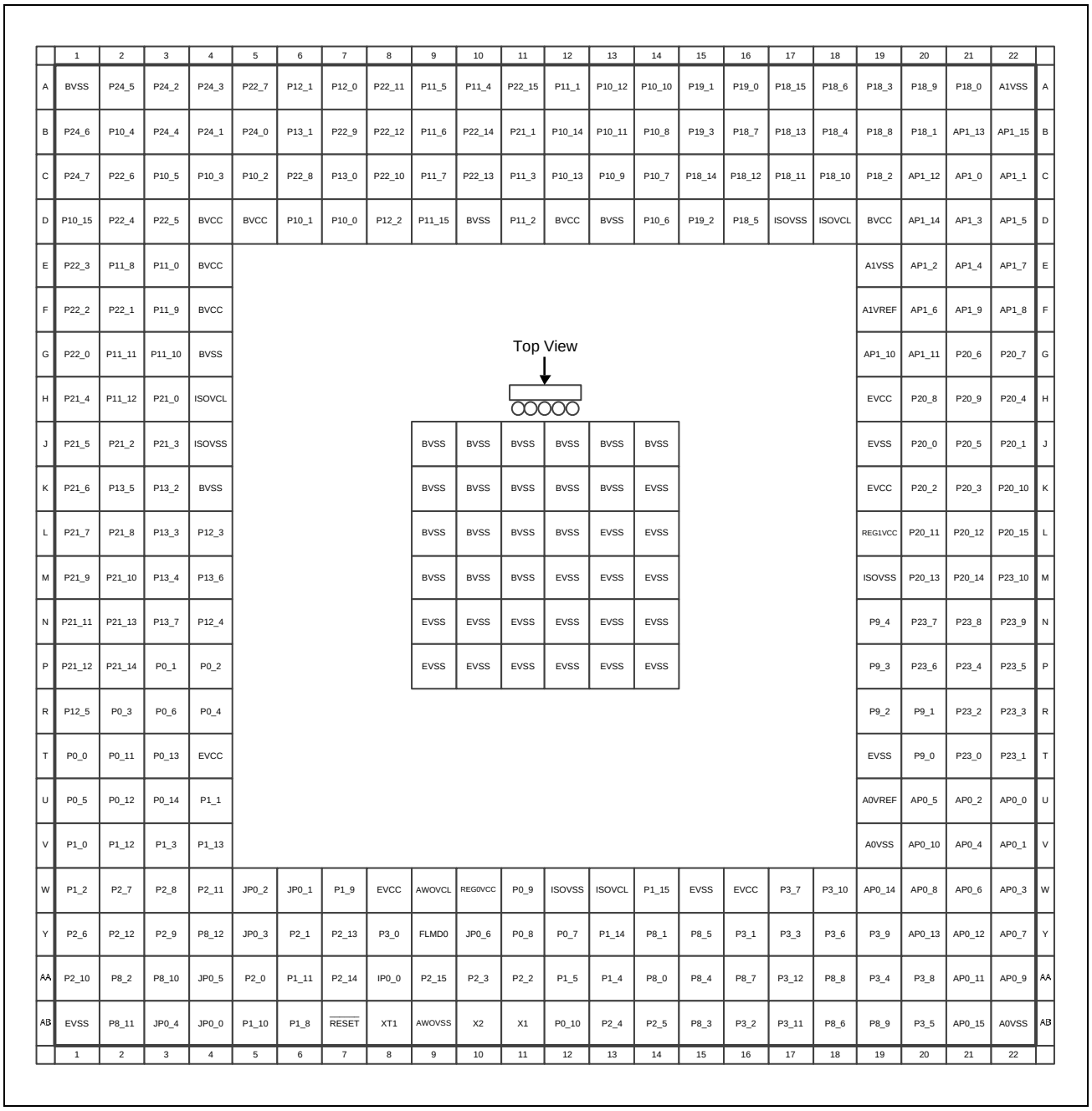
Figure 2A.1 Pin Connection Diagram (176-Pin LQFP)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	BVSS	P10_0	P12_2	P11_5	P11_1	P10_13	P10_10	P10_7	P10_6	P19_2	P18_15	P18_13	P18_6	P18_5	P18_10	P18_8	A1VSS	A
B	P10_3	P10_1	P13_1	P12_0	P11_4	P11_3	P10_14	P10_9	P19_3	P19_1	P18_7	P18_11	P18_3	P18_2	P18_1	AP1_12	AP1_14	B
C	P10_15	P10_5	P10_2	P13_0	P12_1	P11_7	P11_2	P10_11	P18_14	P19_0	P18_4	P18_12	P18_9	P18_0	AP1_13	AP1_15	AP1_0	C
D	P11_9	P11_0	P10_4	BVCC	P11_15	P11_6	P10_12	P10_8	BVSS	BVCC	BVCC	ISOVSS	ISOVCL	A1VSS	AP1_1	AP1_2	AP1_3	D
E	P11_12	P11_10	P11_8	BVCC										A1VREF	AP1_5	AP1_6	AP1_8	E
F	P13_3	P13_2	P11_11	BVSS										AP1_4	AP1_7	AP1_9	P20_4	F
G	P12_3	P13_4	P13_5	ISOVCL			BVSS	BVSS	BVSS	BVSS	BVSS			AP1_10	AP1_11	P20_5	P20_0	G
H	P12_4	P13_7	P13_6	ISOVSS			BVSS	BVSS	BVSS	BVSS	EVSS			EVCC	P20_1	P20_2	P20_3	H
J	P0_0	P0_1	P12_5	P0_2			BVSS	BVSS	BVSS	EVSS	EVSS			REG1VCC	P9_3	P9_4	P9_2	J
K	P0_3	P0_5	P0_4	EVCC			EVSS	EVSS	EVSS	EVSS	EVSS			ISOVSS	AP0_0	P9_0	P9_1	K
L	P0_11	P0_12	P0_6	P0_14			EVSS	EVSS	EVSS	EVSS	EVSS			EVSS	AP0_4	AP0_2	AP0_1	L
M	P0_13	P1_0	P2_9	P2_7										A0VREF	AP0_8	AP0_5	AP0_3	M
N	P1_2	P1_1	P1_3	P2_11										A0VSS	AP0_11	AP0_7	AP0_6	N
P	P1_12	P1_13	P8_10	P8_12	JP0_1	P1_11	P2_13	P2_15	EVCC	REG0VCC	ISOVSS	ISOVCL	P8_6	P8_8	AP0_13	AP0_10	AP0_9	P
R	P2_6	P2_10	JP0_4	JP0_3	P2_1	P1_10	P1_9	P3_0	FLMD0	P0_9	P0_7	P2_5	P1_15	P8_4	P8_7	AP0_14	AP0_12	R
T	P2_8	P2_12	P8_11	JP0_2	P2_0	P2_14	IP0_0	AWOVCL	X1	P2_2	P0_10	P0_8	P2_4	P8_1	P8_5	P8_9	AP0_15	T
U	EVSS	P8_2	JP0_5	JP0_0	P1_8	$\overline{\text{RESET}}$	XT1	AWOVSS	X2	P2_3	JP0_6	P1_5	P1_4	P1_14	P8_0	P8_3	A0VSS	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 2A.2 Pin Connection Diagram (233-Pin FPBGA)

Figure 2A.3 Reserved



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	BVSS	P24_5	P24_2	P24_3	P22_7	P12_1	P12_0	P22_11	P11_5	P11_4	P22_15	P11_1	P10_12	P10_10	P19_1	P19_0	P18_15	P18_6	P18_3	P18_9	P18_0	A1VSS	A
B	P24_6	P10_4	P24_4	P24_1	P24_0	P13_1	P22_9	P22_12	P11_6	P22_14	P21_1	P10_14	P10_11	P10_8	P19_3	P18_7	P18_13	P18_4	P18_8	P18_1	AP1_13	AP1_15	B
C	P24_7	P22_6	P10_5	P10_3	P10_2	P22_8	P13_0	P22_10	P11_7	P22_13	P11_3	P10_13	P10_9	P10_7	P18_14	P18_12	P18_11	P18_10	P18_2	AP1_12	AP1_0	AP1_1	C
D	P10_15	P22_4	P22_5	BVCC	BVCC	P10_1	P10_0	P12_2	P11_15	BVSS	P11_2	BVCC	BVSS	P10_6	P19_2	P18_5	ISOVSS	ISOVCL	BVCC	AP1_14	AP1_3	AP1_5	D
E	P22_3	P11_8	P11_0	BVCC															A1VSS	AP1_2	AP1_4	AP1_7	E
F	P22_2	P22_1	P11_9	BVCC															A1VREF	AP1_6	AP1_9	AP1_8	F
G	P22_0	P11_11	P11_10	BVSS															AP1_10	AP1_11	P20_6	P20_7	G
H	P21_4	P11_12	P21_0	ISOVCL															EVCC	P20_8	P20_9	P20_4	H
J	P21_5	P21_2	P21_3	ISOVSS					BVSS	BVSS	BVSS	BVSS	BVSS	BVSS					EVSS	P20_0	P20_5	P20_1	J
K	P21_6	P13_5	P13_2	BVSS					BVSS	BVSS	BVSS	BVSS	BVSS	EVSS					EVCC	P20_2	P20_3	P20_10	K
L	P21_7	P21_8	P13_3	P12_3					BVSS	BVSS	BVSS	BVSS	EVSS	EVSS					REG1VCC	P20_11	P20_12	P20_15	L
M	P21_9	P21_10	P13_4	P13_6					BVSS	BVSS	BVSS	EVSS	EVSS	EVSS					ISOVSS	P20_13	P20_14	P23_10	M
N	P21_11	P21_13	P13_7	P12_4					EVSS	EVSS	EVSS	EVSS	EVSS	EVSS					P9_4	P23_7	P23_8	P23_9	N
P	P21_12	P21_14	P0_1	P0_2					EVSS	EVSS	EVSS	EVSS	EVSS	EVSS					P9_3	P23_6	P23_4	P23_5	P
R	P12_5	P0_3	P0_6	P0_4															P9_2	P9_1	P23_2	P23_3	R
T	P0_0	P0_11	P0_13	EVCC															EVSS	P9_0	P23_0	P23_1	T
U	P0_5	P0_12	P0_14	P1_1															A0VREF	AP0_5	AP0_2	AP0_0	U
V	P1_0	P1_12	P1_3	P1_13															A0VSS	AP0_10	AP0_4	AP0_1	V
W	P1_2	P2_7	P2_8	P2_11	JP0_2	JP0_1	P1_9	EVCC	AWOVCL	REG0VCC	P0_9	ISOVSS	ISOVCL	P1_15	EVSS	EVCC	P3_7	P3_10	AP0_14	AP0_8	AP0_6	AP0_3	W
Y	P2_6	P2_12	P2_9	P8_12	JP0_3	P2_1	P2_13	P3_0	FLMD0	JP0_6	P0_8	P0_7	P1_14	P8_1	P8_5	P3_1	P3_3	P3_6	P3_9	AP0_13	AP0_12	AP0_7	Y
AA	P2_10	P8_2	P8_10	JP0_5	P2_0	P1_11	P2_14	IP0_0	P2_15	P2_3	P2_2	P1_5	P1_4	P8_0	P8_4	P8_7	P3_12	P8_8	P3_4	P3_8	AP0_11	AP0_9	AA
AB	EVSS	P8_11	JP0_4	JP0_0	P1_10	P1_8	$\overline{\text{RESET}}$	XT1	AWOVSS	X2	X1	P0_10	P2_4	P2_5	P8_3	P3_2	P3_11	P8_6	P8_9	P3_5	AP0_15	A0VSS	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 2A.4 Pin Connection Diagram (324-Pin FPBGA)

Table 2A.1 Pin Assignment 176-Pin LQFP

Pin No.	Pin Name
1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN / $\overline{\text{CSIH1SSI}}$ / MEMC0CLK / RLIN37RX / INTP17
2	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / CAN6TX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$ / PWGA53O / ETNB0RXD2 / MEMC0A22
3	P10_5 / TAUD0I11 / TAUD0O11 / CAN6RX / INTP6 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO / ETNB0RXD3 / PWGA54O
4	BVCC
5	BVSS
6	P10_15 / CSIH3RYI / CSIH3RYO / PWGA24O / RLIN22RX / TAUB0I9 / TAUB0O9 / $\overline{\text{MEMC0RD}}$
7	P11_0 / CSIH2RYI / CSIH2RYO / ADCA1TRG2 / PWGA25O / RLIN22TX / TAUB0I11 / TAUB0O11 / $\overline{\text{MEMC0WR}}$
8	P11_8 / $\overline{\text{CSIG1SSI}}$ / RLIN35TX / PWGA48O / TAUB1I11 / TAUB1O11 / $\overline{\text{MEMC0CS0}}$
9	P11_9 / CSIG1SO / RLIN35RX / INTP15 / PWGA49O / TAUB1I13 / TAUB1O13 / $\overline{\text{MEMC0CS1}}$
10	P11_10 / CSIG1SC / PWGA50O / TAUB1I15 / TAUB1O15 / $\overline{\text{MEMC0CS2}}$
11	P11_11 / CSIG1SI / RLIN25TX / PWGA51O / TAUB1I0 / TAUB1O0 / $\overline{\text{MEMC0CS3}}$ / ETNB0RXDV
12	P11_12 / RLIN25RX / PWGA52O / TAUB1I2 / TAUB1O2 / $\overline{\text{MEMC0WAIT}}$
13	ISOVCL
14	ISOVSS
15	P12_3 / RLIN27RX / PWGA68O / CSIG2SI / $\overline{\text{MEMC0BEN0}}$ / TAUB1I6 / TAUB1O6
16	P12_4 / RLIN27TX / PWGA69O / CSIG2SC / ETNB0MDIO / $\overline{\text{MEMC0BEN1}}$
17	P12_5 / PWGA70O / ETNB0MDC / CSIG2SO / TAUB1I4 / TAUB1O4
18	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
19	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
20	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
21	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
22	EVCC
23	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 / DPIN8 / TAUB0I12 / TAUB0O12
24	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
25	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
26	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / RLIN26RX / PWGA34O
27	P0_12 / RIIC0SCL / DPIN13 / PWGA45O / TAUB0I10 / TAUB0O10 / CSIG0SI / RLIN26TX
28	P0_13 / RLIN32RX / INTP12 / PWGA46O / TAUB0I12 / TAUB0O12 / CSIG0SO / CAN5RX / INTP5
29	P0_14 / INTP17 / RLIN32TX / PWGA47O / TAUB0I14 / TAUB0O14 / CSIG0SC / CAN5TX
30	P1_0 / RLIN33RX / INTP13 / TAUJ2I0 / TAUJ2O0 / $\overline{\text{CSIG4SSI}}$
31	P1_1 / INTP18 / RLIN33TX / CSIG4SC / TAUJ2I1 / TAUJ2O1
32	P1_2 / CAN3RX / INTP3 / DPIN19 / TAUJ2I2 / TAUJ2O2 / CSIG4SI
33	P1_3 / INTP19 / CAN3TX / DPIN23 / CSIG4SO / TAUJ2I3 / TAUJ2O3
34	P1_12 / CAN4RX / INTP4 / RLIN36TX
35	P1_13 / CAN4TX / RLIN36RX / INTP16
36	P2_6 / ADCA0SEL2 / CSIG4RYI / CSIG4RYO
37	EVSS
38	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / RLIN37TX / ADCA0I4S
39	P8_10 / CSIH3CSS3 / DPIN14 / PWGA42O / RLIN37RX / INTP17 / ADCA0I17S
40	P8_11 / TAUJ1I2 / TAUJ1O2 / DPIN15 / PWGA43O / CSIH1CSS4 / RLIN25RX / ADCA0I18S
41	P8_12 / TAUJ1I3 / TAUJ1O3 / DPIN16 / PWGA44O / CSIH1CSS5 / INTP23 / RLIN25TX / ADCA0I19S
42	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT

Table 2A.1 Pin Assignment 176-Pin LQFP

Pin No.	Pin Name
43	JP0_4 / $\overline{\text{DCUTRST}}$
44	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
45	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
46	JP0_1 / INTP1 / TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
47	JP0_0 / INTP0 / TAUJ2I0 / TAUJ2O0 / FPDR / FPDT / DCUTDI / LPDI / LPDIO
48	P2_1 / RLIN27TX / CAN6TX
49	P2_0 / RLIN27RX / CAN6RX / INTP6
50	P1_11 / ADCA1TRG2 / RLIN24TX / DPIN22 / INTP14
51	P1_10 / RLIN24RX / DPIN21 / INTP22 / ADCA1TRG1
52	P1_9 / DPIN20 / INTP21
53	P1_8
54	$\overline{\text{RESET}}$
55	EVCC
56	XT1
57	IP0_0 / XT2
58	AWOVSS
59	AWOVCL
60	REG0VCC
61	X2
62	X1
63	FLMD0
64	P2_3 / RLIN28TX / CSIH4CSS1
65	P2_2 / RLIN28RX / CSIH4CSS0
66	JP0_6 / $\overline{\text{EVTO}}$
67	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / RLIN22TX / TAUB0I6 / TAUB0O6 / CAN4TX
68	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / RLIN22RX / TAUB0I4 / TAUB0O4 / CAN4RX / INTP4
69	P0_8 / INTP16 / RLIN21TX / DPIN6 / CSIH0CSS6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2 / CAN3TX
70	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0 / CAN3RX / INTP3
71	EVSS
72	ISOVSS
73	ISOVCL
74	P1_5 / ADCA1TRG0 / RLIN35TX / DPIN17 / INTP20 / CSIH4SC
75	P1_4 / RLIN35RX / INTP15 / DPIN18 / CSIH4SI
76	P2_4 / RLIN29RX / ADCA0SEL0 / CSIH4SO
77	P2_5 / RLIN29TX / $\overline{\text{CSIH4SSI}}$ / ADCA0SEL1
78	P1_14 / RLIN23RX / CAN7RX / INTP9 / CSIH4RYI / CSIH4RYO
79	P1_15 / RLIN23TX / CAN7TX
80	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / PWGA14O / INTP4 / CSIH0CSS0 / CAN6RX / INTP6 / RIIC1SDA / SENT0RX / ADCA0I0S
81	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / PWGA15O / INTP5 / CSIH1CSS3 / CAN6TX / RIIC1SCL / SENT0SPCO / ADCA0I1S
82	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / INTP7 / PWGA23O / CAN7TX / ADCA0I5S
83	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / PWGA36O / CAN7RX / INTP9 / ADCA0I6S
84	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / INTP9 / PWGA37O / ADCA0I7S
85	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
86	P8_7 / CSIH3CSS0 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S

Table 2A.1 Pin Assignment 176-Pin LQFP

Pin No.	Pin Name
87	P8_8 / CSIH3CSS1 / PWGA40O / ADCA0SEL1 / RLIN34RX / INTP14 / ADCA0I15S
88	P8_9 / CSIH3CSS2 / PWGA41O / ADCA0SEL2 / RLIN34TX / ADCA0I16S
89	A0VSS
90	A0VREF
91	AP0_15 / ADCA0I15
92	AP0_14 / ADCA0I14
93	AP0_13 / ADCA0I13
94	AP0_12 / ADCA0I12
95	AP0_11 / ADCA0I11
96	AP0_10 / ADCA0I10
97	AP0_9 / ADCA0I9
98	AP0_8 / ADCA0I8
99	AP0_7 / ADCA0I7
100	AP0_6 / ADCA0I6
101	AP0_5 / ADCA0I5
102	AP0_4 / ADCA0I4
103	AP0_3 / ADCA0I3
104	AP0_2 / ADCA0I2
105	AP0_1 / ADCA0I1
106	AP0_0 / ADCA0I0
107	EVSS
108	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / TAUJ1I1 / TAUJ1O1 / SENT1RX / RIIC1SDA / ADCA0I2S
109	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / RIIC1SCL / ADCA0I3S
110	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S
111	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / INTP16 / ADCA0I10S
112	P9_4 / CSIH0CSS5 / PWGA33O / TAUJ1I0 / TAUJ1O0 / INTP17 / ADCA0I11S
113	ISOVSS
114	REG1VCC
115	P20_3 / CAN4TX / PWGA67O / RLIN29TX / CSIG3RYI / CSIG3RYO
116	P20_2 / CAN4RX / INTP4 / PWGA66O / RLIN29RX / CSIG3SC
117	P20_1 / RLIN26TX / PWGA65O / CAN6TX / CSIG3SO
118	P20_0 / RLIN26RX / PWGA64O / CAN6RX / INTP6 / CSIG3SI
119	P20_5 / RLIN23TX / INTP23 / PWGA60O / CAN7TX
120	P20_4 / RLIN23RX / INTP22 / PWGA59O / CAN7RX / INTP9 / $\overline{\text{CSIG3SSI}}$
121	EVCC
122	AP1_11 / ADCA1I11
123	AP1_10 / ADCA1I10
124	AP1_9 / ADCA1I9
125	AP1_8 / ADCA1I8
126	AP1_7 / ADCA1I7
127	AP1_6 / ADCA1I6
128	AP1_5 / ADCA1I5
129	AP1_4 / ADCA1I4
130	AP1_3 / ADCA1I3

Table 2A.1 Pin Assignment 176-Pin LQFP

Pin No.	Pin Name
131	AP1_2 / ADCA1I2
132	AP1_1 / ADCA1I1
133	AP1_0 / ADCA1I0
134	AP1_15 / ADCA1I15
135	AP1_14 / ADCA1I14
136	AP1_13 / ADCA1I13
137	AP1_12 / ADCA1I12
138	A1VREF
139	A1VSS
140	BVCC
141	ISOVCL
142	ISOVSS
143	P18_0 / CSIG1RYI / CSIG1RYO / ETNB0LINK / PWGA61O / TAUJ3I0 / TAUJ3O0 / ADCA1I0S
144	P18_1 / PWGA62O / ETNB0TXD0 / TAUJ3I1 / TAUJ3O1 / ADCA1I1S
145	P18_2 / PWGA63O / ETNB0TXD1 / TAUJ3I2 / TAUJ3O2 / ADCA1I2S
146	P18_3 / PWGA71O / ETNB0TXD2 / TAUJ3I3 / TAUJ3O3 / ADCA1I3S
147	P18_4 / CSIH1CSS4 / ETNB0TXD3 / ADCA1I4S
148	P18_5 / CSIH1CSS5 / ETNB0TXEN / ADCA1I5S
149	P18_6 / ADCA1I6S
150	P18_7 / ETNB0TXCLK / ADCA1I7S
151	BVSS
152	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX / INTP1 / MEMC0AD0 / RLIN24RX / MODE2
153	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / MEMC0AD1 / RLIN24TX / TAUJ3I1 / TAUJ3O1
154	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / FLXA0TXDB / ENCA0EC / PWGA5O / MEMC0AD2 / TAUJ3I2 / TAUJ3O2 / FLMD1
155	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO / MEMC0AD3 / FLXA0RXDB
156	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / MEMC0AD4 / TAUJ3I3 / TAUJ3O3
157	P10_11 / PWGA16O / RLIN31RX / INTP11 / FLXA0TXENA / CSIH1CSS0 / TAUB0I1 / TAUB0O1 / MEMC0AD5
158	P10_12 / PWGA17O / FLXA0STPWT / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3 / MEMC0AD6
159	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / RLIN32RX / INTP12 / FLXA0TXENB / TAUB0I5 / TAUB0O5 / MEMC0AD7 / CAN7TX
160	P10_14 / ADCA1TRG0 / PWGA19O / FLXA0RXDA / RLIN32TX / $\overline{\text{CSIH3SSI}}$ / TAUB0I7 / TAUB0O7 / MEMC0AD8 / CAN7RX / INTP9
161	P11_1 / $\overline{\text{CSIH2SSI}}$ / FLXA0TXDA / RLIN20RX / CSIH0CSS7 / INTP20 / PWGA26O / TAUB0I13 / TAUB0O13 / MEMC0AD9
162	P11_2 / CSIH2SO / RLIN32RX / INTP12 / RLIN20TX / PWGA27O / TAUB0I15 / TAUB0O15 / MEMC0AD10 / SFMA0IO3
163	P11_3 / CSIH2SC / CAN3RX / INTP3 / PWGA28O / TAUB1I1 / TAUB1O1 / MEMC0AD11 / RLIN32TX / SFMA0IO2
164	P11_4 / CSIH2SI / CAN3TX / INTP21 / PWGA29O / TAUB1I3 / TAUB1O3 / MEMC0AD12 / SFMA0IO1
165	P11_5 / CAN5RX / INTP5 / RLIN33TX / PWGA30O / CSIH3SI / TAUB1I5 / TAUB1O5 / MEMC0AD13 / SFMA0IO0
166	P11_6 / RLIN33RX / INTP13 / CAN5TX / ADCA1TRG1 / PWGA31O / CSIH3SO / TAUB1I7 / TAUB1O7 / MEMC0AD14 / SFMA0SSL

Table 2A.1 Pin Assignment 176-Pin LQFP

Pin No.	Pin Name
167	P11_7 / INTP5 / PWGA32O / CSIH3SC / TAUB1I9 / TAUB1O9 / MEMC0AD15 / SFMA0CLK
168	P11_15 / CAN2RX / INTP2 / CSIH2CSS4 / PWGA55O / TAUB1I8 / TAUB1O8 / $\overline{\text{MEMC0ASTB}}$ / ETNB0RXERR / RLIN36TX
169	P12_0 / CAN2TX / PWGA56O / TAUB1I10 / TAUB1O10 / $\overline{\text{CSIG2SSI}}$ / MEMC0A16 / RLIN36RX / INTP16
170	P12_1 / RLIN34RX / INTP14 / CSIH2CSS5 / PWGA57O / TAUB1I12 / TAUB1O12 / MEMC0A17
171	P12_2 / INTP19 / RLIN34TX / PWGA58O / TAUB1I14 / TAUB1O14 / MEMC0A18 / CSIG2RYI / CSIG2RYO
172	BVCC
173	BVSS
174	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX / INTP0 / CSCXFOUT / PWGA0O / TAUJ1I3 / TAPA0UP / CSIH1SI / MEMC0A19 / ETNB0RXCLK / TAUJ1O3
175	P10_1 / TAUD0I3 / TAUD0O3 / INTP18 / CAN0TX / PWGA1O / TAUJ3I0 / TAPA0UN / CSIH1SC / ETNB0RXD0 / MEMC0A20 / TAUJ3O0 / MODE0
176	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP / CSIH1SO / ETNB0RXD1 / MEMC0A21 / RLIN37TX / MODE1

Table 2A.2 Pin Assignment 233-Pin FPBGA

Pin No.	Pin Name
A1	BVSS
A2	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX / INTP0 / CSCXFOUT / PWGA0O / TAUJ1I3 / TAPA0UP / CSIH1SI / MEMC0A19 / ETNB0RXCLK / TAUJ1O3
A3	P12_2 / INTP19 / RLIN34TX / PWGA58O / TAUB1I14 / TAUB1O14 / MEMC0A18 / CSIG2RYI / CSIG2RYO
A4	P11_5 / CAN5RX / INTP5 / RLIN33TX / PWGA30O / CSIH3SI / TAUB1I5 / TAUB1O5 / MEMC0AD13 / SFMA0IO0
A5	P11_1 / $\overline{\text{CSIH2SSI}}$ / FLXA0TXDA / RLIN20RX / CSIH0CSS7 / INTP20 / PWGA26O / TAUB0I13 / TAUB0O13 / MEMC0AD9
A6	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / RLIN32RX / INTP12 / FLXA0TXENB / TAUB0I5 / TAUB0O5 / MEMC0AD7 / CAN7TX
A7	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / MEMC0AD4 / TAUJ3I3 / TAUJ3O3
A8	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / MEMC0AD1 / RLIN24TX / TAUJ3I1 / TAUJ3O1
A9	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX / INTP1 / MEMC0AD0 / RLIN24RX / MODE2
A10	P19_2 / ADCA1I18S
A11	P18_15 / ADCA1I15S
A12	P18_13 / ADCA1I13S
A13	P18_6 / ADCA1I6S
A14	P18_5 / CSIH1CSS5 / ETNB0TXEN / ADCA1I5S
A15	P18_10 / ADCA1I10S
A16	P18_8 / ADCA1I8S
A17	A1VSS
B1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN / $\overline{\text{CSIH1SSI}}$ / MEMC0CLK / RLIN37RX / INTP17
B2	P10_1 / TAUD0I3 / TAUD0O3 / INTP18 / CAN0TX / PWGA1O / TAUJ3I0 / TAPA0UN / CSIH1SC / ETNB0RXD0 / MEMC0A20 / TAUJ3O0 / MODE0
B3	P13_1 / MEMC0A20
B4	P12_0 / CAN2TX / PWGA56O / TAUB1I10 / TAUB1O10 / $\overline{\text{CSIG2SSI}}$ / MEMC0A16 / RLIN36RX / INTP16
B5	P11_4 / CSIH2SI / CAN3TX / INTP21 / PWGA29O / TAUB1I3 / TAUB1O3 / MEMC0AD12 / SFMA0IO1
B6	P11_3 / CSIH2SC / CAN3RX / INTP3 / PWGA28O / TAUB1I1 / TAUB1O1 / MEMC0AD11 / RLIN32TX / SFMA0IO2
B7	P10_14 / ADCA1TRG0 / PWGA19O / FLXA0RXDA / RLIN32TX / $\overline{\text{CSIH3SSI}}$ / TAUB0I7 / TAUB0O7 / MEMC0AD8 / CAN7RX / INTP9
B8	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO / MEMC0AD3 / FLXA0RXDB
B9	P19_3 / ADCA1I19S
B10	P19_1 / ADCA1I17S
B11	P18_7 / ETNB0TXCLK / ADCA1I7S
B12	P18_11 / ADCA1I11S
B13	P18_3 / PWGA71O / ETNB0TXD2 / TAUJ3I3 / TAUJ3O3 / ADCA1I3S
B14	P18_2 / PWGA63O / ETNB0TXD1 / TAUJ3I2 / TAUJ3O2 / ADCA1I2S
B15	P18_1 / PWGA62O / ETNB0TXD0 / TAUJ3I1 / TAUJ3O1 / ADCA1I1S
B16	AP1_12 / ADCA1I12
B17	AP1_14 / ADCA1I14
C1	P10_15 / CSIH3RYI / CSIH3RYO / PWGA24O / RLIN22RX / TAUB0I9 / TAUB0O9 / $\overline{\text{MEMC0RD}}$
C2	P10_5 / TAUD0I11 / TAUD0O11 / CAN6RX / INTP6 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO / ETNB0RXD3 / PWGA54O

Table 2A.2 Pin Assignment 233-Pin FPBGA

Pin No.	Pin Name
C3	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP / CSIH1SO / ETNB0RXD1 / MEMC0A21 / RLIN37TX / MODE1
C4	P13_0 / MEMC0A19
C5	P12_1 / RLIN34RX / INTP14 / CSIH2CSS5 / PWGA57O / TAUB1I12 / TAUB1O12 / MEMC0A17
C6	P11_7 / INTP5 / PWGA32O / CSIH3SC / TAUB1I9 / TAUB1O9 / MEMC0AD15 / SFMA0CLK
C7	P11_2 / CSIH2SO / RLIN32RX / INTP12 / RLIN20TX / PWGA27O / TAUB0I15 / TAUB0O15 / MEMC0AD10 / SFMA0IO3
C8	P10_11 / PWGA16O / RLIN31RX / INTP11 / FLXA0TXENA / CSIH1CSS0 / TAUB0I1 / TAUB0O1 / MEMC0AD5
C9	P18_14 / ADCA1I14S
C10	P19_0 / ADCA1I16S
C11	P18_4 / CSIH1CSS4 / ETNB0TXD3 / ADCA1I4S
C12	P18_12 / ADCA1I12S
C13	P18_9 / ADCA1I9S
C14	P18_0 / CSIG1RYI / CSIG1RYO / ETNB0LINK / PWGA61O / TAUJ3I0 / TAUJ3O0 / ADCA1I0S
C15	AP1_13 / ADCA1I13
C16	AP1_15 / ADCA1I15
C17	AP1_0 / ADCA1I0
D1	P11_9 / CSIG1SO / RLIN35RX / INTP15 / PWGA49O / TAUB1I13 / TAUB1O13 / $\overline{\text{MEMC0CS1}}$
D2	P11_0 / CSIH2RYI / CSIH2RYO / ADCA1TRG2 / PWGA25O / RLIN22TX / TAUB0I11 / TAUB0O11 / $\overline{\text{MEMC0WR}}$
D3	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / CAN6TX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$ / PWGA53O / ETNB0RXD2 / MEMC0A22
D4	BVCC
D5	P11_15 / CAN2RX / INTP2 / CSIH2CSS4 / PWGA55O / TAUB1I8 / TAUB1O8 / $\overline{\text{MEMC0ASTB}}$ / ETNB0RXERR / RLIN36TX
D6	P11_6 / RLIN33RX / INTP13 / CAN5TX / ADCA1TRG1 / PWGA31O / CSIH3SO / TAUB1I7 / TAUB1O7 / MEMC0AD14 / SFMA0SSL
D7	P10_12 / PWGA17O / FLXA0STPWT / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3 / MEMC0AD6
D8	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / FLXA0TXDB / ENCA0EC / PWGA5O / MEMC0AD2 / TAUJ3I2 / TAUJ3O2 / FLMD1
D9	BVSS
D10	BVCC
D11	BVCC
D12	ISOVSS
D13	ISOVCL
D14	A1VSS
D15	AP1_1 / ADCA1I1
D16	AP1_2 / ADCA1I2
D17	AP1_3 / ADCA1I3
E1	P11_12 / RLIN25RX / PWGA52O / TAUB1I2 / TAUB1O2 / $\overline{\text{MEMC0WAIT}}$
E2	P11_10 / CSIG1SC / PWGA50O / TAUB1I15 / TAUB1O15 / $\overline{\text{MEMC0CS2}}$
E3	P11_8 / $\overline{\text{CSIG1SSI}}$ / RLIN35TX / PWGA48O / TAUB1I11 / TAUB1O11 / $\overline{\text{MEMC0CS0}}$
E4	BVCC
E14	A1VREF
E15	AP1_5 / ADCA1I5
E16	AP1_6 / ADCA1I6
E17	AP1_8 / ADCA1I8

Table 2A.2 Pin Assignment 233-Pin FPBGA

Pin No.	Pin Name
F1	P13_3 / ETNB0RXERR
F2	P13_2 / ETNB0RXDV
F3	P11_11 / CSIG1SI / RLIN25TX / PWGA51O / TAUB1I0 / TAUB1O0 / $\overline{\text{MEMC0CS3}}$ / ETNB0RXDV
F4	BVSS
F14	AP1_4 / ADCA1I4
F15	AP1_7 / ADCA1I7
F16	AP1_9 / ADCA1I9
F17	P20_4 / RLIN23RX / INTP22 / PWGA59O / CAN7RX / INTP9 / $\overline{\text{CSIG3SSI}}$
G1	P12_3 / RLIN27RX / PWGA68O / CSIG2SI / $\overline{\text{MEMC0BEN0}}$ / TAUB1I6 / TAUB1O6
G2	P13_4
G3	P13_5 / MEMC0A21
G4	ISOVCL
G7	BVSS
G8	BVSS
G9	BVSS
G10	BVSS
G11	BVSS
G14	AP1_10 / ADCA1I10
G15	AP1_11 / ADCA1I11
G16	P20_5 / RLIN23TX / INTP23 / PWGA60O / CAN7TX
G17	P20_0 / RLIN26RX / PWGA64O / CAN6RX / INTP6 / CSIG3SI
H1	P12_4 / RLIN27TX / PWGA69O / CSIG2SC / ETNB0MDIO / $\overline{\text{MEMC0BEN1}}$
H2	P13_7 / PWGA73O
H3	P13_6 / MEMC0A22 / PWGA72O
H4	ISOVSS
H7	BVSS
H8	BVSS
H9	BVSS
H10	BVSS
H11	EVSS
H14	EVCC
H15	P20_1 / RLIN26TX / PWGA65O / CAN6TX / CSIG3SO
H16	P20_2 / CAN4RX / INTP4 / PWGA66O / RLIN29RX / CSIG3SC
H17	P20_3 / CAN4TX / PWGA67O / RLIN29TX / CSIG3RYI / CSIG3RYO
J1	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
J2	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
J3	P12_5 / PWGA70O / ETNB0MDC / CSIG2SO / TAUB1I4 / TAUB1O4
J4	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
J7	BVSS
J8	BVSS
J9	BVSS
J10	EVSS
J11	EVSS
J14	REG1VCC
J15	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / INTP16 / ADCA0I10S

Table 2A.2 Pin Assignment 233-Pin FPBGA

Pin No.	Pin Name
J16	P9_4 / CSIH0CSS5 / PWGA33O / TAUJ1I0 / TAUJ1O0 / INTP17 / ADCA0I11S
J17	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S
K1	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
K2	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
K3	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 / DPIN8 / TAUB0I12 / TAUB0O12
K4	EVCC
K7	EVSS
K8	EVSS
K9	EVSS
K10	EVSS
K11	EVSS
K14	ISOVSS
K15	AP0_0 / ADCA0I0
K16	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / TAUJ1I1 / TAUJ1O1 / SENT1RX / RIIC1SDA / ADCA0I2S
K17	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / RIIC1SCL / ADCA0I3S
L1	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / RLIN26RX / PWGA34O
L2	P0_12 / RIIC0SCL / DPIN13 / PWGA45O / TAUB0I10 / TAUB0O10 / CSIG0SI / RLIN26TX
L3	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
L4	P0_14 / INTP17 / RLIN32TX / PWGA47O / TAUB0I14 / TAUB0O14 / CSIG0SC / CAN5TX
L7	EVSS
L8	EVSS
L9	EVSS
L10	EVSS
L11	EVSS
L14	EVSS
L15	AP0_4 / ADCA0I4
L16	AP0_2 / ADCA0I2
L17	AP0_1 / ADCA0I1
M1	P0_13 / RLIN32RX / INTP12 / PWGA46O / TAUB0I12 / TAUB0O12 / CSIG0SO / CAN5RX / INTP5
M2	P1_0 / RLIN33RX / INTP13 / TAUJ2I0 / TAUJ2O0 / $\overline{\text{CSIG4SSI}}$
M3	P2_9 / PWGA77O
M4	P2_7 / RLIN210RX
M14	A0VREF
M15	AP0_8 / ADCA0I8
M16	AP0_5 / ADCA0I5
M17	AP0_3 / ADCA0I3
N1	P1_2 / CAN3RX / INTP3 / DPIN19 / TAUJ2I2 / TAUJ2O2 / CSIG4SI
N2	P1_1 / INTP18 / RLIN33TX / CSIG4SC / TAUJ2I1 / TAUJ2O1
N3	P1_3 / INTP19 / CAN3TX / DPIN23 / CSIG4SO / TAUJ2I3 / TAUJ2O3
N4	P2_11 / PWGA79O
N14	A0VSS
N15	AP0_11 / ADCA0I11
N16	AP0_7 / ADCA0I7

Table 2A.2 Pin Assignment 233-Pin FPBGA

Pin No.	Pin Name
N17	AP0_6 / ADCA0I6
P1	P1_12 / CAN4RX / INTP4 / RLIN36TX
P2	P1_13 / CAN4TX / RLIN36RX / INTP16
P3	P8_10 / CSIH3CSS3 / DPIN14 / PWGA42O / RLIN37RX / INTP17 / ADCA0I17S
P4	P8_12 / TAUJ1I3 / TAUJ1O3 / DPIN16 / PWGA44O / CSIH1CSS5 / INTP23 / RLIN25TX / ADCA0I19S
P5	JP0_1 / INTP1 / TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
P6	P1_11 / ADCA1TRG2 / RLIN24TX / DPIN22 / INTP14
P7	P2_13 / RLIN211TX
P8	P2_15 / PWGA75O
P9	EVCC
P10	REG0VCC
P11	ISOVSS
P12	ISOVCL
P13	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
P14	P8_8 / CSIH3CSS1 / PWGA40O / ADCA0SEL1 / RLIN34RX / INTP14 / ADCA0I15S
P15	AP0_13 / ADCA0I13
P16	AP0_10 / ADCA0I10
P17	AP0_9 / ADCA0I9
R1	P2_6 / ADCA0SEL2 / CSIG4RYI / CSIG4RYO
R2	P2_10 / PWGA78O
R3	JP0_4 / $\overline{\text{DCUTRST}}$
R4	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
R5	P2_1 / RLIN27TX / CAN6TX
R6	P1_10 / RLIN24RX / DPIN21 / INTP22 / ADCA1TRG1
R7	P1_9 / DPIN20 / INTP21
R8	P3_0 / PWGA76O
R9	FLMD0
R10	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / RLIN22RX / TAUB0I4 / TAUB0O4 / CAN4RX / INTP4
R11	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0 / CAN3RX / INTP3
R12	P2_5 / RLIN29TX / $\overline{\text{CSIH4SSI}}$ / ADCA0SEL1
R13	P1_15 / RLIN23TX / CAN7TX
R14	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / PWGA36O / CAN7RX / INTP9 / ADCA0I6S
R15	P8_7 / CSIH3CSS0 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S
R16	AP0_14 / ADCA0I14
R17	AP0_12 / ADCA0I12
T1	P2_8 / RLIN210TX
T2	P2_12 / RLIN211RX
T3	P8_11 / TAUJ1I2 / TAUJ1O2 / DPIN15 / PWGA43O / CSIH1CSS4 / RLIN25RX / ADCA0I18S
T4	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
T5	P2_0 / RLIN27RX / CAN6RX / INTP6
T6	P2_14 / PWGA74O
T7	IP0_0 / XT2
T8	AWOVCL
T9	X1
T10	P2_2 / RLIN28RX / CSIH4CSS0

Table 2A.2 Pin Assignment 233-Pin FPBGA

Pin No.	Pin Name
T11	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / RLIN22TX / TAUB0I6 / TAUB0O6 / CAN4TX
T12	P0_8 / INTP16 / RLIN21TX / DPIN6 / CSIH0CSS6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2 / CAN3TX
T13	P2_4 / RLIN29RX / ADCA0SEL0 / CSIH4SO
T14	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / PWGA15O / INTP5 / CSIH1CSS3 / CAN6TX / RIIC1SCL / SENT0SPCO / ADCA0I1S
T15	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / INTP9 / PWGA37O / ADCA0I7S
T16	P8_9 / CSIH3CSS2 / PWGA41O / ADCA0SEL2 / RLIN34TX / ADCA0I16S
T17	AP0_15 / ADCA0I15
U1	EVSS
U2	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / RLIN37TX / ADCA0I4S
U3	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT
U4	JP0_0 / INTP0 / TAUJ2I0 / TAUJ2O0 / FPDR / FPDT / DCUTDI / LPDI / LPDIO
U5	P1_8
U6	$\overline{\text{RESET}}$
U7	XT1
U8	AWOVSS
U9	X2
U10	P2_3 / RLIN28TX / CSIH4CSS1
U11	JP0_6 / $\overline{\text{EVTO}}$
U12	P1_5 / ADCA1TRG0 / RLIN35TX / DPIN17 / INTP20 / CSIH4SC
U13	P1_4 / RLIN35RX / INTP15 / DPIN18 / CSIH4SI
U14	P1_14 / RLIN23RX / CAN7RX / INTP9 / CSIH4RYI / CSIH4RYO
U15	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / PWGA14O / INTP4 / CSIH0CSS0 / CAN6RX / INTP6 / RIIC1SDA / SENT0RX / ADCA0I0S
U16	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / INTP7 / PWGA23O / CAN7TX / ADCA0I5S
U17	A0VSS

Table 2A.3 Reserved

Table 2A.4 Pin Assignment 324-Pin FPBGA

Pin No.	Pin Name
A1	BVSS
A2	P24_5 / CAN10RX / INTP20
A3	P24_2 / CAN9TX
A4	P24_3 / CAN9RX / INTP19
A5	P22_7 / MMCA0CMD
A6	P12_1 / RLIN34RX / INTP14 / CSIH2CSS5 / PWGA57O / TAUB1I12 / TAUB1O12 / MEMC0A17
A7	P12_0 / CAN2TX / PWGA56O / TAUB1I10 / TAUB1O10 / $\overline{\text{CSIG2SSI}}$ / MEMC0A16 / RLIN36RX / INTP16
A8	P22_11 / MMCA0DAT2
A9	P11_5 / CAN5RX / INTP5 / RLIN33TX / PWGA30O / CSIH3SI / TAUB1I5 / TAUB1O5 / MEMC0AD13 / SFMA0IO0
A10	P11_4 / CSIH2SI / CAN3TX / INTP21 / PWGA29O / TAUB1I3 / TAUB1O3 / MEMC0AD12 / SFMA0IO1
A11	P22_15 / MMCA0DAT6
A12	P11_1 / $\overline{\text{CSIH2SSI}}$ / FLXA0TXDA / RLIN20RX / CSIH0CSS7 / INTP20 / PWGA26O / TAUB0I13 / TAUB0O13 / MEMC0AD9
A13	P10_12 / PWGA17O / FLXA0STPWT / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3 / MEMC0AD6
A14	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / MEMC0AD4 / TAUJ3I3 / TAUJ3O3
A15	P19_1 / ADCA1I17S
A16	P19_0 / ADCA1I16S
A17	P18_15 / ADCA1I15S
A18	P18_6 / PWGA95O / ADCA1I6S
A19	P18_3 / PWGA71O / ETNB0TXD2 / TAUJ3I3 / TAUJ3O3 / ADCA1I3S
A20	P18_9 / ADCA1I9S
A21	P18_0 / CSIG1RYI / CSIG1RYO / ETNB0LINK / PWGA61O / TAUJ3I0 / TAUJ3O0 / ADCA1I0S
A22	A1VSS
B1	P24_6 / CAN11TX
B2	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / CAN6TX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$ / PWGA53O / ETNB0RXD2 / MEMC0A22
B3	P24_4 / CAN10TX
B4	P24_1 / CAN8RX / INTP18
B5	P24_0 / CAN8TX
B6	P13_1 / MEMC0A20
B7	P22_9 / MMCA0DAT0
B8	P22_12 / MMCA0DAT3
B9	P11_6 / RLIN33RX / INTP13 / CAN5TX / ADCA1TRG1 / PWGA31O / CSIH3SO / TAUB1I7 / TAUB1O7 / MEMC0AD14 / SFMA0SSL
B10	P22_14 / MMCA0DAT5
B11	P21_1 / MMCA0DAT7
B12	P10_14 / ADCA1TRG0 / PWGA19O / FLXA0RXDA / RLIN32TX / $\overline{\text{CSIH3SSI}}$ / TAUB0I7 / TAUB0O7 / MEMC0AD8 / CAN7RX / INTP9
B13	P10_11 / PWGA16O / RLIN31RX / INTP11 / FLXA0TXENA / CSIH1CSS0 / TAUB0I1 / TAUB0O1 / MEMC0AD5
B14	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / FLXA0TXDB / ENCA0EC / PWGA5O / MEMC0AD2 / TAUJ3I2 / TAUJ3O2 / FLMD1
B15	P19_3 / ADCA1I19S
B16	P18_7 / ETNB0TXCLK / ADCA1I7S
B17	P18_13 / ADCA1I13S

Table 2A.4 Pin Assignment 324-Pin FPBGA

Pin No.	Pin Name
B18	P18_4 / CSIH1CSS4 / ETNB0TXD3 / ADCA1I4S
B19	P18_8 / ADCA1I8S
B20	P18_1 / PWGA62O / ETNB0TXD0 / TAUJ3I1 / TAUJ3O1 / ADCA1I1S
B21	AP1_13 / ADCA1I13
B22	AP1_15 / ADCA1I15
C1	P24_7 / CAN11RX / INTP21
C2	P22_6 / ETNB1TXCLK
C3	P10_5 / TAUD0I11 / TAUD0O11 / CAN6RX / INTP6 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO / ETNB0RXD3 / PWGA54O
C4	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN / $\overline{\text{CSIH1SSI}}$ / MEMC0CLK / RLIN37RX / INTP17
C5	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP / CSIH1SO / ETNB0RXD1 / MEMC0A21 / RLIN37TX / MODE1
C6	P22_8 / MMCA0CLK
C7	P13_0 / MEMC0A19
C8	P22_10 / MMCA0DAT1
C9	P11_7 / INTP5 / PWGA32O / CSIH3SC / TAUB1I9 / TAUB1O9 / MEMC0AD15 / SFMA0CLK
C10	P22_13 / MMCA0DAT4
C11	P11_3 / CSIH2SC / CAN3RX / INTP3 / PWGA28O / TAUB1I1 / TAUB1O1 / MEMC0AD11 / RLIN32TX / SFMA0IO2
C12	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / RLIN32RX / INTP12 / FLXA0TXENB / TAUB0I5 / TAUB0O5 / MEMC0AD7 / CAN7TX
C13	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO / MEMC0AD3 / FLXA0RXDB
C14	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / MEMC0AD1 / RLIN24TX / TAUJ3I1 / TAUJ3O1
C15	P18_14 / ADCA1I14S
C16	P18_12 / ADCA1I12S
C17	P18_11 / ADCA1I11S
C18	P18_10 / ADCA1I10S
C19	P18_2 / PWGA63O / ETNB0TXD1 / TAUJ3I2 / TAUJ3O2 / ADCA1I2S
C20	AP1_12 / ADCA1I12
C21	AP1_0 / ADCA1I0
C22	AP1_1 / ADCA1I1
D1	P10_15 / CSIH3RYI / CSIH3RYO / PWGA24O / RLIN22RX / TAUB0I9 / TAUB0O9 / $\overline{\text{MEMC0RD}}$
D2	P22_4 / ETNB1TXD0
D3	P22_5 / ETNB1TXEN
D4	BVCC
D5	BVCC
D6	P10_1 / TAUD0I3 / TAUD0O3 / INTP18 / CAN0TX / PWGA1O / TAUJ3I0 / TAPA0UN / CSIH1SC / ETNB0RXD0 / MEMC0A20 / TAUJ3O0 / MODE0
D7	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX / INTP0 / CSCXFOUT / PWGA0O / TAUJ1I3 / TAPA0UP / CSIH1SI / MEMC0A19 / ETNB0RXCLK / TAUJ1O3
D8	P12_2 / INTP19 / RLIN34TX / PWGA58O / TAUB1I14 / TAUB1O14 / MEMC0A18 / CSIG2RYI / CSIG2RYO
D9	P11_15 / CAN2RX / INTP2 / CSIH2CSS4 / PWGA55O / TAUB1I8 / TAUB1O8 / $\overline{\text{MEMC0ASTB}}$ / ETNB0RXERR / RLIN36TX
D10	BVSS
D11	P11_2 / CSIH2SO / RLIN32RX / INTP12 / RLIN20TX / PWGA27O / TAUB0I15 / TAUB0O15 / MEMC0AD10 / SFMA0IO3

Table 2A.4 Pin Assignment 324-Pin FPBGA

Pin No.	Pin Name
D12	BVCC
D13	BVSS
D14	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX / INTP1 / MEMC0AD0 / RLIN24RX / MODE2
D15	P19_2 / ADCA1I18S
D16	P18_5 / CSIH1CSS5 / ETNB0TXEN / ADCA1I5S
D17	ISOVSS
D18	ISOVCL
D19	BVCC
D20	AP1_14 / ADCA1I14
D21	AP1_3 / ADCA1I3
D22	AP1_5 / ADCA1I5
E1	P22_3 / ETNB1TXD1
E2	P11_8 / $\overline{\text{CSIG1SSI}}$ / RLIN35TX / PWGA48O / TAUB1I11 / TAUB1O11 / $\overline{\text{MEMC0CS0}}$
E3	P11_0 / CSIH2RYI / CSIH2RYO / ADCA1TRG2 / PWGA25O / RLIN22TX / TAUB0I11 / TAUB0O11 / $\overline{\text{MEMC0WR}}$
E4	BVCC
E19	A1VSS
E20	AP1_2 / ADCA1I2
E21	AP1_4 / ADCA1I4
E22	AP1_7 / ADCA1I7
F1	P22_2 / ETNB1TXD2
F2	P22_1 / ETNB1TXD3
F3	P11_9 / CSIG1SO / RLIN35RX / INTP15 / PWGA49O / TAUB1I13 / TAUB1O13 / $\overline{\text{MEMC0CS1}}$
F4	BVCC
F19	A1VREF
F20	AP1_6 / ADCA1I6
F21	AP1_9 / ADCA1I9
F22	AP1_8 / ADCA1I8
G1	P22_0 / ETNB1RXCLK
G2	P11_11 / CSIG1SI / RLIN25TX / PWGA51O / TAUB1I0 / TAUB1O0 / $\overline{\text{MEMC0CS3}}$ / ETNB0RXDV
G3	P11_10 / CSIG1SC / PWGA50O / TAUB1I15 / TAUB1O15 / $\overline{\text{MEMC0CS2}}$
G4	BVSS
G19	AP1_10 / ADCA1I10
G20	AP1_11 / ADCA1I11
G21	P20_6 / PWGA88O
G22	P20_7 / PWGA89O
H1	P21_4 / ETNB1RXD0
H2	P11_12 / RLIN25RX / PWGA52O / TAUB1I2 / TAUB1O2 / $\overline{\text{MEMC0WAIT}}$
H3	P21_0 / ETNB1RXDV
H4	ISOVCL
H19	EVCC
H20	P20_8 / PWGA90O
H21	P20_9 / PWGA91O
H22	P20_4 / RLIN23RX / INTP22 / PWGA59O / CAN7RX / INTP9 / $\overline{\text{CSIG3SSI}}$
J1	P21_5 / ETNB1RXD3

Table 2A.4 Pin Assignment 324-Pin FPBGA

Pin No.	Pin Name
J2	P21_2 / ETNB1RXD2
J3	P21_3 / ETNB1RXD1
J4	ISOVSS
J9	BVSS
J10	BVSS
J11	BVSS
J12	BVSS
J13	BVSS
J14	BVSS
J19	EVSS
J20	P20_0 / RLIN26RX / PWGA64O / CAN6RX / INTP6 / CSIG3SI
J21	P20_5 / RLIN23TX / INTP23 / PWGA60O / CAN7TX
J22	P20_1 / RLIN26TX / PWGA65O / CAN6TX / CSIG3SO
K1	P21_6 / ETNB1MDC
K2	P13_5 / MEMC0A21
K3	P13_2 / ETNB0RXDV
K4	BVSS
K9	BVSS
K10	BVSS
K11	BVSS
K12	BVSS
K13	BVSS
K14	EVSS
K19	EVCC
K20	P20_2 / CAN4RX / INTP4 / PWGA66O / RLIN29RX / CSIG3SC
K21	P20_3 / CAN4TX / PWGA67O / RLIN29TX / CSIG3RYI / CSIG3RYO
K22	P20_10 / PWGA92O
L1	P21_7 / ETNB1MDIO
L2	P21_8 / ETNB1RXERR
L3	P13_3 / ETNB0RXERR
L4	P12_3 / RLIN27RX / PWGA68O / CSIG2SI / $\overline{\text{MEMC0BEN0}}$ / TAUB1I6 / TAUB1O6
L9	BVSS
L10	BVSS
L11	BVSS
L12	BVSS
L13	EVSS
L14	EVSS
L19	REG1VCC
L20	P20_11 / PWGA93O
L21	P20_12 / PWGA94O
L22	P20_15 / RLIN214RX
M1	P21_9
M2	P21_10
M3	P13_4 / ETNB1LINK
M4	P13_6 / MEMC0A22 / PWGA72O

Table 2A.4 Pin Assignment 324-Pin FPBGA

Pin No.	Pin Name
M9	BVSS
M10	BVSS
M11	BVSS
M12	EVSS
M13	EVSS
M14	EVSS
M19	ISOVSS
M20	P20_13 / RLIN215RX / PWGA95O
M21	P20_14 / RLIN215TX
M22	P23_10 / RLIN214TX
N1	P21_11 / RLIN213RX
N2	P21_13 / RLIN212RX
N3	P13_7 / MEMC0A23 / PWGA73O
N4	P12_4 / RLIN27TX / PWGA69O / CSIG2SC / ETNB0MDIO / $\overline{\text{MEMC0BEN1}}$
N9	EVSS
N10	EVSS
N11	EVSS
N12	EVSS
N13	EVSS
N14	EVSS
N19	P9_4 / CSIH0CSS5 / PWGA33O / TAUJ1I0 / TAUJ1O0 / INTP17 / ADCA0I11S
N20	P23_7 / CSIG4SI
N21	P23_8 / CSIG4SC
N22	P23_9 / $\overline{\text{CSIG4SSI}}$
P1	P21_12 / RLIN213TX
P2	P21_14 / RLIN212TX
P3	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
P4	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
P9	EVSS
P10	EVSS
P11	EVSS
P12	EVSS
P13	EVSS
P14	EVSS
P19	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / INTP16 / ADCA0I10S
P20	P23_6 / CSIG4SO
P21	P23_4 / CSIH4RYI / CSIH4RYO
P22	P23_5 / CSIG4RYI / CSIG4RYO
R1	P12_5 / PWGA70O / ETNB0MDC / CSIG2SO / TAUB1I4 / TAUB1O4
R2	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
R3	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
R4	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 / DPIN8 / TAUB0I12 / TAUB0O12
R19	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S

Table 2A.4 Pin Assignment 324-Pin FPBGA

Pin No.	Pin Name
R20	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / RIIC1SCL / ADCA0I3S
R21	P23_2 / CSIH4SI
R22	P23_3 / CSIH4SC
T1	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
T2	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / RLIN26RX / PWGA34O
T3	P0_13 / RLIN32RX / INTP12 / PWGA46O / TAUB0I12 / TAUB0O12 / CSIG0SO / CAN5RX / INTP5
T4	EVCC
T19	EVSS
T20	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / TAUJ1I1 / TAUJ1O1 / SENT1RX / RIIC1SDA / ADCA0I2S
T21	P23_0 / $\overline{\text{CSIH4SSI}}$
T22	P23_1 / CSIH4SO
U1	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
U2	P0_12 / RIIC0SCL / DPIN13 / PWGA45O / TAUB0I10 / TAUB0O10 / CSIG0SI / RLIN26TX
U3	P0_14 / INTP17 / RLIN32TX / PWGA47O / TAUB0I14 / TAUB0O14 / CSIG0SC / CAN5TX
U4	P1_1 / INTP18 / RLIN33TX / CSIG4SC / TAUJ2I1 / TAUJ2O1
U19	A0VREF
U20	AP0_5 / ADCA0I5
U21	AP0_2 / ADCA0I2
U22	AP0_0 / ADCA0I0
V1	P1_0 / RLIN33RX / INTP13 / TAUJ2I0 / TAUJ2O0 / $\overline{\text{CSIG4SSI}}$
V2	P1_12 / CAN4RX / INTP4 / RLIN36TX
V3	P1_3 / INTP19 / CAN3TX / DPIN23 / CSIG4SO / TAUJ2I3 / TAUJ2O3
V4	P1_13 / CAN4TX / RLIN36RX / INTP16
V19	A0VSS
V20	AP0_10 / ADCA0I10
V21	AP0_4 / ADCA0I4
V22	AP0_1 / ADCA0I1
W1	P1_2 / CAN3RX / INTP3 / DPIN19 / TAUJ2I2 / TAUJ2O2 / CSIG4SI
W2	P2_7 / RLIN210RX
W3	P2_8 / RLIN210TX
W4	P2_11 / PWGA79O
W5	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
W6	JP0_1 / INTP1 / TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
W7	P1_9 / DPIN20 / INTP21
W8	EVCC
W9	AWOVCL
W10	REG0VCC
W11	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / RLIN22RX / TAUB0I4 / TAUB0O4 / CAN4RX / INTP4
W12	ISOVSS
W13	ISOVCL
W14	P1_15 / RLIN23TX / CAN7TX
W15	EVSS
W16	EVCC
W17	P3_7 / CAN10RX / INTP20 / PWGA86O

Table 2A.4 Pin Assignment 324-Pin FPBGA

Pin No.	Pin Name
W18	P3_10 / CAN11TX
W19	AP0_14 / ADCA0I14
W20	AP0_8 / ADCA0I8
W21	AP0_6 / ADCA0I6
W22	AP0_3 / ADCA0I3
Y1	P2_6 / ADCA0SEL2 / CSIG4RYI / CSIG4RYO
Y2	P2_12 / RLIN211RX
Y3	P2_9 / PWGA77O
Y4	P8_12 / TAUJ1I3 / TAUJ1O3 / DPIN16 / PWGA44O / CSIH1CSS5 / INTP23 / RLIN25TX / ADCA0I19S
Y5	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
Y6	P2_1 / RLIN27TX / CAN6TX
Y7	P2_13 / RLIN211TX
Y8	P3_0 / PWGA76O
Y9	FLMD0
Y10	JP0_6 / $\overline{\text{EVTO}}$
Y11	P0_8 / INTP16 / RLIN21TX / DPIN6 / CSIH0CSS6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2 / CAN3TX
Y12	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0 / CAN3RX / INTP3
Y13	P1_14 / RLIN23RX / CAN7RX / INTP9 / CSIH4RYI / CSIH4RYO
Y14	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / PWGA15O / INTP5 / CSIH1CSS3 / CAN6TX / RIIC1SCL / SENT0SPCO / ADCA0I1S
Y15	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / INTP9 / PWGA37O / ADCA0I7S
Y16	P3_1 / PWGA80O
Y17	P3_3 / CAN8RX / INTP18 / PWGA82O
Y18	P3_6 / PWGA85O / CAN9TX
Y19	P3_9 / CAN11RX / INTP21
Y20	AP0_13 / ADCA0I13
Y21	AP0_12 / ADCA0I12
Y22	AP0_7 / ADCA0I7
AA1	P2_10 / PWGA78O
AA2	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / RLIN37TX / ADCA0I4S
AA3	P8_10 / CSIH3CSS3 / DPIN14 / PWGA42O / RLIN37RX / INTP17 / ADCA0I17S
AA4	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT
AA5	P2_0 / RLIN27RX / CAN6RX / INTP6
AA6	P1_11 / ADCA1TRG2 / RLIN24TX / DPIN22 / INTP14
AA7	P2_14 / PWGA74O
AA8	IP0_0 / XT2
AA9	P2_15 / PWGA75O
AA10	P2_3 / RLIN28TX / CSIH4CSS1
AA11	P2_2 / RLIN28RX / CSIH4CSS0
AA12	P1_5 / ADCA1TRG0 / RLIN35TX / DPIN17 / INTP20 / CSIH4SC
AA13	P1_4 / RLIN35RX / INTP15 / DPIN18 / CSIH4SI
AA14	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / PWGA14O / INTP4 / CSIH0CSS0 / CAN6RX / INTP6 / RIIC1SDA / SENT0RX / ADCA0I0S
AA15	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / PWGA36O / CAN7RX / INTP9 / ADCA0I6S
AA16	P8_7 / CSIH3CSS0 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S
AA17	P3_12 / CSIH4CSS1

Table 2A.4 Pin Assignment 324-Pin FPBGA

Pin No.	Pin Name
AA18	P8_8 / CSIH3CSS1 / PWGA40O / ADCA0SEL1 / RLIN34RX / INTP14 / ADCA0I15S
AA19	P3_4 / PWGA83O / CAN8TX
AA20	P3_8 / PWGA87O / CAN10TX
AA21	AP0_11 / ADCA0I11
AA22	AP0_9 / ADCA0I9
AB1	EVSS
AB2	P8_11 / TAUJ1I2 / TAUJ1O2 / DPIN15 / PWGA43O / CSIH1CSS4 / RLIN25RX / ADCA0I18S
AB3	JP0_4 / $\overline{\text{DCUTRST}}$
AB4	JP0_0 / INTP0 / TAUJ2I0 / TAUJ2O0 / FPDR / FPDT / DCUTDI / LPDI / LPDIO
AB5	P1_10 / RLIN24RX / DPIN21 / INTP22 / ADCA1TRG1
AB6	P1_8
AB7	$\overline{\text{RESET}}$
AB8	XT1
AB9	AWOVSS
AB10	X2
AB11	X1
AB12	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / RLIN22TX / TAUB0I6 / TAUB0O6 / CAN4TX
AB13	P2_4 / RLIN29RX / ADCA0SEL0 / CSIH4SO
AB14	P2_5 / RLIN29TX / $\overline{\text{CSIH4SSI}}$ / ADCA0SEL1
AB15	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / INTP7 / PWGA23O / CAN7TX / ADCA0I5S
AB16	P3_2 / PWGA81O
AB17	P3_11 / CSIH4CSS0
AB18	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
AB19	P8_9 / CSIH3CSS2 / PWGA41O / ADCA0SEL2 / RLIN34TX / ADCA0I16S
AB20	P3_5 / CAN9RX / INTP19 / PWGA84O
AB21	AP0_15 / ADCA0I15
AB22	A0VSS

2A.2 Pin Description

Table 2A.5 Pin Functions

Pin Name	No. of Pins				IO	Pin Function	Unit
	176 Pins	233 Pins	272 Pins	324 Pins			
AnVREF	✓	✓	—	✓	—	ADCAn voltage supply and reference voltage	ADCAn
	n = 0, 1	n = 0, 1	—	n = 0, 1			
AnVSS	✓	✓	—	✓	—	ADCAn ground	
	n = 0, 1	n = 0, 1	—	n = 0, 1			
ADCA0Im	✓	✓	—	✓	I	ADCA0 input channel m with 12-bit resolution	
	m = 0 to 15	m = 0 to 15	—	m = 0 to 15			
ADCA1Im	✓	✓	—	✓	I	ADCA1 input channel m with 12-bit resolution	
	m = 0 to 15	m = 0 to 15	—	m = 0 to 15			
ADCA0ImS	✓	✓	—	✓	I	ADCA0 input channel m with 10-bit resolution	
	m = 0 to 11, 14 to 19	m = 0 to 11, 14 to 19	—	m = 0 to 11, 14 to 19			
ADCA1ImS	✓	✓	—	✓	I	ADCA1 input channel m with 10-bit resolution	
	m = 0 to 7	m = 0 to 19	—	m = 0 to 19			
ADCA0SELy	✓	✓	—	✓	O	Selection pin y for ADCA0 input and external MPX	
	y = 0 to 2	y = 0 to 2	—	y = 0 to 2			
ADCAnTRGy	✓	✓	—	✓	I	ADCAn external trigger pin y	
	n = 0, 1 y = 0 to 2	n = 0, 1 y = 0 to 2	—	n = 0, 1 y = 0 to 2			
AP0_m	✓	✓	—	✓	IO	Analog port 0_m	Port
	m = 0 to 15	m = 0 to 15	—	m = 0 to 15			
AP1_m	✓	✓	—	✓	IO	Analog port 1_m	
	m = 0 to 15	m = 0 to 15	—	m = 0 to 15			
APO	✓	✓	—	✓	O	Port output signal for analog input	LPS0
AWOVCL	✓	✓	—	✓	—	Voltage regulator for Always-On area (AWO area) capacitor connection	Power
AWOVSS	✓	✓	—	✓	—	Internal logic for Always-On area (AWO area) ground	
BVCC	✓	✓	—	✓	—	Port buffer voltage supply	
BVSS	✓	✓	—	✓	—	Port buffer ground	
CANzRX	✓	✓	—	✓	I	CANz receive data input	RCFDCn
	z = 0 to 7	z = 0 to 7	—	z = 0 to 11			
CANzTX	✓	✓	—	✓	O	CANz transmit data output	
	z = 0 to 7	z = 0 to 7	—	z = 0 to 11			
CSCXFOUT	✓	✓	—	✓	O	Clock output	Clock
CSIGnRYI	✓	✓	—	✓	I	CSIGn ready (1) / busy (0) input signal	CSIGn
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
CSIGnRYO	✓	✓	—	✓	O	CSIGn ready (1) / busy (0) output signal	
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
CSIGnSC	✓	✓	—	✓	IO	CSIGn serial clock signal	
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
CSIGnSI	✓	✓	—	✓	I	CSIGn serial data input	
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
CSIGnSO	✓	✓	—	✓	O	CSIGn serial data output	
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
$\overline{\text{CSIGnSSI}}$	✓	✓	—	✓	I	CSIGn SS function control input signal	
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
CSIHnCSS0	✓	✓	—	✓	O	CSIHn serial peripheral chip select signal 0	CSIHn
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
CSIHnCSS1	✓	✓	—	✓	O	CSIHn serial peripheral chip select signal 1	
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			

Table 2A.5 Pin Functions

Pin Name	No. of Pins				IO	Pin Function	Unit
	176 Pins	233 Pins	272 Pins	324 Pins			
CSIHnCSS2	✓	✓	—	✓	O	CSIHn serial peripheral chip select signal 2	CSIHn
	n = 0 to 3	n = 0 to 3	—	n = 0 to 3			
CSIHnCSS3	✓	✓	—	✓	O	CSIHn serial peripheral chip select signal 3	
	n = 0 to 3	n = 0 to 3	—	n = 0 to 3			
CSIHnCSS4	✓	✓	—	✓	O	CSIHn serial peripheral chip select signal 4	
	n = 0 to 2	n = 0 to 2	—	n = 0 to 2			
CSIHnCSS5	✓	✓	—	✓	O	CSIHn serial peripheral chip select signal 5	
	n = 0 to 2	n = 0 to 2	—	n = 0 to 2			
CSIHnCSS6	✓	✓	—	✓	O	CSIHn serial peripheral chip select signal 6	
	n = 0	n = 0	—	n = 0			
CSIHnCSS7	✓	✓	—	✓	O	CSIHn serial peripheral chip select signal 7	
	n = 0	n = 0	—	n = 0			
CSIHnRYI	✓	✓	—	✓	I	CSIHn ready (1) / busy (0) input signal	
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
CSIHnRYO	✓	✓	—	✓	O	CSIHn ready (1) / busy (0) output signal	
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
CSIHnSC	✓	✓	—	✓	IO	CSIHn serial clock signal	
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
CSIHnSI	✓	✓	—	✓	I	CSIHn serial data input	
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
CSIHnSO	✓	✓	—	✓	O	CSIHn serial data output	
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
$\overline{\text{CSIHnSSI}}$	✓	✓	—	✓	I	CSIHn slave select input signal	
	n = 0 to 4	n = 0 to 4	—	n = 0 to 4			
$\overline{\text{DCURDY}}$	✓	✓	—	✓	O	Debug ready	OCD
DCUTCK	✓	✓	—	✓	I	Debug clock	
DCUTDI	✓	✓	—	✓	I	Debug data input	
DCUTDO	✓	✓	—	✓	O	Debug data output	
DCUTMS	✓	✓	—	✓	I	Debug mode select	
$\overline{\text{DCUTRST}}$	✓	✓	—	✓	I	Debug reset	
DPINm	✓	✓	—	✓	I	Digital port input m	LPS0
	m = 0 to 23	m = 0 to 23	—	m = 0 to 23			
DPO	✓	✓	—	✓	O	Port output signal for digital input	
ENCA0TINm	✓	✓	—	✓	I	ENCA0 capture trigger input m	ENCAn
	m = 0, 1	m = 0, 1	—	m = 0, 1			
ENCA0E0	✓	✓	—	✓	I	ENCA0 encoder input 0	
ENCA0E1	✓	✓	—	✓	I	ENCA0 encoder input 1	
ENCA0EC	✓	✓	—	✓	I	ENCA0 encoder clear input	
ETNBnLINK	✓	✓	—	✓	I	PHY link status	ETNBn
	n = 0	n = 0	—	n = 0, 1			
ETNBnMDC	✓	✓	—	✓	O	PHY management clock	
	n = 0	n = 0	—	n = 0, 1			
ETNBnMDIO	✓	✓	—	✓	IO	Management transmit / receive data signal	
	n = 0	n = 0	—	n = 0, 1			
ETNBnRXCLK	✓	✓	—	✓	I	MII receive clock	
	n = 0	n = 0	—	n = 0, 1			
ETNBnRXD[3:0]	✓	✓	—	✓	I	MII receive data input	
	n = 0	n = 0	—	n = 0, 1			
ETNBnRXDV	✓	✓	—	✓	I	MII receive data valid	
	n = 0	n = 0	—	n = 0, 1			

Table 2A.5 Pin Functions

Pin Name	No. of Pins				IO	Pin Function	Unit
	176 Pins	233 Pins	272 Pins	324 Pins			
ETNBnRXERR	✓	✓	—	✓	I	MII receive error	ETNBn
	n = 0	n = 0	—	n = 0, 1			
ETNBnTXCLK	✓	✓	—	✓	I	MII transmit clock	
	n = 0	n = 0	—	n = 0, 1			
ETNBnTXD[3:0]	✓	✓	—	✓	O	MII transmit data output	
	n = 0	n = 0	—	n = 0, 1			
ETNBnTXEN	✓	✓	—	✓	O	MII transmit data enable	
	n = 0	n = 0	—	n = 0, 1			
EVCC	✓	✓	—	✓	—	Port buffer voltage supply	Power
EVSS	✓	✓	—	✓	—	Port buffer ground	
$\overline{\text{EVTO}}$	✓	✓	—	✓	O	Event output	TEU_OUT
FLMD0	✓	✓	—	✓	I	Operating mode select pin 0	Mode
FLMD1	✓	✓	—	✓	I	Operating mode select pin 1	
FLXA0RXDA	✓	✓	—	✓	I	FLXA0 channel A receive data input	FLXAn
FLXA0RXDB	✓	✓	—	✓	I	FLXA0 channel B receive data input	
FLXA0STPWT	✓	✓	—	✓	I	FLXA0 stop watch trigger input	
FLXA0TXDA	✓	✓	—	✓	O	FLXA0 channel A transmit data output	
FLXA0TXDB	✓	✓	—	✓	O	FLXA0 channel B transmit data output	
FLXA0TXENA	✓	✓	—	✓	O	FLXA0 channel A transmit enable	
FLXA0TXENB	✓	✓	—	✓	O	FLXA0 channel B transmit enable	
FPDR	✓	✓	—	✓	I	Serial Communication Interface RXD	FLASH
FPDT	✓	✓	—	✓	O	Serial Communication Interface TXD	
FPCK	✓	✓	—	✓	I	Serial Communication Interface clock	
INTPm	✓	✓	—	✓	I	External interrupt input m	INTC
	m = 0 to 23	m = 0 to 23	—	m = 0 to 23			
IP0_0	✓	✓	—	✓	I	Input port 0_0	Port
ISOVCL	✓	✓	—	✓	—	Voltage regulator for Isolated area (ISO area) capacitor connection	Power
ISOVSS	✓	✓	—	✓	—	Internal logic for Isolated area (ISO area) ground	
JP0_m	✓	✓	—	✓	IO	JTAG port 0_m	JTAG
	m = 0 to 6	m = 0 to 6	—	m = 0 to 6			
KR0Im	✓	✓	—	✓	I	KR0 key input signal	KRn
	m = 0 to 7	m = 0 to 7	—	m = 0 to 7			
LPDCLK	✓	✓	—	✓	I	LPD clock input (4-pin mode)	LPD
LPDCLKOUT	✓	✓	—	✓	O	LPD clock output (4-pin mode)	
LPDI	✓	✓	—	✓	I	LPD data input (4-pin mode)	
LPDIO	✓	✓	—	✓	IO	LPD data input / output (1-pin mode)	
LPDO	✓	✓	—	✓	O	LPD data output (4-pin mode)	
MEMC0Am	✓	✓	—	✓	O	MEMC0 address m	MEMCn
	m = 16 to 22	m = 16 to 22	—	m = 16 to 23			
MEMC0ADm	✓	✓	—	✓	IO	MEMC0 address / data m	
	m = 0 to 15	m = 0 to 15	—	m = 0 to 15			
$\overline{\text{MEMC0ASTB}}$	✓	✓	—	✓	O	MEMC0 address strobe	
$\overline{\text{MEMC0BENm}}$	✓	✓	—	✓	O	MEMC0 byte enable m	
	m = 0, 1	m = 0, 1	—	m = 0, 1			
MEMC0CLK	✓	✓	—	✓	O	MEMC0 clock output	
$\overline{\text{MEMC0CSm}}$	✓	✓	—	✓	O	MEMC0 chip select m	
	m = 0 to 3	m = 0 to 3	—	m = 0 to 3			
$\overline{\text{MEMC0RD}}$	✓	✓	—	✓	O	MEMC0 read strobe	
$\overline{\text{MEMC0WAIT}}$	✓	✓	—	✓	I	MEMC0 wait input	
$\overline{\text{MEMC0WR}}$	✓	✓	—	✓	O	MEMC0 write strobe	

Table 2A.5 Pin Functions

Pin Name	No. of Pins				IO	Pin Function	Unit
	176 Pins	233 Pins	272 Pins	324 Pins			
MMCA0CLK	—	—	—	✓	O	MMCA Clock	MMCAn
MMCA0CMD	—	—	—	✓	IO	MMCA Command / Response	
MMCA0DATm	—	—	—	✓	IO	MMCA Data[7:0]	
				m = 0 to 7			
MODEm	✓	✓	—	✓	I	Sub operating mode select	Mode
	m = 0 to 2	m = 0 to 2	—	m = 0 to 2			
NMI	✓	✓	—	✓	I	External non-maskable interrupt input	INTC
P0_m	✓	✓	—	✓	IO	Port 0_m	Port
	m = 0 to 14	m = 0 to 14	—	m = 0 to 14			
P1_m	✓	✓	—	✓	IO	Port 1_m	
	m = 0 to 5, 8 to 15	m = 0 to 5, 8 to 15	—	m = 0 to 5, 8 to 15			
P2_m	✓	✓	—	✓	IO	Port 2_m	
	m = 0 to 6	m = 0 to 15	—	m = 0 to 15			
P3_m	—	✓	—	✓	IO	Port3_m	
		m = 0	—	m = 0 to 12			
P8_m	✓	✓	—	✓	IO	Port 8_m	
	m = 0 to 12	m = 0 to 12	—	m = 0 to 12			
P9_m	✓	✓	—	✓	IO	Port 9_m	
	m = 0 to 4	m = 0 to 4	—	m = 0 to 4			
P10_m	✓	✓	—	✓	IO	Port 10_m	
	m = 0 to 15	m = 0 to 15	—	m = 0 to 15			
P11_m	✓	✓	—	✓	IO	Port 11_m	
	m = 0 to 12, 15	m = 0 to 12, 15	—	m = 0 to 12, 15			
P12_m	✓	✓	—	✓	IO	Port 12_m	
	m = 0 to 5	m = 0 to 5	—	m = 0 to 5			
P13_m	—	✓	—	✓	IO	Port 13_m	
		m = 0 to 7	—	m = 0 to 7			
P18_m	✓	✓	—	✓	IO	Port 18_m	
	m = 0 to 7	m = 0 to 15	—	m = 0 to 15			
P19_m	—	✓	—	✓	IO	Port19_m	
		m = 0 to 3	—	m = 0 to 3			
P20_m	✓	✓	—	✓	IO	Port 20_m	
	m = 0 to 5	m = 0 to 5	—	m = 0 to 15			
P21_m	—	—	—	✓	IO	Port21_m	
			—	m = 0 to 14			
P22_m	—	—	—	✓	IO	Port22_m	
			—	m = 0 to 15			
P23_m	—	—	—	✓	IO	Port23_m	
				m = 0 to 10			
P24_m	—	—	—	✓	IO	Port24_m	
				m = 0 to 7			
PWGAnO	✓	✓	—	✓	O	PWGAn output signal	PWGAn
	n = 0 to 71	n = 0 to 79	—	n = 0 to 95			
REGnVCC	✓	✓	—	✓	—	Voltage regulators voltage supply	Power
	n = 0, 1	n = 0, 1	—	n = 0, 1	—		
$\overline{\text{RESET}}$	✓	✓	—	✓	I	External reset input	Reset
$\overline{\text{RESETOUT}}$	✓	✓	—	✓	O	Reset output	

Table 2A.5 Pin Functions

Pin Name	No. of Pins				IO	Pin Function	Unit
	176 Pins	233 Pins	272 Pins	324 Pins			
RIICnSCL	✓	✓	—	✓	IO	RIICn serial clock	RIICn
	n = 0, 1	n = 0, 1	—	n = 0, 1			
RIICnSDA	✓	✓	—	✓	IO	RIICn serial data	
	n = 0, 1	n = 0, 1	—	n = 0, 1			
RLIN2mRX	✓	✓	—	✓	I	RLIN2m receive data input	RLIN24n
	m = 0 to 9	m = 0 to 11	—	m = 0 to 15			
RLIN2mTX	✓	✓	—	✓	O	RLIN2m transmit data output	
	m = 0 to 9	m = 0 to 11	—	m = 0 to 15			
RLIN3nRX	✓	✓	—	✓	I	RLIN3n receive data input	RLIN3n
	n = 0 to 7	n = 0 to 7	—	n = 0 to 7			
RLIN3nTX	✓	✓	—	✓	O	RLIN3n transmit data output	
	n = 0 to 7	n = 0 to 7	—	n = 0 to 7			
RTCA0OUT	✓	✓	—	✓	O	RTCA0 1Hz output	RTCAn
SELDPk	✓	✓	—	✓	O	External multiplexer select signal output k for the digital port	LPS0
	k = 0 to 2	k = 0 to 2	—	k = 0 to 2			
SENTnRX	✓	✓	—	✓	I	SENT receive data input	RSENTn
	n = 0, 1	n = 0, 1	—	n = 0, 1			
SENTnSPCO	✓	✓	—	✓	O	SENT SPC Extension Output	
	n = 0, 1	n = 0, 1	—	n = 0, 1			
SFMA0CLK	✓	✓	—	✓	O	SFMA0 clock	SFMAn
SFMA0IOm	✓	✓	—	✓	IO	SFMA0 master data input / output	
	m = 0 to 3	m = 0 to 3	—	m = 0 to 3			
SFMA0SSL	✓	✓	—	✓	O	SFMA0 slave select	
TAPA0ESO	✓	✓	—	✓	I	Hi-Z control	TAPAn
TAPA0UN	✓	✓	—	✓	O	Motor control output U phase (negative)	
TAPA0UP	✓	✓	—	✓	O	Motor control output U phase (positive)	
TAPA0VN	✓	✓	—	✓	O	Motor control output V phase (negative)	
TAPA0VP	✓	✓	—	✓	O	Motor control output V phase (positive)	
TAPA0WN	✓	✓	—	✓	O	Motor control output W phase (negative)	
TAPA0WP	✓	✓	—	✓	O	Motor control output W phase (positive)	
TAUBnIm	✓	✓	—	✓	I	TAUBn channel input m	TAUBn
	n = 0, 1 m = 0 to 15	n = 0, 1 m = 0 to 15	—	n = 0, 1 m = 0 to 15			
TAUBnOm	✓	✓	—	✓	O	TAUBn channel output m	
	n = 0, 1 m = 0 to 15	n = 0, 1 m = 0 to 15	—	n = 0, 1 m = 0 to 15			
TAUD0Im	✓	✓	—	✓	I	TAUD0 channel input m	TAUDn
	m = 0 to 15	m = 0 to 15	—	m = 0 to 15			
TAUD0Om	✓	✓	—	✓	O	TAUD0 channel output m	
	m = 0 to 15	m = 0 to 15	—	m = 0 to 15			
TAUJnIm	✓	✓	—	✓	I	TAUJn channel input m	TAUJn
	n = 0 to 3 m = 0 to 3	n = 0 to 3 m = 0 to 3	—	n = 0 to 3 m = 0 to 3			
TAUJnOm	✓	✓	—	✓	O	TAUJn channel output m	
	n = 0 to 3 m = 0 to 3	n = 0 to 3 m = 0 to 3	—	n = 0 to 3 m = 0 to 3			
X1, X2	✓	✓	—	✓	—	Main OSC connections	MOSC
XT1, XT2	✓	✓	—	✓	—	Sub OSC connections	SOSC

CAUTION

When pin functions for a peripheral module are allocated to multiple pins, use the pins from the same port group or nearby pins as the pins for a given channel.

- **(e.g.)** When RS-CANFD channel 0 is used:

  CAN0TX P0_0 P10_1
  CAN0RX P0_1 P10_0

  Use one of the following pin combinations:
  - P0_0 and P0_1, or
  - P10_0 and P10_1.

  The combinations of P0_0 and P10_0, and P0_1 and P10_1 are not allowed.

- **(e.g.)** When CSIH4 is used:

  CSIH4SC P1_5 P23_3
  CSIH4SO P2_4 P23_1
  CSIH4SI P1_4 P23_2

  Use one of the following pin combinations:
  - P1_5, P2_4 and P1_4, or
  - P23_3, 23_1 and P23_2.

  The pin combinations of the following are not allowed:
  - P1_5, P2_4 and P23_2
  - P1_5, P23_1 and P1_4
  - P23_3, P2_4 and P23_2
  - P1_5, P23_1 and P23_2
  - P23_3, P2_4 and P1_4
  - P23_3, P23_1 and P1_4.

Section 2B Pin Function of RH850/F1KM-S4, RH850/F1KM-S2

This section describes the pin and port functions.

2B.1 Pin Connection Diagram

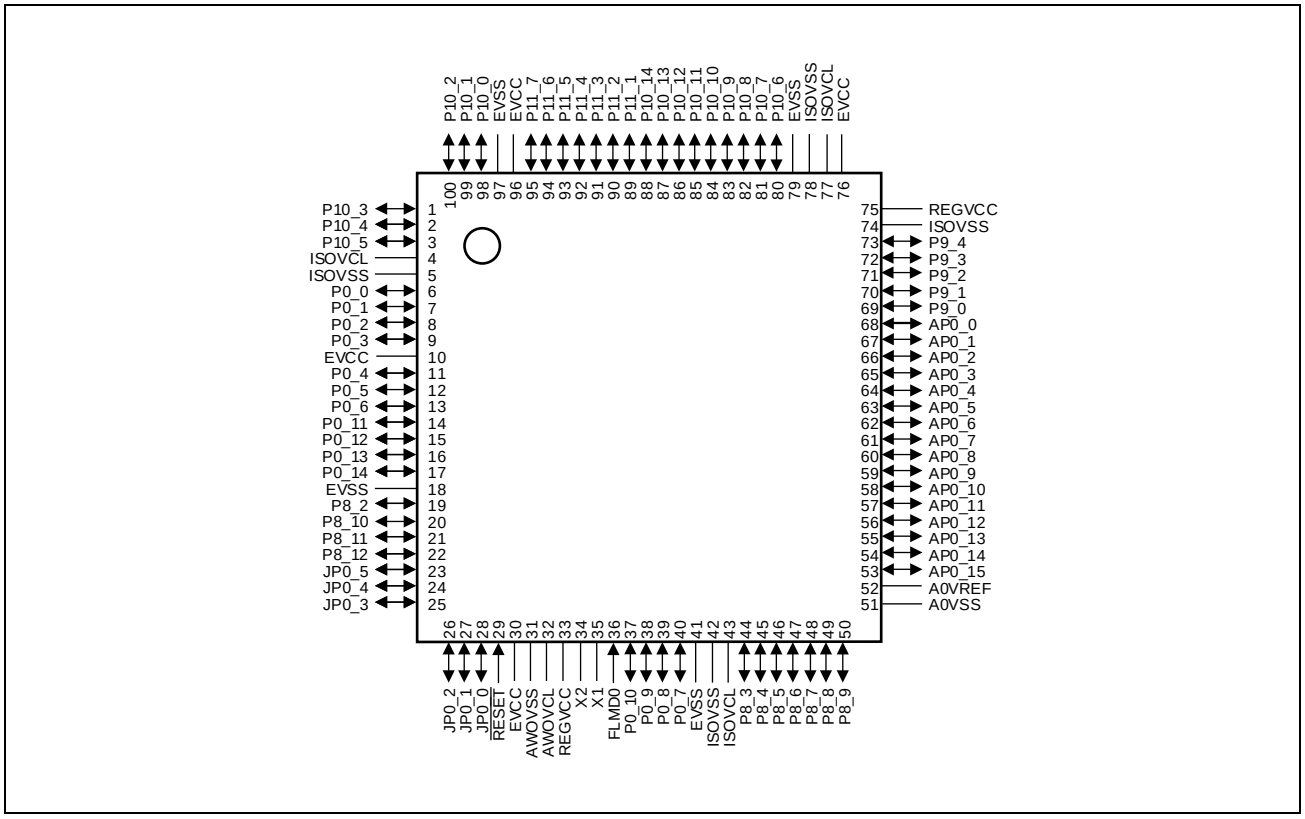


Figure 2B.1 Pin Connection Diagram in RH850/F1KM-S4 and RH850/F1KM-S2 (100-Pin LQFP)

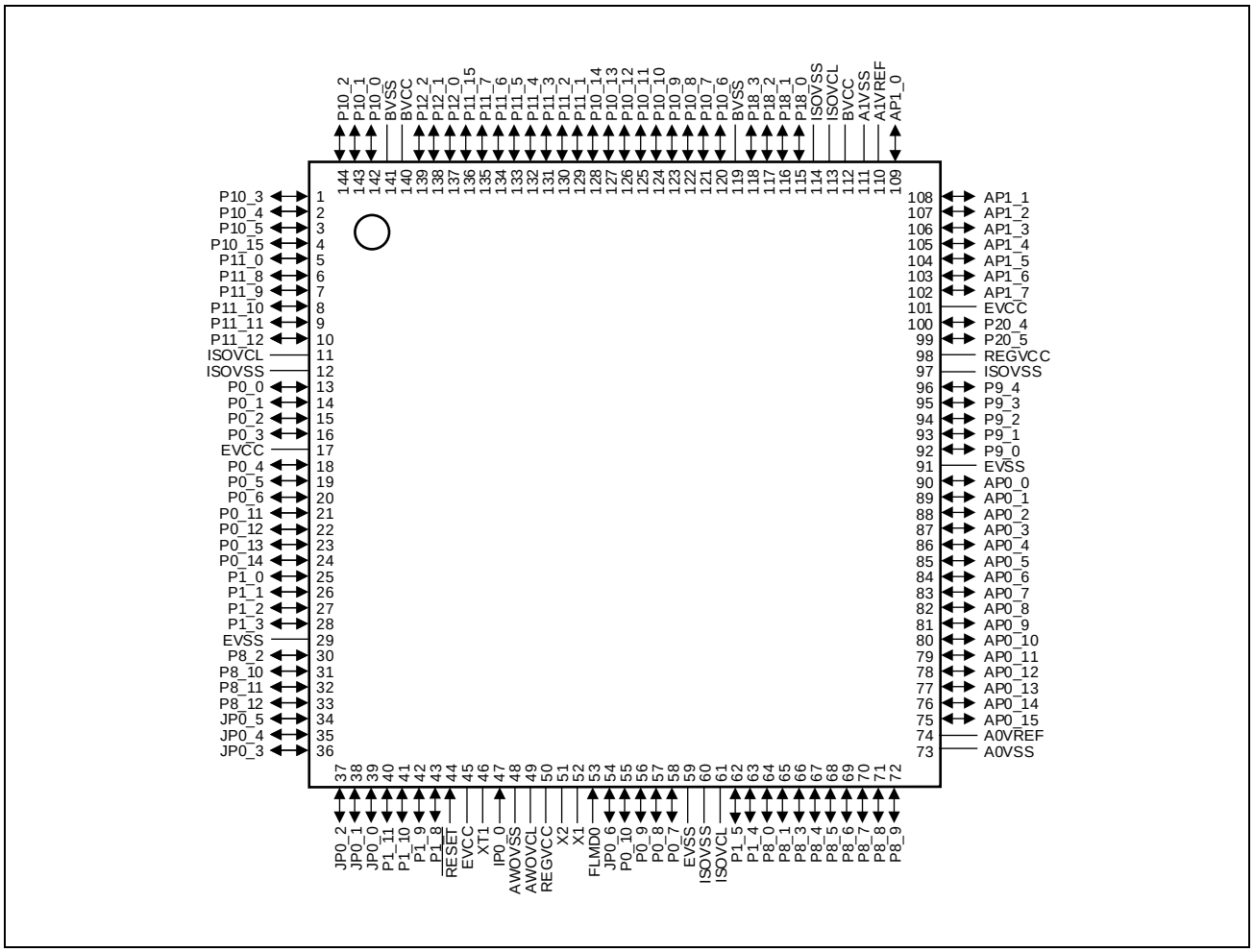


Figure 2B.2 Pin Connection Diagram in RH850/F1KM-S4 and RH850/F1KM-S2 (144-Pin LQFP)

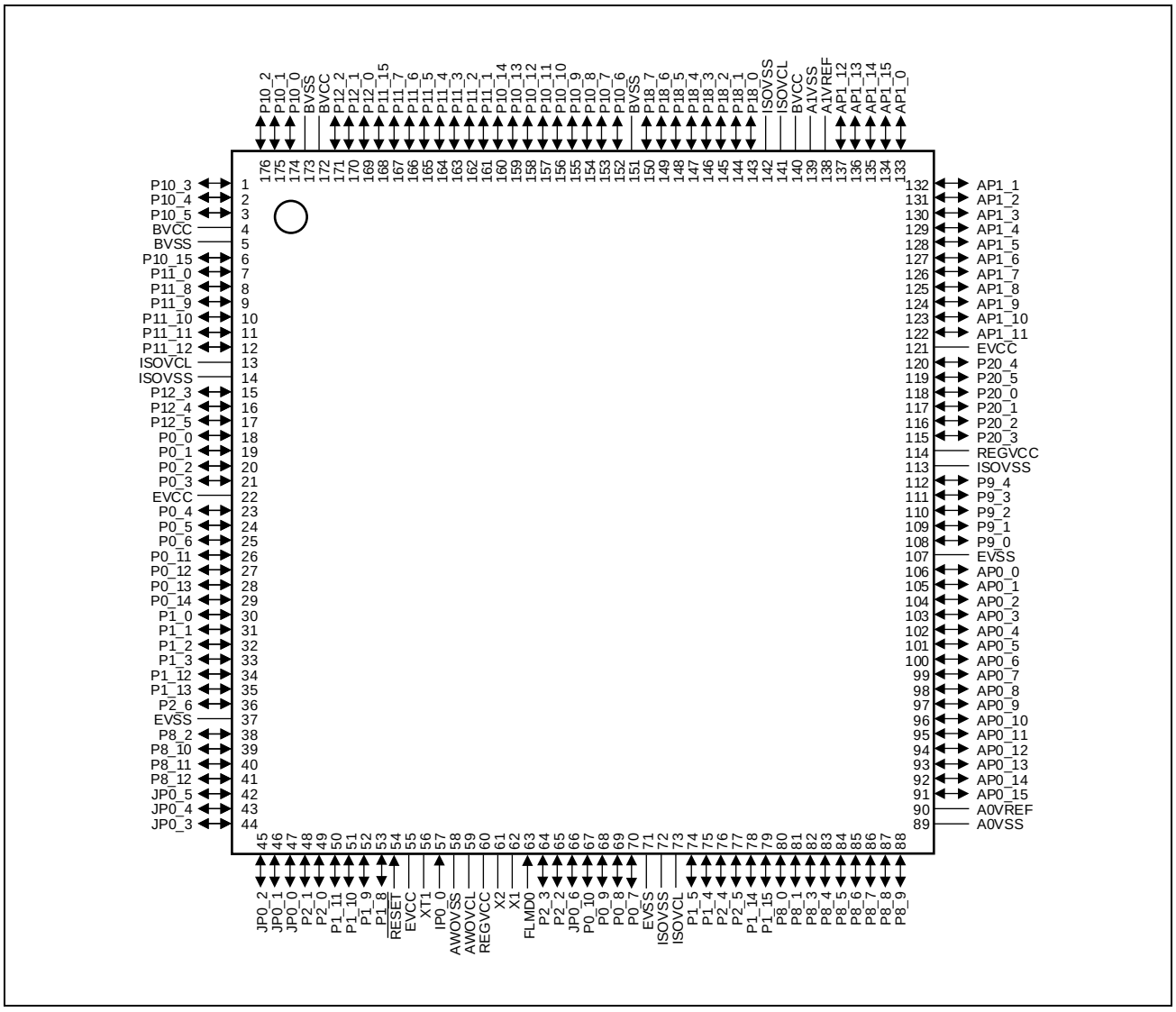
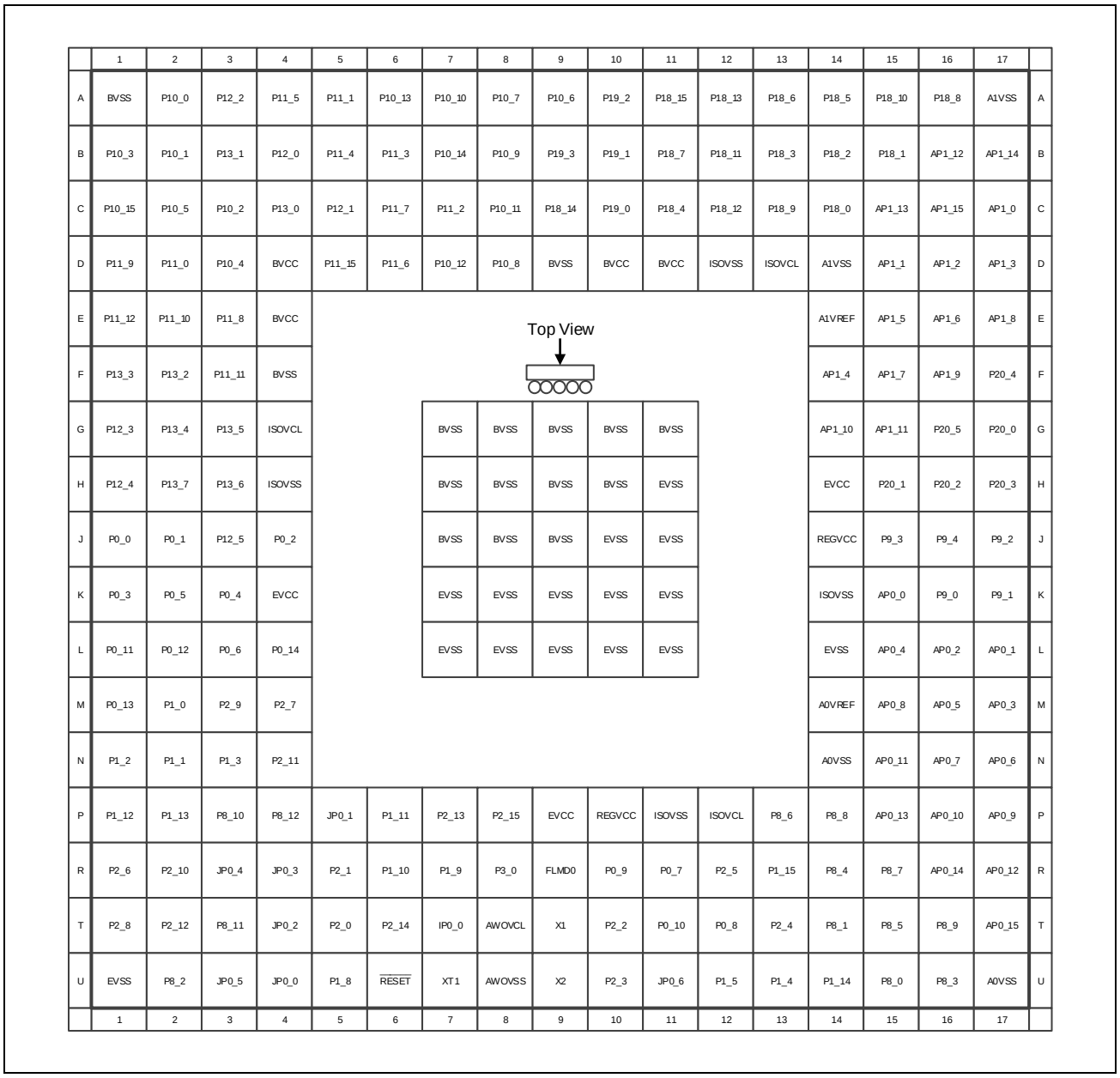
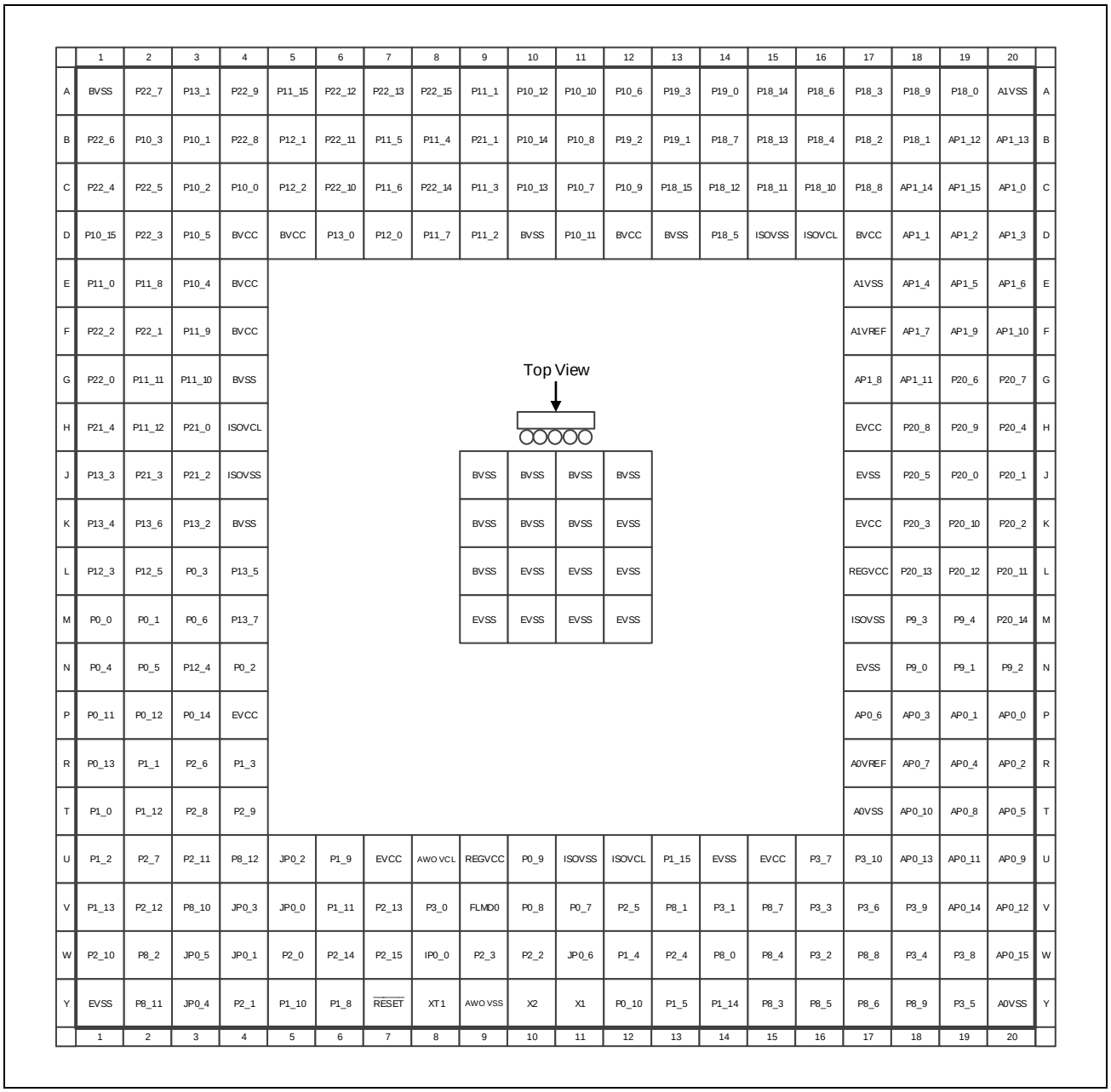


Figure 2B.3 Pin Connection Diagram in RH850/F1KM-S4 and RH850/F1KM-S2 (176-Pin LQFP)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	BVSS	P10_0	P12_2	P11_5	P11_1	P10_13	P10_10	P10_7	P10_6	P19_2	P18_15	P18_13	P18_6	P18_5	P18_10	P18_8	A1VSS	A
B	P10_3	P10_1	P13_1	P12_0	P11_4	P11_3	P10_14	P10_9	P19_3	P19_1	P18_7	P18_11	P18_3	P18_2	P18_1	AP1_12	AP1_14	B
C	P10_15	P10_5	P10_2	P13_0	P12_1	P11_7	P11_2	P10_11	P18_14	P19_0	P18_4	P18_12	P18_9	P18_0	AP1_13	AP1_15	AP1_0	C
D	P11_9	P11_0	P10_4	BVCC	P11_15	P11_6	P10_12	P10_8	BVSS	BVCC	BVCC	ISOVSS	ISOVCL	A1VSS	AP1_1	AP1_2	AP1_3	D
E	P11_12	P11_10	P11_8	BVCC										A1VREF	AP1_5	AP1_6	AP1_8	E
F	P13_3	P13_2	P11_11	BVSS										AP1_4	AP1_7	AP1_9	P20_4	F
G	P12_3	P13_4	P13_5	ISOVCL			BVSS	BVSS	BVSS	BVSS	BVSS			AP1_10	AP1_11	P20_5	P20_0	G
H	P12_4	P13_7	P13_6	ISOVSS			BVSS	BVSS	BVSS	BVSS	EVSS			EVCC	P20_1	P20_2	P20_3	H
J	P0_0	P0_1	P12_5	P0_2			BVSS	BVSS	BVSS	EVSS	EVSS			REGVCC	P9_3	P9_4	P9_2	J
K	P0_3	P0_5	P0_4	EVCC			EVSS	EVSS	EVSS	EVSS	EVSS			ISOVSS	AP0_0	P9_0	P9_1	K
L	P0_11	P0_12	P0_6	P0_14			EVSS	EVSS	EVSS	EVSS	EVSS			EVSS	AP0_4	AP0_2	AP0_1	L
M	P0_13	P1_0	P2_9	P2_7										A0VREF	AP0_8	AP0_5	AP0_3	M
N	P1_2	P1_1	P1_3	P2_11										A0VSS	AP0_11	AP0_7	AP0_6	N
P	P1_12	P1_13	P8_10	P8_12	JP0_1	P1_11	P2_13	P2_15	EVCC	REGVCC	ISOVSS	ISOVCL	P8_6	P8_8	AP0_13	AP0_10	AP0_9	P
R	P2_6	P2_10	JP0_4	JP0_3	P2_1	P1_10	P1_9	P3_0	FLMD0	P0_9	P0_7	P2_5	P1_15	P8_4	P8_7	AP0_14	AP0_12	R
T	P2_8	P2_12	P8_11	JP0_2	P2_0	P2_14	IP0_0	AWOVCL	X1	P2_2	P0_10	P0_8	P2_4	P8_1	P8_5	P8_9	AP0_15	T
U	EVSS	P8_2	JP0_5	JP0_0	P1_8	$\overline{\text{RESET}}$	XT1	AWOVSS	X2	P2_3	JP0_6	P1_5	P1_4	P1_14	P8_0	P8_3	A0VSS	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 2B.4 Pin Connection Diagram in RH850/F1KM-S4 (233-Pin FPBGA)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	BVSS	P22_7	P13_1	P22_9	P11_15	P22_12	P22_13	P22_15	P11_1	P10_12	P10_10	P10_6	P19_3	P19_0	P18_14	P18_6	P18_3	P18_9	P18_0	A1VSS	A
B	P22_6	P10_3	P10_1	P22_8	P12_1	P22_11	P11_5	P11_4	P21_1	P10_14	P10_8	P19_2	P19_1	P18_7	P18_13	P18_4	P18_2	P18_1	AP1_12	AP1_13	B
C	P22_4	P22_5	P10_2	P10_0	P12_2	P22_10	P11_6	P22_14	P11_3	P10_13	P10_7	P10_9	P18_15	P18_12	P18_11	P18_10	P18_8	AP1_14	AP1_15	AP1_0	C
D	P10_15	P22_3	P10_5	BVCC	BVCC	P13_0	P12_0	P11_7	P11_2	BVSS	P10_11	BVCC	BVSS	P18_5	ISOVSS	ISOVCL	BVCC	AP1_1	AP1_2	AP1_3	D
E	P11_0	P11_8	P10_4	BVCC													A1VSS	AP1_4	AP1_5	AP1_6	E
F	P22_2	P22_1	P11_9	BVCC													A1VREF	AP1_7	AP1_9	AP1_10	F
G	P22_0	P11_11	P11_10	BVSS													AP1_8	AP1_11	P20_6	P20_7	G
H	P21_4	P11_12	P21_0	ISOVCL													EVCC	P20_8	P20_9	P20_4	H
J	P13_3	P21_3	P21_2	ISOVSS					BVSS	BVSS	BVSS	BVSS					EVSS	P20_5	P20_0	P20_1	J
K	P13_4	P13_6	P13_2	BVSS					BVSS	BVSS	BVSS	EVSS					EVCC	P20_3	P20_10	P20_2	K
L	P12_3	P12_5	P0_3	P13_5					BVSS	EVSS	EVSS	EVSS					REGVCC	P20_13	P20_12	P20_11	L
M	P0_0	P0_1	P0_6	P13_7					EVSS	EVSS	EVSS	EVSS					ISOVSS	P9_3	P9_4	P20_14	M
N	P0_4	P0_5	P12_4	P0_2													EVSS	P9_0	P9_1	P9_2	N
P	P0_11	P0_12	P0_14	EVCC													AP0_6	AP0_3	AP0_1	AP0_0	P
R	P0_13	P1_1	P2_6	P1_3													A0VREF	AP0_7	AP0_4	AP0_2	R
T	P1_0	P1_12	P2_8	P2_9													A0VSS	AP0_10	AP0_8	AP0_5	T
U	P1_2	P2_7	P2_11	P8_12	JP0_2	P1_9	EVCC	AWOVCL	REGVCC	P0_9	ISOVSS	ISOVCL	P1_15	EVSS	EVCC	P3_7	P3_10	AP0_13	AP0_11	AP0_9	U
V	P1_13	P2_12	P8_10	JP0_3	JP0_0	P1_11	P2_13	P3_0	FLMD0	P0_8	P0_7	P2_5	P8_1	P3_1	P8_7	P3_3	P3_6	P3_9	AP0_14	AP0_12	V
W	P2_10	P8_2	JP0_5	JP0_1	P2_0	P2_14	P2_15	IP0_0	P2_3	P2_2	JP0_6	P1_4	P2_4	P8_0	P8_4	P3_2	P8_8	P3_4	P3_8	AP0_15	W
Y	EVSS	P8_11	JP0_4	P2_1	P1_10	P1_8	$\overline{\text{RESET}}$	XT1	AWOVSS	X2	X1	P0_10	P1_5	P1_14	P8_3	P8_5	P8_6	P8_9	P3_5	A0VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 2B.5 Pin Connection Diagram in RH850/F1KM-S4 (272-Pin FPBGA)

Table 2B.1 Pin Assignment 100-Pin LQFP (RH850/F1KM-S4)

Pin No.	Pin Name
1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / $\overline{\text{CSIH1SSI}}$ / TAPA0VN
2	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / CAN6TX / KR0I2 / ADCA0TRG2 / $\overline{\text{CSIG0SSI}}$ / ADCA0SEL0 / TAPA0WP
3	P10_5 / TAUD0I11 / TAUD0O11 / CAN6RX / INTP6 / RLIN21TX / KR0I3 / CSIG0RYI / CSIG0RYO / ADCA0SEL1 / TAPA0WN
4	ISOVCL
5	ISOVSS
6	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
7	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
8	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
9	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
10	EVCC
11	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 / DPIN8 / TAUB0I12 / TAUB0O12
12	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
13	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
14	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / PWGA34O
15	P0_12 / RIIC0SCL / DPIN13 / PWGA45O / TAUB0I10 / TAUB0O10 / CSIG0SI
16	P0_13 / INTP12 / PWGA46O / TAUB0I12 / TAUB0O12 / CSIG0SO / CAN5RX / INTP5 / RLIN32RX
17	P0_14 / PWGA47O / TAUB0I14 / TAUB0O14 / CSIG0SC / CAN5TX / RLIN32TX
18	EVSS
19	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / ADCA0I4S
20	P8_10 / DPIN14 / PWGA42O / ADCA0I17S / CSIH3CSS3
21	P8_11 / TAUJ1I2 / TAUJ1O2 / DPIN15 / PWGA43O / ADCA0I18S / CSIH1CSS4
22	P8_12 / TAUJ1I3 / TAUJ1O3 / DPIN16 / PWGA44O / ADCA0I19S / CSIH1CSS5
23	JP0_5 / NMI / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT / RTCA0OUT
24	JP0_4 / $\overline{\text{DCUTRST}}$
25	JP0_3 / INTP3 / TAUJ0I2 / TAUJ0O2 / DCUTMS / CSCXFOUT
26	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
27	JP0_1 / INTP1 / TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
28	JP0_0 / INTP0 / FPDR / FPDT / DCUTDI / LPDI/ LPDIO / TAUJ2I0 / TAUJ2O0
29	$\overline{\text{RESET}}$
30	EVCC
31	AWOVSS
32	AWOVCL
33	REGVCC
34	X2
35	X1
36	FLMD0
37	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / RLIN22TX / TAUB0I6 / TAUB0O6 / CAN4TX
38	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / RLIN22RX / TAUB0I4 / TAUB0O4 / CAN4RX / INTP4
39	P0_8 / RLIN21TX / DPIN6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2 / CAN3TX / CSIH0CSS6
40	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0 / CAN3RX / INTP3
41	EVSS
42	ISOVSS
43	ISOVCL

Table 2B.1 Pin Assignment 100-Pin LQFP (RH850/F1KM-S4)

Pin No.	Pin Name
44	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / INTP7 / PWGA23O / CAN7TX / ADCA0I5S
45	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / PWGA36O / CAN7RX / INTP9 / ADCA0I6S
46	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / PWGA37O / ADCA0I7S / INTP9
47	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
48	P8_7 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S / CSIH3CSS0
49	P8_8 / PWGA40O / ADCA0SEL1 / ADCA0I15S / CSIH3CSS1
50	P8_9 / PWGA41O / ADCA0SEL2 / ADCA0I16S / CSIH3CSS2
51	A0VSS
52	A0VREF
53	AP0_15 / ADCA0I15
54	AP0_14 / ADCA0I14
55	AP0_13 / ADCA0I13
56	AP0_12 / ADCA0I12
57	AP0_11 / ADCA0I11
58	AP0_10 / ADCA0I10
59	AP0_9 / ADCA0I9
60	AP0_8 / ADCA0I8
61	AP0_7 / ADCA0I7
62	AP0_6 / ADCA0I6
63	AP0_5 / ADCA0I5
64	AP0_4 / ADCA0I4
65	AP0_3 / ADCA0I3
66	AP0_2 / ADCA0I2
67	AP0_1 / ADCA0I1
68	AP0_0 / ADCA0I0
69	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / TAUJ1I1 / TAUJ1O1 / SENT1RX / RIIC1SDA / ADCA0I2S
70	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / RIIC1SCL / ADCA0I3S
71	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S
72	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / ADCA0I10S
73	P9_4 / CSIH0CSS5 / PWGA33O / TAUJ1I0 / TAUJ1O0 / ADCA0I11S
74	ISOVSS
75	REGVCC
76	EVCC
77	ISOVCL
78	ISOVSS
79	EVSS
80	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX / INTP1 / MODE2
81	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / TAUJ3I1 / TAUJ3O1
82	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / FLXA0TXDB / ENCA0EC / PWGA5O / TAUJ3I2 / TAUJ3O2 / FLMD1
83	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO / FLXA0RXDB
84	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / TAUJ3I3 / TAUJ3O3
85	P10_11 / PWGA16O / RLIN31RX / INTP11 / FLXA0TXENA / CSIH1CSS0 / TAUB0I1 / TAUB0O1
86	P10_12 / PWGA17O / FLXA0STPWT / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3

Table 2B.1 Pin Assignment 100-Pin LQFP (RH850/F1KM-S4)

Pin No.	Pin Name
87	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / INTP12 / FLXA0TXENB / TAUB0I5 / TAUB0O5 / CAN7TX / RLIN32RX
88	P10_14 / PWGA19O / FLXA0RXDA / TAUB0I7 / TAUB0O7 / CAN7RX / INTP9 / RLIN32TX / $\overline{\text{CSIH3SSI}}$
89	P11_1 / $\overline{\text{CSIH2SSI}}$ / FLXA0TXDA / RLIN20RX / PWGA26O / TAUB0I13 / TAUB0O13 / CSIH0CSS7
90	P11_2 / CSIH2SO / INTP12 / RLIN20TX / PWGA27O / TAUB0I15 / TAUB0O15 / RLIN32RX
91	P11_3 / CSIH2SC / CAN3RX / INTP3 / PWGA28O / RLIN32TX
92	P11_4 / CSIH2SI / CAN3TX / PWGA29O
93	P11_5 / CAN5RX / INTP5 / PWGA30O / CSIH3SI
94	P11_6 / INTP13 / CAN5TX / PWGA31O / CSIH3SO
95	P11_7 / INTP5 / PWGA32O / CSIH3SC
96	EVCC
97	EVSS
98	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX / INTP0 / PWGA0O / CSIH1SI / CSCXFOUT / TAUJ1I3 / TAUJ1O3 / TAPA0UP
99	P10_1 / TAUD0I3 / TAUD0O3 / CAN0TX / PWGA1O / CSIH1SC / MODE0 / TAUJ3I0 / TAUJ3O0 / TAPA0UN
100	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / CSIH1SO / MODE1 / TAPA0VP

Table 2B.2 Pin Assignment 100-Pin LQFP (RH850/F1KM-S2)

Pin No.	Pin Name
1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / $\overline{\text{CSIH1SSI}}$ / TAPA0VN
2	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / CAN6TX / KR0I2 / ADCA0TRG2 / $\overline{\text{CSIG0SSI}}$ / ADCA0SEL0 / TAPA0WP
3	P10_5 / TAUD0I11 / TAUD0O11 / CAN6RX / INTP6 / RLIN21TX / KR0I3 / CSIG0RYI / CSIG0RYO / ADCA0SEL1 / TAPA0WN
4	ISOVCL
5	ISOVSS
6	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
7	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
8	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
9	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
10	EVCC
11	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 / DPIN8 / TAUB0I12 / TAUB0O12
12	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
13	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
14	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / PWGA34O
15	P0_12 / RIIC0SCL / DPIN13 / PWGA45O / TAUB0I10 / TAUB0O10 / CSIG0SI
16	P0_13 / INTP12 / PWGA46O / TAUB0I12 / TAUB0O12 / CSIG0SO / CAN5RX / INTP5 / RLIN32RX
17	P0_14 / PWGA47O / TAUB0I14 / TAUB0O14 / CSIG0SC / CAN5TX / RLIN32TX
18	EVSS
19	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / ADCA0I4S
20	P8_10 / DPIN14 / PWGA42O / ADCA0I17S / CSIH3CSS3
21	P8_11 / TAUJ1I2 / TAUJ1O2 / DPIN15 / PWGA43O / ADCA0I18S / CSIH1CSS4
22	P8_12 / TAUJ1I3 / TAUJ1O3 / DPIN16 / PWGA44O / ADCA0I19S / CSIH1CSS5
23	JP0_5 / NMI / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT / RTCA0OUT
24	JP0_4 / $\overline{\text{DCUTRST}}$
25	JP0_3 / INTP3 / TAUJ0I2 / TAUJ0O2 / DCUTMS / CSCXFOUT
26	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
27	JP0_1 / INTP1 / TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
28	JP0_0 / INTP0 / FPDR / FPDT / DCUTDI / LPDI/ LPDIO / TAUJ2I0 / TAUJ2O0
29	$\overline{\text{RESET}}$
30	EVCC
31	AWOVSS
32	AWOVCL
33	REGVCC
34	X2
35	X1
36	FLMD0
37	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / RLIN22TX / TAUB0I6 / TAUB0O6 / CAN4TX
38	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / RLIN22RX / TAUB0I4 / TAUB0O4 / CAN4RX / INTP4
39	P0_8 / RLIN21TX / DPIN6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2 / CAN3TX / CSIH0CSS6
40	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0 / CAN3RX / INTP3
41	EVSS
42	ISOVSS
43	ISOVCL

Table 2B.2 Pin Assignment 100-Pin LQFP (RH850/F1KM-S2)

Pin No.	Pin Name
44	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / INTP7 / PWGA23O / CAN7TX / ADCA0I5S
45	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / PWGA36O / CAN7RX / INTP9 / ADCA0I6S
46	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / PWGA37O / ADCA0I7S / INTP9
47	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
48	P8_7 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S / CSIH3CSS0
49	P8_8 / PWGA40O / ADCA0SEL1 / ADCA0I15S / CSIH3CSS1
50	P8_9 / PWGA41O / ADCA0SEL2 / ADCA0I16S / CSIH3CSS2
51	A0VSS
52	A0VREF
53	AP0_15 / ADCA0I15
54	AP0_14 / ADCA0I14
55	AP0_13 / ADCA0I13
56	AP0_12 / ADCA0I12
57	AP0_11 / ADCA0I11
58	AP0_10 / ADCA0I10
59	AP0_9 / ADCA0I9
60	AP0_8 / ADCA0I8
61	AP0_7 / ADCA0I7
62	AP0_6 / ADCA0I6
63	AP0_5 / ADCA0I5
64	AP0_4 / ADCA0I4
65	AP0_3 / ADCA0I3
66	AP0_2 / ADCA0I2
67	AP0_1 / ADCA0I1
68	AP0_0 / ADCA0I0
69	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / TAUJ1I1 / TAUJ1O1 / SENT1RX / RIIC1SDA / ADCA0I2S
70	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / RIIC1SCL / ADCA0I3S
71	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S
72	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / ADCA0I10S
73	P9_4 / CSIH0CSS5 / PWGA33O / TAUJ1I0 / TAUJ1O0 / ADCA0I11S
74	ISOVSS
75	REGVCC
76	EVCC
77	ISOVCL
78	ISOVSS
79	EVSS
80	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX / INTP1 / MODE2
81	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / TAUJ3I1 / TAUJ3O1
82	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / ENCA0EC / PWGA5O / TAUJ3I2 / TAUJ3O2 / FLMD1
83	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO
84	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / TAUJ3I3 / TAUJ3O3
85	P10_11 / PWGA16O / RLIN31RX / INTP11 / CSIH1CSS0 / TAUB0I1 / TAUB0O1
86	P10_12 / PWGA17O / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3

Table 2B.2 Pin Assignment 100-Pin LQFP (RH850/F1KM-S2)

Pin No.	Pin Name
87	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / INTP12 / TAUB0I5 / TAUB0O5 / CAN7TX / RLIN32RX
88	P10_14 / PWGA19O / TAUB0I7 / TAUB0O7 / CAN7RX / INTP9 / RLIN32TX / $\overline{\text{CSIH3SSI}}$
89	P11_1 / $\overline{\text{CSIH2SSI}}$ / RLIN20RX / PWGA26O / TAUB0I13 / TAUB0O13 / CSIH0CSS7
90	P11_2 / CSIH2SO / INTP12 / RLIN20TX / PWGA27O / TAUB0I15 / TAUB0O15 / RLIN32RX
91	P11_3 / CSIH2SC / CAN3RX / INTP3 / PWGA28O / RLIN32TX
92	P11_4 / CSIH2SI / CAN3TX / PWGA29O
93	P11_5 / CAN5RX / INTP5 / PWGA30O / CSIH3SI
94	P11_6 / INTP13 / CAN5TX / PWGA31O / CSIH3SO
95	P11_7 / INTP5 / PWGA32O / CSIH3SC
96	EVCC
97	EVSS
98	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX / INTP0 / PWGA0O / CSIH1SI / CSCXFOUT / TAUJ1I3 / TAUJ1O3 / TAPA0UP
99	P10_1 / TAUD0I3 / TAUD0O3 / CAN0TX / PWGA1O / CSIH1SC / MODE0 / TAUJ3I0 / TAUJ3O0 / TAPA0UN
100	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / CSIH1SO / MODE1 / TAPA0VP

Table 2B.3 Pin Assignment 144-Pin LQFP (RH850/F1KM-S4)

Pin No.	Pin Name
1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN / $\overline{\text{CSIH1SSI}}$
2	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / CAN6TX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$ / PWGA53O
3	P10_5 / TAUD0I11 / TAUD0O11 / CAN6RX / INTP6 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO / PWGA54O
4	P10_15 / CSIH3RYI / CSIH3RYO / PWGA24O / RLIN22RX / TAUB0I9 / TAUB0O9
5	P11_0 / CSIH2RYI / CSIH2RYO / ADCA1TRG2 / PWGA25O / RLIN22TX / TAUB0I11 / TAUB0O11
6	P11_8 / $\overline{\text{CSIG1SSI}}$ / RLIN35TX / PWGA48O
7	P11_9 / CSIG1SO / RLIN35RX / INTP15 / PWGA49O
8	P11_10 / CSIG1SC / PWGA50O
9	P11_11 / CSIG1SI / RLIN25TX / PWGA51O
10	P11_12 / RLIN25RX / PWGA52O
11	ISOVCL
12	ISOVSS
13	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
14	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
15	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
16	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
17	EVCC
18	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 /DPIN8 / TAUB0I12 / TAUB0O12
19	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
20	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
21	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / PWGA34O
22	P0_12 / RIIC0SCL / DPIN13 / PWGA45O / TAUB0I10 / TAUB0O10 / CSIG0SI
23	P0_13 / RLIN32RX / INTP12 / PWGA46O / TAUB0I12 / TAUB0O12 / CSIG0SO / CAN5RX / INTP5
24	P0_14 / INTP17 / RLIN32TX / PWGA47O / TAUB0I14 / TAUB0O14 / CSIG0SC / CAN5TX
25	P1_0 / RLIN33RX / INTP13 / TAUJ2I0 / TAUJ2O0
26	P1_1 / INTP18 / RLIN33TX / TAUJ2I1 / TAUJ2O1
27	P1_2 / CAN3RX / INTP3 / DPIN19 / TAUJ2I2 / TAUJ2O2
28	P1_3 / INTP19 / CAN3TX / DPIN23 / TAUJ2I3 / TAUJ2O3
29	EVSS
30	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / ADCA0I4S
31	P8_10 / CSIH3CSS3 / DPIN14 / PWGA42O / ADCA0I17S
32	P8_11 / TAUJ1I2 / TAUJ1O2 / DPIN15 / PWGA43O / CSIH1CSS4 / RLIN25RX / ADCA0I18S
33	P8_12 / TAUJ1I3 / TAUJ1O3 / DPIN16 / PWGA44O / CSIH1CSS5 / INTP23 / RLIN25TX / ADCA0I19S
34	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT
35	JP0_4 / $\overline{\text{DCUTRST}}$
36	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
37	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
38	JP0_1 / INTP1 /TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
39	JP0_0 / INTP0 / FPDR / FPDT / DCUTDI / LPDI / LPDIO / TAUJ2I0 / TAUJ2O0
40	P1_11 / ADCA1TRG2 / RLIN24TX / DPIN22 / INTP14
41	P1_10 / RLIN24RX / DPIN21 / INTP22 / ADCA1TRG1
42	P1_9 / DPIN20 / INTP21

Table 2B.3 Pin Assignment 144-Pin LQFP (RH850/F1KM-S4)

Pin No.	Pin Name
43	P1_8
44	$\overline{\text{RESET}}$
45	EVCC
46	XT1
47	IP0_0 / XT2
48	AWOVSS
49	AWOVCL
50	REGVCC
51	X2
52	X1
53	FLMD0
54	JP0_6 / $\overline{\text{EVTO}}$
55	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / RLIN22TX / TAUB0I6 / TAUB0O6 / CAN4TX
56	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / RLIN22RX / TAUB0I4 / TAUB0O4 / CAN4RX / INTP4
57	P0_8/ INTP16 / RLIN21TX / DPIN6 / CSIH0CSS6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2 / CAN3TX
58	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0 / CAN3RX / INTP3
59	EVSS
60	ISOVSS
61	ISOVCL
62	P1_5 / ADCA1TRG0 / RLIN35TX / DPIN17 / INTP20
63	P1_4 / RLIN35RX / INTP15 / DPIN18
64	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / PWGA14O / INTP4 / CSIH0CSS0 / CAN6RX / INTP6 / ADCA0I0S / RIIC1SDA / SENT0RX
65	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / PWGA15O / INTP5 / CSIH1CSS3 / CAN6TX / ADCA0I1S / RIIC1SCL / SENT0SPCO
66	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / INTP7 / PWGA23O / CAN7TX / ADCA0I5S
67	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / PWGA36O / CAN7RX / INTP9 / ADCA0I6S
68	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / INTP9 / PWGA37O / ADCA0I7S
69	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
70	P8_7 / CSIH3CSS0 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S
71	P8_8 / CSIH3CSS1 / PWGA40O / ADCA0SEL1 / RLIN34RX / INTP14 / ADCA0I15S
72	P8_9 / CSIH3CSS2 / PWGA41O / ADCA0SEL2 / RLIN34TX / ADCA0I16S
73	A0VSS
74	A0VREF
75	AP0_15 / ADCA0I15
76	AP0_14 / ADCA0I14
77	AP0_13 / ADCA0I13
78	AP0_12 / ADCA0I12
79	AP0_11 / ADCA0I11
80	AP0_10 / ADCA0I10
81	AP0_9 / ADCA0I9
82	AP0_8 / ADCA0I8
83	AP0_7 / ADCA0I7
84	AP0_6 / ADCA0I6
85	AP0_5 / ADCA0I5
86	AP0_4 / ADCA0I4

Table 2B.3 Pin Assignment 144-Pin LQFP (RH850/F1KM-S4)

Pin No.	Pin Name
87	AP0_3 / ADCA0I3
88	AP0_2 / ADCA0I2
89	AP0_1 / ADCA0I1
90	AP0_0 / ADCA0I0
91	EVSS
92	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / ADCA0I2S / TAUJ1I1 / TAUJ1O1 / SENT1RX / RIIC1SDA
93	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / ADCA0I3S / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / RIIC1SCL
94	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S
95	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / INTP16 / ADCA0I10S
96	P9_4 / CSIH0CSS5 / PWGA33O / TAUJ1I0 / TAUJ1O0 / INTP17 / ADCA0I11S
97	ISOVSS
98	REGVCC
99	P20_5 / RLIN23TX / INTP23 / PWGA60O / CAN7TX
100	P20_4 / RLIN23RX / INTP22 / PWGA59O / CAN7RX / INTP9
101	EVCC
102	AP1_7 / ADCA1I7
103	AP1_6 / ADCA1I6
104	AP1_5 / ADCA1I5
105	AP1_4 / ADCA1I4
106	AP1_3 / ADCA1I3
107	AP1_2 / ADCA1I2
108	AP1_1 / ADCA1I1
109	AP1_0 / ADCA1I0
110	A1VREF
111	A1VSS
112	BVCC
113	ISOVCL
114	ISOVSS
115	P18_0 / CSIG1RYI / CSIG1RYO / PWGA61O / ADCA1I0S / TAUJ3I0 / TAUJ3O0
116	P18_1 / PWGA62O / ADCA1I1S / TAUJ3I1 / TAUJ3O1
117	P18_2 / PWGA63O / ADCA1I2S / TAUJ3I2 / TAUJ3O2
118	P18_3 / ADCA1I3S / TAUJ3I3 / TAUJ3O3
119	BVSS
120	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX /INTP1 / RLIN24RX / MODE2
121	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / RLIN24TX / TAUJ3I1 / TAUJ3O1
122	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / FLXA0TXDB / ENCA0EC / PWGA5O / FLMD1 / TAUJ3I2 / TAUJ3O2
123	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO / FLXA0RXDB
124	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / TAUJ3I3 / TAUJ3O3
125	P10_11 / PWGA16O / RLIN31RX / INTP11 / FLXA0TXENA / CSIH1CSS0 / TAUB0I1 / TAUB0O1
126	P10_12 / PWGA17O / FLXA0STPWT / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3
127	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / RLIN32RX / INTP12 / FLXA0TXENB / TAUB0I5 / TAUB0O5 / CAN7TX
128	P10_14 / ADCA1TRG0 / PWGA19O / FLXA0RXDA / RLIN32TX / $\overline{\text{CSIH3SSI}}$ / TAUB0I7 / TAUB0O7 / CAN7RX / INTP9

Table 2B.3 Pin Assignment 144-Pin LQFP (RH850/F1KM-S4)

Pin No.	Pin Name
129	P11_1 / $\overline{\text{CSIH2SSI}}$ / FLXA0TXDA / RLIN20RX / CSIH0CSS7 / INTP20 / PWGA26O / TAUB0I13 / TAUB0O13
130	P11_2 / CSIH2SO / RLIN32RX / INTP12 / RLIN20TX / PWGA27O / TAUB0I15 / TAUB0O15 / SFMA0IO3
131	P11_3 / CSIH2SC / CAN3RX / INTP3 / PWGA28O / RLIN32TX / SFMA0IO2
132	P11_4 / CSIH2SI / CAN3TX / INTP21 / PWGA29O / SFMA0IO1
133	P11_5 / CAN5RX / INTP5 / RLIN33TX / PWGA30O / CSIH3SI / SFMA0IO0
134	P11_6 / RLIN33RX / INTP13 / CAN5TX / ADCA1TRG1 / PWGA31O / CSIH3SO / SFMA0SSL
135	P11_7 / INTP5 / PWGA32O / CSIH3SC / SFMA0CLK
136	P11_15 / CAN2RX / INTP2 / CSIH2CSS4 / PWGA55O
137	P12_0 / CAN2TX / PWGA56O
138	P12_1 / RLIN34RX / INTP14 / CSIH2CSS5 / PWGA57O
139	P12_2 / INTP19 / RLIN34TX / PWGA58O
140	BVCC
141	BVSS
142	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX /INTP0 / CSCXFOUT / PWGA0O / TAPA0UP / CSIH1SI / TAUJ1I3 / TAUJ1O3
143	P10_1 / TAUD0I3 / TAUD0O3 / INTP18 / CAN0TX / PWGA1O / TAPA0UN / CSIH1SC / MODE0 / TAUJ3I0 / TAUJ3O0
144	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP / CSIH1SO / MODE1

Table 2B.4 Pin Assignment 144-Pin LQFP (RH850/F1KM-S2)

Pin No.	Pin Name
1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN / $\overline{\text{CSIH1SSI}}$
2	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / CAN6TX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$ / PWGA53O
3	P10_5 / TAUD0I11 / TAUD0O11 / CAN6RX / INTP6 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO / PWGA54O
4	P10_15 / CSIH3RYI / CSIH3RYO / PWGA24O / RLIN22RX / TAUB0I9 / TAUB0O9
5	P11_0 / CSIH2RYI / CSIH2RYO / ADCA1TRG2 / PWGA25O / RLIN22TX / TAUB0I11 / TAUB0O11
6	P11_8 / $\overline{\text{CSIG1SSI}}$ / RLIN35TX / PWGA48O
7	P11_9 / CSIG1SO / RLIN35RX / INTP15 / PWGA49O
8	P11_10 / CSIG1SC / PWGA50O
9	P11_11 / CSIG1SI / RLIN25TX / PWGA51O
10	P11_12 / RLIN25RX / PWGA52O
11	ISOVCL
12	ISOVSS
13	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
14	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
15	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
16	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
17	EVCC
18	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 /DPIN8 / TAUB0I12 / TAUB0O12
19	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
20	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
21	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / PWGA34O
22	P0_12 / RIIC0SCL / DPIN13 / PWGA45O / TAUB0I10 / TAUB0O10 / CSIG0SI
23	P0_13 / RLIN32RX / INTP12 / PWGA46O / TAUB0I12 / TAUB0O12 / CSIG0SO / CAN5RX / INTP5
24	P0_14 / INTP17 / RLIN32TX / PWGA47O / TAUB0I14 / TAUB0O14 / CSIG0SC / CAN5TX
25	P1_0 / RLIN33RX / INTP13 / TAUJ2I0 / TAUJ2O0
26	P1_1 / INTP18 / RLIN33TX / TAUJ2I1 / TAUJ2O1
27	P1_2 / CAN3RX / INTP3 / DPIN19 / TAUJ2I2 / TAUJ2O2
28	P1_3 / INTP19 / CAN3TX / DPIN23 / TAUJ2I3 / TAUJ2O3
29	EVSS
30	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / ADCA0I4S
31	P8_10 / CSIH3CSS3 / DPIN14 / PWGA42O / ADCA0I17S
32	P8_11 / TAUJ1I2 / TAUJ1O2 / DPIN15 / PWGA43O / CSIH1CSS4 / RLIN25RX / ADCA0I18S
33	P8_12 / TAUJ1I3 / TAUJ1O3 / DPIN16 / PWGA44O / CSIH1CSS5 / INTP23 / RLIN25TX / ADCA0I19S
34	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT
35	JP0_4 / $\overline{\text{DCUTRST}}$
36	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
37	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
38	JP0_1 / INTP1 /TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
39	JP0_0 / INTP0 / FPDR / FPDT / DCUTDI / LPDI / LPDIO / TAUJ2I0 / TAUJ2O0
40	P1_11 / ADCA1TRG2 / RLIN24TX / DPIN22 / INTP14
41	P1_10 / RLIN24RX / DPIN21 / INTP22 / ADCA1TRG1
42	P1_9 / DPIN20 / INTP21

Table 2B.4 Pin Assignment 144-Pin LQFP (RH850/F1KM-S2)

Pin No.	Pin Name
43	P1_8
44	$\overline{\text{RESET}}$
45	EVCC
46	XT1
47	IP0_0 / XT2
48	AWOVSS
49	AWOVCL
50	REGVCC
51	X2
52	X1
53	FLMD0
54	JP0_6 / $\overline{\text{EVTO}}$
55	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / RLIN22TX / TAUB0I6 / TAUB0O6 / CAN4TX
56	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / RLIN22RX / TAUB0I4 / TAUB0O4 / CAN4RX / INTP4
57	P0_8/ INTP16 / RLIN21TX / DPIN6 / CSIH0CSS6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2 / CAN3TX
58	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0 / CAN3RX / INTP3
59	EVSS
60	ISOVSS
61	ISOVCL
62	P1_5 / ADCA1TRG0 / RLIN35TX / DPIN17 / INTP20
63	P1_4 / RLIN35RX / INTP15 / DPIN18
64	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / PWGA14O / INTP4 / CSIH0CSS0 / CAN6RX / INTP6 / ADCA0I0S / RIIC1SDA / SENT0RX
65	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / PWGA15O / INTP5 / CSIH1CSS3 / CAN6TX / ADCA0I1S / RIIC1SCL / SENT0SPCO
66	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / INTP7 / PWGA23O / CAN7TX / ADCA0I5S
67	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / PWGA36O / CAN7RX / INTP9 / ADCA0I6S
68	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / INTP9 / PWGA37O / ADCA0I7S
69	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
70	P8_7 / CSIH3CSS0 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S
71	P8_8 / CSIH3CSS1 / PWGA40O / ADCA0SEL1 / RLIN34RX / INTP14 / ADCA0I15S
72	P8_9 / CSIH3CSS2 / PWGA41O / ADCA0SEL2 / RLIN34TX / ADCA0I16S
73	A0VSS
74	A0VREF
75	AP0_15 / ADCA0I15
76	AP0_14 / ADCA0I14
77	AP0_13 / ADCA0I13
78	AP0_12 / ADCA0I12
79	AP0_11 / ADCA0I11
80	AP0_10 / ADCA0I10
81	AP0_9 / ADCA0I9
82	AP0_8 / ADCA0I8
83	AP0_7 / ADCA0I7
84	AP0_6 / ADCA0I6
85	AP0_5 / ADCA0I5
86	AP0_4 / ADCA0I4

Table 2B.4 Pin Assignment 144-Pin LQFP (RH850/F1KM-S2)

Pin No.	Pin Name
87	AP0_3 / ADCA0I3
88	AP0_2 / ADCA0I2
89	AP0_1 / ADCA0I1
90	AP0_0 / ADCA0I0
91	EVSS
92	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / ADCA0I2S / TAUJ1I1 / TAUJ1O1 / SENT1RX / RIIC1SDA
93	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / ADCA0I3S / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / RIIC1SCL
94	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S
95	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / INTP16 / ADCA0I10S
96	P9_4 / CSIH0CSS5 / PWGA33O / TAUJ1I0 / TAUJ1O0 / INTP17 / ADCA0I11S
97	ISOVSS
98	REGVCC
99	P20_5 / RLIN23TX / INTP23 / PWGA60O / CAN7TX
100	P20_4 / RLIN23RX / INTP22 / PWGA59O / CAN7RX / INTP9
101	EVCC
102	AP1_7 / ADCA1I7
103	AP1_6 / ADCA1I6
104	AP1_5 / ADCA1I5
105	AP1_4 / ADCA1I4
106	AP1_3 / ADCA1I3
107	AP1_2 / ADCA1I2
108	AP1_1 / ADCA1I1
109	AP1_0 / ADCA1I0
110	A1VREF
111	A1VSS
112	BVCC
113	ISOVCL
114	ISOVSS
115	P18_0 / CSIG1RYI / CSIG1RYO / PWGA61O / ADCA1I0S / TAUJ3I0 / TAUJ3O0
116	P18_1 / PWGA62O / ADCA1I1S / TAUJ3I1 / TAUJ3O1
117	P18_2 / PWGA63O / ADCA1I2S / TAUJ3I2 / TAUJ3O2
118	P18_3 / ADCA1I3S / TAUJ3I3 / TAUJ3O3
119	BVSS
120	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX /INTP1 / RLIN24RX / MODE2
121	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / RLIN24TX / TAUJ3I1 / TAUJ3O1
122	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / ENCA0EC / PWGA5O / FLMD1 / TAUJ3I2 / TAUJ3O2
123	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO
124	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / TAUJ3I3 / TAUJ3O3
125	P10_11 / PWGA16O / RLIN31RX / INTP11 / CSIH1CSS0 / TAUB0I1 / TAUB0O1
126	P10_12 / PWGA17O / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3
127	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / RLIN32RX / INTP12 / TAUB0I5 / TAUB0O5 / CAN7TX
128	P10_14 / ADCA1TRG0 / PWGA19O / RLIN32TX / $\overline{\text{CSIH3SSI}}$ / TAUB0I7 / TAUB0O7 / CAN7RX / INTP9

Table 2B.4 Pin Assignment 144-Pin LQFP (RH850/F1KM-S2)

Pin No.	Pin Name
129	P11_1 / $\overline{\text{CSIH2SSI}}$ / RLIN20RX / CSIH0CSS7 / INTP20 / PWGA26O / TAUB0I13 / TAUB0O13
130	P11_2 / CSIH2SO / RLIN32RX / INTP12 / RLIN20TX / PWGA27O / TAUB0I15 / TAUB0O15 / SFMA0IO3
131	P11_3 / CSIH2SC / CAN3RX / INTP3 / PWGA28O / RLIN32TX / SFMA0IO2
132	P11_4 / CSIH2SI / CAN3TX / INTP21 / PWGA29O / SFMA0IO1
133	P11_5 / CAN5RX / INTP5 / RLIN33TX / PWGA30O / CSIH3SI / SFMA0IO0
134	P11_6 / RLIN33RX / INTP13 / CAN5TX / ADCA1TRG1 / PWGA31O / CSIH3SO / SFMA0SSL
135	P11_7 / INTP5 / PWGA32O / CSIH3SC / SFMA0CLK
136	P11_15 / CAN2RX / INTP2 / CSIH2CSS4 / PWGA55O
137	P12_0 / CAN2TX / PWGA56O
138	P12_1 / RLIN34RX / INTP14 / CSIH2CSS5 / PWGA57O
139	P12_2 / INTP19 / RLIN34TX / PWGA58O
140	BVCC
141	BVSS
142	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX /INTP0 / CSCXFOUT / PWGA0O / TAPA0UP / CSIH1SI / TAUJ1I3 / TAUJ1O3
143	P10_1 / TAUD0I3 / TAUD0O3 / INTP18 / CAN0TX / PWGA1O / TAPA0UN / CSIH1SC / MODE0 / TAUJ3I0 / TAUJ3O0
144	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP / CSIH1SO / MODE1

Table 2B.5 Pin Assignment 176-Pin LQFP (RH850/F1KM-S4)

Pin No.	Pin Name
1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN / $\overline{\text{CSIH1SSI}}$ / MEMC0CLK / RLIN37RX / INTP17
2	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / CAN6TX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$ / PWGA53O / ETNB0RXD2 / MEMC0A22
3	P10_5 / TAUD0I11 / TAUD0O11 / CAN6RX / INTP6 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO / ETNB0RXD3 / PWGA54O
4	BVCC
5	BVSS
6	P10_15 / CSIH3RYI / CSIH3RYO / PWGA24O / RLIN22RX / TAUB0I9 / TAUB0O9 / $\overline{\text{MEMC0RD}}$
7	P11_0 / CSIH2RYI / CSIH2RYO / ADCA1TRG2 / PWGA25O / RLIN22TX / TAUB0I11 / TAUB0O11 / $\overline{\text{MEMC0WR}}$
8	P11_8 / $\overline{\text{CSIG1SSI}}$ / RLIN35TX / PWGA48O / TAUB1I11 / TAUB1O11 / $\overline{\text{MEMC0CS0}}$
9	P11_9 / CSIG1SO / RLIN35RX / INTP15 / PWGA49O / TAUB1I13 / TAUB1O13 / $\overline{\text{MEMC0CS1}}$
10	P11_10 / CSIG1SC / PWGA50O / TAUB1I15 / TAUB1O15 / $\overline{\text{MEMC0CS2}}$
11	P11_11 / CSIG1SI / RLIN25TX / PWGA51O / TAUB1I0 / TAUB1O0 / $\overline{\text{MEMC0CS3}}$ / ETNB0RXDV
12	P11_12 / RLIN25RX / PWGA52O / TAUB1I2 / TAUB1O2 / $\overline{\text{MEMC0WAIT}}$
13	ISOVCL
14	ISOVSS
15	P12_3 / RLIN27RX / PWGA68O / CSIG2SI / $\overline{\text{MEMC0BEN0}}$ / TAUB1I6 / TAUB1O6
16	P12_4 / RLIN27TX / PWGA69O / CSIG2SC / ETNB0MDIO / $\overline{\text{MEMC0BEN1}}$
17	P12_5 / PWGA70O / ETNB0MDC / CSIG2SO / TAUB1I4 / TAUB1O4
18	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
19	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
20	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
21	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
22	EVCC
23	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 /DPIN8 / TAUB0I12 / TAUB0O12
24	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
25	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
26	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / RLIN26RX / PWGA34O
27	P0_12 / RIIC0SCL / DPIN13 / PWGA45O / TAUB0I10 / TAUB0O10 / CSIG0SI / RLIN26TX
28	P0_13 / RLIN32RX / INTP12 / PWGA46O / TAUB0I12 / TAUB0O12 / CSIG0SO / CAN5RX / INTP5
29	P0_14 / INTP17 / RLIN32TX / PWGA47O / TAUB0I14 / TAUB0O14 / CSIG0SC / CAN5TX
30	P1_0 / RLIN33RX / INTP13 / TAUJ2I0 / TAUJ2O0
31	P1_1 / INTP18 / RLIN33TX / TAUJ2I1 / TAUJ2O1
32	P1_2 / CAN3RX / INTP3 / DPIN19 / TAUJ2I2 / TAUJ2O2
33	P1_3 / INTP19 / CAN3TX / DPIN23 / TAUJ2I3 / TAUJ2O3
34	P1_12 / CAN4RX / INTP4 / RLIN36TX
35	P1_13 / CAN4TX / RLIN36RX / INTP16
36	P2_6 / ADCA0SEL2
37	EVSS
38	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / RLIN37TX / ADCA0I4S
39	P8_10 / CSIH3CSS3 / DPIN14 / PWGA42O / RLIN37RX / INTP17 / ADCA0I17S
40	P8_11 / TAUJ1I2 / TAUJ1O2 / DPIN15 / PWGA43O / CSIH1CSS4 / RLIN25RX / ADCA0I18S
41	P8_12 / TAUJ1I3 / TAUJ1O3 / DPIN16 / PWGA44O / CSIH1CSS5 / INTP23 / RLIN25TX / ADCA0I19S
42	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT

Table 2B.5 Pin Assignment 176-Pin LQFP (RH850/F1KM-S4)

Pin No.	Pin Name
43	JP0_4 / $\overline{\text{DCUTRST}}$
44	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
45	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
46	JP0_1 / INTP1 /TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
47	JP0_0 / INTP0 / FPDR / FPDT / DCUTDI / LPDI / LPDIO / TAUJ2I0 / TAUJ2O0
48	P2_1 / RLIN27TX / CAN6TX
49	P2_0 / RLIN27RX / INTP6 / CAN6RX
50	P1_11 / ADCA1TRG2 / RLIN24TX / DPIN22 / INTP14
51	P1_10 / RLIN24RX / DPIN21 / INTP22 / ADCA1TRG1
52	P1_9 / DPIN20 / INTP21
53	P1_8
54	$\overline{\text{RESET}}$
55	EVCC
56	XT1
57	IP0_0 / XT2
58	AWOVSS
59	AWOVCL
60	REGVCC
61	X2
62	X1
63	FLMD0
64	P2_3 / RLIN28TX
65	P2_2 / RLIN28RX
66	JP0_6 / $\overline{\text{EVTO}}$
67	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / RLIN22TX / TAUB0I6 / TAUB0O6 / CAN4TX
68	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / RLIN22RX / TAUB0I4 / TAUB0O4 / CAN4RX / INTP4
69	P0_8/ INTP16 / RLIN21TX / DPIN6 / CSIH0CSS6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2 / CAN3TX
70	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0 / CAN3RX / INTP3
71	EVSS
72	ISOVSS
73	ISOVCL
74	P1_5 / ADCA1TRG0 / RLIN35TX / DPIN17 / INTP20
75	P1_4 / RLIN35RX / INTP15 / DPIN18
76	P2_4 / RLIN29RX / ADCA0SEL0
77	P2_5 / RLIN29TX / ADCA0SEL1
78	P1_14 / RLIN23RX / CAN7RX / INTP9
79	P1_15 / RLIN23TX / CAN7TX
80	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / PWGA14O / INTP4 / CSIH0CSS0 / CAN6RX / INTP6 / ADCA0I0S / RIIC1SDA / SENT0RX
81	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / PWGA15O / INTP5 / CSIH1CSS3 / CAN6TX / ADCA0I1S / RIIC1SCL / SENT0SPCO
82	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / INTP7 / PWGA23O / CAN7TX / ADCA0I5S
83	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / PWGA36O / CAN7RX / INTP9 / ADCA0I6S
84	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / INTP9 / PWGA37O / ADCA0I7S
85	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
86	P8_7 / CSIH3CSS0 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S

Table 2B.5 Pin Assignment 176-Pin LQFP (RH850/F1KM-S4)

Pin No.	Pin Name
87	P8_8 / CSIH3CSS1 / PWGA40O / ADCA0SEL1 / RLIN34RX / INTP14 / ADCA0I15S
88	P8_9 / CSIH3CSS2 / PWGA41O / ADCA0SEL2 / RLIN34TX / ADCA0I16S
89	A0VSS
90	A0VREF
91	AP0_15 / ADCA0I15
92	AP0_14 / ADCA0I14
93	AP0_13 / ADCA0I13
94	AP0_12 / ADCA0I12
95	AP0_11 / ADCA0I11
96	AP0_10 / ADCA0I10
97	AP0_9 / ADCA0I9
98	AP0_8 / ADCA0I8
99	AP0_7 / ADCA0I7
100	AP0_6 / ADCA0I6
101	AP0_5 / ADCA0I5
102	AP0_4 / ADCA0I4
103	AP0_3 / ADCA0I3
104	AP0_2 / ADCA0I2
105	AP0_1 / ADCA0I1
106	AP0_0 / ADCA0I0
107	EVSS
108	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / ADCA0I2S / TAUJ1I1 / TAUJ1O1 / SENT1RX / RIIC1SDA
109	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / ADCA0I3S / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / RIIC1SCL
110	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S
111	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / INTP16 / ADCA0I10S
112	P9_4 / CSIH0CSS5 / PWGA33O / TAUJ1I0 / TAUJ1O0 / INTP17 / ADCA0I11S
113	ISOVSS
114	REGVCC
115	P20_3 / CAN4TX / PWGA67O / RLIN29TX / CSIG3RYI / CSIG3RYO
116	P20_2 / CAN4RX / INTP4 / PWGA66O / RLIN29RX / CSIG3SC
117	P20_1 / RLIN26TX / PWGA65O / CAN6TX / CSIG3SO
118	P20_0 / RLIN26RX / PWGA64O / INTP6 / CAN6RX / CSIG3SI
119	P20_5 / RLIN23TX / INTP23 / PWGA60O / CAN7TX
120	P20_4 / RLIN23RX / INTP22 / PWGA59O / CAN7RX / INTP9 / $\overline{\text{CSIG3SSI}}$
121	EVCC
122	AP1_11 / ADCA1I11
123	AP1_10 / ADCA1I10
124	AP1_9 / ADCA1I9
125	AP1_8 / ADCA1I8
126	AP1_7 / ADCA1I7
127	AP1_6 / ADCA1I6
128	AP1_5 / ADCA1I5
129	AP1_4 / ADCA1I4
130	AP1_3 / ADCA1I3

Table 2B.5 Pin Assignment 176-Pin LQFP (RH850/F1KM-S4)

Pin No.	Pin Name
131	AP1_2 / ADCA1I2
132	AP1_1 / ADCA1I1
133	AP1_0 / ADCA1I0
134	AP1_15 / ADCA1I15
135	AP1_14 / ADCA1I14
136	AP1_13 / ADCA1I13
137	AP1_12 / ADCA1I12
138	A1VREF
139	A1VSS
140	BVCC
141	ISOVCL
142	ISOVSS
143	P18_0 / CSIG1RYI / CSIG1RYO / ETNB0LINK / PWGA61O / ADCA1I0S / TAUJ3I0 / TAUJ3O0
144	P18_1 / PWGA62O / ETNB0TXD0 / ADCA1I1S / TAUJ3I1 / TAUJ3O1
145	P18_2 / PWGA63O / ETNB0TXD1 / ADCA1I2S / TAUJ3I2 / TAUJ3O2
146	P18_3 / PWGA71O / ETNB0TXD2 / ADCA1I3S / TAUJ3I3 / TAUJ3O3
147	P18_4 / CSIH1CSS4 / ETNB0TXD3 / ADCA1I4S
148	P18_5 / CSIH1CSS5 / ETNB0TXEN / ADCA1I5S
149	P18_6 / ADCA1I6S
150	P18_7 / ETNB0TXCLK / ADCA1I7S
151	BVSS
152	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX /INTP1 / MEMC0AD0 / RLIN24RX / MODE2
153	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / MEMC0AD1 / RLIN24TX / TAUJ3I1 / TAUJ3O1
154	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / FLXA0TXDB / ENCA0EC / PWGA5O / MEMC0AD2 / FLMD1 / TAUJ3I2 / TAUJ3O2
155	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO / MEMC0AD3 / FLXA0RXDB
156	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / MEMC0AD4 / TAUJ3I3 / TAUJ3O3
157	P10_11 / PWGA16O / RLIN31RX / INTP11 / FLXA0TXENA / CSIH1CSS0 / TAUB0I1 / TAUB0O1 / MEMC0AD5
158	P10_12 / PWGA17O / FLXA0STPWT / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3 / MEMC0AD6
159	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / RLIN32RX / INTP12 / FLXA0TXENB / TAUB0I5 / TAUB0O5 / MEMC0AD7 / CAN7TX
160	P10_14 / ADCA1TRG0 / PWGA19O / FLXA0RXDA / RLIN32TX / $\overline{\text{CSIH3SSI}}$ / TAUB0I7 / TAUB0O7 / MEMC0AD8 / CAN7RX / INTP9
161	P11_1 / $\overline{\text{CSIH2SSI}}$ / FLXA0TXDA / RLIN20RX / CSIH0CSS7 / INTP20 / PWGA26O / TAUB0I13 / TAUB0O13 / MEMC0AD9
162	P11_2 / CSIH2SO / RLIN32RX / INTP12 / RLIN20TX / PWGA27O / TAUB0I15 / TAUB0O15 / MEMC0AD10 / SFMA0IO3
163	P11_3 / CSIH2SC / CAN3RX / INTP3 / PWGA28O / TAUB1I1 / TAUB1O1 / MEMC0AD11 / RLIN32TX / SFMA0IO2
164	P11_4 / CSIH2SI / CAN3TX / INTP21 / PWGA29O / TAUB1I3 / TAUB1O3 / MEMC0AD12 / SFMA0IO1
165	P11_5 / CAN5RX / INTP5 / RLIN33TX / PWGA30O / CSIH3SI / TAUB1I5 / TAUB1O5 / MEMC0AD13 / SFMA0IO0
166	P11_6 / RLIN33RX / INTP13 / CAN5TX / ADCA1TRG1 / PWGA31O / CSIH3SO / TAUB1I7 / TAUB1O7 / MEMC0AD14 / SFMA0SSL

Table 2B.5 Pin Assignment 176-Pin LQFP (RH850/F1KM-S4)

Pin No.	Pin Name
167	P11_7 / INTP5 / PWGA32O / CSIH3SC / TAUB1I9 / TAUB1O9 / MEMC0AD15 / SFMA0CLK
168	P11_15 / CAN2RX / INTP2 / CSIH2CSS4 / PWGA55O / TAUB1I8 / TAUB1O8 / $\overline{\text{MEMC0ASTB}}$ / ETNB0RXERR / RLIN36TX
169	P12_0 / CAN2TX / PWGA56O / TAUB1I10 / TAUB1O10 / $\overline{\text{CSIG2SSI}}$ / MEMC0A16 / RLIN36RX / INTP16
170	P12_1 / RLIN34RX / INTP14 / CSIH2CSS5 / PWGA57O / TAUB1I12 / TAUB1O12 / MEMC0A17
171	P12_2 / INTP19 / RLIN34TX / PWGA58O / TAUB1I14 / TAUB1O14 / MEMC0A18 / CSIG2RYI / CSIG2RYO
172	BVCC
173	BVSS
174	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX /INTP0 / CSCXFOUT / PWGA0O / TAPA0UP / CSIH1SI / MEMC0A19 / ETNB0RXCLK / TAUJ1I3 / TAUJ1O3
175	P10_1 / TAUD0I3 / TAUD0O3 / INTP18 / CAN0TX / PWGA1O / TAPA0UN / CSIH1SC / ETNB0RXD0 / MEMC0A20 / MODE0 / TAUJ3I0 / TAUJ3O0
176	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP / CSIH1SO / ETNB0RXD1 / MEMC0A21 / RLIN37TX / MODE1

Table 2B.6 Pin Assignment 176-Pin LQFP (RH850/F1KM-S2)

Pin No.	Pin Name
1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN / $\overline{\text{CSIH1SSI}}$ / RLIN37RX / INTP17
2	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / CAN6TX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$ / PWGA53O
3	P10_5 / TAUD0I11 / TAUD0O11 / CAN6RX / INTP6 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO / PWGA54O
4	BVCC
5	BVSS
6	P10_15 / CSIH3RYI / CSIH3RYO / PWGA24O / RLIN22RX / TAUB0I9 / TAUB0O9
7	P11_0 / CSIH2RYI / CSIH2RYO / ADCA1TRG2 / PWGA25O / RLIN22TX / TAUB0I11 / TAUB0O11
8	P11_8 / $\overline{\text{CSIG1SSI}}$ / RLIN35TX / PWGA48O / TAUB1I11 / TAUB1O11
9	P11_9 / CSIG1SO / RLIN35RX / INTP15 / PWGA49O / TAUB1I13 / TAUB1O13
10	P11_10 / CSIG1SC / PWGA50O / TAUB1I15 / TAUB1O15
11	P11_11 / CSIG1SI / RLIN25TX / PWGA51O / TAUB1I0 / TAUB1O0
12	P11_12 / RLIN25RX / PWGA52O / TAUB1I2 / TAUB1O2
13	ISOVCL
14	ISOVSS
15	P12_3 / RLIN27RX / PWGA68O / CSIG2SI / TAUB1I6 / TAUB1O6
16	P12_4 / RLIN27TX / PWGA69O / CSIG2SC
17	P12_5 / PWGA70O / CSIG2SO / TAUB1I4 / TAUB1O4
18	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
19	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
20	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
21	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
22	EVCC
23	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 /DPIN8 / TAUB0I12 / TAUB0O12
24	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
25	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
26	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / RLIN26RX / PWGA34O
27	P0_12 / RIIC0SCL / DPIN13 / PWGA45O / TAUB0I10 / TAUB0O10 / CSIG0SI / RLIN26TX
28	P0_13 / RLIN32RX / INTP12 / PWGA46O / TAUB0I12 / TAUB0O12 / CSIG0SO / CAN5RX / INTP5
29	P0_14 / INTP17 / RLIN32TX / PWGA47O / TAUB0I14 / TAUB0O14 / CSIG0SC / CAN5TX
30	P1_0 / RLIN33RX / INTP13 / TAUJ2I0 / TAUJ2O0
31	P1_1 / INTP18 / RLIN33TX / TAUJ2I1 / TAUJ2O1
32	P1_2 / CAN3RX / INTP3 / DPIN19 / TAUJ2I2 / TAUJ2O2
33	P1_3 / INTP19 / CAN3TX / DPIN23 / TAUJ2I3 / TAUJ2O3
34	P1_12 / CAN4RX / INTP4 / RLIN36TX
35	P1_13 / CAN4TX / RLIN36RX / INTP16
36	P2_6 / ADCA0SEL2
37	EVSS
38	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / RLIN37TX / ADCA0I4S
39	P8_10 / CSIH3CSS3 / DPIN14 / PWGA42O / RLIN37RX / INTP17 / ADCA0I17S
40	P8_11 / TAUJ1I2 / TAUJ1O2 / DPIN15 / PWGA43O / CSIH1CSS4 / RLIN25RX / ADCA0I18S
41	P8_12 / TAUJ1I3 / TAUJ1O3 / DPIN16 / PWGA44O / CSIH1CSS5 / INTP23 / RLIN25TX / ADCA0I19S
42	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT

Table 2B.6 Pin Assignment 176-Pin LQFP (RH850/F1KM-S2)

Pin No.	Pin Name
43	JP0_4 / $\overline{\text{DCUTRST}}$
44	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
45	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
46	JP0_1 / INTP1 /TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
47	JP0_0 / INTP0 / FPDR / FPDT / DCUTDI / LPDI / LPDIO / TAUJ2I0 / TAUJ2O0
48	P2_1 / RLIN27TX / CAN6TX
49	P2_0 / RLIN27RX / INTP6 / CAN6RX
50	P1_11 / ADCA1TRG2 / RLIN24TX / DPIN22 / INTP14
51	P1_10 / RLIN24RX / DPIN21 / INTP22 / ADCA1TRG1
52	P1_9 / DPIN20 / INTP21
53	P1_8
54	$\overline{\text{RESET}}$
55	EVCC
56	XT1
57	IP0_0 / XT2
58	AWOVSS
59	AWOVCL
60	REGVCC
61	X2
62	X1
63	FLMD0
64	P2_3 / RLIN28TX
65	P2_2 / RLIN28RX
66	JP0_6 / $\overline{\text{EVTO}}$
67	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / RLIN22TX / TAUB0I6 / TAUB0O6 / CAN4TX
68	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / RLIN22RX / TAUB0I4 / TAUB0O4 / CAN4RX / INTP4
69	P0_8/ INTP16 / RLIN21TX / DPIN6 / CSIH0CSS6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2 / CAN3TX
70	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0 / CAN3RX / INTP3
71	EVSS
72	ISOVSS
73	ISOVCL
74	P1_5 / ADCA1TRG0 / RLIN35TX / DPIN17 / INTP20
75	P1_4 / RLIN35RX / INTP15 / DPIN18
76	P2_4 / RLIN29RX / ADCA0SEL0
77	P2_5 / RLIN29TX / ADCA0SEL1
78	P1_14 / RLIN23RX / CAN7RX / INTP9
79	P1_15 / RLIN23TX / CAN7TX
80	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / PWGA14O / INTP4 / CSIH0CSS0 / CAN6RX / INTP6 / ADCA0I0S / RIIC1SDA / SENT0RX
81	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / PWGA15O / INTP5 / CSIH1CSS3 / CAN6TX / ADCA0I1S / RIIC1SCL / SENT0SPCO
82	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / INTP7 / PWGA23O / CAN7TX / ADCA0I5S
83	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / PWGA36O / CAN7RX / INTP9 / ADCA0I6S
84	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / INTP9 / PWGA37O / ADCA0I7S
85	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
86	P8_7 / CSIH3CSS0 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S

Table 2B.6 Pin Assignment 176-Pin LQFP (RH850/F1KM-S2)

Pin No.	Pin Name
87	P8_8 / CSIH3CSS1 / PWGA40O / ADCA0SEL1 / RLIN34RX / INTP14 / ADCA0I15S
88	P8_9 / CSIH3CSS2 / PWGA41O / ADCA0SEL2 / RLIN34TX / ADCA0I16S
89	A0VSS
90	A0VREF
91	AP0_15 / ADCA0I15
92	AP0_14 / ADCA0I14
93	AP0_13 / ADCA0I13
94	AP0_12 / ADCA0I12
95	AP0_11 / ADCA0I11
96	AP0_10 / ADCA0I10
97	AP0_9 / ADCA0I9
98	AP0_8 / ADCA0I8
99	AP0_7 / ADCA0I7
100	AP0_6 / ADCA0I6
101	AP0_5 / ADCA0I5
102	AP0_4 / ADCA0I4
103	AP0_3 / ADCA0I3
104	AP0_2 / ADCA0I2
105	AP0_1 / ADCA0I1
106	AP0_0 / ADCA0I0
107	EVSS
108	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / ADCA0I2S / TAUJ1I1 / TAUJ1O1 / SENT1RX / RIIC1SDA
109	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / ADCA0I3S / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / RIIC1SCL
110	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S
111	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / INTP16 / ADCA0I10S
112	P9_4 / CSIH0CSS5 / PWGA33O / TAUJ1I0 / TAUJ1O0 / INTP17 / ADCA0I11S
113	ISOVSS
114	REGVCC
115	P20_3 / CAN4TX / PWGA67O / RLIN29TX / CSIG3RYI / CSIG3RYO
116	P20_2 / CAN4RX / INTP4 / PWGA66O / RLIN29RX / CSIG3SC
117	P20_1 / RLIN26TX / PWGA65O / CAN6TX / CSIG3SO
118	P20_0 / RLIN26RX / PWGA64O / INTP6 / CAN6RX / CSIG3SI
119	P20_5 / RLIN23TX / INTP23 / PWGA60O / CAN7TX
120	P20_4 / RLIN23RX / INTP22 / PWGA59O / CAN7RX / INTP9 / $\overline{\text{CSIG3SSI}}$
121	EVCC
122	AP1_11 / ADCA1I11
123	AP1_10 / ADCA1I10
124	AP1_9 / ADCA1I9
125	AP1_8 / ADCA1I8
126	AP1_7 / ADCA1I7
127	AP1_6 / ADCA1I6
128	AP1_5 / ADCA1I5
129	AP1_4 / ADCA1I4
130	AP1_3 / ADCA1I3

Table 2B.6 Pin Assignment 176-Pin LQFP (RH850/F1KM-S2)

Pin No.	Pin Name
131	AP1_2 / ADCA1I2
132	AP1_1 / ADCA1I1
133	AP1_0 / ADCA1I0
134	AP1_15 / ADCA1I15
135	AP1_14 / ADCA1I14
136	AP1_13 / ADCA1I13
137	AP1_12 / ADCA1I12
138	A1VREF
139	A1VSS
140	BVCC
141	ISOVCL
142	ISOVSS
143	P18_0 / CSIG1RYI / CSIG1RYO / PWGA61O / ADCA1I0S / TAUJ3I0 / TAUJ3O0
144	P18_1 / PWGA62O / ADCA1I1S / TAUJ3I1 / TAUJ3O1
145	P18_2 / PWGA63O / ADCA1I2S / TAUJ3I2 / TAUJ3O2
146	P18_3 / PWGA71O / ADCA1I3S / TAUJ3I3 / TAUJ3O3
147	P18_4 / CSIH1CSS4 / ADCA1I4S
148	P18_5 / CSIH1CSS5 / ADCA1I5S
149	P18_6 / ADCA1I6S
150	P18_7 / ADCA1I7S
151	BVSS
152	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX /INTP1 / RLIN24RX / MODE2
153	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / RLIN24TX / TAUJ3I1 / TAUJ3O1
154	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / ENCA0EC / PWGA5O / FLMD1 / TAUJ3I2 / TAUJ3O2
155	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO
156	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / TAUJ3I3 / TAUJ3O3
157	P10_11 / PWGA16O / RLIN31RX / INTP11 / CSIH1CSS0 / TAUB0I1 / TAUB0O1
158	P10_12 / PWGA17O / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3
159	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / RLIN32RX / INTP12 / TAUB0I5 / TAUB0O5 / CAN7TX
160	P10_14 / ADCA1TRG0 / PWGA19O / RLIN32TX / $\overline{\text{CSIH3SSI}}$ / TAUB0I7 / TAUB0O7 / CAN7RX / INTP9
161	P11_1 / $\overline{\text{CSIH2SSI}}$ / RLIN20RX / CSIH0CSS7 / INTP20 / PWGA26O / TAUB0I13 / TAUB0O13
162	P11_2 / CSIH2SO / RLIN32RX / INTP12 / RLIN20TX / PWGA27O / TAUB0I15 / TAUB0O15 / SFMA0IO3
163	P11_3 / CSIH2SC / CAN3RX / INTP3 / PWGA28O / TAUB1I1 / TAUB1O1 / RLIN32TX / SFMA0IO2
164	P11_4 / CSIH2SI / CAN3TX / INTP21 / PWGA29O / TAUB1I3 / TAUB1O3 / SFMA0IO1
165	P11_5 / CAN5RX / INTP5 / RLIN33TX / PWGA30O / CSIH3SI / TAUB1I5 / TAUB1O5 / SFMA0IO0
166	P11_6 / RLIN33RX / INTP13 / CAN5TX / ADCA1TRG1 / PWGA31O / CSIH3SO / TAUB1I7 / TAUB1O7 / SFMA0SSL

Table 2B.6 Pin Assignment 176-Pin LQFP (RH850/F1KM-S2)

Pin No.	Pin Name
167	P11_7 / INTP5 / PWGA32O / CSIH3SC / TAUB1I9 / TAUB1O9 / SFMA0CLK
168	P11_15 / CAN2RX / INTP2 / CSIH2CSS4 / PWGA55O / TAUB1I8 / TAUB1O8 / RLIN36TX
169	P12_0 / CAN2TX / PWGA56O / TAUB1I10 / TAUB1O10 / $\overline{\text{CSIG2SSI}}$ / RLIN36RX / INTP16
170	P12_1 / RLIN34RX / INTP14 / CSIH2CSS5 / PWGA57O / TAUB1I12 / TAUB1O12
171	P12_2 / INTP19 / RLIN34TX / PWGA58O / TAUB1I14 / TAUB1O14 / CSIG2RYI / CSIG2RYO
172	BVCC
173	BVSS
174	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX /INTP0 / CSCXFOUT / PWGA0O / TAPA0UP / CSIH1SI / TAUJ1I3 / TAUJ1O3
175	P10_1 / TAUD0I3 / TAUD0O3 / INTP18 / CAN0TX / PWGA1O / TAPA0UN / CSIH1SC / MODE0 / TAUJ3I0 / TAUJ3O0
176	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP / CSIH1SO / RLIN37TX / MODE1

Table 2B.7 Pin Assignment 233-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
A1	BVSS
A2	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX / INTP0 / CSCXFOUT / PWGA0O / TAPA0UP / CSIH1SI / MEMC0A19 / ETNB0RXCLK / TAUJ1I3 / TAUJ1O3
A3	P12_2 / INTP19 / RLIN34TX / PWGA58O / TAUB1I14 / TAUB1O14 / MEMC0A18 / CSIG2RYI / CSIG2RYO
A4	P11_5 / CAN5RX / INTP5 / RLIN33TX / PWGA30O / CSIH3SI / TAUB1I5 / TAUB1O5 / MEMC0AD13 / SFMA0IO0
A5	P11_1 / $\overline{\text{CSIH2SSI}}$ / FLXA0TXDA / RLIN20RX / CSIH0CSS7 / INTP20 / PWGA26O / TAUB0I13 / TAUB0O13 / MEMC0AD9
A6	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / RLIN32RX / INTP12 / FLXA0TXENB / TAUB0I5 / TAUB0O5 / MEMC0AD7 / CAN7TX
A7	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / MEMC0AD4 / TAUJ3I3 / TAUJ3O3
A8	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / MEMC0AD1 / RLIN24TX / TAUJ3I1 / TAUJ3O1
A9	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX / INTP1 / MEMC0AD0 / RLIN24RX / MODE2
A10	P19_2 / ADCA1I18S
A11	P18_15 / ADCA1I15S
A12	P18_13 / ADCA1I13S
A13	P18_6 / ADCA1I6S
A14	P18_5 / CSIH1CSS5 / ETNB0TXEN / ADCA1I5S
A15	P18_10 / ADCA1I10S
A16	P18_8 / ADCA1I8S
A17	A1VSS
B1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN / $\overline{\text{CSIH1SSI}}$ / MEMC0CLK / RLIN37RX / INTP17
B2	P10_1 / TAUD0I3 / TAUD0O3 / INTP18 / CAN0TX / PWGA1O / TAPA0UN / CSIH1SC / ETNB0RXD0 / MEMC0A20 / MODE0 / TAUJ3I0 / TAUJ3O0
B3	P13_1 / MEMC0A20
B4	P12_0 / CAN2TX / PWGA56O / TAUB1I10 / TAUB1O10 / $\overline{\text{CSIG2SSI}}$ / MEMC0A16 / RLIN36RX / INTP16
B5	P11_4 / CSIH2SI / CAN3TX / INTP21 / PWGA29O / TAUB1I3 / TAUB1O3 / MEMC0AD12 / SFMA0IO1
B6	P11_3 / CSIH2SC / CAN3RX / INTP3 / PWGA28O / TAUB1I1 / TAUB1O1 / MEMC0AD11 / RLIN32TX / SFMA0IO2
B7	P10_14 / ADCA1TRG0 / PWGA19O / FLXA0RXDA / RLIN32TX / $\overline{\text{CSIH3SSI}}$ / TAUB0I7 / TAUB0O7 / MEMC0AD8 / CAN7RX / INTP9
B8	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO / MEMC0AD3 / FLXA0RXDB
B9	P19_3 / ADCA1I19S
B10	P19_1 / ADCA1I17S
B11	P18_7 / ETNB0TXCLK / ADCA1I7S
B12	P18_11 / ADCA1I11S
B13	P18_3 / PWGA71O / ETNB0TXD2 / ADCA1I3S / TAUJ3I3 / TAUJ3O3
B14	P18_2 / PWGA63O / ETNB0TXD1 / ADCA1I2S / TAUJ3I2 / TAUJ3O2
B15	P18_1 / PWGA62O / ETNB0TXD0 / ADCA1I1S / TAUJ3I1 / TAUJ3O1
B16	AP1_12 / ADCA1I12
B17	AP1_14 / ADCA1I14
C1	P10_15 / CSIH3RYI / CSIH3RYO / PWGA24O / RLIN22RX / TAUB0I9 / TAUB0O9 / $\overline{\text{MEMC0RD}}$
C2	P10_5 / TAUD0I11 / TAUD0O11 / CAN6RX / INTP6 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO / ETNB0RXD3 / PWGA54O

Table 2B.7 Pin Assignment 233-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
C3	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP / CSIH1SO / ETNB0RXD1 / MEMC0A21 / RLIN37TX / MODE1
C4	P13_0 / MEMC0A19
C5	P12_1 / RLIN34RX / INTP14 / CSIH2CSS5 / PWGA57O / TAUB1I12 / TAUB1O12 / MEMC0A17
C6	P11_7 / INTP5 / PWGA32O / CSIH3SC / TAUB1I9 / TAUB1O9 / MEMC0AD15 / SFMA0CLK
C7	P11_2 / CSIH2SO / RLIN32RX / INTP12 / RLIN20TX / PWGA27O / TAUB0I15 / TAUB0O15 / MEMC0AD10 / SFMA0IO3
C8	P10_11 / PWGA16O / RLIN31RX / INTP11 / FLXA0TXENA / CSIH1CSS0 / TAUB0I1 / TAUB0O1 / MEMC0AD5
C9	P18_14 / ADCA1I14S
C10	P19_0 / ADCA1I16S
C11	P18_4 / CSIH1CSS4 / ETNB0TXD3 / ADCA1I4S
C12	P18_12 / ADCA1I12S
C13	P18_9 / ADCA1I9S
C14	P18_0 / CSIG1RYI / CSIG1RYO / ETNB0LINK / PWGA61O / ADCA1I0S / TAUJ3I0 / TAUJ3O0
C15	AP1_13 / ADCA1I13
C16	AP1_15 / ADCA1I15
C17	AP1_0 / ADCA1I0
D1	P11_9 / CSIG1SO / RLIN35RX / INTP15 / PWGA49O / TAUB1I13 / TAUB1O13 / $\overline{\text{MEMC0CS1}}$
D2	P11_0 / CSIH2RYI / CSIH2RYO / ADCA1TRG2 / PWGA25O / RLIN22TX / TAUB0I11 / TAUB0O11 / $\overline{\text{MEMC0WR}}$
D3	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / CAN6TX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$ / PWGA53O / ETNB0RXD2 / MEMC0A22
D4	BVCC
D5	P11_15 / CAN2RX / INTP2 / CSIH2CSS4 / PWGA55O / TAUB1I8 / TAUB1O8 / $\overline{\text{MEMC0ASTB}}$ / ETNB0RXERR / RLIN36TX
D6	P11_6 / RLIN33RX / INTP13 / CAN5TX / ADCA1TRG1 / PWGA31O / CSIH3SO / TAUB1I7 / TAUB1O7 / MEMC0AD14 / SFMA0SSL
D7	P10_12 / PWGA17O / FLXA0STPWT / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3 / MEMC0AD6
D8	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / FLXA0TXDB / ENCA0EC / PWGA5O / MEMC0AD2 / FLMD1 / TAUJ3I2 / TAUJ3O2
D9	BVSS
D10	BVCC
D11	BVCC
D12	ISOVSS
D13	ISOVCL
D14	A1VSS
D15	AP1_1 / ADCA1I1
D16	AP1_2 / ADCA1I2
D17	AP1_3 / ADCA1I3
E1	P11_12 / RLIN25RX / PWGA52O / TAUB1I2 / TAUB1O2 / $\overline{\text{MEMC0WAIT}}$
E2	P11_10 / CSIG1SC / PWGA50O / TAUB1I15 / TAUB1O15 / $\overline{\text{MEMC0CS2}}$
E3	P11_8 / $\overline{\text{CSIG1SSI}}$ / RLIN35TX / PWGA48O / TAUB1I11 / TAUB1O11 / $\overline{\text{MEMC0CS0}}$
E4	BVCC
E14	A1VREF
E15	AP1_5 / ADCA1I5
E16	AP1_6 / ADCA1I6
E17	AP1_8 / ADCA1I8

Table 2B.7 Pin Assignment 233-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
F1	P13_3 / ETNB0RXERR
F2	P13_2 / ETNB0RXDV
F3	P11_11 / CSIG1SI / RLIN25TX / PWGA51O / TAUB1I0 / TAUB1O0 / $\overline{\text{MEMC0CS3}}$ / ETNB0RXDV
F4	BVSS
F14	AP1_4 / ADCA1I4
F15	AP1_7 / ADCA1I7
F16	AP1_9 / ADCA1I9
F17	P20_4 / RLIN23RX / INTP22 / PWGA59O / CAN7RX / INTP9 / $\overline{\text{CSIG3SSI}}$
G1	P12_3 / RLIN27RX / PWGA68O / CSIG2SI / $\overline{\text{MEMC0BEN0}}$ / TAUB1I6 / TAUB1O6
G2	P13_4
G3	P13_5 / MEMC0A21
G4	ISOVCL
G7	BVSS
G8	BVSS
G9	BVSS
G10	BVSS
G11	BVSS
G14	AP1_10 / ADCA1I10
G15	AP1_11 / ADCA1I11
G16	P20_5 / RLIN23TX / INTP23 / PWGA60O / CAN7TX
G17	P20_0 / RLIN26RX / PWGA64O / CAN6RX / INTP6 / CSIG3SI
H1	P12_4 / RLIN27TX / PWGA69O / CSIG2SC / ETNB0MDIO / $\overline{\text{MEMC0BEN1}}$
H2	P13_7 / PWGA73O
H3	P13_6 / MEMC0A22 / PWGA72O
H4	ISOVSS
H7	BVSS
H8	BVSS
H9	BVSS
H10	BVSS
H11	EVSS
H14	EVCC
H15	P20_1 / RLIN26TX / PWGA65O / CAN6TX / CSIG3SO
H16	P20_2 / CAN4RX / INTP4 / PWGA66O / RLIN29RX / CSIG3SC
H17	P20_3 / CAN4TX / PWGA67O / RLIN29TX / CSIG3RYI / CSIG3RYO
J1	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
J2	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
J3	P12_5 / PWGA70O / ETNB0MDC / CSIG2SO / TAUB1I4 / TAUB1O4
J4	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
J7	BVSS
J8	BVSS
J9	BVSS
J10	EVSS
J11	EVSS
J14	REGVCC
J15	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / INTP16 / ADCA0I10S

Table 2B.7 Pin Assignment 233-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
J16	P9_4 / CSIH0CSS5 / PWGA33O / TAUJ1I0 / TAUJ1O0 / INTP17 / ADCA0I11S
J17	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S
K1	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
K2	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
K3	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 / DPIN8 / TAUB0I12 / TAUB0O12
K4	EVCC
K7	EVSS
K8	EVSS
K9	EVSS
K10	EVSS
K11	EVSS
K14	ISOVSS
K15	AP0_0 / ADCA0I0
K16	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / ADCA0I2S / TAUJ1I1 / TAUJ1O1 / SENT1RX / RIIC1SDA
K17	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / ADCA0I3S / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / RIIC1SCL
L1	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / RLIN26RX / PWGA34O
L2	P0_12 / RIIC0SCL / DPIN13 / PWGA45O / TAUB0I10 / TAUB0O10 / CSIG0SI / RLIN26TX
L3	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
L4	P0_14 / INTP17 / RLIN32TX / PWGA47O / TAUB0I14 / TAUB0O14 / CSIG0SC / CAN5TX
L7	EVSS
L8	EVSS
L9	EVSS
L10	EVSS
L11	EVSS
L14	EVSS
L15	AP0_4 / ADCA0I4
L16	AP0_2 / ADCA0I2
L17	AP0_1 / ADCA0I1
M1	P0_13 / RLIN32RX / INTP12 / PWGA46O / TAUB0I12 / TAUB0O12 / CSIG0SO / CAN5RX / INTP5
M2	P1_0 / RLIN33RX / INTP13 / TAUJ2I0 / TAUJ2O0
M3	P2_9 / PWGA77O
M4	P2_7 / RLIN210RX
M14	A0VREF
M15	AP0_8 / ADCA0I8
M16	AP0_5 / ADCA0I5
M17	AP0_3 / ADCA0I3
N1	P1_2 / CAN3RX / INTP3 / DPIN19 / TAUJ2I2 / TAUJ2O2
N2	P1_1 / INTP18 / RLIN33TX / TAUJ2I1 / TAUJ2O1
N3	P1_3 / INTP19 / CAN3TX / DPIN23 / TAUJ2I3 / TAUJ2O3
N4	P2_11 / PWGA79O
N14	A0VSS
N15	AP0_11 / ADCA0I11
N16	AP0_7 / ADCA0I7

Table 2B.7 Pin Assignment 233-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
N17	AP0_6 / ADCA0I6
P1	P1_12 / CAN4RX / INTP4 / RLIN36TX
P2	P1_13 / CAN4TX / RLIN36RX / INTP16
P3	P8_10 / CSIH3CSS3 / DPIN14 / PWGA42O / RLIN37RX / INTP17 / ADCA0I17S
P4	P8_12 / TAUJ1I3 / TAUJ1O3 / DPIN16 / PWGA44O / CSIH1CSS5 / INTP23 / RLIN25TX / ADCA0I19S
P5	JP0_1 / INTP1 / TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
P6	P1_11 / ADCA1TRG2 / RLIN24TX / DPIN22 / INTP14
P7	P2_13 / RLIN211TX
P8	P2_15 / PWGA75O
P9	EVCC
P10	REGVCC
P11	ISOVSS
P12	ISOVCL
P13	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
P14	P8_8 / CSIH3CSS1 / PWGA40O / ADCA0SEL1 / RLIN34RX / INTP14 / ADCA0I15S
P15	AP0_13 / ADCA0I13
P16	AP0_10 / ADCA0I10
P17	AP0_9 / ADCA0I9
R1	P2_6 / ADCA0SEL2
R2	P2_10 / PWGA78O
R3	JP0_4 / $\overline{\text{DCUTRST}}$
R4	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
R5	P2_1 / RLIN27TX / CAN6TX
R6	P1_10 / RLIN24RX / DPIN21 / INTP22 / ADCA1TRG1
R7	P1_9 / DPIN20 / INTP21
R8	P3_0 / PWGA76O
R9	FLMD0
R10	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / RLIN22RX / TAUB0I4 / TAUB0O4 / CAN4RX / INTP4
R11	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0 / CAN3RX / INTP3
R12	P2_5 / RLIN29TX / ADCA0SEL1
R13	P1_15 / RLIN23TX / CAN7TX
R14	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / PWGA36O / CAN7RX / INTP9 / ADCA0I6S
R15	P8_7 / CSIH3CSS0 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S
R16	AP0_14 / ADCA0I14
R17	AP0_12 / ADCA0I12
T1	P2_8 / RLIN210TX
T2	P2_12 / RLIN211RX
T3	P8_11 / TAUJ1I2 / TAUJ1O2 / DPIN15 / PWGA43O / CSIH1CSS4 / RLIN25RX / ADCA0I18S
T4	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
T5	P2_0 / RLIN27RX / CAN6RX / INTP6
T6	P2_14 / PWGA74O
T7	IP0_0 / XT2
T8	AWOVCL
T9	X1
T10	P2_2 / RLIN28RX

Table 2B.7 Pin Assignment 233-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
T11	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / RLIN22TX / TAUB0I6 / TAUB0O6 / CAN4TX
T12	P0_8 / INTP16 / RLIN21TX / DPIN6 / CSIH0CSS6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2 / CAN3TX
T13	P2_4 / RLIN29RX / ADCA0SEL0
T14	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / PWGA15O / INTP5 / CSIH1CSS3 / CAN6TX / ADCA0I1S / RIIC1SCL / SENT0SPCO
T15	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / INTP9 / PWGA37O / ADCA0I7S
T16	P8_9 / CSIH3CSS2 / PWGA41O / ADCA0SEL2 / RLIN34TX / ADCA0I16S
T17	AP0_15 / ADCA0I15
U1	EVSS
U2	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / RLIN37TX / ADCA0I4S
U3	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT
U4	JP0_0 / INTP0 / FPDR / FPDT / DCUTDI / LPDI / LPDIO / TAUJ2I0 / TAUJ2O0
U5	P1_8
U6	$\overline{\text{RESET}}$
U7	XT1
U8	AWOVSS
U9	X2
U10	P2_3 / RLIN28TX
U11	JP0_6 / $\overline{\text{EVTO}}$
U12	P1_5 / ADCA1TRG0 / RLIN35TX / DPIN17 / INTP20
U13	P1_4 / RLIN35RX / INTP15 / DPIN18
U14	P1_14 / RLIN23RX / CAN7RX / INTP9
U15	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / PWGA14O / INTP4 / CSIH0CSS0 / CAN6RX / INTP6 / ADCA0I0S / RIIC1SDA / SENT0RX
U16	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 /CSIH0CSS1 / INTP7/ PWGA23O / CAN7TX / ADCA0I5S
U17	A0VSS

Table 2B.8 Pin Assignment 272-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
A1	BVSS
A2	P22_7
A3	P13_1 / MEMC0A20
A4	P22_9
A5	P11_15 / CAN2RX / INTP2 / CSIH2CSS4 / PWGA55O / TAUB1I8 / TAUB1O8 / $\overline{\text{MEMC0ASTB}}$ / ETNB0RXERR / RLIN36TX
A6	P22_12
A7	P22_13
A8	P22_15
A9	P11_1 / $\overline{\text{CSIH2SSI}}$ / FLXA0TXDA / RLIN20RX / CSIH0CSS7 / INTP20 / PWGA26O / TAUB0I13 / TAUB0O13 / MEMC0AD9
A10	P10_12 / PWGA17O / FLXA0STPWT / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3 / MEMC0AD6
A11	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / MEMC0AD4 / TAUJ3I3 / TAUJ3O3
A12	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX / INTP1 / MEMC0AD0 / RLIN24RX / MODE2
A13	P19_3 / ADCA1I19S
A14	P19_0 / ADCA1I16S
A15	P18_14 / ADCA1I14S
A16	P18_6 / ADCA1I6S
A17	P18_3 / PWGA71O / ETNB0TXD2 / ADCA1I3S / TAUJ3I3 / TAUJ3O3
A18	P18_9 / ADCA1I9S
A19	P18_0 / CSIG1RYI / CSIG1RYO / ETNB0LINK / PWGA61O / ADCA1I0S / TAUJ3I0 / TAUJ3O0
A20	A1VSS
B1	P22_6
B2	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN / $\overline{\text{CSIH1SSI}}$ / MEMC0CLK / RLIN37RX / INTP17
B3	P10_1 / TAUD0I3 / TAUD0O3 / INTP18 / CAN0TX / PWGA1O / TAPA0UN / CSIH1SC / ETNB0RXD0 / MEMC0A20 / MODE0 / TAUJ3I0 / TAUJ3O0
B4	P22_8
B5	P12_1 / RLIN34RX / INTP14 / CSIH2CSS5 / PWGA57O / TAUB1I12 / TAUB1O12 / MEMC0A17
B6	P22_11
B7	P11_5 / CAN5RX / INTP5 / RLIN33TX / PWGA30O / CSIH3SI / TAUB1I5 / TAUB1O5 / MEMC0AD13 / SFMA0IO0
B8	P11_4 / CSIH2SI / CAN3TX / INTP21 / PWGA29O / TAUB1I3 / TAUB1O3 / MEMC0AD12 / SFMA0IO1
B9	P21_1
B10	P10_14 / ADCA1TRG0 / PWGA19O / FLXA0RXDA / RLIN32TX / $\overline{\text{CSIH3SSI}}$ / TAUB0I7 / TAUB0O7 / MEMC0AD8 / CAN7RX / INTP9
B11	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / FLXA0TXDB / ENCA0EC / PWGA5O / MEMC0AD2 / FLMD1 / TAUJ3I2 / TAUJ3O2
B12	P19_2 / ADCA1I18S
B13	P19_1 / ADCA1I17S
B14	P18_7 / ETNB0TXCLK / ADCA1I7S
B15	P18_13 / ADCA1I13S
B16	P18_4 / CSIH1CSS4 / ETNB0TXD3 / ADCA1I4S
B17	P18_2 / PWGA63O / ETNB0TXD1 / ADCA1I2S / TAUJ3I2 / TAUJ3O2
B18	P18_1 / PWGA62O / ETNB0TXD0 / ADCA1I1S / TAUJ3I1 / TAUJ3O1
B19	AP1_12 / ADCA1I12

Table 2B.8 Pin Assignment 272-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
B20	AP1_13 / ADCA1I13
C1	P22_4
C2	P22_5
C3	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP / CSIH1SO / ETNB0RXD1 / MEMC0A21 / RLIN37TX / MODE1
C4	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX / INTP0 / CSCXFOUT / PWGA0O / TAPA0UP / CSIH1SI / MEMC0A19 / ETNB0RXCLK / TAUJ1I3 / TAUJ1O3
C5	P12_2 / INTP19 / RLIN34TX / PWGA58O / TAUB1I14 / TAUB1O14 / MEMC0A18 / CSIG2RYI / CSIG2RYO
C6	P22_10
C7	P11_6 / RLIN33RX / INTP13 / CAN5TX / ADCA1TRG1 / PWGA31O / CSIH3SO / TAUB1I7 / TAUB1O7 / MEMC0AD14 / SFMA0SSL
C8	P22_14
C9	P11_3 / CSIH2SC / CAN3RX / INTP3 / PWGA28O / TAUB1I1 / TAUB1O1 / MEMC0AD11 / RLIN32TX / SFMA0IO2
C10	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / RLIN32RX / INTP12 / FLXA0TXENB / TAUB0I5 / TAUB0O5 / MEMC0AD7 / CAN7TX
C11	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / MEMC0AD1 / RLIN24TX / TAUJ3I1 / TAUJ3O1
C12	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO / MEMC0AD3 / FLXA0RXDB
C13	P18_15 / ADCA1I15S
C14	P18_12 / ADCA1I12S
C15	P18_11 / ADCA1I11S
C16	P18_10 / ADCA1I10S
C17	P18_8 / ADCA1I8S
C18	AP1_14 / ADCA1I14
C19	AP1_15 / ADCA1I15
C20	AP1_0 / ADCA1I0
D1	P10_15 / CSIH3RYI / CSIH3RYO / PWGA24O / RLIN22RX / TAUB0I9 / TAUB0O9 / $\overline{\text{MEMC0RD}}$
D2	P22_3
D3	P10_5 / TAUD0I11 / TAUD0O11 / CAN6RX / INTP6 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO / ETNB0RXD3 / PWGA54O
D4	BVCC
D5	BVCC
D6	P13_0 / MEMC0A19
D7	P12_0 / CAN2TX / PWGA56O / TAUB1I10 / TAUB1O10 / $\overline{\text{CSIG2SSI}}$ / MEMC0A16 / RLIN36RX / INTP16
D8	P11_7 / INTP5 / PWGA32O / CSIH3SC / TAUB1I9 / TAUB1O9 / MEMC0AD15 / SFMA0CLK
D9	P11_2 / CSIH2SO / RLIN32RX / INTP12 / RLIN20TX / PWGA27O / TAUB0I15 / TAUB0O15 / MEMC0AD10 / SFMA0IO3
D10	BVSS
D11	P10_11 / PWGA16O / RLIN31RX / INTP11 / FLXA0TXENA / CSIH1CSS0 / TAUB0I1 / TAUB0O1 / MEMC0AD5
D12	BVCC
D13	BVSS
D14	P18_5 / CSIH1CSS5 / ETNB0TXEN / ADCA1I5S
D15	ISOVSS
D16	ISOVCL
D17	BVCC

Table 2B.8 Pin Assignment 272-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
D18	AP1_1 / ADCA1I1
D19	AP1_2 / ADCA1I2
D20	AP1_3 / ADCA1I3
E1	P11_0 / CSIH2RYI / CSIH2RYO / ADCA1TRG2 / PWGA25O / RLIN22TX / TAUB0I11 / TAUB0O11 / $\overline{\text{MEMC0WR}}$
E2	P11_8 / $\overline{\text{CSIG1SSI}}$ / RLIN35TX / PWGA48O / TAUB1I11 / TAUB1O11 / $\overline{\text{MEMC0CS0}}$
E3	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / CAN6TX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$ / PWGA53O / ETNB0RXD2 / MEMC0A22
E4	BVCC
E17	A1VSS
E18	AP1_4 / ADCA1I4
E19	AP1_5 / ADCA1I5
E20	AP1_6 / ADCA1I6
F1	P22_2
F2	P22_1
F3	P11_9 / CSIG1SO / RLIN35RX / INTP15 / PWGA49O / TAUB1I13 / TAUB1O13 / $\overline{\text{MEMC0CS1}}$
F4	BVCC
F17	A1VREF
F18	AP1_7 / ADCA1I7
F19	AP1_9 / ADCA1I9
F20	AP1_10 / ADCA1I10
G1	P22_0
G2	P11_11 / CSIG1SI / RLIN25TX / PWGA51O / TAUB1I0 / TAUB1O0 / $\overline{\text{MEMC0CS3}}$ / ETNB0RXDV
G3	P11_10 / CSIG1SC / PWGA50O / TAUB1I15 / TAUB1O15 / $\overline{\text{MEMC0CS2}}$
G4	BVSS
G17	AP1_8 / ADCA1I8
G18	AP1_11 / ADCA1I11
G19	P20_6 / PWGA88O
G20	P20_7 / PWGA89O
H1	P21_4
H2	P11_12 / RLIN25RX / PWGA52O / TAUB1I2 / TAUB1O2 / $\overline{\text{MEMC0WAIT}}$
H3	P21_0
H4	ISOVCL
H17	EVCC
H18	P20_8 / PWGA90O
H19	P20_9 / PWGA91O
H20	P20_4 / RLIN23RX / INTP22 / PWGA59O / CAN7RX / INTP9 / $\overline{\text{CSIG3SSI}}$
J1	P13_3 / ETNB0RXERR
J2	P21_3
J3	P21_2
J4	ISOVSS
J9	BVSS
J10	BVSS
J11	BVSS
J12	BVSS
J17	EVSS
J18	P20_5 / RLIN23TX / INTP23 / PWGA60O / CAN7TX

Table 2B.8 Pin Assignment 272-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
J19	P20_0 / RLIN26RX / PWGA64O / CAN6RX / INTP6 / CSIG3SI
J20	P20_1 / RLIN26TX / PWGA65O / CAN6TX / CSIG3SO
K1	P13_4
K2	P13_6 / MEMC0A22 / PWGA72O
K3	P13_2 / ETNB0RXDV
K4	BVSS
K9	BVSS
K10	BVSS
K11	BVSS
K12	EVSS
K17	EVCC
K18	P20_3 / CAN4TX / PWGA67O / RLIN29TX / CSIG3RYI / CSIG3RYO
K19	P20_10 / PWGA92O
K20	P20_2 / CAN4RX / INTP4 / PWGA66O / RLIN29RX / CSIG3SC
L1	P12_3 / RLIN27RX / PWGA68O / CSIG2SI / $\overline{\text{MEMC0BEN0}}$ / TAUB1I6 / TAUB1O6
L2	P12_5 / PWGA70O / ETNB0MDC / CSIG2SO / TAUB1I4 / TAUB1O4
L3	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
L4	P13_5 / MEMC0A21
L9	BVSS
L10	EVSS
L11	EVSS
L12	EVSS
L17	REGVCC
L18	P20_13 / PWGA95O
L19	P20_12 / PWGA94O
L20	P20_11 / PWGA93O
M1	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
M2	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
M3	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
M4	P13_7 / MEMC0A23 / PWGA73O
M9	EVSS
M10	EVSS
M11	EVSS
M12	EVSS
M17	ISOVSS
M18	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / INTP16 / ADCA0I10S
M19	P9_4 / CSIH0CSS5 / PWGA33O / TAUJ1I0 / TAUJ1O0 / INTP17 / ADCA0I11S
M20	P20_14
N1	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 / DPIN8 / TAUB0I12 / TAUB0O12
N2	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
N3	P12_4 / RLIN27TX / PWGA69O / CSIG2SC / ETNB0MDIO / $\overline{\text{MEMC0BEN1}}$
N4	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
N17	EVSS

Table 2B.8 Pin Assignment 272-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
N18	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / ADCA0I2S / TAUJ1I1 / TAUJ1O1 / SENT1RX / RIIC1SDA
N19	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / ADCA0I3S / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / RIIC1SCL
N20	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S
P1	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / RLIN26RX / PWGA34O
P2	P0_12 / RIIC0SCL / DPIN13 / PWGA45O / TAUB0I10 / TAUB0O10 / CSIG0SI / RLIN26TX
P3	P0_14 / INTP17 / RLIN32TX / PWGA47O / TAUB0I14 / TAUB0O14 / CSIG0SC / CAN5TX
P4	EVCC
P17	AP0_6 / ADCA0I6
P18	AP0_3 / ADCA0I3
P19	AP0_1 / ADCA0I1
P20	AP0_0 / ADCA0I0
R1	P0_13 / RLIN32RX / INTP12 / PWGA46O / TAUB0I12 / TAUB0O12 / CSIG0SO / CAN5RX / INTP5
R2	P1_1 / INTP18 / RLIN33TX / TAUJ2I1 / TAUJ2O1
R3	P2_6 / ADCA0SEL2
R4	P1_3 / INTP19 / CAN3TX / DPIN23 / TAUJ2I3 / TAUJ2O3
R17	A0VREF
R18	AP0_7 / ADCA0I7
R19	AP0_4 / ADCA0I4
R20	AP0_2 / ADCA0I2
T1	P1_0 / RLIN33RX / INTP13 / TAUJ2I0 / TAUJ2O0
T2	P1_12 / CAN4RX / INTP4 / RLIN36TX
T3	P2_8 / RLIN210TX
T4	P2_9 / PWGA77O
T17	A0VSS
T18	AP0_10 / ADCA0I10
T19	AP0_8 / ADCA0I8
T20	AP0_5 / ADCA0I5
U1	P1_2 / CAN3RX / INTP3 / DPIN19 / TAUJ2I2 / TAUJ2O2
U2	P2_7 / RLIN210RX
U3	P2_11 / PWGA79O
U4	P8_12 / TAUJ1I3 / TAUJ1O3 / DPIN16 / PWGA44O / CSIH1CSS5 / INTP23 / RLIN25TX / ADCA0I19S
U5	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
U6	P1_9 / DPIN20 / INTP21
U7	EVCC
U8	AWOVCL
U9	REGVCC
U10	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / RLIN22RX / TAUB0I4 / TAUB0O4 / CAN4RX / INTP4
U11	ISOVSS
U12	ISOVCL
U13	P1_15 / RLIN23TX / CAN7TX
U14	EVSS
U15	EVCC
U16	P3_7 / PWGA86O
U17	P3_10

Table 2B.8 Pin Assignment 272-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
U18	AP0_13 / ADCA0I13
U19	AP0_11 / ADCA0I11
U20	AP0_9 / ADCA0I9
V1	P1_13 / CAN4TX / RLIN36RX / INTP16
V2	P2_12 / RLIN211RX
V3	P8_10 / CSIH3CSS3 / DPIN14 / PWGA42O / RLIN37RX / INTP17 / ADCA0I17S
V4	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
V5	JP0_0 / INTP0 / FPDR / FPDT / DCUTDI / LPDI / LPDIO / TAUJ2I0 / TAUJ2O0
V6	P1_11 / ADCA1TRG2 / RLIN24TX / DPIN22 / INTP14
V7	P2_13 / RLIN211TX
V8	P3_0 / PWGA76O
V9	FLMD0
V10	P0_8 / INTP16 / RLIN21TX / DPIN6 / CSIH0CSS6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2 / CAN3TX
V11	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0 / CAN3RX / INTP3
V12	P2_5 / RLIN29TX / ADCA0SEL1
V13	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / PWGA15O / INTP5 / CSIH1CSS3 / CAN6TX / ADCA0I1S / RIIC1SCL / SENT0SPCO
V14	P3_1 / PWGA80O
V15	P8_7 / CSIH3CSS0 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S
V16	P3_3 / PWGA82O
V17	P3_6 / PWGA85O
V18	P3_9
V19	AP0_14 / ADCA0I14
V20	AP0_12 / ADCA0I12
W1	P2_10 / PWGA78O
W2	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / RLIN37TX / ADCA0I4S
W3	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT
W4	JP0_1 / INTP1 / TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
W5	P2_0 / RLIN27RX / CAN6RX / INTP6
W6	P2_14 / PWGA74O
W7	P2_15 / PWGA75O
W8	IP0_0 / XT2
W9	P2_3 / RLIN28TX
W10	P2_2 / RLIN28RX
W11	JP0_6 / $\overline{\text{EVTO}}$
W12	P1_4 / RLIN35RX / INTP15 / DPIN18
W13	P2_4 / RLIN29RX / ADCA0SEL0
W14	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / PWGA14O / INTP4 / CSIH0CSS0 / CAN6RX / INTP6 / ADCA0I0S / RIIC1SDA / SENT0RX
W15	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / PWGA36O / CAN7RX / INTP9 / ADCA0I6S
W16	P3_2 / PWGA81O
W17	P8_8 / CSIH3CSS1 / PWGA40O / ADCA0SEL1 / RLIN34RX / INTP14 / ADCA0I15S
W18	P3_4 / PWGA83O
W19	P3_8 / PWGA87O
W20	AP0_15 / ADCA0I15
Y1	EVSS

Table 2B.8 Pin Assignment 272-Pin FPBGA (RH850/F1KM-S4)

Pin No.	Pin Name
Y2	P8_11 / TAUJ1I2 / TAUJ1O2 / DPIN15 / PWGA43O / CSIH1CSS4 / RLIN25RX / ADCA0I18S
Y3	JP0_4 / $\overline{\text{DCUTRST}}$
Y4	P2_1 / RLIN27TX / CAN6TX
Y5	P1_10 / RLIN24RX / DPIN21 / INTP22 / ADCA1TRG1
Y6	P1_8
Y7	$\overline{\text{RESET}}$
Y8	XT1
Y9	AWOVSS
Y10	X2
Y11	X1
Y12	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / RLIN22TX / TAUB0I6 / TAUB0O6 / CAN4TX
Y13	P1_5 / ADCA1TRG0 / RLIN35TX / DPIN17 / INTP20
Y14	P1_14 / RLIN23RX / CAN7RX / INTP9
Y15	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / INTP7 / PWGA23O / CAN7TX / ADCA0I5S
Y16	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / INTP9 / PWGA37O / ADCA0I7S
Y17	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
Y18	P8_9 / CSIH3CSS2 / PWGA41O / ADCA0SEL2 / RLIN34TX / ADCA0I16S
Y19	P3_5 / PWGA84O
Y20	A0VSS

2B.2 Pin Description

Table 2B.9 Pin Functions (RH850/F1KM-S4, RH850/F1KM-S2)

Pin Name	No. of Pins					IO	Pin Function	Unit
	100 Pins	144 Pins	176 Pins	233 Pins*1	272 Pins*1			
AnVREF	✓	✓	✓	✓	✓	—	ADCAn voltage supply and reference voltage	ADCAn
	n = 0	n = 0, 1	n = 0, 1	n = 0, 1	n = 0, 1			
AnVSS	✓	✓	✓	✓	✓	—	ADCAn ground	
	n = 0	n = 0, 1	n = 0, 1	n = 0, 1	n = 0, 1			
ADCA0Im	✓	✓	✓	✓	✓	I	ADCA0 input channel m with 12-bit resolution	
	m = 0 to 15	m = 0 to 15	m = 0 to 15	m = 0 to 15	m = 0 to 15			
ADCA1Im	—	✓	✓	✓	✓	I	ADCA1 input channel m with 12-bit resolution	
		m = 0 to 7	m = 0 to 15	m = 0 to 15	m = 0 to 15			
ADCA0ImS	✓	✓	✓	✓	✓	I	ADCA0 input channel m with 10-bit resolution	
	m = 2 to 11, 14 to 19	m = 0 to 11, 14 to 19	m = 0 to 11, 14 to 19	m = 0 to 11, 14 to 19	m = 0 to 11, 14 to 19			
ADCA1ImS	—	✓	✓	✓	✓	I	ADCA1 input channel m with 10-bit resolution	
		m = 0 to 3	m = 0 to 7	m = 0 to 19	m = 0 to 19			
ADCA0SELy	✓	✓	✓	✓	✓	O	Selection pin y for ADCA0 input and external MPX	
	y = 0 to 2	y = 0 to 2	y = 0 to 2	y = 0 to 2	y = 0 to 2			
ADCAnTRGy	✓	✓	✓	✓	✓	I	ADCAn external trigger pin y	
	n = 0, y = 0 to 2	n = 0, 1, y = 0 to 2	n = 0, 1, y = 0 to 2	n = 0, 1, y = 0 to 2	n = 0, 1, y = 0 to 2			
AP0_m	✓	✓	✓	✓	✓	IO	Analog port 0_m	Port
	m = 0 to 15	m = 0 to 15	m = 0 to 15	m = 0 to 15	m = 0 to 15			
AP1_m	—	✓	✓	✓	✓	IO	Analog port 1_m	
		m = 0 to 7	m = 0 to 15	m = 0 to 15	m = 0 to 15			
APO	✓	✓	✓	✓	✓	O	Port output signal for analog input	LPS0
AWOVCL	✓	✓	✓	✓	✓	—	Voltage regulator for Always-On area (AWO area) capacitor connection	Power
AWOVSS	✓	✓	✓	✓	✓	—	Internal logic for Always-On area (AWO area) ground	
BVCC	—	✓	✓	✓	✓	—	Port buffer voltage supply	
BVSS	—	✓	✓	✓	✓	—	Port buffer ground	
CANzRX	✓	✓	✓	✓	✓	I	CANz receive data input	RCFDCn
	z = 0 to 7	z = 0 to 7	z = 0 to 7	z = 0 to 7	z = 0 to 7			
CANzTX	✓	✓	✓	✓	✓	O	CANz transmit data output	
	z = 0 to 7	z = 0 to 7	z = 0 to 7	z = 0 to 7	z = 0 to 7			
CSCXFOUT	✓	✓	✓	✓	✓	O	Clock output	Clock
CSIGnRYI	✓	✓	✓	✓	✓	I	CSIGn ready (1) / busy (0) input signal	CSIGn
	n = 0	n = 0, 1	n = 0 to 3	n = 0 to 3	n = 0 to 3			
CSIGnRYO	✓	✓	✓	✓	✓	O	CSIGn ready (1) / busy (0) output signal	
	n = 0	n = 0, 1	n = 0 to 3	n = 0 to 3	n = 0 to 3			
CSIGnSC	✓	✓	✓	✓	✓	IO	CSIGn serial clock signal	
	n = 0	n = 0, 1	n = 0 to 3	n = 0 to 3	n = 0 to 3			
CSIGnSI	✓	✓	✓	✓	✓	I	CSIGn serial data input	
	n = 0	n = 0, 1	n = 0 to 3	n = 0 to 3	n = 0 to 3			
CSIGnSO	✓	✓	✓	✓	✓	O	CSIGn serial data output	
	n = 0	n = 0, 1	n = 0 to 3	n = 0 to 3	n = 0 to 3			
$\overline{\text{CSIGnSSI}}$	✓	✓	✓	✓	✓	I	CSIGn SS function control input signal	
	n = 0	n = 0, 1	n = 0 to 3	n = 0 to 3	n = 0 to 3			
CSIHnCSS0	✓	✓	✓	✓	✓	O	CSIHn serial peripheral chip select signal 0	CSIHn
	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3			
CSIHnCSS1	✓	✓	✓	✓	✓	O	CSIHn serial peripheral chip select signal 1	
	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3			

Table 2B.9 Pin Functions (RH850/F1KM-S4, RH850/F1KM-S2)

Pin Name	No. of Pins					IO	Pin Function	Unit
	100 Pins	144 Pins	176 Pins	233 Pins*1	272 Pins*1			
CSIHnCSS2	✓	✓	✓	✓	✓	O	CSIHn serial peripheral chip select signal 2	CSIHn
	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3			
CSIHnCSS3	✓	✓	✓	✓	✓	O	CSIHn serial peripheral chip select signal 3	
	n = 0, 2, 3	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3			
CSIHnCSS4	✓	✓	✓	✓	✓	O	CSIHn serial peripheral chip select signal 4	
	n = 0, 1	n = 0 to 2	n = 0 to 2	n = 0 to 2	n = 0 to 2			
CSIHnCSS5	✓	✓	✓	✓	✓	O	CSIHn serial peripheral chip select signal 5	
	n = 0, 1	n = 0 to 2	n = 0 to 2	n = 0 to 2	n = 0 to 2			
CSIHnCSS6	✓	✓	✓	✓	✓	O	CSIHn serial peripheral chip select signal 6	
	n = 0	n = 0	n = 0	n = 0	n = 0			
CSIHnCSS7	✓	✓	✓	✓	✓	O	CSIHn serial peripheral chip select signal 7	
	n = 0	n = 0	n = 0	n = 0	n = 0			
CSIHnRYI	✓	✓	✓	✓	✓	I	CSIHn ready (1) / busy (0) input signal	
	n = 0, 1	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3			
CSIHnRYO	✓	✓	✓	✓	✓	O	CSIHn ready (1) / busy (0) output signal	
	n = 0, 1	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3			
CSIHnSC	✓	✓	✓	✓	✓	IO	CSIHn serial clock signal	
	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3			
CSIHnSI	✓	✓	✓	✓	✓	I	CSIHn serial data input	
	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3			
CSIHnSO	✓	✓	✓	✓	✓	O	CSIHn serial data output	
	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3			
$\overline{\text{CSIHnSSI}}$	✓	✓	✓	✓	✓	I	CSIHn slave select input signal	
	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3	n = 0 to 3			
$\overline{\text{DCURDY}}$	✓	✓	✓	✓	✓	O	Debug ready	OCD
DCUTCK	✓	✓	✓	✓	✓	I	Debug clock	
DCUTDI	✓	✓	✓	✓	✓	I	Debug data input	
DCUTDO	✓	✓	✓	✓	✓	O	Debug data output	
DCUTMS	✓	✓	✓	✓	✓	I	Debug mode select	
$\overline{\text{DCUTRST}}$	✓	✓	✓	✓	✓	I	Debug reset	OCD
DPINm	✓	✓	✓	✓	✓	I	Digital port input m	LPS0
	m = 1 to 16	m = 0 to 23	m = 0 to 23	m = 0 to 23	m = 0 to 23			
DPO	✓	✓	✓	✓	✓	O	Port output signal for digital input	
ENCA0TINm	✓	✓	✓	✓	✓	I	ENCA0 capture trigger input m	ENCAn
	m = 0, 1	m = 0, 1	m = 0, 1	m = 0, 1	m = 0, 1			
ENCA0E0	✓	✓	✓	✓	✓	I	ENCA0 encoder input 0	
ENCA0E1	✓	✓	✓	✓	✓	I	ENCA0 encoder input 1	
ENCA0EC	✓	✓	✓	✓	✓	I	ENCA0 encoder clear input	
ETNB0LINK*1	—	—	✓	✓	✓	I	PHY link status	ETNBn
ETNB0MDC*1	—	—	✓	✓	✓	O	PHY management clock	
ETNB0MDIO*1	—	—	✓	✓	✓	IO	Management transmit / receive data signal	
ETNB0RXCLK*1	—	—	✓	✓	✓	I	MII receive clock	
ETNB0RXD[3:0]*1	—	—	✓	✓	✓	I	MII receive data input	
ETNB0RXDV*1	—	—	✓	✓	✓	I	MII receive data valid	
ETNB0RXERR*1	—	—	✓	✓	✓	I	MII receive error	

Table 2B.9 Pin Functions (RH850/F1KM-S4, RH850/F1KM-S2)

Pin Name	No. of Pins					IO	Pin Function	Unit
	100 Pins	144 Pins	176 Pins	233 Pins*1	272 Pins*1			
ETNB0TXCLK*1	—	—	✓	✓	✓	I	MII transmit clock	ETNBn
ETNB0TXD[3:0] *1	—	—	✓	✓	✓	O	MII transmit data output	
ETNB0TXEN*1	—	—	✓	✓	✓	O	MII transmit data enable	
EVCC	✓	✓	✓	✓	✓	—	Port buffer voltage supply	Power
EVSS	✓	✓	✓	✓	✓	—	Port buffer ground	
$\overline{\text{EVTO}}$	—	✓	✓	✓	✓	O	Event output	TEU_OUT
FLMD0	✓	✓	✓	✓	✓	I	Operating mode select pin 0	Mode
FLMD1	✓	✓	✓	✓	✓	I	Operating mode select pin 1	
FLXA0RXDA*1	✓	✓	✓	✓	✓	I	FLXA0 channel A receive data input	FLXAn
FLXA0RXDB*1	✓	✓	✓	✓	✓	I	FLXA0 channel B receive data input	
FLXA0STPWT*1	✓	✓	✓	✓	✓	I	FLXA0 stop watch trigger input	
FLXA0TXDA*1	✓	✓	✓	✓	✓	O	FLXA0 channel A transmit data output	
FLXA0TXDB*1	✓	✓	✓	✓	✓	O	FLXA0 channel B transmit data output	
FLXA0TXENA*1	✓	✓	✓	✓	✓	O	FLXA0 channel A transmit enable	
FLXA0TXENB*1	✓	✓	✓	✓	✓	O	FLXA0 channel B transmit enable	
FPDR	✓	✓	✓	✓	✓	I	Serial Communication Interface RXD	FLASH
FPDT	✓	✓	✓	✓	✓	O	Serial Communication Interface TXD	
FPCK	✓	✓	✓	✓	✓	I	Serial Communication Interface clock	
INTPm	✓	✓	✓	✓	✓	I	External interrupt input m	INTC
	m = 0 to 13	m = 0 to 23	m = 0 to 23	m = 0 to 23	m = 0 to 23			
IP0_0	—	✓	✓	✓	✓	I	Input port 0_0	Port
ISOVCL	✓	✓	✓	✓	✓	—	Voltage regulator for Isolated area (ISO area) capacitor connection	Power
ISOVSS	✓	✓	✓	✓	✓	—	Internal logic for Isolated area (ISO area) ground	
JP0_m	✓	✓	✓	✓	✓	IO	JTAG port 0_m	JTAG
	m = 0 to 5	m = 0 to 6	m = 0 to 6	m = 0 to 6	m = 0 to 6			
KR0Im	✓	✓	✓	✓	✓	I	KR0 key input signal	KRn
	m = 0 to 7	m = 0 to 7	m = 0 to 7	m = 0 to 7	m = 0 to 7			
LPDCLK	✓	✓	✓	✓	✓	I	LPD clock input (4-pin mode)	LPD
LPDCLKOUT	✓	✓	✓	✓	✓	O	LPD clock output (4-pin mode)	
LPDI	✓	✓	✓	✓	✓	I	LPD data input (4-pin mode)	
LPDIO	✓	✓	✓	✓	✓	IO	LPD data input / output (1-pin mode)	
LPDO	✓	✓	✓	✓	✓	O	LPD data output (4-pin mode)	
MEMC0Am*1	—	—	✓	✓	✓	O	MEMC0 address m	MEMCn
			m = 16 to 22	m = 16 to 22	m = 16 to 23			
MEMC0ADm*1	—	—	✓	✓	✓	IO	MEMC0 address / data m	
			m = 0 to 15	m = 0 to 15	m = 0 to 15			
$\overline{\text{MEMC0ASTB}}$ *1	—	—	✓	✓	✓	O	MEMC0 address strobe	
$\overline{\text{MEMC0BENm}}$ *1	—	—	✓	✓	✓	O	MEMC0 byte enable m	
			m = 0, 1	m = 0, 1	m = 0, 1			
MEMC0CLK*1	—	—	✓	✓	✓	O	MEMC0 clock output	
$\overline{\text{MEMC0CSm}}$ *1	—	—	✓	✓	✓	O	MEMC0 chip select m	
			m = 0 to 3	m = 0 to 3	m = 0 to 3			
$\overline{\text{MEMC0RD}}$ *1	—	—	✓	✓	✓	O	MEMC0 read strobe	
$\overline{\text{MEMC0WAIT}}$ *1	—	—	✓	✓	✓	I	MEMC0 wait input	
$\overline{\text{MEMC0WR}}$ *1	—	—	✓	✓	✓	O	MEMC0 write strobe	
MODEm	✓	✓	✓	✓	✓	I	Sub operating mode select	Mode
	m = 0 to 2	m = 0 to 2	m = 0 to 2	m = 0 to 2	m = 0 to 2			
NMI	✓	✓	✓	✓	✓	I	External non-maskable interrupt input	INTC

Table 2B.9 Pin Functions (RH850/F1KM-S4, RH850/F1KM-S2)

Pin Name	No. of Pins					IO	Pin Function	Unit
	100 Pins	144 Pins	176 Pins	233 Pins*1	272 Pins*1			
P0_m	✓	✓	✓	✓	✓	IO	Port 0_m	Port
	m = 0 to 14	m = 0 to 14	m = 0 to 14	m = 0 to 14	m = 0 to 14			
P1_m	—	✓	✓	✓	✓	IO	Port 1_m	
		m = 0 to 5, 8 to 11	m = 0 to 5, 8 to 15	m = 0 to 5, 8 to 15	m = 0 to 5, 8 to 15			
P2_m	—	—	✓	✓	✓	IO	Port 2_m	
			m = 0 to 6	m = 0 to 15	m = 0 to 15			
P3_m*1	—	—	—	✓	✓	IO	Port3_m	
				m = 0	m = 0 to 10			
P8_m	✓	✓	✓	✓	✓	IO	Port 8_m	
	m = 2 to 12	m = 0 to 12	m = 0 to 12	m = 0 to 12	m = 0 to 12			
P9_m	✓	✓	✓	✓	✓	IO	Port 9_m	
	m = 0 to 4	m = 0 to 4	m = 0 to 4	m = 0 to 4	m = 0 to 4			
P10_m	✓	✓	✓	✓	✓	IO	Port 10_m	
	m = 0 to 14	m = 0 to 15	m = 0 to 15	m = 0 to 15	m = 0 to 15			
P11_m	✓	✓	✓	✓	✓	IO	Port 11_m	
	m = 1 to 7	m = 0 to 12, 15	m = 0 to 12, 15	m = 0 to 12, 15	m = 0 to 12, 15			
P12_m	—	✓	✓	✓	✓	IO	Port 12_m	
		m = 0 to 2	m = 0 to 5	m = 0 to 5	m = 0 to 5			
P13_m*1	—	—	—	✓	✓	IO	Port 13_m	
				m = 0 to 7	m = 0 to 7			
P18_m	—	✓	✓	✓	✓	IO	Port 18_m	
		m = 0 to 3	m = 0 to 7	m = 0 to 15	m = 0 to 15			
P19_m*1	—	—	—	✓	✓	IO	Port19_m	
				m = 0 to 3	m = 0 to 3			
P20_m	—	✓	✓	✓	✓	IO	Port 20_m	
		m = 4, 5	m = 0 to 5	m = 0 to 5	m = 0 to 14			
P21_m*1	—	—	—	—	✓	IO	Port21_m	
					m = 0 to 4			
P22_m*1	—	—	—	—	✓	IO	Port22_m	
					m = 0 to 15			
PWGAnO	✓	✓	✓	✓	✓	O	PWGAn output signal	PWGAn
	n = 0 to 13, 16 to 23, 26 to 47	n = 0 to 63	n = 0 to 71	n = 0 to 79	n = 0 to 95			
REGVCC	✓	✓	✓	✓	✓	—	Voltage regulators voltage supply	Power
$\overline{\text{RESET}}$	✓	✓	✓	✓	✓	I	External reset input	Reset
$\overline{\text{RESETOUT}}$	✓	✓	✓	✓	✓	O	Reset output	
RIICnSCL	✓	✓	✓	✓	✓	IO	RIICn serial clock	RIICn
	n = 0, 1	n = 0, 1	n = 0, 1	n = 0, 1	n = 0, 1			
RIICnSDA	✓	✓	✓	✓	✓	IO	RIICn serial data	
	n = 0, 1	n = 0, 1	n = 0, 1	n = 0, 1	n = 0, 1			
RLIN2mRX	✓	✓	✓	✓	✓	I	RLIN2m receive data input	RLIN24n
	m = 0 to 2	m = 0 to 5	m = 0 to 9	m = 0 to 11	m = 0 to 11			
RLIN2mTX	✓	✓	✓	✓	✓	O	RLIN2m transmit data output	
	m = 0 to 2	m = 0 to 5	m = 0 to 9	m = 0 to 11	m = 0 to 11			
RLIN3nRX	✓	✓	✓	✓	✓	I	RLIN3n receive data input	RLIN3n
	n = 0 to 2	n = 0 to 5	n = 0 to 7	n = 0 to 7	n = 0 to 7			
RLIN3nTX	✓	✓	✓	✓	✓	O	RLIN3n transmit data output	
	n = 0 to 2	n = 0 to 5	n = 0 to 7	n = 0 to 7	n = 0 to 7			
RTCA0OUT	✓	✓	✓	✓	✓	O	RTCA0 1Hz output	RTCAn

Table 2B.9 Pin Functions (RH850/F1KM-S4, RH850/F1KM-S2)

Pin Name	No. of Pins					IO	Pin Function	Unit
	100 Pins	144 Pins	176 Pins	233 Pins*1	272 Pins*1			
SELDPk	✓	✓	✓	✓	✓	O	External multiplexer select signal output k for the digital port	LPS0
	k = 0 to 2	k = 0 to 2	k = 0 to 2	k = 0 to 2	k = 0 to 2			
SENTnRX	✓	✓	✓	✓	✓	I	SENT receive data input	RSENTn
	n = 1	n = 0 to 1	n = 0 to 1	n = 0 to 1	n = 0 to 1			
SENTnSPCO	✓	✓	✓	✓	✓	O	SENT SPC Extension Output	
	n = 1	n = 0 to 1	n = 0 to 1	n = 0 to 1	n = 0 to 1			
SFMA0CLK	—	✓	✓	✓	✓	O	SFMA0 clock	SFMAn
SFMA0IOm	—	✓	✓	✓	✓	IO	SFMA0 master data input / output	
		m = 0 to 3	m = 0 to 3	m = 0 to 3	m = 0 to 3			
SFMA0SSL	—	✓	✓	✓	✓	O	SFMA0 slave select	
TAPA0ESO	✓	✓	✓	✓	✓	I	Hi-Z control	TAPAn
TAPA0UN	✓	✓	✓	✓	✓	O	Motor control output U phase (negative)	
TAPA0UP	✓	✓	✓	✓	✓	O	Motor control output U phase (positive)	
TAPA0VN	✓	✓	✓	✓	✓	O	Motor control output V phase (negative)	
TAPA0VP	✓	✓	✓	✓	✓	O	Motor control output V phase (positive)	
TAPA0WN	✓	✓	✓	✓	✓	O	Motor control output W phase (negative)	
TAPA0WP	✓	✓	✓	✓	✓	O	Motor control output W phase (positive)	
TAUBnIm	✓	✓	✓	✓	✓	I	TAUBn channel input m	TAUBn
	n = 0, m = 0 to 8, 10, 12 to 15	n = 0, m = 0 to 15	n = 0, 1, m = 0 to 15	n = 0, 1, m = 0 to 15	n = 0, 1, m = 0 to 15			
TAUBnOm	✓	✓	✓	✓	✓	O	TAUBn channel output m	
	n = 0, m = 0 to 8, 10, 12 to 15	n = 0, m = 0 to 15	n = 0, 1, m = 0 to 15	n = 0, 1, m = 0 to 15	n = 0, 1, m = 0 to 15			
TAUD0Im	✓	✓	✓	✓	✓	I	TAUD0 channel input m	TAUDn
	m = 0 to 15	m = 0 to 15	m = 0 to 15	m = 0 to 15	m = 0 to 15			
TAUD0Om	✓	✓	✓	✓	✓	O	TAUD0 channel output m	
	m = 0 to 15	m = 0 to 15	m = 0 to 15	m = 0 to 15	m = 0 to 15			
TAUJnIm	✓	✓	✓	✓	✓	I	TAUJn channel input m	TAUJn
	n = 0 to 3, m = 0 to 3	n = 0 to 3, m = 0 to 3	n = 0 to 3, m = 0 to 3	n = 0 to 3, m = 0 to 3	n = 0 to 3, m = 0 to 3			
TAUJnOm	✓	✓	✓	✓	✓	O	TAUJn channel output m	
	n = 0 to 3, m = 0 to 3	n = 0 to 3, m = 0 to 3	n = 0 to 3, m = 0 to 3	n = 0 to 3, m = 0 to 3	n = 0 to 3, m = 0 to 3			
X1, X2	✓	✓	✓	✓	✓	—	Main OSC connections	MOSC
XT1, XT2	—	✓	✓	✓	✓	—	Sub OSC connections	SOSC

Note 1. Only available for RH850/F1KM-S4.

CAUTION

When pin functions for a peripheral module are allocated to multiple pins, use the pins from the same port group or nearby pins as the pins for a given channel.

- **(e.g.)** When RS-CANFD channel 0 is used:

  CAN0TX P0_0 P10_1

  CAN0RX P0_1 P10_0

  Use one of the following pin combinations:

  - P0_0 and P0_1, or
  - P10_0 and P10_1.

  The combinations of P0_0 and P10_0, and P0_1 and P10_1 are not allowed.

Section 2C Pin Function of RH850/F1KM-S1

This section describes the pin and port functions.

2C.1 Pin Connection Diagram

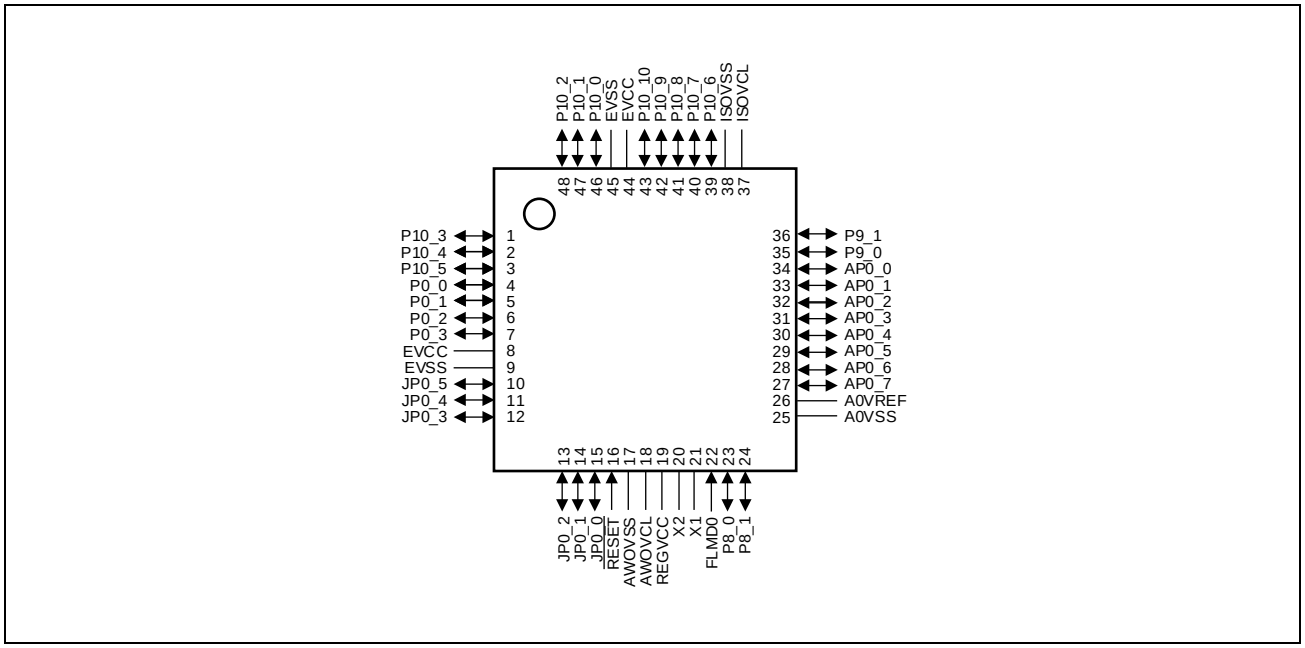


Figure 2C.1 Pin Connection Diagram (48-Pin LQFP)

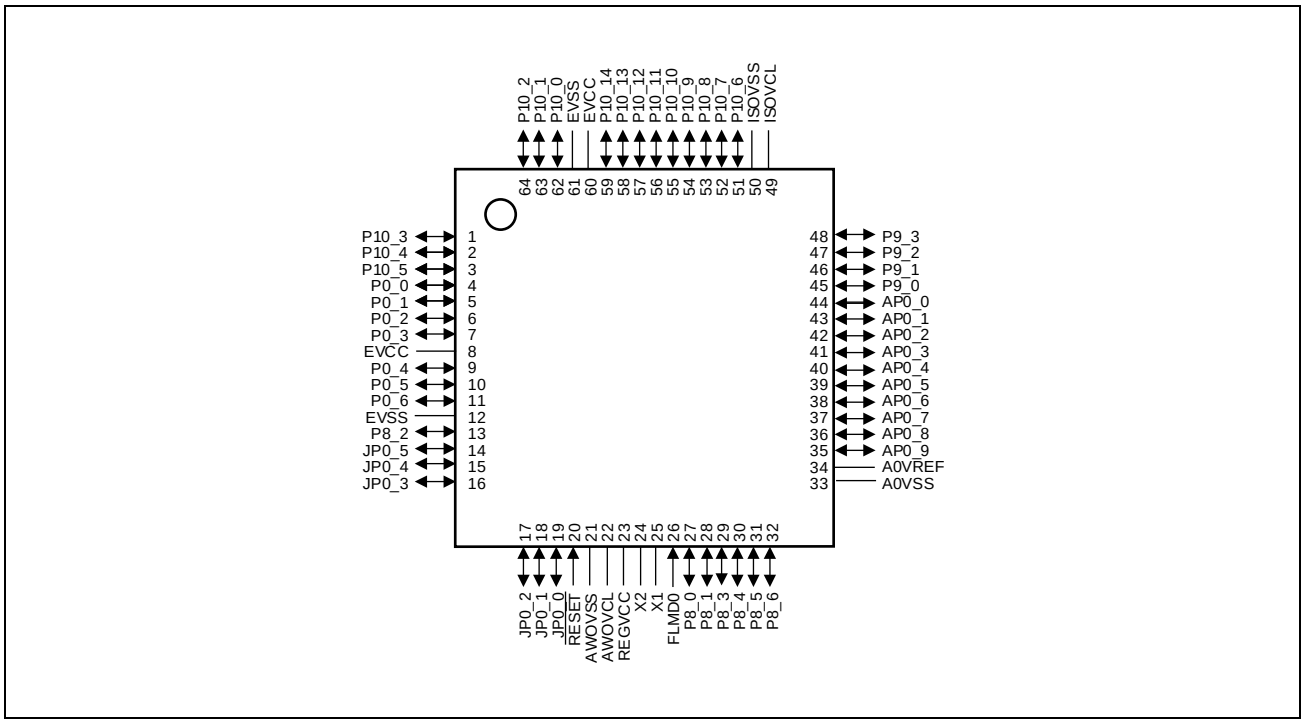


Figure 2C.2 Pin Connection Diagram (64-Pin LQFP)

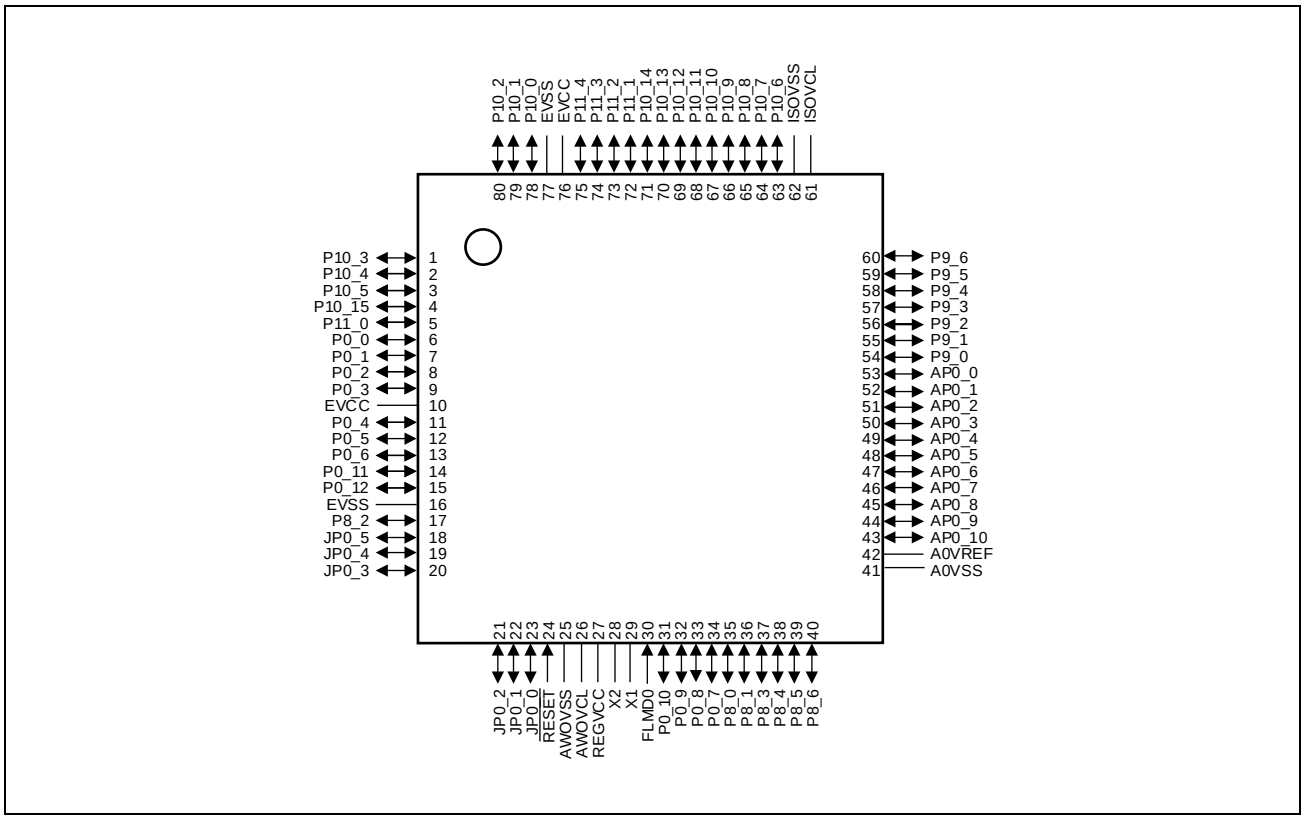


Figure 2C.3 Pin Connection Diagram (80-Pin LQFP)

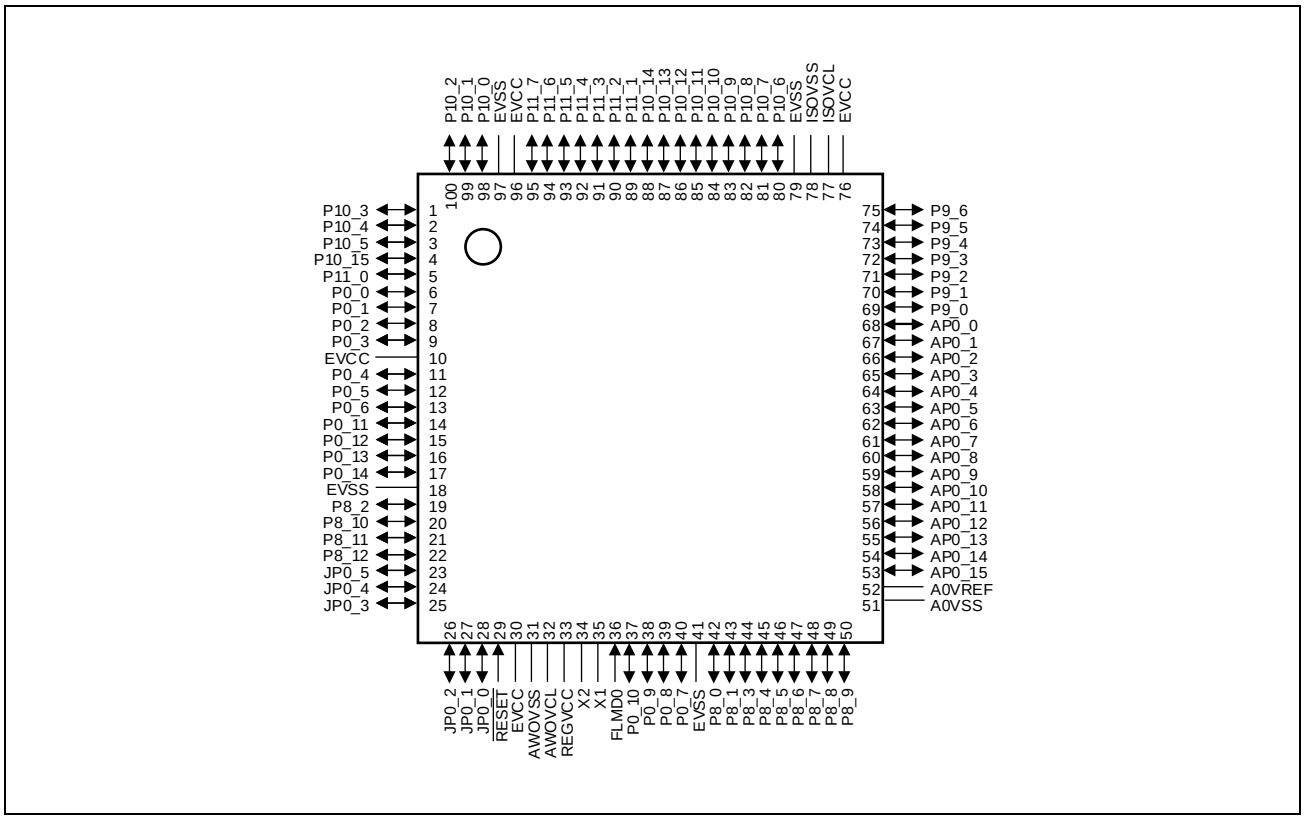


Figure 2C.4 Pin Connection Diagram (100-Pin LQFP)

Table 2C.1 Pin Assignment 48-Pin LQFP

Pin No.	Pin Name
1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN
2	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$
3	P10_5 / TAUD0I11 / TAUD0O11 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO
4	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
5	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
6	P0_2 / TAUD0I6 / TAUD0O6 / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
7	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / DPIN1 / CSIH0SO / TAUJ1I0 / TAUJ1O0
8	EVCC
9	EVSS
10	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT
11	JP0_4 / $\overline{\text{DCUTRST}}$
12	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
13	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
14	JP0_1 / INTP1 / TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
15	JP0_0 / INTP0 / FPDR / FPDT / TAUJ2I0 / TAUJ2O0 / DCUTDI / LPDI/ LPDIO
16	$\overline{\text{RESET}}$
17	AWOVSS
18	AWOVCL
19	REGVCC
20	X2
21	X1
22	FLMD0
23	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / INTP4 / CSIH0CSS0 / SENT0RX / ADCA0I0S / RIIC1SDA
24	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / INTP5 / SENT0SPCO / ADCA0I1S / RIIC1SCL
25	A0VSS
26	A0VREF
27	AP0_7 / ADCA0I7
28	AP0_6 / ADCA0I6
29	AP0_5 / ADCA0I5
30	AP0_4 / ADCA0I4
31	AP0_3 / ADCA0I3
32	AP0_2 / ADCA0I2
33	AP0_1 / ADCA0I1
34	AP0_0 / ADCA0I0
35	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / KR0I4 / TAUJ1I1 / TAUJ1O1 / SENT1RX / ADCA0I2S / RIIC1SDA
36	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / ADCA0I3S / RIIC1SCL
37	ISOVCL
38	ISOVSS
39	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / MODE2
40	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / TAUJ3I1 / TAUJ3O1
41	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / ENCA0EC / PWGA5O / TAUJ3I2 / TAUJ3O2 / FLMD1
42	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO
43	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / TAUJ3I3 / TAUJ3O3
44	EVCC

Table 2C.1 Pin Assignment 48-Pin LQFP

Pin No.	Pin Name
45	EVSS
46	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX / INTP0 / CSCXFOUT / PWGA0O / TAUJ1I3 / TAPA0UP / TAUJ1O3
47	P10_1 / TAUD0I3 / TAUD0O3 / CAN0TX / PWGA1O / TAUJ3I0 / TAPA0UN / TAUJ3O0 / MODE0
48	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP /MODE1

Table 2C.2 Pin Assignment 64-Pin LQFP

Pin No.	Pin Name
1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN
2	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$
3	P10_5 / TAUD0I11 / TAUD0O11 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO
4	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
5	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
6	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
7	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
8	EVCC
9	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / SELDP0 / DPIN8
10	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1
11	P0_6 / INTP2 / DPIN10 / SELDP2
12	EVSS
13	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / PWGA22O / ADCA0I4S
14	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT
15	JP0_4 / $\overline{\text{DCUTRST}}$
16	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
17	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
18	JP0_1 / INTP1 / TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
19	JP0_0 / INTP0 / FPDR / FPDT / TAUJ2I0 / TAUJ2O0 / DCUTDI / LPDI/ LPDIO
20	$\overline{\text{RESET}}$
21	AWOVSS
22	AWOVCL
23	REGVCC
24	X2
25	X1
26	FLMD0
27	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / PWGA14O / INTP4 / CSIH0CSS0 / SENT0RX / ADCA0I0S / RIIC1SDA
28	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / PWGA15O / INTP5 / SENT0SPCO / ADCA0I1S / RIIC1SCL
29	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / PWGA23O / ADCA0I5S
30	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / ADCA0I6S
31	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / ADCA0I7S
32	P8_6 / NMI / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
33	A0VSS
34	A0VREF
35	AP0_9 / ADCA0I9
36	AP0_8 / ADCA0I8
37	AP0_7 / ADCA0I7
38	AP0_6 / ADCA0I6
39	AP0_5 / ADCA0I5
40	AP0_4 / ADCA0I4
41	AP0_3 / ADCA0I3
42	AP0_2 / ADCA0I2
43	AP0_1 / ADCA0I1
44	AP0_0 / ADCA0I0

Table 2C.2 Pin Assignment 64-Pin LQFP

Pin No.	Pin Name
45	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / KR0I4 / TAUJ1I1 / TAUJ1O1 / SENT1RX / ADCA0I2S / RIIC1SDA
46	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / ADCA0I3S / RIIC1SCL
47	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / ADCA0I9S
48	P9_3 / KR0I7 / PWGA21O / TAUJ1I1 / TAUJ1O1 / ADCA0I10S
49	ISOVCL
50	ISOVSS
51	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX / INTP1 / MODE2
52	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / TAUJ3I1 / TAUJ3O1
53	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / ENCA0EC / PWGA5O / TAUJ3I2 / TAUJ3O2 / FLMD1
54	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO
55	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / TAUJ3I3 / TAUJ3O3
56	P10_11 / PWGA16O / RLIN31RX / INTP11
57	P10_12 / PWGA17O / RLIN31TX
58	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O
59	P10_14 / PWGA19O
60	EVCC
61	EVSS
62	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX / INTP0 / CSCXFOUT / PWGA0O / TAUJ1I3 / TAPA0UP / TAUJ1O3
63	P10_1 / TAUD0I3 / TAUD0O3 / CAN0TX / PWGA1O / TAUJ3I0 / TAPA0UN / TAUJ3O0 / MODE0
64	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP /MODE1

Table 2C.3 Pin Assignment 80-Pin LQFP

Pin No.	Pin Name
1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN / $\overline{\text{CSIH1SSI}}$
2	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$
3	P10_5 / TAUD0I11 / TAUD0O11 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO
4	P10_15 / TAUB0I9 / TAUB0O9
5	P11_0 / CSIH2RYI / CSIH2RYO / TAUB0I11 / TAUB0O11
6	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
7	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
8	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
9	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
10	EVCC
11	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 / DPIN8 / TAUB0I12 / TAUB0O12
12	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
13	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC
14	P0_11 / RIIC0SDA / CSIH1CSS2 / TAUB0I8 / TAUB0O8
15	P0_12 / RIIC0SCL / TAUB0I10 / TAUB0O10 / CSIG0SI
16	EVSS
17	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / ADCA0I4S
18	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT
19	JP0_4 / $\overline{\text{DCUTRST}}$
20	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
21	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
22	JP0_1 / INTP1 / TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
23	JP0_0 / INTP0 / FPDR / FPDT / TAUJ2I0 / TAUJ2O0 / DCUTDI / LPDI/ LPDIO
24	$\overline{\text{RESET}}$
25	AWOVSS
26	AWOVCL
27	REGVCC
28	X2
29	X1
30	FLMD0
31	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / TAUB0I6 / TAUB0O6
32	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / TAUB0I4 / TAUB0O4
33	P0_8 / RLIN21TX / DPIN6 / CSIH0CSS6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2
34	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0
35	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / PWGA14O / INTP4 / CSIH0CSS0 / SENT0RX / ADCA0I0S / RIIC1SDA
36	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / PWGA15O / INTP5 / CSIH1CSS3 / SENT0SPCO / ADCA0I1S / RIIC1SCL
37	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / INTP7 / PWGA23O / ADCA0I5S
38	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / ADCA0I6S
39	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / ADCA0I7S
40	P8_6 / NMI / CSIH0CSS4 / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
41	A0VSS
42	A0VREF
43	AP0_10 / ADCA0I10
44	AP0_9 / ADCA0I9

Table 2C.3 Pin Assignment 80-Pin LQFP

Pin No.	Pin Name
45	AP0_8 / ADCA0I8
46	AP0_7 / ADCA0I7
47	AP0_6 / ADCA0I6
48	AP0_5 / ADCA0I5
49	AP0_4 / ADCA0I4
50	AP0_3 / ADCA0I3
51	AP0_2 / ADCA0I2
52	AP0_1 / ADCA0I1
53	AP0_0 / ADCA0I0
54	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / TAUJ1I1 / TAUJ1O1 / SENT1RX / ADCA0I2S / RIIC1SDA
55	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / ADCA0I3S / RIIC1SCL
56	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S
57	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / ADCA0I10S
58	P9_4 / CSIH0CSS5 / TAUJ1I0 / TAUJ1O0 / ADCA0I11S
59	P9_5 / CSIH0CSS6 / TAUJ1I1 / TAUJ1O1 / ADCA0I12S
60	P9_6 / CSIH0CSS7 / ADCA0I13S
61	ISOVCL
62	ISOVSS
63	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX / INTP1 / MODE2
64	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / TAUJ3I1 / TAUJ3O1
65	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / ENCA0EC / PWGA5O / TAUJ3I2 / TAUJ3O2 / FLMD1
66	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO
67	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / TAUJ3I3 / TAUJ3O3
68	P10_11 / PWGA16O / RLIN31RX / INTP11 / CSIH1CSS0 / TAUB0I1 / TAUB0O1
69	P10_12 / PWGA17O / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3
70	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / RLIN32RX / INTP12 / TAUB0I5 / TAUB0O5
71	P10_14 / PWGA19O / RLIN32TX / TAUB0I7 / TAUB0O7
72	P11_1 / $\overline{\text{CSIH2SSI}}$ / RLIN20RX / CSIH0CSS7 / TAUB0I13 / TAUB0O13
73	P11_2 / CSIH2SO / RLIN32RX / INTP12 / RLIN20TX / TAUB0I15 / TAUB0O15
74	P11_3 / CSIH2SC / RLIN32TX
75	P11_4 / CSIH2SI
76	EVCC
77	EVSS
78	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX / INTP0 / CSCXFOUT / PWGA0O / TAUJ1I3 / TAPA0UP / CSIH1SI / TAUJ1O3
79	P10_1 / TAUD0I3 / TAUD0O3 / CAN0TX / PWGA1O / TAUJ3I0 / TAPA0UN / CSIH1SC / TAUJ3O0 / MODE0
80	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP / CSIH1SO / MODE1

Table 2C.4 Pin Assignment 100-Pin LQFP

Pin No.	Pin Name
1	P10_3 / TAUD0I7 / TAUD0O7 / RIIC0SCL / KR0I1 / PWGA3O / ADCA0TRG1 / TAPA0VN / $\overline{\text{CSIH1SSI}}$
2	P10_4 / TAUD0I9 / TAUD0O9 / RLIN21RX / KR0I2 / ADCA0SEL0 / ADCA0TRG2 / TAPA0WP / $\overline{\text{CSIG0SSI}}$
3	P10_5 / TAUD0I11 / TAUD0O11 / RLIN21TX / KR0I3 / ADCA0SEL1 / TAPA0WN / CSIG0RYI / CSIG0RYO
4	P10_15 / CSIH3RYI / CSIH3RYO / PWGA24O / RLIN22RX / TAUB0I9 / TAUB0O9
5	P11_0 / CSIH2RYI / CSIH2RYO / PWGA25O / RLIN22TX / TAUB0I11 / TAUB0O11
6	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / $\overline{\text{CSIH0SSI}}$ / DPO / TAUJ2I1 / TAUJ2O1
7	P0_1 / TAUD0I4 / TAUD0O4 / CAN0RX / INTP0 / RLIN20TX / PWGA11O / CSIH0SI / APO / TAUJ2I2 / TAUJ2O2
8	P0_2 / TAUD0I6 / TAUD0O6 / CAN1RX / INTP1 / RLIN30TX / PWGA12O / CSIH0SC / DPO / TAUJ2I3 / TAUJ2O3
9	P0_3 / TAUD0I8 / TAUD0O8 / RLIN30RX / INTP10 / CAN1TX / DPIN1 / PWGA13O / CSIH0SO / TAUJ1I0 / TAUJ1O0
10	EVCC
11	P0_4 / RLIN31RX / INTP11 / CAN2TX / PWGA10O / CSIH1SI / SELDP0 / DPIN8 / TAUB0I12 / TAUB0O12
12	P0_5 / CAN2RX / INTP2 / RLIN31TX / DPIN9 / SELDP1 / CSIH1SO / TAUB0I14 / TAUB0O14
13	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
14	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / PWGA34O
15	P0_12 / RIIC0SCL / DPIN13 / PWGA45O / TAUB0I10 / TAUB0O10 / CSIG0SI
16	P0_13 / RLIN32RX / INTP12 / PWGA46O / TAUB0I12 / TAUB0O12 / CSIG0SO / CAN5RX / INTP5
17	P0_14 / RLIN32TX / PWGA47O / TAUB0I14 / TAUB0O14 / CSIG0SC / CAN5TX
18	EVSS
19	P8_2 / TAUJ0I0 / TAUJ0O0 / DPIN2 / CSIH0CSS0 / INTP6 / PWGA22O / ADCA0I4S
20	P8_10 / CSIH3CSS3 / DPIN14 / PWGA42O / ADCA0I17S
21	P8_11 / TAUJ1I2 / TAUJ1O2 / DPIN15 / PWGA43O / CSIH1CSS4 / ADCA0I18S
22	P8_12 / TAUJ1I3 / TAUJ1O3 / DPIN16 / PWGA44O / CSIH1CSS5 / ADCA0I19S
23	JP0_5 / NMI / RTCA0OUT / TAUJ0I3 / TAUJ0O3 / $\overline{\text{DCURDY}}$ / LPDCLKOUT
24	JP0_4 / $\overline{\text{DCUTRST}}$
25	JP0_3 / INTP3 / CSCXFOUT / TAUJ0I2 / TAUJ0O2 / DCUTMS
26	JP0_2 / INTP2 / TAUJ0I1 / TAUJ0O1 / FPCK / DCUTCK / LPDCLK
27	JP0_1 / INTP1 / TAUJ0I0 / TAUJ0O0 / FPDT / DCUTDO / LPDO
28	JP0_0 / INTP0 / FPDR / FPDT / TAUJ2I0 / TAUJ2O0 / DCUTDI / LPDI/ LPDIO
29	$\overline{\text{RESET}}$
30	EVCC
31	AWOVSS
32	AWOVCL
33	REGVCC
34	X2
35	X1
36	FLMD0
37	P0_10 / INTP3 / CSIH1CSS1 / DPIN11 / RLIN22TX / TAUB0I6 / TAUB0O6 / CAN4TX
38	P0_9 / INTP12 / CSIH1CSS0 / DPIN7 / RLIN22RX / TAUB0I4 / TAUB0O4 / CAN4RX / INTP4
39	P0_8 / RLIN21TX / DPIN6 / CSIH0CSS6 / $\overline{\text{CSIH1SSI}}$ / TAUB0I2 / TAUB0O2 / CAN3TX
40	P0_7 / RLIN21RX / DPIN5 / CSCXFOUT / CSIH1RYI / CSIH1RYO / TAUB0I0 / TAUB0O0 / CAN3RX / INTP3
41	EVSS
42	P8_0 / TAUJ0I0 / TAUJ0O0 / DPIN2 / PWGA14O / INTP4 / CSIH0CSS0 / SENT0RX / ADCA0I0S / RIIC1SDA
43	P8_1 / TAPA0ESO / TAUJ0O1 / DPIN0 / PWGA15O / INTP5 / CSIH1CSS3 / SENT0SPCO / ADCA0I1S / RIIC1SCL
44	P8_3 / TAUJ0I1 / TAUJ0O1 / DPIN3 / CSIH0CSS1 / INTP7 / PWGA23O / ADCA0I5S

Table 2C.4 Pin Assignment 100-Pin LQFP

Pin No.	Pin Name
45	P8_4 / TAUJ0I2 / TAUJ0O2 / DPIN4 / CSIH0CSS2 / INTP8 / PWGA36O / ADCA0I6S
46	P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / PWGA37O / ADCA0I7S
47	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / $\overline{\text{RESETOUT}}$
48	P8_7 / CSIH3CSS0 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S
49	P8_8 / CSIH3CSS1 / PWGA40O / ADCA0SEL1 / ADCA0I15S
50	P8_9 / CSIH3CSS2 / PWGA41O / ADCA0SEL2 / ADCA0I16S
51	A0VSS
52	A0VREF
53	AP0_15 / ADCA0I15
54	AP0_14 / ADCA0I14
55	AP0_13 / ADCA0I13
56	AP0_12 / ADCA0I12
57	AP0_11 / ADCA0I11
58	AP0_10 / ADCA0I10
59	AP0_9 / ADCA0I9
60	AP0_8 / ADCA0I8
61	AP0_7 / ADCA0I7
62	AP0_6 / ADCA0I6
63	AP0_5 / ADCA0I5
64	AP0_4 / ADCA0I4
65	AP0_3 / ADCA0I3
66	AP0_2 / ADCA0I2
67	AP0_1 / ADCA0I1
68	AP0_0 / ADCA0I0
69	P9_0 / NMI / PWGA8O / TAUD0I0 / TAUD0O0 / ADCA0TRG0 / CSIH2CSS0 / KR0I4 / TAUJ1I1 / TAUJ1O1 / SENT1RX / ADCA0I2S / RIIC1SDA
70	P9_1 / INTP11 / PWGA9O / TAUD0I2 / TAUD0O2 / KR0I5 / CSIH2CSS1 / TAUJ1I2 / TAUJ1O2 / SENT1SPCO / ADCA0I3S / RIIC1SCL
71	P9_2 / KR0I6 / PWGA20O / TAPA0ESO / CSIH2CSS2 / ADCA0I9S
72	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / ADCA0I10S
73	P9_4 / CSIH0CSS5 / PWGA33O / TAUJ1I0 / TAUJ1O0 / ADCA0I11S
74	P9_5 / CSIH0CSS6 / PWGA34O / TAUJ1I1 / TAUJ1O1 / ADCA0I12S
75	P9_6 / CSIH0CSS7 / PWGA35O / ADCA0I13S
76	EVCC
77	ISOVCL
78	ISOVSS
79	EVSS
80	P10_6 / TAUD0I13 / TAUD0O13 / CSIG0SO / ENCA0TIN0 / ADCA0SEL2 / CAN1RX / INTP1 / MODE2
81	P10_7 / TAUD0I15 / TAUD0O15 / CSIG0SC / ENCA0TIN1 / PWGA4O / CAN1TX / TAUJ3I1 / TAUJ3O1
82	P10_8 / TAUD0I10 / TAUD0O10 / CSIG0SI / ENCA0EC / PWGA5O / TAUJ3I2 / TAUJ3O2 / FLMD1
83	P10_9 / TAUD0I12 / TAUD0O12 / RLIN30RX / INTP10 / ENCA0E0 / PWGA6O / CSIH0RYI / CSIH0RYO
84	P10_10 / TAUD0I14 / TAUD0O14 / RLIN30TX / ENCA0E1 / PWGA7O / CSIH0CSS1 / TAUJ3I3 / TAUJ3O3
85	P10_11 / PWGA16O / RLIN31RX / INTP11 / CSIH1CSS0 / TAUB0I1 / TAUB0O1
86	P10_12 / PWGA17O / RLIN31TX / CSIH1CSS1 / TAUB0I3 / TAUB0O3
87	P10_13 / $\overline{\text{CSIH0SSI}}$ / PWGA18O / RLIN32RX / INTP12 / TAUB0I5 / TAUB0O5
88	P10_14 / PWGA19O / RLIN32TX / $\overline{\text{CSIH3SSI}}$ / TAUB0I7 / TAUB0O7

Table 2C.4 Pin Assignment 100-Pin LQFP

Pin No.	Pin Name
89	P11_1 / $\overline{\text{CSIH2SSI}}$ / RLIN20RX / CSIH0CSS7 / PWGA26O / TAUB0I13 / TAUB0O13
90	P11_2 / CSIH2SO / RLIN32RX / INTP12 / RLIN20TX / PWGA27O / TAUB0I15 / TAUB0O15
91	P11_3 / CSIH2SC / CAN3RX / INTP3 / PWGA28O / RLIN32TX
92	P11_4 / CSIH2SI / CAN3TX / PWGA29O
93	P11_5 / CAN5RX / INTP5 / RLIN33TX / PWGA30O / CSIH3SI
94	P11_6 / RLIN33RX / INTP13 / CAN5TX / PWGA31O / CSIH3SO
95	P11_7 / INTP5 / PWGA32O / CSIH3SC
96	EVCC
97	EVSS
98	P10_0 / TAUD0I1 / TAUD0O1 / CAN0RX / INTP0 / CSCXFOUT / PWGA0O / TAUJ1I3 / TAPA0UP / CSIH1SI / TAUJ1O3
99	P10_1 / TAUD0I3 / TAUD0O3 / CAN0TX / PWGA1O / TAUJ3I0 / TAPA0UN / CSIH1SC / TAUJ3O0 / MODE0
100	P10_2 / TAUD0I5 / TAUD0O5 / RIIC0SDA / KR0I0 / PWGA2O / ADCA0TRG0 / TAPA0VP / CSIH1SO / MODE1

2C.2 Pin Description

Table 2C.5 Pin Functions

Pin Name	No. of Pins				IO	Pin Function	Unit
	48 Pins	64 Pins	80 Pins	100 Pins			
A0VREF	✓	✓	✓	✓	—	ADCAn voltage supply and reference voltage	ADCAn
A0VSS	✓	✓	✓	✓	—	ADCAn ground	
ADCA0Im	✓	✓	✓	✓	I	ADCA0 input channel m with 12-bit resolution	
	m = 0 to 7	m = 0 to 9	m = 0 to 10	m = 0 to 15			
ADCA0ImS	✓	✓	✓	✓	I	ADCA0 input channel m with 10-bit resolution	
	m = 0 to 3	m = 0 to 10	m = 0 to 13	m = 0 to 19			
ADCA0SELy	✓	✓	✓	✓	O	External MPX selection pin y for ADCA0 input	
	y = 0 to 2	y = 0 to 2	y = 0 to 2	y = 0 to 2			
ADCA0TRGy	✓	✓	✓	✓	I	ADCA0 external trigger pin y	
	y = 0 to 2	y = 0 to 2	y = 0 to 2	y = 0 to 2			
AP0_m	✓	✓	✓	✓	IO	Analog port 0_m	Port
	m = 0 to 7	m = 0 to 9	m = 0 to 10	m = 0 to 15			
APO	✓	✓	✓	✓	O	Port output signal for analog input	LPS0
AWOVCL	✓	✓	✓	✓	—	Voltage regulator for Always-On area (AWO area) capacitor connection	Power
AWOVSS	✓	✓	✓	✓	—	Internal logic for Always-On area (AWO area) ground	
CANzRX	✓	✓	✓	✓	I	CANz receive data input	RCFDCn
	z = 0	z = 0 to 2	z = 0 to 2	z = 0 to 5			
CANzTX	✓	✓	✓	✓	O	CANz transmit data output	
	z = 0	z = 0 to 2	z = 0 to 2	z = 0 to 5			
CSCXFOUT	✓	✓	✓	✓	O	Clock output	Clock
CSIG0RYI	✓	✓	✓	✓	I	CSIGn ready (1) / busy (0) input signal	CSIGn
CSIG0RYO	✓	✓	✓	✓	O	CSIGn ready (1) / busy (0) output signal	
CSIG0SC	✓	✓	✓	✓	IO	CSIGn serial clock signal	
CSIG0SI	✓	✓	✓	✓	I	CSIGn serial data input	
CSIG0SO	✓	✓	✓	✓	O	CSIGn serial data output	
$\overline{\text{CSIG0SSI}}$	✓	✓	✓	✓	I	CSIGn SS function control input signal	
CSIHnCSS0	✓	✓	✓	✓	O	CSIHn serial peripheral chip select signal 0	CSIHn
	n = 0	n = 0	n = 0 to 2	n = 0 to 3			
CSIHnCSS1	✓	✓	✓	✓	O	CSIHn serial peripheral chip select signal 1	
	n = 0	n = 0	n = 0 to 2	n = 0 to 3			
CSIHnCSS2	—	✓	✓	✓	O	CSIHn serial peripheral chip select signal 2	
		n = 0	n = 0 to 2	n = 0 to 3			
CSIHnCSS3	—	✓	✓	✓	O	CSIHn serial peripheral chip select signal 3	
		n = 0	n = 0 to 2	n = 0 to 3			
CSIHnCSS4	—	—	✓	✓	O	CSIHn serial peripheral chip select signal 4	
			n = 0	n = 0, 1			
CSIHnCSS5	—	—	✓	✓	O	CSIHn serial peripheral chip select signal 5	
			n = 0	n = 0, 1			
CSIHnCSS6	—	—	✓	✓	O	CSIHn serial peripheral chip select signal 6	
			n = 0	n = 0			
CSIHnCSS7	—	—	✓	✓	O	CSIHn serial peripheral chip select signal 7	
			n = 0	n = 0			
CSIHnRYI	✓	✓	✓	✓	I	CSIHn ready (1) / busy (0) input signal	
	n = 0	n = 0	n = 0 to 2	n = 0 to 3			
CSIHnRYO	✓	✓	✓	✓	O	CSIHn ready (1) / busy (0) output signal	
	n = 0	n = 0	n = 0 to 2	n = 0 to 3			
CSIHnSC	✓	✓	✓	✓	IO	CSIHn serial clock signal	
	n = 0	n = 0	n = 0 to 2	n = 0 to 3			

Table 2C.5 Pin Functions

Pin Name	No. of Pins				IO	Pin Function	Unit
	48 Pins	64 Pins	80 Pins	100 Pins			
CSIHnSI	✓	✓	✓	✓	I	CSIHn serial data input	CSIHn
	n = 0	n = 0	n = 0 to 2	n = 0 to 3			
CSIHnSO	✓	✓	✓	✓	O	CSIHn serial data output	
	n = 0	n = 0	n = 0 to 2	n = 0 to 3			
$\overline{\text{CSIHnSSI}}$	✓	✓	✓	✓	I	CSIHn slave select input signal	
	n = 0	n = 0	n = 0 to 2	n = 0 to 3			
$\overline{\text{DCURDY}}$	✓	✓	✓	✓	O	Debug ready	OCD
DCUTCK	✓	✓	✓	✓	I	Debug clock	
DCUTDI	✓	✓	✓	✓	I	Debug data input	
DCUTDO	✓	✓	✓	✓	O	Debug data output	
DCUTMS	✓	✓	✓	✓	I	Debug mode select	
$\overline{\text{DCUTRST}}$	✓	✓	✓	✓	I	Debug reset	
DPINm	✓	✓	✓	✓	I	Digital port input m	LPS0
	m = 0 to 2	m = 0 to 4, 8 to 10	m = 0 to 11	m = 0 to 16			
DPO	✓	✓	✓	✓	O	Port output signal for digital input	
ENCA0TINm	✓	✓	✓	✓	I	ENCA0 capture trigger input m	ENCAn
	m = 0, 1	m = 0, 1	m = 0, 1	m = 0, 1			
ENCA0EC	✓	✓	✓	✓	I	ENCA0 encoder clear input	
ENCA0E0	✓	✓	✓	✓	I	ENCA0 encoder input 0	
ENCA0E1	✓	✓	✓	✓	I	ENCA0 encoder input 1	
EVCC	✓	✓	✓	✓	—	Port buffer voltage supply	Power
EVSS	✓	✓	✓	✓	—	Port buffer ground	
FLMD0	✓	✓	✓	✓	I	Operating mode select pin 0	Mode
FLMD1	✓	✓	✓	✓	I	Operating mode select pin 1	
FPDR	✓	✓	✓	✓	I	Serial Communication Interface RXD	FLASH
FPDT	✓	✓	✓	✓	O	Serial Communication Interface TXD	
FPCK	✓	✓	✓	✓	I	Serial Communication Interface clock	
INTPm	✓	✓	✓	✓	I	External interrupt input m	INTC
	m = 0 to 5, 10, 11	m = 0 to 5, 10, 11	m = 0 to 8, 10 to 12	m = 0 to 8, 10 to 13			
ISOVCL	✓	✓	✓	✓	—	Voltage regulator for Isolated area (ISO area) capacitor connection	Power
ISOVSS	✓	✓	✓	✓	—	Internal logic for Isolated area (ISO area) ground	
JP0_m	✓	✓	✓	✓	IO	JTAG port 0_m	JTAG
	m = 0 to 5	m = 0 to 5	m = 0 to 5	m = 0 to 5			
KR0Im	✓	✓	✓	✓	I	KR0 key input signal	KRn
	m = 0 to 5	m = 0 to 7	m = 0 to 7	m = 0 to 7			
LPDCLK	✓	✓	✓	✓	I	LPD clock input (4-pin mode)	LPD
LPDCLKOUT	✓	✓	✓	✓	O	LPD clock output (4-pin mode)	
LPDI	✓	✓	✓	✓	I	LPD data input (4-pin mode)	
LPDIO	✓	✓	✓	✓	IO	LPD data input / output (1-pin mode)	
LPDO	✓	✓	✓	✓	O	LPD data output (4-pin mode)	
MODEm	✓	✓	✓	✓	I	Sub operating mode select (Boundary scan)	Mode
	m = 0 to 2	m = 0 to 2	m = 0 to 2	m = 0 to 2			
NMI	✓	✓	✓	✓	I	External non-maskable interrupt input	INTC
P0_m	✓	✓	✓	✓	IO	Port 0_m	Port
	m = 0 to 3	m = 0 to 6	m = 0 to 12	m = 0 to 14			
P8_m	✓	✓	✓	✓	IO	Port 8_m	
	m = 0 to 1	m = 0 to 6	m = 0 to 6	m = 0 to 12			
P9_m	✓	✓	✓	✓	IO	Port 9_m	
	m = 0 to 1	m = 0 to 3	m = 0 to 6	m = 0 to 6			

Table 2C.5 Pin Functions

Pin Name	No. of Pins				IO	Pin Function	Unit
	48 Pins	64 Pins	80 Pins	100 Pins			
P10_m	✓	✓	✓	✓	IO	Port 10_m	Port
	m = 0 to 10	m = 0 to 14	m = 0 to 15	m = 0 to 15			
P11_m	—	—	✓	✓	IO	Port 11_m	
			m = 0 to 4	m = 0 to 7			
PWGAnO	✓	✓	✓	✓	O	PWGAn output signal	PWGAn
	n = 0 to 12	n = 0 to 23	m =0 to 23	n = 0 to 47			
REGVCC	✓	✓	✓	✓	—	Voltage regulators voltage supply	Power
$\overline{\text{RESET}}$	✓	✓	✓	✓	I	External reset input	Reset
$\overline{\text{RESETOUT}}$	—	✓	✓	✓	O	Reset output	
RIICnSCL	✓	✓	✓	✓	IO	RIICn serial clock	RIICn
	n = 0 to 1	n = 0 to 1	n = 0 to 1	n = 0 to 1			
RIICnSDA	✓	✓	✓	✓	IO	RIICn serial data	
	n = 0 to 1	n = 0 to 1	n = 0 to 1	n = 0 to 1			
RLIN2mRX	✓	✓	✓	✓	I	RLIN2m receive data input	RLIN24n
	m = 0 to 1	m = 0 to 1	m = 0 to 1	m = 0 to 2			
RLIN2mTX	✓	✓	✓	✓	O	RLIN2m transmit data output	
	m = 0 to 1	m = 0 to 1	m = 0 to 1	m = 0 to 2			
RLIN3nRX	✓	✓	✓	✓	I	RLIN3n receive data input	RLIN3n
	n = 0	n = 0 to 1	n = 0 to 2	n = 0 to 3			
RLIN3nTX	✓	✓	✓	✓	O	RLIN3n transmit data output	
	n = 0	n = 0 to 1	n = 0 to 2	n = 0 to 3			
SENTnRX	✓	✓	✓	✓	I	SENT data input	RSENTn
	n = 0 to 1	n = 0 to 1	n = 0 to 1	n = 0 to 1			
SENTnSPCO	✓	✓	✓	✓	O	SENT SPC extension output	
	n = 0 to 1	n = 0 to 1	n = 0 to 1	n = 0 to 1			
RTCA0OUT	✓	✓	✓	✓	O	RTCA0 1Hz output	RTCAn
SELDPk	—	✓	✓	✓	O	External multiplexer selection output signal k for digital port	LPS0
		k = 0 to 2	k = 0 to 2	k = 0 to 2			
TAPA0ESO	✓	✓	✓	✓	I	Hi-Z control	TAPAn
TAPA0UN	✓	✓	✓	✓	O	Motor control output U phase (negative)	
TAPA0UP	✓	✓	✓	✓	O	Motor control output U phase (positive)	
TAPA0VN	✓	✓	✓	✓	O	Motor control output V phase (negative)	
TAPA0VP	✓	✓	✓	✓	O	Motor control output V phase (positive)	
TAPA0WN	✓	✓	✓	✓	O	Motor control output W phase (negative)	
TAPA0WP	✓	✓	✓	✓	O	Motor control output W phase (positive)	
TAUD0Im	✓	✓	✓	✓	I	TAUD0 channel input m	TAUDn
	m = 0 to 15	m = 0 to 15	m = 0 to 15	m = 0 to 15			
TAUD0Om	✓	✓	✓	✓	O	TAUD0 channel output m	
	m = 0 to 15	m = 0 to 15	m = 0 to 15	m = 0 to 15			
TAUB0Im	—	—	✓	✓	I	TAUBn channel input m	TAUBn
			m = 0 to 15	m = 0 to 15			
TAUB0Om	—	—	✓	✓	O	TAUBn channel output m	
			m = 0 to 15	m = 0 to 15			

Table 2C.5 Pin Functions

Pin Name	No. of Pins				IO	Pin Function	Unit
	48 Pins	64 Pins	80 Pins	100 Pins			
TAUJnIm	✓	✓	✓	✓	I	TAUJn channel input m	TAUJn
	n = 0 to 3 m = 0 to 3	n = 0 to 3 m = 0 to 3	n = 0 to 3 m = 0 to 3	n = 0 to 3 m = 0 to 3			
TAUJnOm	✓	✓	✓	✓	O	TAUJn channel output m	
	n = 0 to 3 m = 0 to 3	n = 0 to 3 m = 0 to 3	n = 0 to 3 m = 0 to 3	n = 0 to 3 m = 0 to 3			
X1, X2	✓	✓	✓	✓	—	MainOSC connections	MOSC

CAUTION

When pin functions for a peripheral module are allocated to multiple pins, use the pins from the same port group or nearby pins as the pins for a given channel.

- **(e.g.)** When RS-CANFD channel 0 is used:

  CAN0TX P0_0 P10_1

  CAN0RX P0_1 P10_0

  Use one of the following pin combinations:

  - P0_0 and P0_1, or
  - P10_0 and P10_1.

  The combinations of P0_0 and P10_0, and P0_1 and P10_1 are not allowed.

Section 3A Electrical Characteristics of RH850/F1KH-D8

3A.1 Overview

The electrical spec of this device is guaranteed by the following operational condition. But, this condition is different depends on each characteristics, so refer to each chapter for more detail.

3A.1.1 Pin Groups

3A.1.1.1 324-Pin Version

Symbol	Pin Group Supplied by	Related Pins/Ports
PgR0	REG0VCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
PgE	EVCC, EVSS	Related ports: JP0, P0, P1, P2, P3, P8, P9, P20, P23 Related pins: $\overline{\text{RESET}}$, FLMD0
PgB	BVCC, BVSS	Related ports: P10, P11, P12, P13, P18, P19, P21, P22, P24
PgA0	A0VREF, A0VSS	Related port: AP0
PgA1	A1VREF, A1VSS	Related port: AP1

3A.1.1.2 Reserved

3A.1.1.3 233-Pin Version

Symbol	Pin Group Supplied by	Related Pins/Ports
PgR0	REG0VCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
PgE	EVCC, EVSS	Related ports: JP0, P0, P1, P2, P3, P8, P9, P20 Related pins: $\overline{\text{RESET}}$, FLMD0
PgB	BVCC, BVSS	Related ports: P10, P11, P12, P13, P18, P19
PgA0	A0VREF, A0VSS	Related port: AP0
PgA1	A1VREF, A1VSS	Related port: AP1

3A.1.1.4 176-Pin Version

Symbol	Pin Group Supplied by	Related Pins/Ports
PgR0	REG0VCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
PgE	EVCC, EVSS	Related ports: JP0, P0, P1, P2, P8, P9, P20 Related pins: $\overline{\text{RESET}}$, FLMD0
PgB	BVCC, BVSS	Related ports: P10, P11, P12, P18
PgA0	A0VREF, A0VSS	Related port: AP0
PgA1	A1VREF, A1VSS	Related port: AP1

3A.1.2 General Measurement Conditions

3A.1.2.1 Common Conditions

- Power supply
  - REG0VCC = EVCC = VPOC*[1] to 5.5 V
  - REG1VCC = VPOC*[1] to 3.6 V, REG1VCC ≤ REG0VCC
  - BVCC = VPOC*[1] to REG0VCC
  - A0VREF = 3.0 V to 5.5 V
  - A1VREF = 3.0 V to 5.5 V
  - AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V
- Capacitance of the internal regulator
  - CAWOVCL: 0.1 µF ±30%
  - CISOVCL: 0.1 µF ±30% per pin
- Operating temperature
  - Tj = –40 to +130°C@R7F7017xx3ABG*[2]
  - Tj = –40 to +150°C@R7F7017xx4ABG*[2]
    @R7F7017yy3AFP*[2]

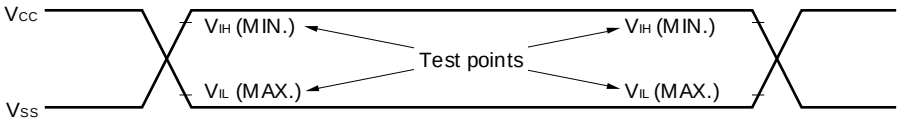
  xx = 10, 11, 14, 15
  yy = 08, 09
- Load conditions
  - CL = 30 pF

Note 1. “VPOC” means POC (power-on clear) detection voltage. For more detail, see **Section 3A.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.

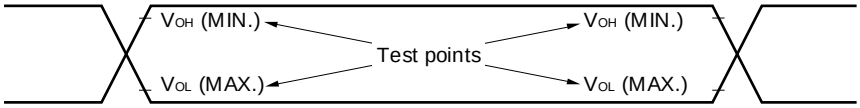
Note 2. Regarding operation temperature of each product, see **Section 1A.3, RH850/F1KH Product Lineup**.

3A.1.2.2 AC Characteristic Measurement Condition

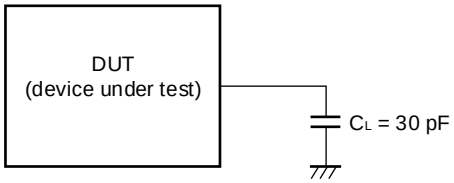
(1) AC Test Input Measurement Points



(2) AC Test Output Measurement Points



(3) Load Conditions



CAUTION

If the load capacitance exceeds 30pF due to the circuit configuration, it is recommended to insert a buffer in order to reduce capacitance to less than 30pF.

3A.2 Absolute Maximum Ratings

CAUTIONS

1. Do not directly connect outputs (or input/outputs) to each other, power supply and ground.
2. Even momentarily exceeding the absolute maximum rating for just one item creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings. The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.
3. When designing an external circuit ensure that the connections don't conflict with the port state of this device.

3A.2.1 Supply Voltages

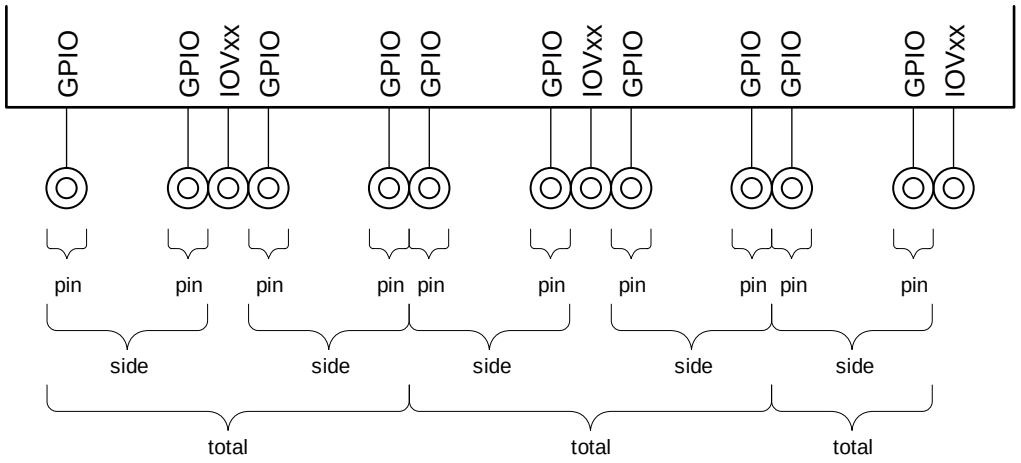
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System supply voltage	REG0VCC		–0.5		6.5	V
	REG1VCC		–0.5		6.5	V
	AWOVSS		–0.5		0.5	V
	ISOVSS		–0.5		0.5	V
Port supply voltage	EVCC		–0.5		6.5	V
	BVCC		–0.5		6.5	V
	EVSS		–0.5		0.5	V
	BVSS		–0.5		0.5	V
A/D-converter supply voltage	A0VREF		–0.5		6.5	V
	A1VREF		–0.5		6.5	V
	A0VSS		–0.5		0.5	V
	A1VSS		–0.5		0.5	V

3A.2.2 Port Voltages

Item	Pin Group*1	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	PgR0	VI		–0.5		REG0VCC + 0.5 (Do not exceed 6.5 V)	V
	PgE			–0.5		EVCC + 0.5 (Do not exceed 6.5 V)	V
	PgB			–0.5		BVCC + 0.5 (Do not exceed 6.5 V)	V
	PgA0			–0.5		A0VREF + 0.5 (Do not exceed 6.5 V)	V
	PgA1			–0.5		A1VREF + 0.5 (Do not exceed 6.5 V)	V

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

3A.2.3 Port Current



Definition of the condition:

- Per pin: Output current of one GPIO
- Per side: Total output current of all GPIO pins on one side of one IOVxx
- Total: Total output current of both sides of one IOVxx

Note:

- GPIO: General-purpose I/O pin (JP0, P0, P1, P2, P3, P8, P9, P10, P11, P12, P13, P18, P19, P20, P21, P22, P23, P24, AP0, AP1)
- IOVxx: Power supply pin for I/O pins (EVCC/EVSS, BVCC/BVSS, A0VREF/A0VSS, A1VREF/A1VSS)

3A.2.3.1 324-Pin Version

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (total of P9_0 to P9_4, P20_10 to P20_15)			–48	mA
			Per side (total of P20_0 to P20_9)			–48	mA
			Per side (total of P0_0 to P0_3)			–40	mA
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12)			–48	mA
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0)			–48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P1_4, P1_5, P1_14, P1_15, P2_2 to P2_5, P8_0, P8_1, P8_3 to P8_9)			–48	mA
			Per side (total of P3_1 to P3_12)			–48	mA
			Per side (total of P23_0 to P23_10)			–48	mA
			Total (EVCC)			–60	mA
		PgB	Per pin			–10	mA
			Per side (total of P18_0 to P18_7)			–48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)			–48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1)			–48	mA
			Per side (total of P10_0 to P10_2)			–30	mA
			Per side (total of P10_3 to P10_5)			–30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7)			–48	mA
			Per side (total of P21_0, P21_2 to P21_14, P22_0 to P22_2)			–48	mA
			Per side (total of P22_3 to P22_8)			–48	mA
			Per side (total of P21_1, P22_9 to P22_15)			–48	mA
			Per side (total of P24_0 to P24_7)			–48	mA
			Total (BVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
		PgA1	Per pin			–10	mA
			Total (A1VREF)			–48	mA

(324-pin version)

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0 to P9_4, P20_10 to P20_15)			48	mA
			Per side (total of P20_0 to P20_9)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12)			48	mA
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0, P8_2, P8_10 to P8_12)			48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P2_2, P2_3)			48	mA
			Per side (total of P1_4, P1_5, P1_14, P1_15, P2_4, P2_5, P8_0, P8_1, P8_3 to P8_9)			48	mA
			Per side (total of P3_3 to P3_12)			48	mA
			Per side (total of P23_0 to P23_10)			48	mA
			Total (EVCC)			60	mA
		PgB	Per pin			10	mA
			Per side (total of P18_0 to P18_7)			48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)			48	mA
			Per side (total of P10_6 to P10_14, P11_1, P11_2)			48	mA
			Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1)			48	mA
			Per side (total of P10_0 to P10_2)			30	mA
			Per side (total of P10_3 to P10_5)			30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7)			48	mA
			Per side (total of P21_0, P21_2 to P21_14 , P22_0 to P22_6)			48	mA
			Per side (total of P21_1, P22_7 to P22_15)			48	mA
			Per side (total of P24_0 to P24_7)			48	mA
			Total (BVCC)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VREF)			48	mA
		PgA1	Per pin			10	mA
			Total (A1VREF)			48	mA

3A.2.3.2 Reserved

3A.2.3.3 233-Pin Version

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			–48	mA
			Per side (total of P0_0 to P0_3)			–40	mA
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12)			–48	mA
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0)			–48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P1_4, P1_5, P1_14, P1_15, P2_2 to P2_5, P8_0, P8_1, P8_3 to P8_9)			–48	mA
			Total (EVCC)			–60	mA
		PgB	Per pin			–10	mA
			Per side (total of P18_0 to P18_7)			–48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)			–48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1)			–48	mA
			Per side (total of P10_0 to P10_2)			–30	mA
			Per side (total of P10_3 to P10_5)			–30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7)			–48	mA
			Total (BVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
		PgA1	Per pin			–10	mA
			Total (A1VREF)			–48	mA

(233-pin version)

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12)			48	mA
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0, P8_2, P8_10 to P8_12)			48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P2_2, P2_3)			48	mA
			Per side (total of P1_4, P1_5, P1_14, P1_15, P2_4, P2_5, P8_0, P8_1, P8_3 to P8_9)			48	mA
			Total (EVCC)			60	mA
		PgB	Per pin			10	mA
			Per side (total of P18_0 to P18_7)			48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)			48	mA
			Per side (total of P10_6 to P10_14, P11_1, P11_2)			48	mA
			Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1)			48	mA
			Per side (total of P10_0 to P10_2)			30	mA
			Per side (total of P10_3 to P10_5)			30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7)			48	mA
			Total (BVCC)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VREF)			48	mA
		PgA1	Per pin			10	mA
			Total (A1VREF)			48	mA

3A.2.3.4 176-Pin Version

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			–48	mA
			Per side (total of P0_0 to P0_3)			–40	mA
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6, P8_2, P8_10 to P8_12)			–48	mA
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11, P2_0, P2_1)			–48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P1_4, P1_5, P1_14, P1_15, P2_2 to P2_5, P8_0, P8_1, P8_3 to P8_9)			–48	mA
			Total (EVCC)			–60	mA
		PgB	Per pin			–10	mA
			Per side (total of P10_6 to P10_9, P18_0 to P18_7)			–48	mA
			Per side (total of P10_10 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2)			–48	mA
			Per side (total of P10_0 to P10_2)			–30	mA
			Per side (total of P10_3 to P10_5)			–30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5)			–48	mA
			Total (BVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
		PgA1	Per pin			–10	mA
			Total (A1VREF)			–48	mA
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6)			48	mA
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P2_0, P2_1, P8_2, P8_10 to P8_12)			48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P2_2, P2_3)			48	mA
			Per side (total of P1_4, P1_5, P1_14, P1_15, P2_4, P2_5, P8_0, P8_1, P8_3 to P8_9)			48	mA
			Total (EVSS)			60	mA
		PgB	Per pin			10	mA
			Per side (total of P18_0 to P18_7)			48	mA
			Per side (total of P10_6 to P10_14, P11_1, P11_2)			48	mA
			Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2)			48	mA
			Per side (total of P10_0 to P10_2)			30	mA
			Per side (total of P10_3 to P10_5)			30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5)			48	mA
			Total (BVSS)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA
		PgA1	Per pin			10	mA
			Total (A1VSS)			48	mA

3A.2.4 Temperature Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Storage temperature	Tstg		–55		150	°C
Junction temperature	Tj	R7F7017xx3ABG	–40		130	°C
		R7F7017xx4ABG R7F7017yy3AFP	–40		150	°C

Note: xx = 10, 11, 14, 15
yy = 08, 09

Regarding operation temperature of each product, see **Section 1A.3, RH850/F1KH Product Lineup**.

3A.3 Operational Condition

3A.3.1 Recommended Operating Conditions

Products of CPU frequency 240 MHz max.

(1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f_{CPUCLK_H}	CKDIVMD = 1			240	MHz
		CKDIVMD = 0			120	MHz
	f_{CPUCLK_M}				120	MHz
	f_{CPUCLK_L}	for OSTMn			60	MHz
		for MEMC*5				
	f_{CPUCLK_UL}				30	MHz
Peripheral clock (clock domain) frequency*1	f_{CKSCLK_AWDTA}	for WDTA0			240*2	kHz
	f_{CKSCLK_ATAUJ}	for TAUJ0			40	MHz
		for TAUJ2				
	f_{CKSCLK_ARTCA}	for RTCA0			4	MHz
	f_{CKSCLK_AADCA}	for ADCA0			40	MHz
	f_{CKSCLK_AFOUT}	for FOUT			24	MHz
	$f_{CKSCLK\_ICPUCLK}$	for CPU subsystem			240 / 120	MHz
	f_{CKSCLK_IPERI1}	for TAUD0			80	MHz
		for TAUJ1				
		for TAUJ3				
		for ENCA0				
		for TAPA0				
		for PIC0				
		for SFMA0				
	f_{CKSCLK_IPERI2}	for TAUBn			40	MHz
		for RCFDCn (clkc)				
		for RSENTn				
		for PWBAn				
		for PWGAn				
		for PWSAn				
		for MMCA0				
	f_{CKSCLK_ILIN}	for RLIN24n			40	MHz
		for RLIN3n				
	f_{CKSCLK_IADCA}	for ADCA1			40	MHz
	f_{CKSCLK_ICAN}	for RCFDCn (PCLK)			80	MHz
	$f_{CKSCLK\_ICANOSC}$	for RCFDCn (clk_xincan)			24	MHz
	f_{CKSCLK_ICSI}	for CSIGn			80	MHz
		for CSIHn				
	f_{CKSCLK_IIIC}	for RIICn			40	MHz
	$f_{LS\ IntOSC}$	for WDTA1			240*2	kHz
		for WDTA2				
	f_{EMCLK}	for LPSn			8	MHz

(2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply	REG0VCC	REG0VCC = EVCC	VPOC*3		5.5	V
	EVCC					
	REG1VCC	REG1VCC ≤ REG0VCC	VPOC*3		3.6	V
	BVCC		VPOC*3		REG0VCC	V
	A0VREF		3.0		5.5	V
	A1VREF					
Normal operation voltage	AWOVCL		1.1	1.25	1.35	V
	ISOVCL					
Limited operation voltage*4	AWOVCL		1.35		1.43	V
	ISOVCL					

Note 1. For clock specification of peripherals, see **Section 12AB, Clock Controller of RH850/F1KH-D8, RH850/F1KM-S4, RH850/F1KM-S2** of the ***RH850/F1KH, RH850/F1KM User's Manual: Hardware***.

Note 2. This frequency depends on the internal oscillator (LS IntOSC).

Note 3. "VPOC" means POC (power-on clear) detection voltage (TYP. 2.85 V). For detail, see **Section 3A.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.
In addition, the guaranteed operation in DC characteristic.
And AC characteristic is guaranteed when more than 3.0 V.
When the power supply voltage is VPOC to 3.0 V, the device does not malfunction.

Note 4. Reliability restrictions from 1.35 V to 1.43 V.

Note 5. Devided by 2 on MEMC internal.

Products of CPU frequency 160 MHz max.

(1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f_{CPUCLK_H}				160	MHz
	f_{CPUCLK_M}				80	MHz
	f_{CPUCLK_L}	for OSTMn			40	MHz
		for MEMC*5				
	f_{CPUCLK_UL}				20	MHz
Peripheral clock (clock domain) frequency*1	f_{CKSCLK_AWDTA}	for WDTA0			240*2	kHz
	f_{CKSCLK_ATAUJ}	for TAUJ0			40	MHz
		for TAUJ2				
	f_{CKSCLK_ARTCA}	for RTCA0			4	MHz
	f_{CKSCLK_AADCA}	for ADCA0			40	MHz
	f_{CKSCLK_AFOUT}	for FOUT			24	MHz
	$f_{CKSCLK\_ICPUCLK}$	for CPU subsystem			160	MHz
	f_{CKSCLK_IPERI1}	for TAUD0			80	MHz
		for TAUJ1				
		for TAUJ3				
		for ENCA0				
		for TAPA0				
		for PIC0				
		for SFMA0				
	f_{CKSCLK_IPERI2}	for TAUBn			40	MHz
		for RCFDCn (clkc)				
		for RSENTn				
		for PWBAn				
		for PWGAn				
		for PWSAn				
		for MMCA0				
	f_{CKSCLK_ILIN}	for RLIN24n			40	MHz
		for RLIN3n				
	f_{CKSCLK_IADCA}	for ADCA1			40	MHz
	f_{CKSCLK_ICAN}	for RCFDCn (pclk)			80	MHz
	$f_{CKSCLK\_ICANOSC}$	for RCFDCn (clk_xincan)			24	MHz
	f_{CKSCLK_ICSI}	for CSIGn			80	MHz
		for CSIHn				
	f_{CKSCLK_IIIC}	for RIICn			40	MHz
	$f_{LS\ IntOSC}$	for WDTA1			240*2	kHz
		for WDTA2				
	f_{EMCLK}	for LPSn			8	MHz
Power supply	REG0VCC	REG0VCC = EVCC	VPOC*3		5.5	V
	EVCC					
	REG1VCC	REG1VCC ≤ REG0VCC	VPOC*3		3.6	V
	BVCC		VPOC*3		REG0VCC	V
	A0VREF		3.0		5.5	V
	A1VREF					

(2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Normal operation voltage	AWOVCL		1.1	1.25	1.35	V
	ISOVCL					
Limited operation voltage*4	AWOVCL		1.35		1.43	V

Note 1. For clock specification of peripherals, see **Section 12AB, Clock Controller of RH850/F1KH-D8, RH850/F1KM-S4, RH850/F1KM-S2** of the ***RH850/F1KH, RH850/F1KM User's Manual: Hardware***.

Note 2. This frequency depends on the internal oscillator (LS IntOSC).

Note 3. "VPOC" means POC (power-on clear) detection voltage (TYP. 2.85 V). For detail, see **Section 3A.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.
In addition, the guaranteed operation in DC characteristic.
And AC characteristic is guaranteed when more than 3.0 V.
When the power supply voltage is VPOC to 3.0 V, the device does not malfunction.

Note 4. Reliability restrictions from 1.35 V to 1.43 V.

Note 5. Devided by 2 on MEMC internal.

3A.3.2 Oscillator Characteristics

Condition: REG0VCC = EVCC = VPOC to 5.5 V, REG1VCC = VPOC to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = VPOC to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C

(1) MainOSC (In Case of Using a Crystal/Ceramic)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MainOSC frequency*3	f_{MOSC}		8		24	MHz
MainOSC current consumption	I_{MOSC}	After stabilization		1.9*2	2.3*2	mA
MainOSC oscillation start point	V_{MOSCSP}		VPOC			V
MainOSC oscillation operating point	V_{MOSCOP}			0.5 × REG0VCC *2		V
MainOSC oscillation amplitude	$V_{MOSCAMP}$		0.4 × REG0VCC – 0.2*2			V
MainOSC oscillation stabilization time	t_{MSTB}			2*1,*2		ms
MainOSC transconductance	g_{m_MOSC}	MOSCS.MOSCCLKACT = 0, MOSCC.MOSCAMPSEL[1:0] = 00		11.1*2		mA/V
		MOSCS.MOSCCLKACT = 0, MOSCC.MOSCAMPSEL[1:0] = 01		10.6*2		mA/V
		MOSCS.MOSCCLKACT = 0, MOSCC.MOSCAMPSEL[1:0] = 10		9.3*2		mA/V
		MOSCS.MOSCCLKACT = 0, MOSCC.MOSCAMPSEL[1:0] = 11		7.8*2		mA/V
		MOSCS.MOSCCLKACT = 1, MOSCC.MOSCAMPSEL[1:0] = 00		8.6*2		mA/V
		MOSCS.MOSCCLKACT = 1, MOSCC.MOSCAMPSEL[1:0] = 01		7.8*2		mA/V
		MOSCS.MOSCCLKACT = 1, MOSCC.MOSCAMPSEL[1:0] = 10		6.1*2		mA/V
		MOSCS.MOSCCLKACT = 1, MOSCC.MOSCAMPSEL[1:0] = 11		4.0*2		mA/V

Note 1. Oscillator stabilization time is time until being set (“1”) in MOSCS.MOSCCLKACT bit after MOSCE.MOSCENTRG bit is written “1”, and depends on the setting value of MOSCST register. Please decide appropriate oscillation stabilization time by matching test with resonator and oscillation circuit.

Note 2. This is reference value.

Note 3. The following four crystal/ceramic resonator frequencies are supported: 8 MHz, 16 MHz, 20 MHz and 24 MHz.

(2) MainOSC (In Case of External Clock Input to X1)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
X1 clock Input frequency*1	f_{EX}		8		24	MHz
X1 clock Input cycle time	t_{EXCYC}		41.7		125	ns
X1 High level Input voltage	V_{IH}		0.7 × REG0VCC		REG0VCC + 0.5	V
		@Flash Programing Interface*2	0.8 × REG0VCC		REG0VCC + 0.5	V
X1 Low level Input voltage	V_{IL}		–0.5		0.3 × REG0VCC	V
		@Flash Programing Interface*2	–0.5		0.2 × REG0VCC	V
X1 Input leakage current	I_{LIH}	VI = REG0VCC			0.5	µA
	I_{LIL}	VI = 0 V			–0.5	µA
X1 clock Input low-level pulse width	t_{EXL}	f_{EX} = 8 MHz	58			ns
		f_{EX} = 16 MHz	26			ns
		f_{EX} = 20 MHz	20			ns
		f_{EX} = 24 MHz	16			ns
X1 clock Input high-level pulse width	t_{EXH}	f_{EX} = 8 MHz	58			ns
		f_{EX} = 16 MHz	26			ns
		f_{EX} = 20 MHz	20			ns
		f_{EX} = 24 MHz	16			ns
X1 clock Input period jitter			–0.3		0.3	ns

Note 1. The following four external clock input frequencies are supported: 8 MHz, 16 MHz, 20 MHz and 24 MHz.

Note 2. X2 should be open and its parasitic capacitance should be less than 5 pF.

(3) SubOSC

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SubOSC frequency	f_{SOSC}	Crystal	30	32.768	38	kHz
SubOSC current consumption	I_{SOSC}	After stabilization		1.5*2	4*2	µA
SubOSC DC operating point	$V_{SOSCDCOP}$			0.65*2		V
SubOSC oscillation stabilization time	t_{SSTB}			*1		s

Note 1. Oscillator stabilization time is time until being set (“1”) in SOSCS.SOSCCLKACT bit after SOSCE.SOSCENTRG bit is written “1”, and depends on the setting value of SOSCST register. Please decide appropriate oscillation stabilization time by matching test with resonator and oscillation circuit.

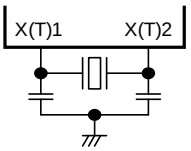
Note 2. This is reference value.

CAUTION

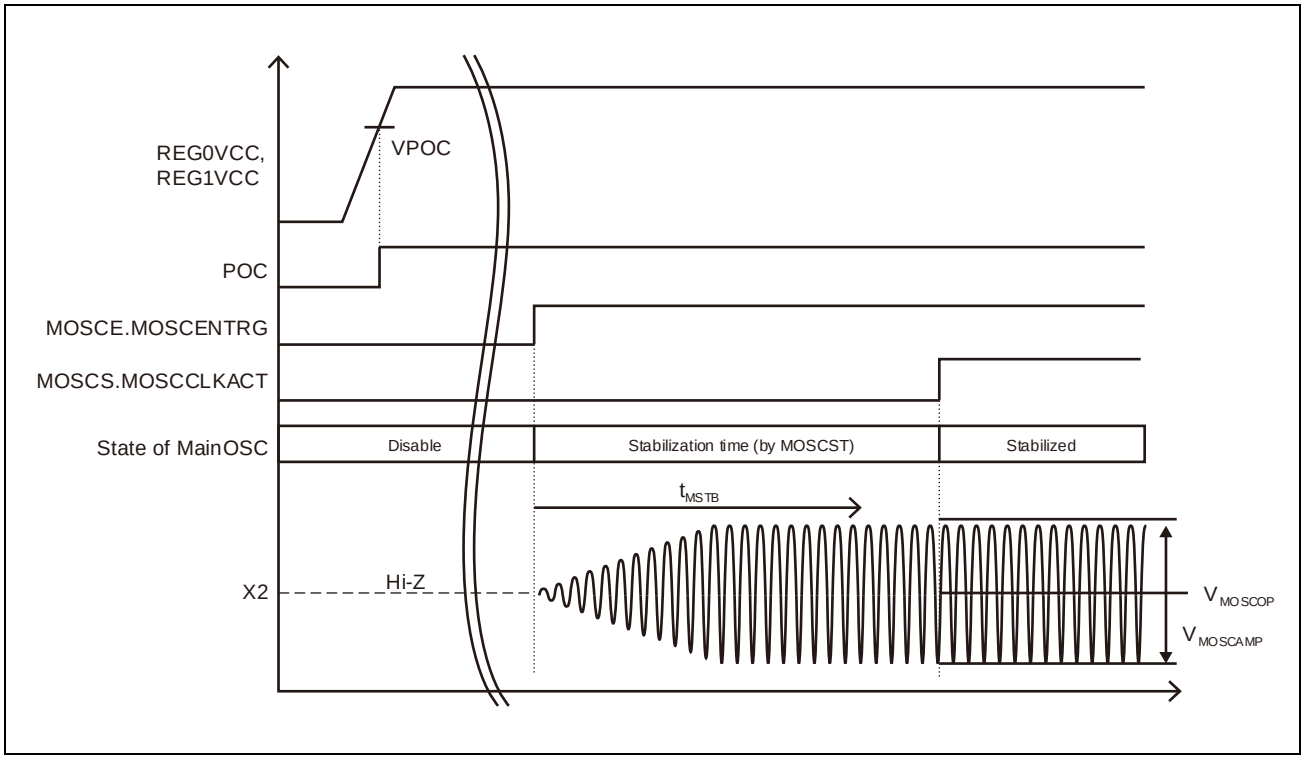
The oscillation stabilization time differs according the matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by an oscillator matching test.

NOTE

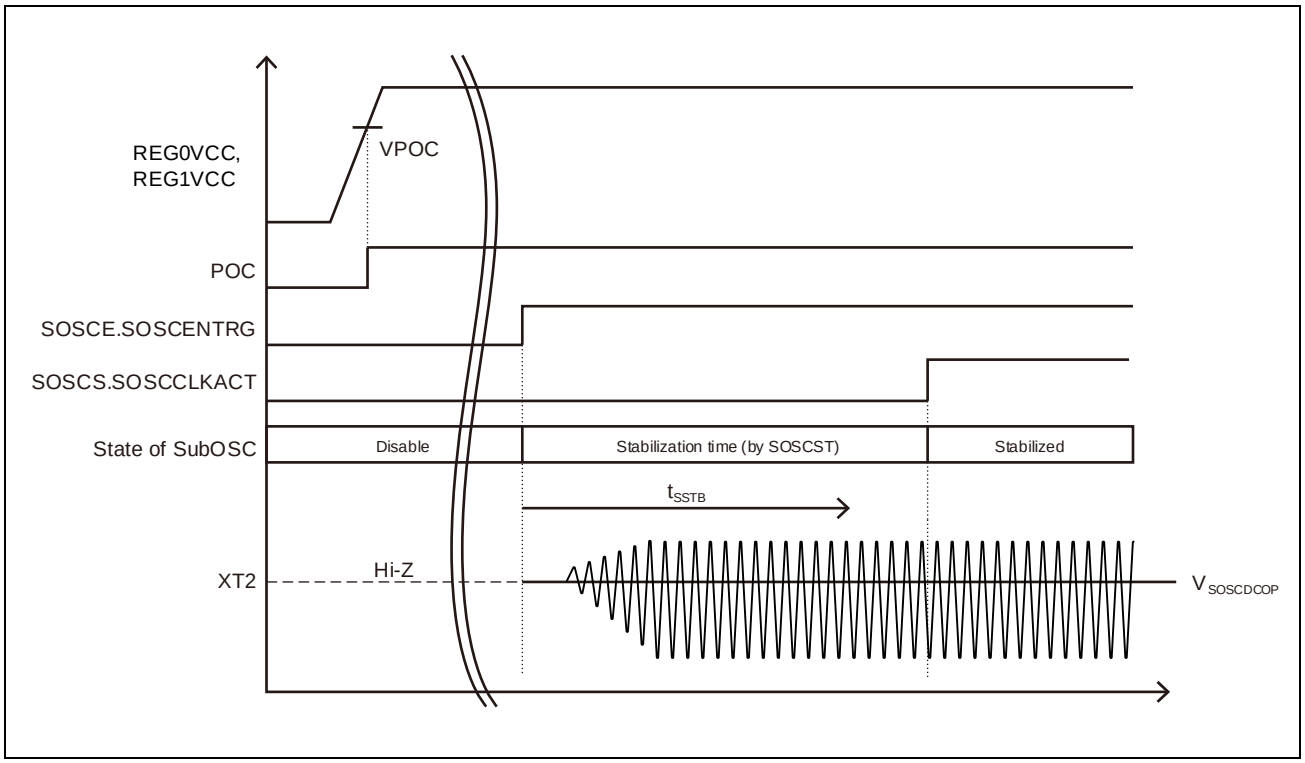
Recommended oscillator circuit is shown below.



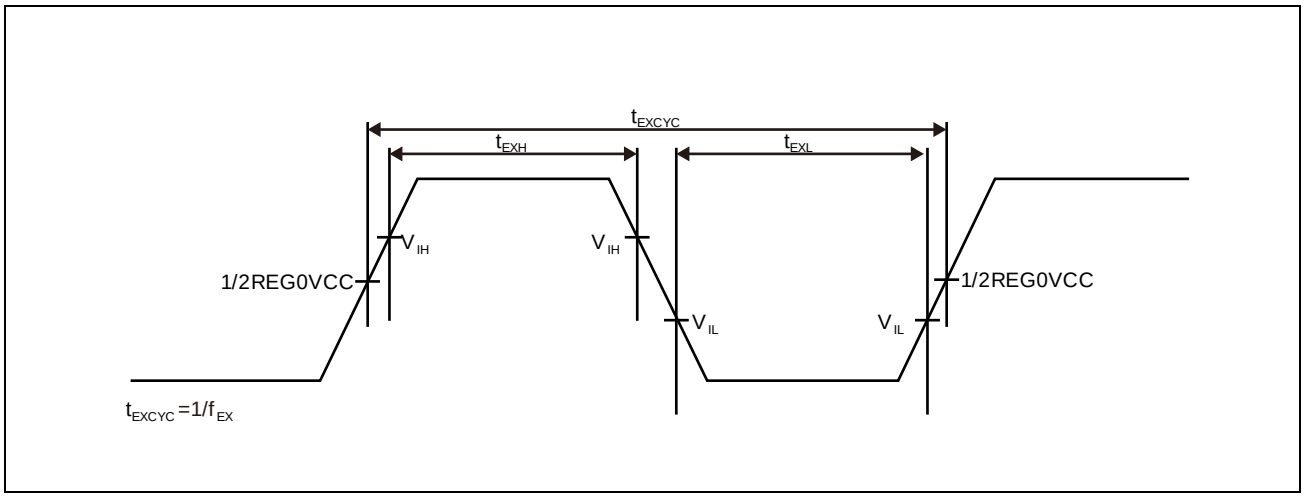
MainOSC



SubOSC



External clock



3A.3.3 Internal Oscillator Characteristics

Condition: REG0VCC = EVCC = VPOC to 5.5 V, REG1VCC = VPOC to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = VPOC to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LS IntOSC frequency	f_{RL}		220.8	240	259.2	kHz
HS IntOSC frequency*3	f_{RH}		7.6	8	8.4	MHz
		After user trimming @ trimming temp*2	7.92	8	8.08	MHz
HS IntOSC current consumption	I_{RH}	After stabilization			170*1	µA
HS IntOSC oscillation stabilization time	t_{RHSTB}				54.4	µs

Note 1. This is reference value.

Note 2. The HS IntOSC frequency may not meet the specification range (8.00 MHz ±0.08 MHz after user trimming @ trimming temp) in the while writing/erasing the code/data flash.

Note 3. The HS IntOSC frequency may not meet the specification range in the Cyclic STOP/Cyclic RUN mode.

3A.3.4 PLL Characteristics

3A.3.4.1 PLL0 (for CPU, with SSCG) Characteristics

Condition: REG0VCC = EVCC = VPOC to 5.5 V, REG1VCC = VPOC to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = VPOC to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Input frequency	$f_{PLL0CLKIN}$	MainOSC			8		24	MHz
		HS IntOSC*3			7.6	8.0	8.4	MHz
		HS IntOSC After user trimming @ trimming temp*3			7.92	8.0	8.08	MHz
Output frequency	$f_{CPLL0OUT}$	SSCG mode	MainOSC	Products of CPU frequency 240 MHz max.	105.8		240	MHz
				Products of CPU frequency 160 MHz max.	105.8		160	MHz
			HS IntOSC*3		67		84	MHz
			HS IntOSC After user trimming @ trimming temp*3		69.8		80.8	MHz
Modulation frequency	f_{MOD}				20		100	kHz
Frequency dithering range*2	f_{DIT}				0.82	1.0	1.18	%
					1.64	2.0	2.36	%
					2.46	3.0	3.54	%
					3.28	4.0	4.72	%
					4.10	5.0	5.90	%
					4.92	6.0	7.08	%
					6.56	8.0	9.44	%
					8.20	10.0	11.80	%
Lock time*1	t_{LCK0}	SSCG mode	PLL0ST = 0000 $1B80_H$		814.9	880	956.6	µs

Note 1. Lock time is time until being set (“1”) in PLL0S.PLL0CLKACT bit after PLL0E.PLL0ENTRG bit is written “1”.

Note 2. "Frequency dithering range” is set by PLL0ADJ[2:0] bits of PLL0C registers.

Note 3. The HS IntOSC has a frequency deviation. When the HSIntOSC is used the frequency deviation should be considered for the customer application as it affects peripheral functions (e.g. TAUx, ADCAn, etc.).

3A.3.4.2 PLL1 (for CPU/Peripheral) Characteristics

Condition: REG0VCC = EVCC = VPOC to 5.5 V, REG1VCC = VPOC to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = VPOC to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input frequency	$f_{PLL1CLKIN}$	MainOSC	8		24	MHz
		HS IntOSC*3	7.6	8.0	8.4	MHz
		HS IntOSC After user trimming @ trimming temp*3	7.92	8.0	8.08	MHz
Output frequency	$f_{CPLL1OUT}$	MainOSC	80		120	MHz
		HS IntOSC*3	76	80	84	MHz
	$f_{PPLLOUT}$		76	80	84	MHz
Output period jitter*1	t_{CPJ1}		–100		100	ps
Long term jitter*1	t_{LTJ}	term = 1 µs	–500		500	ps
		term = 10 µs	–1		1	ns
		term = 20 µs	–2		2	ns
Lock time*2	t_{LCK1}		104	112.3	122.1	µs

Note 1. This is reference value.

Note 2. Lock time is time until being set (“1”) in PLL1S.PLL1CLKACT bit after PLL1E.PLL1ENTRG bit is written “1”.

Note 3. The HS IntOSC has a frequency deviation. When the HSIntOSC is used the frequency deviation should be considered for the customer application as it affects peripheral functions (e.g. TAUx, ADCAn, etc.).

3A.4 DC Characteristics

3A.4.1 Capacitance

Condition: REG0VCC = REG1VCC = EVCC = BVCC = A0VREF = A1VREF = AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, Ta = 25°C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI*1	f = 1 MHz			10	pF
Input/output capacitance	CIO*2	0 V for non measurement pins			10	pF

Note 1. CI: Capacitance between the input pin and ground

Note 2. CIO: Capacitance between the input/output pin and ground

3A.4.2 Pin Characteristics

Condition: Some of the conditions mentioned in this chapter can be selected by software and described in the hardware user's manual.

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Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
$\overline{\text{RESET}}$	—	—	✓	—	—	—	—	—	—
FLMD0	—	✓	—	—	—	—	—	✓	✓
AP0_0	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_1	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_2	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_3	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_4	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_5	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_6	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_7	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_8	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_9	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_10	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_11	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_12	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_13	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_14	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_15	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_0	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_1	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_2	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_3	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_4	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_5	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_6	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_7	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_8	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_9	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_10	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_11	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_12	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_13	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_14	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_15	✓	—	—	—	—	✓	Slow	—	✓*1
IP0_0	—	—	—	—	—	—	—	—	—
JP0_0	—	✓	—	✓	✓	—	Slow	✓	✓
JP0_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
JP0_2	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
JP0_3	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
JP0_4	—	—	—	✓	—*5	—	Slow	✓	✓
JP0_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓

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Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
JP0_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_2	—	✓	—	✓	—	—	Slow/Fast*2	✓	✓
P0_3	—	✓	—	✓	—	—	Slow/Fast*2	✓	✓
P0_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_5	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P0_6	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P0_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_5	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P1_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_15	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_0	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P10_1	—	✓	—	✓	✓	—	Slow/Fast*3	✓	✓
P10_2	—	✓	—	✓	✓	—	Slow/Fast*3	✓	✓
P10_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_4	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P10_5	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P10_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓

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Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P10_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_15	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_2	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P11_3	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P11_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_6	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P11_7	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P11_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_10	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P11_11	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P11_12	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P11_15	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P12_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P12_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P12_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P12_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P12_4	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P12_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P13_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P13_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P13_2	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P13_3	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P13_4	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P13_5	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P13_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P13_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P18_0	—	✓	—	✓	✓	✓	Slow/Fast	✓	✓*4
P18_1	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_2	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_3	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_4	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_5	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_6	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_7	—	✓	—	✓	✓	✓	Slow/Fast	✓	✓*4
P18_8	—	✓	—	✓	✓	✓	Slow/Fast	✓	✓*4
P18_9	—	✓	—	✓	✓	✓	Slow/Fast	✓	✓*4

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Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P18_10	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_11	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_12	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_13	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_14	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_15	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P19_0	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P19_1	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P19_2	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P19_3	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P2_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_4	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P2_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_15	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_15	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P21_0	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P21_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓

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Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P21_2	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P21_3	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P21_4	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P21_5	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P21_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P21_7	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P21_8	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P21_9	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P21_10	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P21_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P21_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P21_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P21_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_0	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P22_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_6	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P22_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P22_15	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P23_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P23_1	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P23_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P23_3	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P23_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P23_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P23_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P23_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P23_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P23_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P23_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P24_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P24_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P24_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P24_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓

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Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P24_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P24_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P24_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P24_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P8_0	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_1	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_2	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_3	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_4	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_5	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_6	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_7	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_8	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_9	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_10	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_11	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_12	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_0	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_1	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_2	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_3	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_4	—	✓	—	✓	—	✓	Slow	✓	✓*4

Note 1. Pull-down resistor for ADC diagnostic purpose. Control via ADC self-diagnostic register.

Note 2. Supports Cload: 100 pF

Note 3. Supports Cload: 50 pF

Note 4. Pull-down resistors for ADC diagnostic and internal pull-down purposes. For ADC diagnostic, control via ADC self-diagnostic register. For internal pull-down, control via PD register.

Note 5. TTL is selected for Boundary scan mode or Nexus in normal operating mode.

Note 6. Only available for 324-pin devices.

Condition: REG0VCC = EVCC = VPOC to 5.5 V, REG1VCC = VPOC to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = VPOC to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

(1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH	CMOS		0.65 × IOVCC		IOVCC + 0.3	V
		SHMT1*3		0.65 × IOVCC		IOVCC + 0.3	V
		SHMT2		0.75 × IOVCC		IOVCC + 0.3	V
		SHMT4		0.8 × IOVCC		IOVCC + 0.3	V
		TTL	IOVCC = VPOC to 3.6 V	2.0		IOVCC + 0.3	V
			IOVCC = 3.6 V to 5.5 V	2.2		IOVCC + 0.3	V
		IP0_0 pin		0.7 × REG0VCC		REG0VCC	V
Low level input voltage	VIL	CMOS		–0.3		0.35 × IOVCC	V
		SHMT1		–0.3		0.35 × IOVCC	V
		SHMT2		–0.3		0.25 × IOVCC	V
		SHMT4		–0.3		0.5 × IOVCC	V
		TTL		–0.3		0.8	V
		IP0_0 pin		0		0.3 × REG0VCC	V
Input hysteresis for Schmitt	VH	SHMT1		0.3			V
		SHMT2		0.2 × IOVCC			V
		SHMT4		0.1			V
Input leakage current	ILIH	IP0_0 pin, VI = REG0VCC				0.5	µA
		$\overline{\text{RESET}}$, FLMD0, JP0, P0, P1, P2, P3, P8, P9, P20, P23 pin, VI = EVCC*2				0.5	µA
		P10, P11, P12, P13, P18, P19, P21, P22, P24 pin, VI = BVCC*2				0.5	µA
		AP0 pin, VI = A0VREF*2, Tj ≤ 130°C				0.3	µA
		AP0 pin, VI = A0VREF*2				0.5	µA
		AP1 pin, VI = A1VREF*2, Tj ≤ 130°C				0.3	µA
		AP1 pin, VI = A1VREF*2				0.5	µA
	ILIL	IP0_0 pin, VI = 0 V				–0.5	µA
		$\overline{\text{RESET}}$, FLMD0, JP0, P0, P1, P2, P3, P8, P9, P20 P23 pin, VI = 0 V*2				–0.5	µA
		P10, P11, P12, P13, P18, P19, P21, P22 P24 pin, VI = 0V*2				–0.5	µA
		AP0 pin, VI = 0 V*2, Tj ≤ 130°C				–0.3	µA
		AP0 pin, VI = 0 V*2				–0.5	µA
		AP1 pin, VI = 0 V*2, Tj ≤ 130°C				–0.3	µA
		AP1 pin, VI = 0 V*2				–0.5	µA
Internal pull-up resistance	RU	except FLMD0 pin, VI = 0 V		20 (275 µA)	40	100	kΩ
		FLMD0 pin, VI = 0V*3		4 (1375 µA)		36	kΩ
Internal pull-down resistance	RD	except FLMD0 pin, VI = IOVCC		20 (275 µA)	40	100	kΩ
		FLMD0 pin, VI = EVCC		4 (1375 µA)		36	kΩ

(2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High level output voltage	VOH	Fast mode	IOH = –5 mA (6 pins)*4	IOVCC – 1.0			V
			IOH = –3 mA (10 pins)*4	IOVCC – 1.0			V
			IOH = –1 mA (16 pins)*4	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins)*4	IOVCC – 0.5			V
		Slow mode	IOH = –1 mA (16 pins)*4	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins)*4	IOVCC – 0.5			V
Low level output voltage	VOL	Fast mode	IOL = 5 mA (6 pins)*4			0.4	V
			IOL = 3 mA (10 pins)*4			0.4	V
			IOL = 1 mA (16 pins)*4			0.4	V
		Slow mode	IOL = 1 mA (16 pins)*4			0.4	V
Rise/Fall time	t_{KRP}/t_{KFP}	Fast mode (except below pins)*5	CL = 30 pF			7	ns
			CL = 50 pF			12	ns
			CL = 100 pF			24	ns
		Fast mode (P0_5, P0_6, P1_5, P2_4, P10_1, P10_2, P11_2, P11_3, P11_6, P11_7, P23_1, P23_3)*6	CL = 50 pF			6	ns
		Fast mode (P0_2, P0_3)*6	CL = 100 pF			6.15	ns
		Slow mode*5	CL = 30 pF			37	ns
			CL = 50 pF			62	ns
			CL = 100 pF			124	ns
Output frequency	f_O	Fast mode	CL = 30 pF			40	MHz
		Slow mode	CL = 30 pF			10	MHz
			CL = 50 pF			6	MHz
			CL = 100 pF			3	MHz

Note 1. “IOVCC” means the pins are assigned to the power supply (EVCC, BVCC, A0VREF and A1VREF).

Note 2. Not select the analog input function of ADCn.

Note 3. When the internal pull-up resistor of FLMD0 pin is applied by FLMDCNT register, please connect 86 kΩ or more as external pull-down resistor.

Note 4. The number of pin indicates simultaneous ON.

Note 5. Measurement point: 0.1 × IOVCC to 0.9 × IOVCC

Note 6. Measurement point: 0.2 × IOVCC to 0.8 × IOVCC

3A.4.2.1 Output Current

(1) 324-Pin Version

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_10 to P20_15			–30	mA
				P20_0 to P20_9			–30	mA
				P0_0 to P0_3			–20	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0			–30	mA
				JP0_6, P0_7 to P0_10, P1_4, P1_5, P1_14, P1_15, P2_2 to P2_5, P8_0, P8_1, P8_3 to P8_9			–30	mA
				P3_1 to P3_12			–30	mA
				P23_0 to P23_10			–30	mA
			Total (EVCC)				–60	mA
		PgB	Per side	P18_0 to P18_7			–30	mA
				P18_8 to P18_15, P19_0 to P19_3			–30	mA
				P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1			–30	mA
				P10_0 to P10_2			–15	mA
				P10_3 to P10_5			–15	mA
				P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7			–30	mA
				P21_0, P21_2 to P21_14, P22_0 to P22_2			–30	mA
				P22_3 to P22_8			–30	mA
				P21_1, P22_9 to P22_15			–30	mA
				P24_0 to P24_7			–30	mA
			Total (BVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
		PgA1	Total (A1VREF)				–16	mA

(324-pin version)

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_10 to P20_15			30	mA
				P20_0 to P20_9			30	mA
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12			30	mA
				JP0_0 to JP0_5, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0, P8_2, P8_10 to P8_12			30	mA
				JP0_6, P0_7 to P0_10, P2_2, P2_3			30	mA
				P1_4, P1_5, P1_14, P1_15, P2_4, P2_5, P8_0, P8_1, P8_3 to P8_9			30	mA
				P3_1 to P3_12			30	mA
				P23_0 to P23_10			30	mA
			Total (EVCC)				60	mA
		PgB	Per side	P18_0 to P18_7			30	mA
				P18_8 to P18_15, P19_0 to P19_3			30	mA
				P10_6 to P10_14, P11_1, P11_2			30	mA
				P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1			30	mA
				P10_0 to P10_2			15	mA
				P10_3 to P10_5			15	mA
				P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7			30	mA
				P21_0, P21_2 to P21_14, P22_0 to P22_6			30	mA
				P21_1, P22_7 to P22_15			30	mA
				P24_0 to P24_7			30	mA
			Total (BVCC)				60	mA
		PgA0	Total (A0VREF)				16	mA
		PgA1	Total (A1VREF)				16	mA

Note: For detail of the definition of “side” and “total”, see **Section 3A.2.3, Port Current**.

(2) Reserved

(3) 233-Pin Version

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5			–30	mA
				P0_0 to P0_3			–20	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0			–30	mA
				JP0_6, P0_7 to P0_10, P1_4, P1_5, P1_14, P1_15, P2_2 to P2_5, P8_0, P8_1, P8_3 to P8_9			–30	mA
			Total (EVCC)				–60	mA
		PgB	Per side	P18_0 to P18_7			–30	mA
				P18_8 to P18_15, P19_0 to P19_3			–30	mA
				P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1			–30	mA
				P10_0 to P10_2			–15	mA
				P10_3 to P10_5			–15	mA
				P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7			–30	mA
			Total (BVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
		PgA1	Total (A1VREF)				–16	mA
Low-level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5			30	mA
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12			30	mA
				JP0_0 to JP0_5, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15 P3_0, P8_2, P8_10 to P8_12			30	mA
				JP0_6, P0_7 to P0_10, P2_2, P2_3			30	mA
				P1_4, P1_5, P1_14, P1_15, P2_4, P2_5, P8_0, P8_1, P8_3 to P8_9			30	mA
			Total (EVCC)				60	mA
		PgB	Per side	P18_0 to P18_7			30	mA
				P18_8 to P18_15, P19_0 to P19_3			30	mA
				P10_6 to P10_14, P11_1, P11_2			30	mA
				P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1			30	mA
				P10_0 to P10_2			15	mA
				P10_3 to P10_5			15	mA
				P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7			30	mA
			Total (BVCC)				60	mA
		PgA0	Total (A0VREF)				16	mA
		PgA1	Total (A1VREF)				16	mA

Note: For detail of the definition of “side” and “total”, see **Section 3A.2.3, Port Current**.

(4) 176-Pin Version

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5			–30	mA
				P0_0 to P0_3			–20	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2, P1_8 to P1_11, P2_0, P2_1			–30	mA
				JP0_6, P0_7 to P0_10, P1_4, P1_5, P1_14, P1_15, P2_2 to P2_5, P8_0, P8_1, P8_3 to P8_9			–30	mA
			Total (EVCC)				–60	mA
		PgB	Per side	P10_6 to P10_9, P18_0 to P18_7			–30	mA
				P10_10 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2			–30	mA
				P10_0 to P10_2			–15	mA
				P10_3 to P10_5			–15	mA
				P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5			–30	mA
			Total (BVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
		PgA1	Total (A1VREF)				–16	mA
Low-level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5			11	mA
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6			30	mA
				JP0_0 to JP0_5, P1_8 to P1_11, P2_0, P2_1, P8_2, P8_10 to P8_12			30	mA
				JP0_6, P0_7 to P0_10, P2_2, P2_3			30	mA
				P1_4, P1_5, P1_14, P1_15, P2_4, P2_5, P8_0, P8_1, P8_3 to P8_9			30	mA
			Total (EVCC)				60	mA
		PgB	Per side	P18_0 to P18_7			30	mA
				P10_6 to P10_14, P11_1, P11_2			30	mA
				P11_3 to P11_7, P11_15, P12_0 to P12_2			30	mA
				P10_0 to P10_2			15	mA
				P10_3 to P10_5			15	mA
				P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5			30	mA
			Total (BVCC)				60	mA
		PgA0	Total (A0VREF)				16	mA
		PgA1	Total (A1VREF)				16	mA

Note: For detail of the definition of “side” and “total”, see **Section 3A.2.3, Port Current**.

3A.4.3 Power Supply Currents

Condition: REG0VCC, REG1VCC, EVCC, BVCC, A0VREF and A1VREF total current. But the I/O buffer is stopped.

Products of CPU frequency 240 MHz max.

Item	Symbol	Condition					MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2	Power supply				
RUN mode current	IDDR	Run (240 MHz)	Run	–40 to 150°C	Run (#1)	Total		113	330	mA
						REG1VCC		92	290	mA
				25°C	Stop (#1)	Total		107		mA
						REG1VCC		88		mA
RUN mode current (During data/code flash programming)	IDDR3	Run (240 MHz)	Run	–40 to 150°C	Run (#2)	Total		133	350	mA
						REG1VCC		92	290	mA
RUN mode current (With code flash background operation)	IDDRBGO	Run (240 MHz)	Run	–40 to 150°C	Run (#6)	Total		133	350	mA
						REG1VCC		92	290	mA
RUN mode current (HALT state)	IDDH	Run (240 MHz)	Run	–40 to 150°C	Run (#3)	Total		108	325	mA
						REG1VCC		88	286	mA

Products of CPU frequency 160 MHz max.

Item	Symbol	Condition					MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2	Power supply				
RUN mode current	IDDR	Run (160 MHz)	Run	–40 to 150°C	Run (#1)	Total		83	293	mA
						REG1VCC		62	253	mA
				25°C	Stop (#1)	Total		77		mA
						REG1VCC		58		mA
RUN mode current (During data/code flash programming)	IDDR3	Run (160 MHz)	Run	–40 to 150°C	Run (#2)	Total		103	313	mA
						REG1VCC		62	253	mA
RUN mode current (With code flash background operation)	IDDRBGO	Run (160 MHz)	Run	–40 to 150°C	Run (#6)	Total		103	313	mA
						REG1VCC		62	253	mA
RUN mode current (HALT state)	IDDH	Run (160 MHz)	Run	–40 to 150°C	Run (#3)	Total		78	288	mA
						REG1VCC		58	249	mA

Products of CPU frequency 240 MHz max, 160 MHz max.

Item	Symbol	Condition					MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2	Power supply				
STOP mode current	IDDS	Stop	Stop	–40 to 90°C	Stop (#2)	Total		2.2	48	mA
						REG1VCC		2	45	mA
				110°C	Stop (#2)	Total			88	mA
						REG1VCC			83	mA
				135°C	Stop (#2)	Total			138	mA
						REG1VCC			130	mA
DeepSTOP mode current	IDDDS	Power off	Power off	–40 to 85°C	Stop (#3)	Total		52	800	µA
						REG1VCC		1	10	µA
				105°C	Stop (#3)	Total			1480	µA
						REG1VCC			30	µA
				125°C	Stop (#3)	Total			2140	µA
						REG1VCC			60	µA
Cyclic RUN mode current	IDDCR	Run (HS IntOSC)	Stop	–40 to 90°C	Run (#4)	Total		9.8	58	mA
						REG1VCC		9.1	49	mA
				115°C	Run (#4)	Total			97	mA
						REG1VCC			86	mA
				135°C	Run (#4)	Total			146	mA
						REG1VCC			133	mA
Cyclic STOP mode current	IDDCS	Stop	Stop	–40 to 90°C	Run (#5)	Total		2.4	50	mA
						REG1VCC		2.2	47	mA
				110°C	Run (#5)	Total			88	mA
						REG1VCC			83	mA
				135°C	Run (#5)	Total			138	mA
						REG1VCC			130	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- REG0VCC = EVCC = BVCC = A0VREF = A1VREF = 5.0 V
- REG1VCC = 3.3 V
- AWOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V

Note 2. Operating condition of each peripheral function is shown in the table of next page.

Caution: It must be ensured that the junction temperature in the Ta range remains below Tj ≤ 150°C and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

Function		Run						Stop		
		(#1)	(#2)	(#3)	(#4)	(#5)	(#6)	(#1)	(#2)	(#3)
AWO	MainOSC	Run	Run	Run	Stop	Stop	Run	Run	Stop	Stop
	SubOSC	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	HS IntOSC	Run	Run	Run	Run	Stop	Run	Run	Stop	Stop
	FOUT	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	LPS	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	RRAM	Read/Write	Read/Write	No access	Fetch	No access	Read/Write	Read/Write	No access	No access
	WDTA0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	TAUJ0, TAUJ2	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Run	Stop	Stop	Stop
	RTCA0	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Run	Stop	Stop	Stop
	CLMA0	Run	Run	Run	Run	Stop	Run	Stop	Stop	Stop
	CLMA1	Run	Run	Run	Stop	Stop	Run	Stop	Stop	Stop
	ADCA0	Run*1	Run*1	Run*1	Stop	Stop	Run*1	Stop	Stop	Stop

Function		Run						Stop		
		(#1)	(#2)	(#3)	(#4)	(#5)	(#6)	(#1)	(#2)	(#3)
ISO	CPU1 (PE1)	Run (PLL0)	Run (PLL0)	HALT (PLL0)	Run (HS IntOSC)	Stop	Run (PLL0)	Run (PLL0)	Stop	Power off
	CPU2 (PE2)	Run (PLL0)	Run (PLL0)	HALT (PLL0)	Stop	Stop	Run (PLL0)	Run (PLL0)	Stop	
	ICUMD	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	DMA	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	PLL0	Run	Run	Run	Stop	Stop	Run	Run	Stop	
	PLL1	Run	Run	Run	Stop	Stop	Run	Run	Stop	
	Code flash (FLI0)	Fetch	Fetch	No access	No access	No access	Fetch	Fetch	No access	
	Code flash (FLI1)	Fetch	Fetch	No access	No access	No access	Write/Erase	Fetch	No access	
	Code flash (FLI2)	Fetch	Fetch	No access	No access	No access	Fetch	Fetch	No access	
	Code flash (FLI3)	Fetch	Fetch	No access	No access	No access	Fetch	Fetch	No access	
	Data flash	Read	Write/Erase	No access	No access	No access	No access	Read	No access	
	LRAM (PE1)	Read/Write	Read/Write	No access	No access	No access	Read/Write	Read/Write	No access	
	LRAM (PE2)	Read/Write	Read/Write	No access	No access	No access	Read/Write	Read/Write	No access	
	GRAM	Read/Write*2	Read/Write*2	No access	No access	No access	Read/Write*2	Read/Write*2	No access	
	OSTMn	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	WDTA1	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	WDTA2	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	TAUD0	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	TAUBn	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	TAUJ1, TAUJ3	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	TAPA, PIC	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	ENCA0	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	PWM-diag	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	RLIN3n	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	RLIN24n	Wait	Wait	Wait	Stop	Stop	Wait	Stop	Stop	
	RCFDCn	Wait	Wait	Wait	Stop	Stop	Wait	Stop	Stop	
	CSIGn	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	CSIHn	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	RIICn	Wait	Wait	Wait	Stop	Stop	Wait	Stop	Stop	
	FlexRay	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	ETNBn	Wait	Wait	Wait	Stop	Stop	Wait	Stop	Stop	
	SFMA0	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	KR	Wait	Wait	Wait	Stop	Stop	Wait	Stop	Stop	
	RSENTn	Run	Run	Run	Stop	Stop	Wait	Stop	Stop	
	MMCAn	Run	Run	Run	Stop	Stop	Wait	Stop	Stop	
	CLMA2	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	CLMA3	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	ADCA1	Run	Run	Run	Stop	Stop	Run	Stop	Stop	

Note 1. T&H used.

Note 2. GRZF not used.

3A.4.4 Injection Currents

Table 3A.1 Definition of Pin Group (324-Pin Version)

Symbol	Power Supply for Pin Group	Pin
PgR0	REG0VCC, AWOVSS	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P2, P3, P20, P23
PgB	BVCC, BVSS	P10, P11, P12, P13, P21, P22, P24
PgE’	EVCC, EVSS	P8, P9
PgB’	BVCC, BVSS	P18, P19
PgA0	A0VREF, A0VSS	AP0
PgA1	A1VREF, A1VSS	AP1

Table 3A.2 Reserved

Table 3A.3 Definition of Pin Group (233-Pin Version)

Symbol	Power Supply for Pin Group	Pin
PgR0	REG0VCC, AWOVSS	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P2, P3, P20
PgB	BVCC, BVSS	P10, P11, P12, P13
PgE’	EVCC, EVSS	P8, P9
PgB’	BVCC, BVSS	P18, P19
PgA0	A0VREF, A0VSS	AP0
PgA1	A1VREF, A1VSS	AP1

Table 3A.4 Definition of Pin Group (176-Pin Version)

Symbol	Power Supply for Pin Group	Pin
PgR0	REG0VCC, AWOVSS	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P2, P20
PgB	BVCC, BVSS	P10, P11, P12
PgE’	EVCC, EVSS	P8, P9
PgB’	BVCC, BVSS	P18
PgA0	A0VREF, A0VSS	AP0
PgA1	A1VREF, A1VSS	AP1

3A.4.4.1 Absolute Maximum Ratings

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJPM}	PgE	Per pin			10	mA
			Total			60	mA
		PgB	Per pin			10	mA
			Total			60	mA
		PgE’	Per pin			10	mA
			Total			60	mA
		PgB’	Per pin			10	mA
			Total			60	mA
		PgA0	Per pin			10	mA
			Total			60	mA
		PgA1	Per pin			10	mA
			Total			60	mA
		PgR0	Per pin			10	mA
Negative overload current VIN < VSS	I_{INJNM}	PgE	Per pin			–10	mA
			Total			–60	mA
		PgB	Per pin			–10	mA
			Total			–60	mA
		PgE’	Per pin			–10	mA
			Total			–60	mA
		PgB’	Per pin			–10	mA
			Total			–60	mA
		PgA0	Per pin			–10	mA
			Total			–60	mA
		PgA1	Per pin			–10	mA
			Total			–60	mA
		PgR0	Per pin			–10	mA

CAUTIONS

1. The DC injection current (Total) must satisfy the specifications of the injection current per pin.
2. In case of an injected current condition for PgA0 and PgA1, TESH0SN is kept when the injected current is applied to an adjacent pin where the ADC self-diagnosis is executed. When an injected current is applied to the same pin where the ADC self-diagnosis is executed the TESH0SN deviating value will increase sharply with increasing absolute value of injection current.

3A.4.4.2 DC Characteristics for Overload Current

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJP}	PgE	Per pin			2	mA
			Total			50	mA
		PgB	Per pin			2	mA
			Total			50	mA
		PgE’	Per pin			3	mA
			Total			20	mA
		PgB’	Per pin			3	mA
			Total			20	mA
		PgA0	Per pin			3	mA
			Total			20	mA
		PgA1	Per pin			3	mA
			Total			20	mA
		PgR0	Per pin			2	mA
Negative overload current VIN < VSS	I_{INJN}	PgE	Per pin			–2	mA
			Total			–50	mA
		PgB	Per pin			–2	mA
			Total			–50	mA
		PgE’	Per pin			–3	mA
			Total			–20	mA
		PgB’	Per pin			–3	mA
			Total			–20	mA
		PgA0	Per pin			–3	mA
			Total			–20	mA
		PgA1	Per pin			–3	mA
			Total			–20	mA
		PgR0	Per pin			–2	mA

NOTE

These specifications are not tested on sorting and are specified based on the device characterization.

3A.4.5 Power Management Characteristics

3A.4.5.1 Regulator Characteristics

Condition: REG0VCC = EVCC = VPOC to 5.5 V, REG1VCC = VPOC to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = VPOC to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	REG0VCC		VPOC*1		5.5	V
	REG1VCC	REG1VCC ≤ REG0VCC	VPOC*1		3.6	V
Output voltage	AWOVCL	AWOVCL pin	1.15	1.25	1.35	V
	ISOVCL	ISOVCL pin	1.15	1.25	1.35	V
Capacitance	CAWOVCL	AWOVCL pin	0.07	0.10	0.13	µF
	CISOVCL	ISOVCL pin	0.07	0.10	0.13	µF
Equivalent series resistance for load capacitance	RVRAWO	for CAWOVCL			40*2	mΩ
	RVRISO	for CISOVCL			40*2	mΩ
Inrush current during power-on	REG0VCC				200	mA
	REG1VCC				350	mA

Note 1. “VPOC” means POC (power-on clear) detection voltage (typ. 2.85 V). For detail, see **Section 3A.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.

Note 2. This is reference value.

3A.4.5.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics

Condition: REG0VCC = EVCC = VPOC to 5.5 V, REG1VCC = VPOC to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = VPOC to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Detection voltage (REG0VCC, REG1VCC)	VPOC	POC			2.7	2.85	3.0	V
Detection voltage (REG0VCC)	VLVI0	LVI	Rise		3.87	4.0	4.13	V
			Fall		3.9	4.0	4.1	V
	VLVI1		Rise		3.57	3.7	3.83	V
			Fall		3.6	3.7	3.8	V
	VLVI2		Rise		3.37	3.5	3.63	V
			Fall		3.4	3.5	3.6	V
	VVLVI	VLVI			1.8	1.9	2.0	V
Detection voltage (ISOVCL)	VCVMH	CVM	High voltage[Caution]		1.35	1.39	1.43	V
	VCVML*8		Low voltage[Caution]		1.10	1.15	1.20	V
Response time	t_{D_POC1}*6	POC	At power-on (Rise)	*1			2	ms
				*2			6.3	ms
			After power-on (Rise)	*3			2	ms
				*4			5	ms
	t_{D_POC2}*7		After power-on (Fall)	*5			5	µs
	t_{D_LVI}	LVI					2	ms
	t_{D_VLVI}	VLVI		*3			2	ms
				*4			5	ms
	t_{D_CVM}	CVM			0.2		10	µs
Setup time	t_{S_LVI}	LVI	LVICNT0,1 bits are set to 1 (except 00_B), then LVI is ready to operate				80	µs
REG0VCC, REG1VCC minimum width	t_{W_POC}	POC			0.2			ms
REG0VCC minimum width	t_{W_LVI}	LVI			0.2			ms
	t_{W_VLVI}	VLVI			0.2			ms

Note 1. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms

Note 2. Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms

Note 3. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 20 V/ms

Note 4. Voltage slope (t_{VS}): 20 V/ms < t_{VS} ≤ 500 V/ms

Note 5. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 500 V/ms

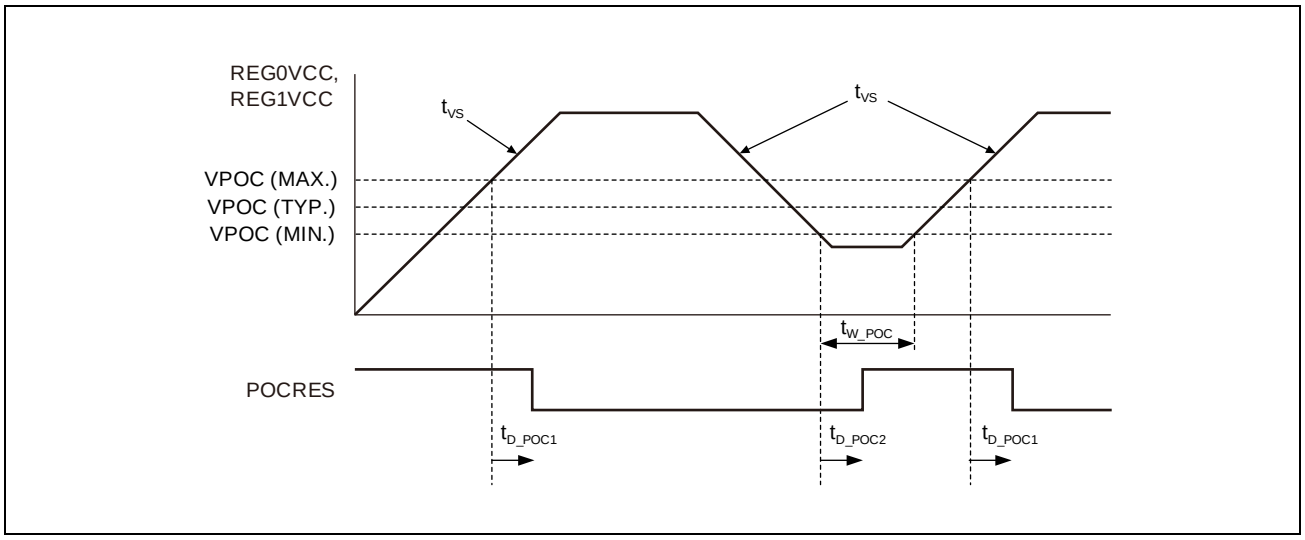
Note 6. t_{D_POC1} is the time from detection voltage to release of reset signal.

Note 7. t_{D_POC2} is the time from detection voltage to occurrence of reset signal.

Note 8. The CVM monitors the internal voltage regulator output to ensure that ISOVCL is upper than specified minimum level.

Caution: A detection of the voltage ISOVCL outside the specified level of VCVMH and VCVML is not ensured by CVM.

POC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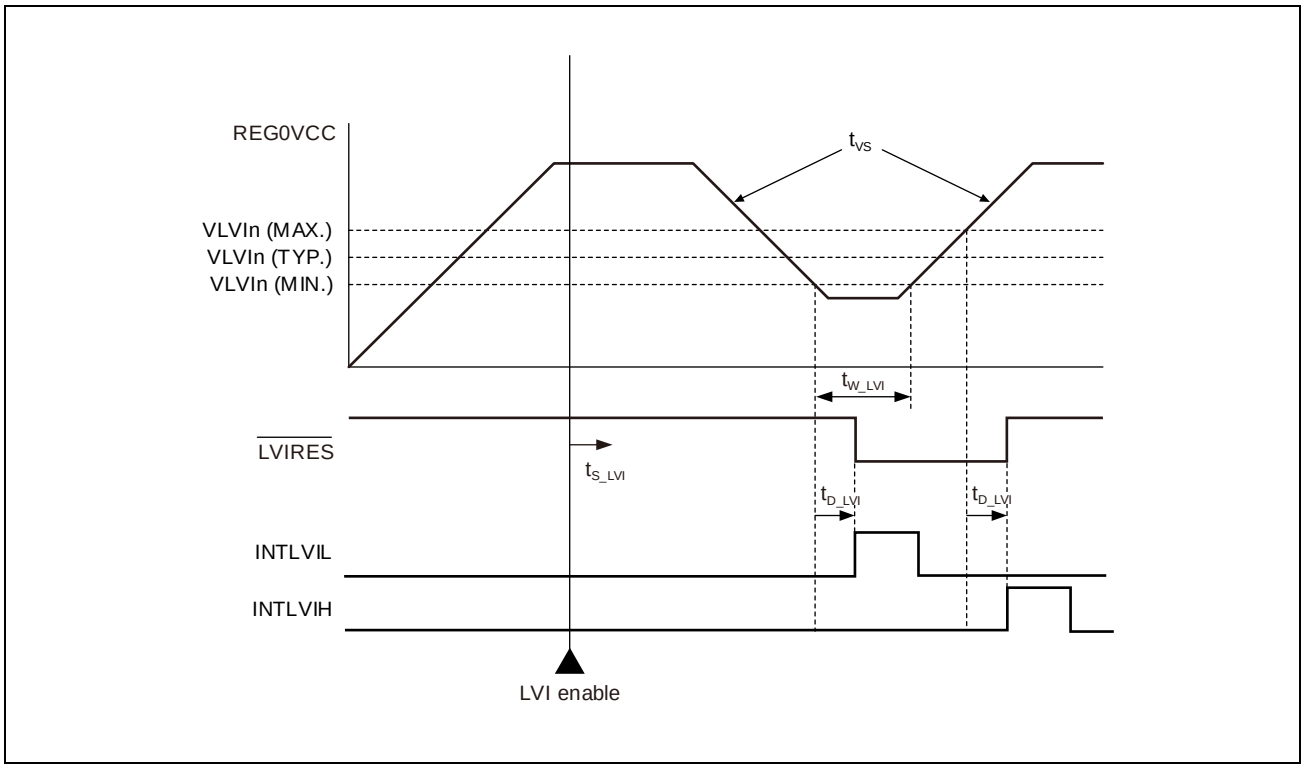
tD_POC1
tD_POC2
tD_POC1

LVI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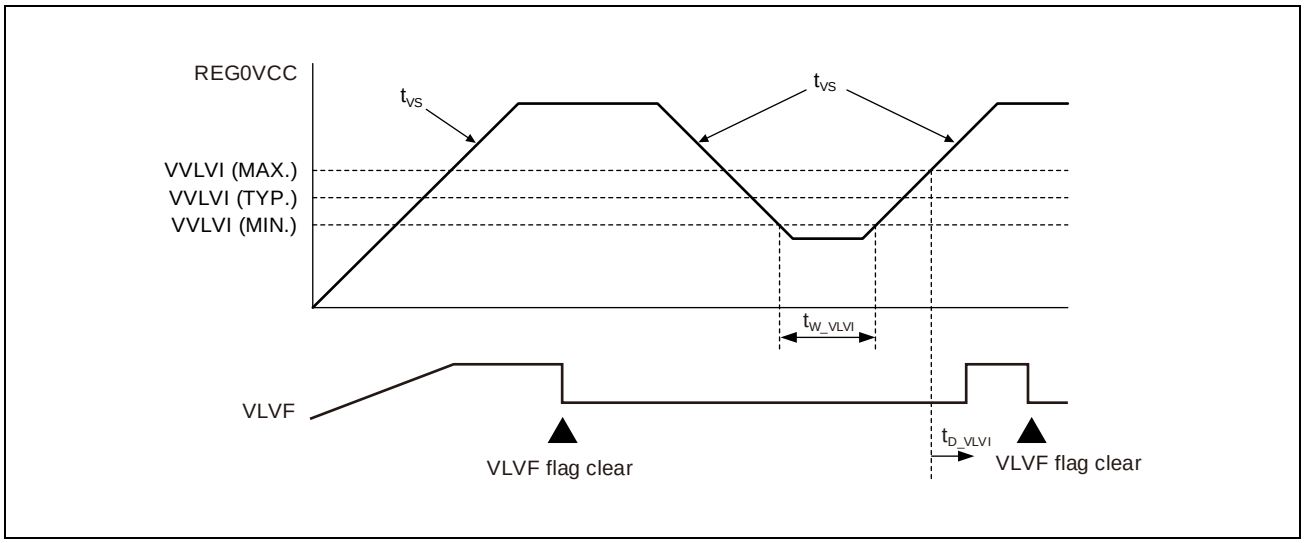
VLVI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VVLVI (TYP.)
VVLVI (MIN.)
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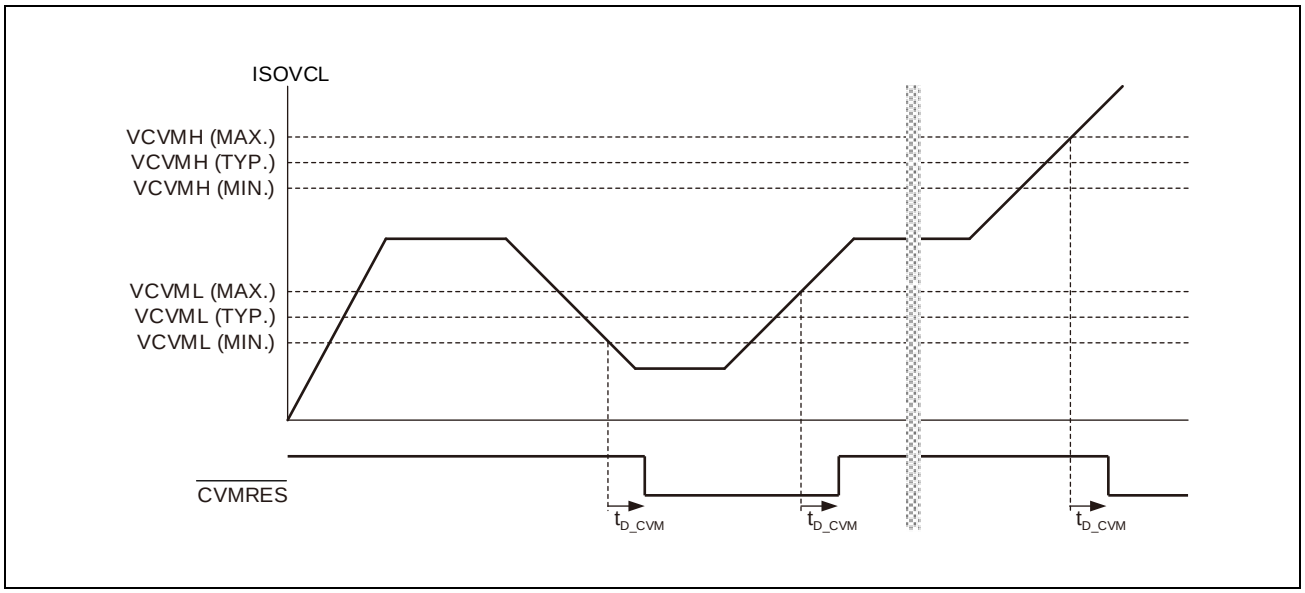
VLVF
VLVF flag clear
tD_VLVI
VLVF flag clear

CVM


ISOVCL
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VCVMH (TYP.)
VCVMH (MIN.)
VCVML (MAX.)
VCVML (TYP.)
VCVML (MIN.)
CVMRES
tD_CVM
tD_CVM
tD_CVM

3A.4.5.3 Power Up/Down Timing

Condition: REG0VCC = EVCC = VPOC to 5.5 V, REG1VCC = VPOC to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = VPOC to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

CAUTION

REG1VCC must not be greater than REG0VCC during power up/down.

Table 3A.5 In Case the $\overline{\text{RESET}}$ Pin is Used (for Normal Operating Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REG0VCC, REG1VCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REG0VCC ↑, REG1VCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 hold time (vs $\overline{\text{RESET}}$ ↑)	t_{HMDR}		1			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↓)	t_{SMDF}		0			µs
$\overline{\text{RESET}}$ ↓ to REG0VCC ↓, REG1VCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms

Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

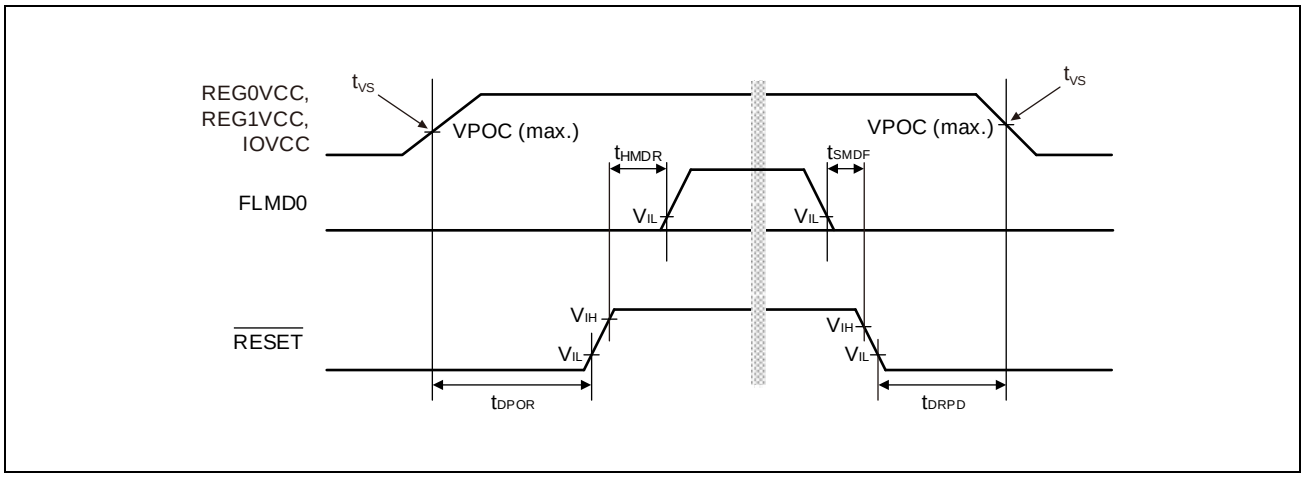


Table 3A.6 In Case the $\overline{\text{RESET}}$ Pin is Used (for Serial Programming Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REG0VCC, REG1VCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REG0VCC ↑, REG1VCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
$\overline{\text{RESET}}$ ↓ to REG0VCC ↓, REG1VCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms

Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

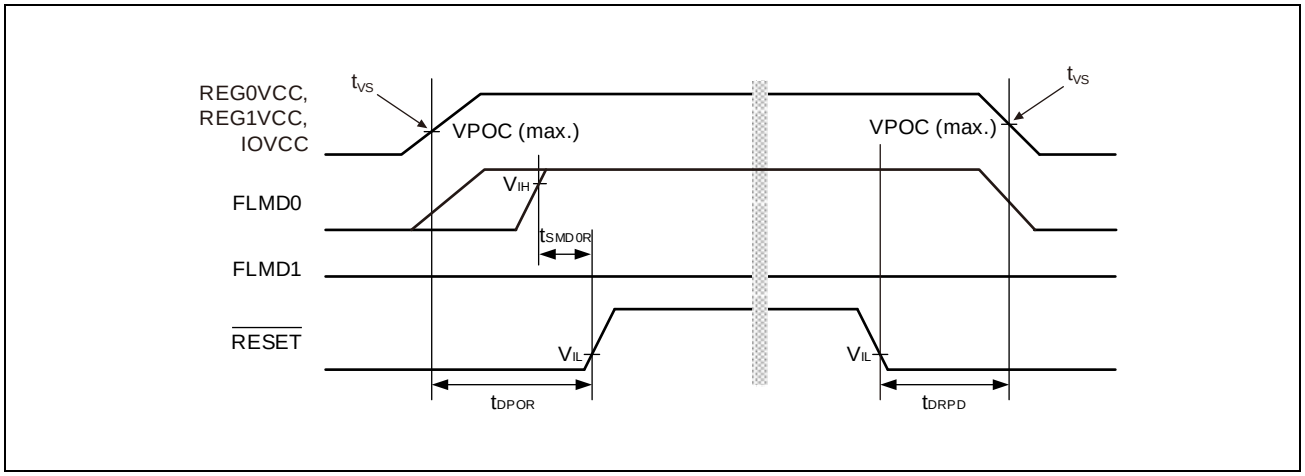


Table 3A.7 In Case the $\overline{\text{RESET}}$ Pin is Used (for Boundary Scan Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REG0VCC, REG1VCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REG0VCC ↑, REG1VCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
FLMD1,MODE0,MODE1 setup time (vs FLMD0 ↑)	t_{SMD1R}		1			µs
FLMD0 hold time (vs $\overline{\text{RESET}}$ ↓)	t_{HMD0F}		1			µs
FLMD1, MODE0, MODE1, MODE2 hold time (vs FLMD0 ↓)	t_{HMD1F}		1			µs
$\overline{\text{RESET}}$ ↓ to REG0VCC ↓, REG1VCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms
$\overline{\text{DCUTRST}}$ input delay time (vs $\overline{\text{RESET}}$ ↑)	t_{DRTRST}		1			ms
$\overline{\text{RESET}}$ hold time (vs $\overline{\text{DCUTRST}}$ ↓)	t_{HRTRST}		0			ms

Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

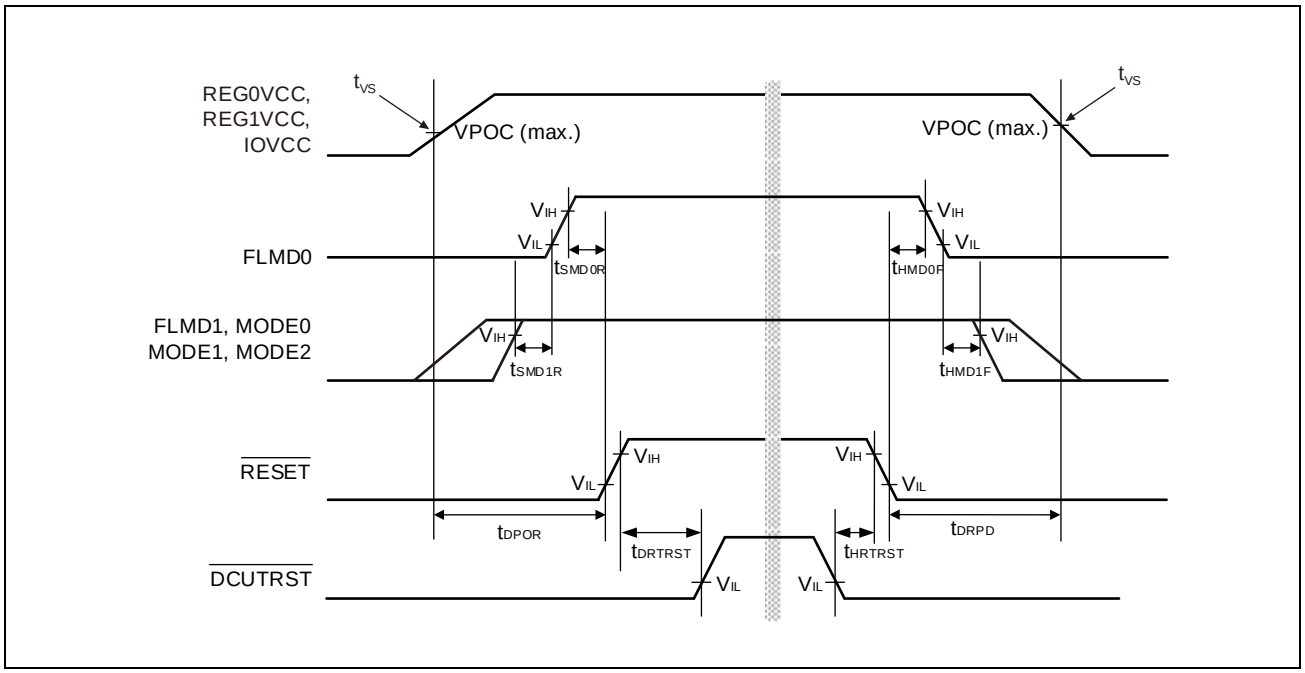


Table 3A.8 In Case the $\overline{\text{RESET}}$ Pin is Used (for User Boot Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REG0VCC, REG1VCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REG0VCC ↑, REG1VCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
FLMD1, MODE0, MODE1, MODE2 setup time (vs FLMD0 ↑)	t_{SMD1R}		1			µs
FLMD0 hold time (vs $\overline{\text{RESET}}$ ↓)	t_{HMD0F}		1			µs
FLMD1, MODE0, MODE1, MODE2 hold time (vs FLMD0 ↓)	t_{HMD1F}		1			µs
$\overline{\text{RESET}}$ ↓ to REG0VCC ↓, REG1VCC ↓ and IOVCC ↓ delay time	t_{DRPD}		0			ms

Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

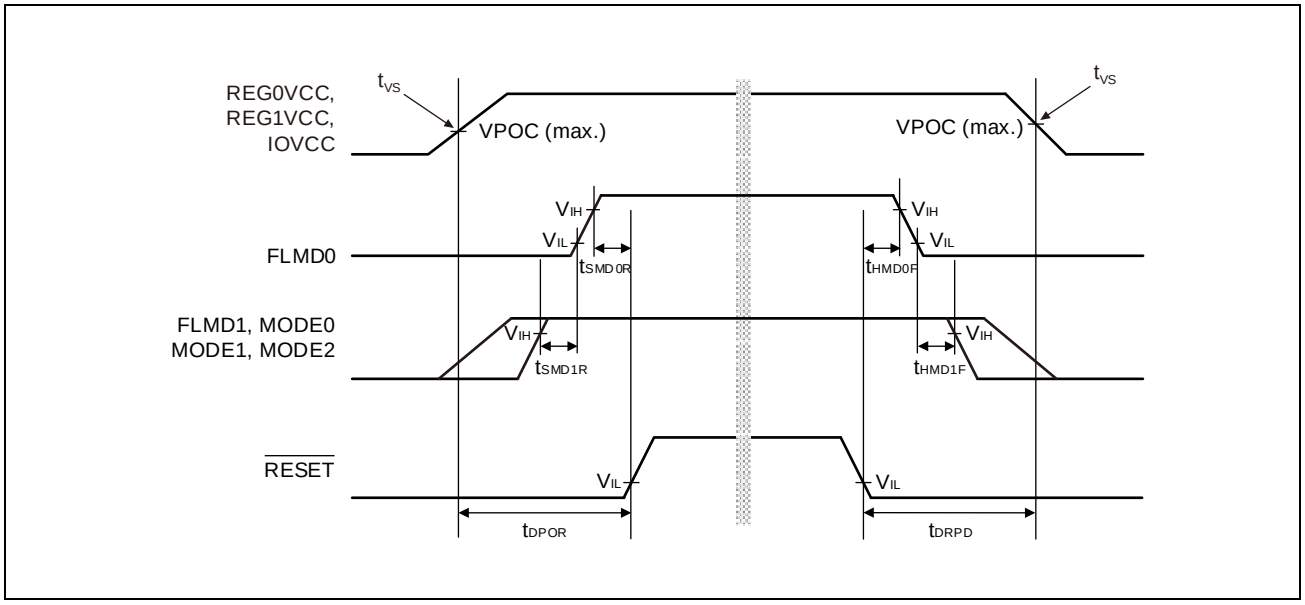
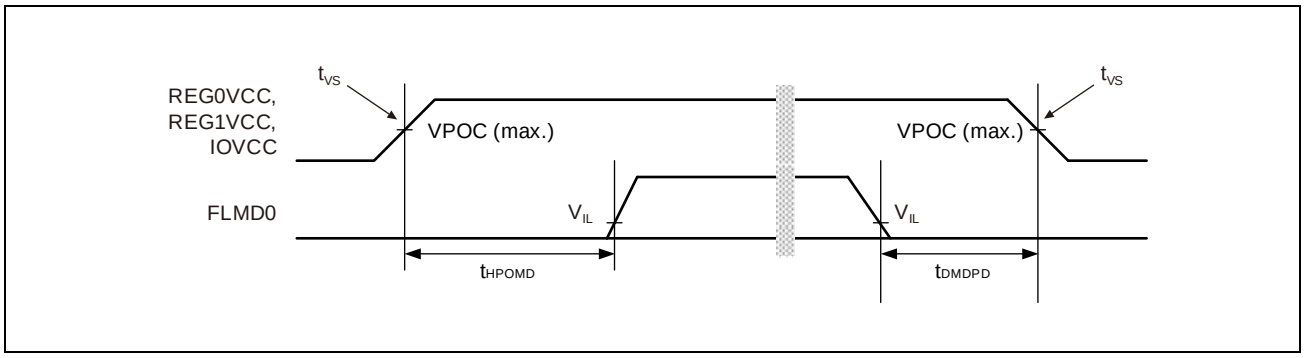


Table 3A.9 In Case the $\overline{\text{RESET}}$ Pin is Not Used and Fixed to High Level by Pull-up*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REG0VCC, REG1VCC and IOVCC*2)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REG0VCC ↑, REG1VCC ↑ and IOVCC*2 ↑ to FLMD0 hold time	t_{HPOMD}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 ↓ to REG0VCC ↓, REG1VCC ↓ and IOVCC*2 ↓ delay time	t_{DMDPD}		1			µs

Note 1. This operating condition is available only in normal operation mode (include self-programming mode). When the device is used in except normal operation mode, please use the $\overline{\text{RESET}}$ pin.

Note 2. IOVCC means EVCC, BVCC, A0VREF and A1VREF.



3A.4.5.4 CPU Reset Release Timing

Condition: REG0VCC = EVCC = VPOC to 5.5 V, REG1VCC = VPOC to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = VPOC to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3A.10 In Case the $\overline{\text{RESET}}$ Pin is Not Used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REG0VCC ↑ and REG1VCC ↑ to CPU reset release*1	t_{DPCRR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms			2.58	ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms			8.3	ms

Note 1. This is reference value.

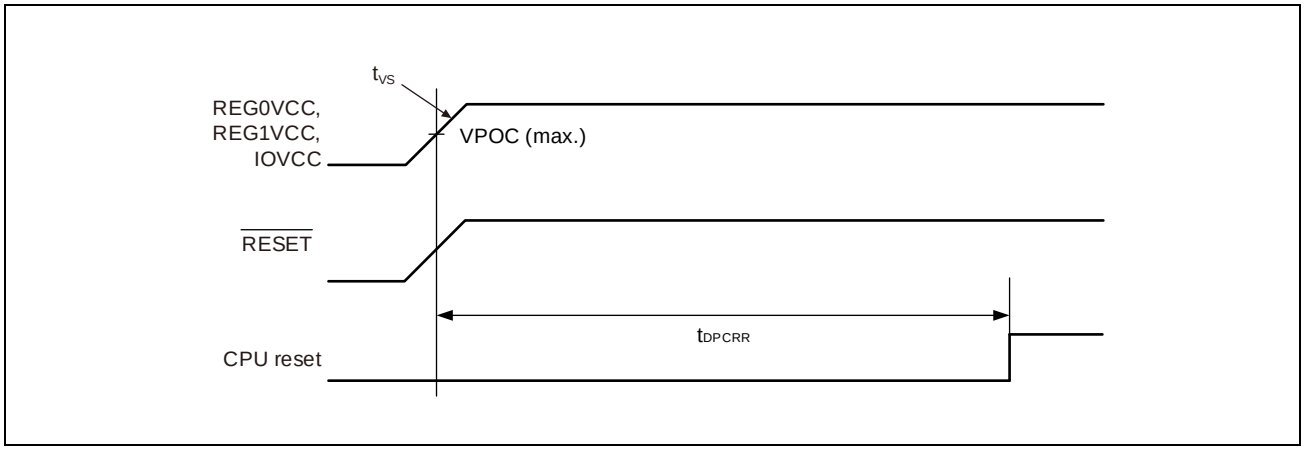
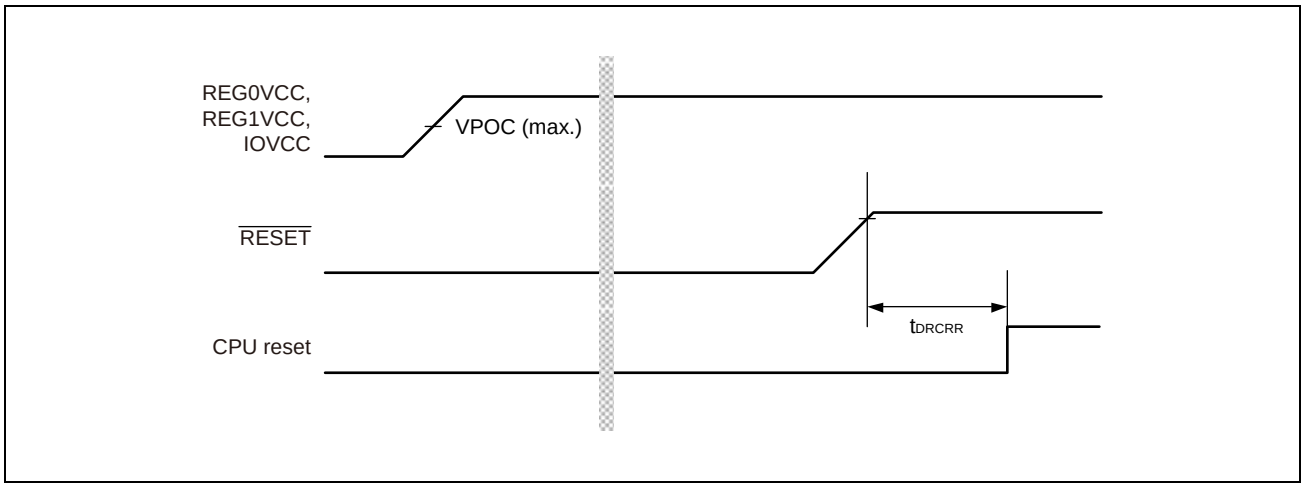


Table 3A.11 In Case the $\overline{\text{RESET}}$ Pin is Used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ ↑ to CPU reset release*1	t_{DRCRR}				32*2	µs

Note 1. This is reference value.

Note 2. In case the time until releasing the $\overline{\text{RESET}}$ pin is longer than t_{DPCRR}.



3A.5 AC Characteristics

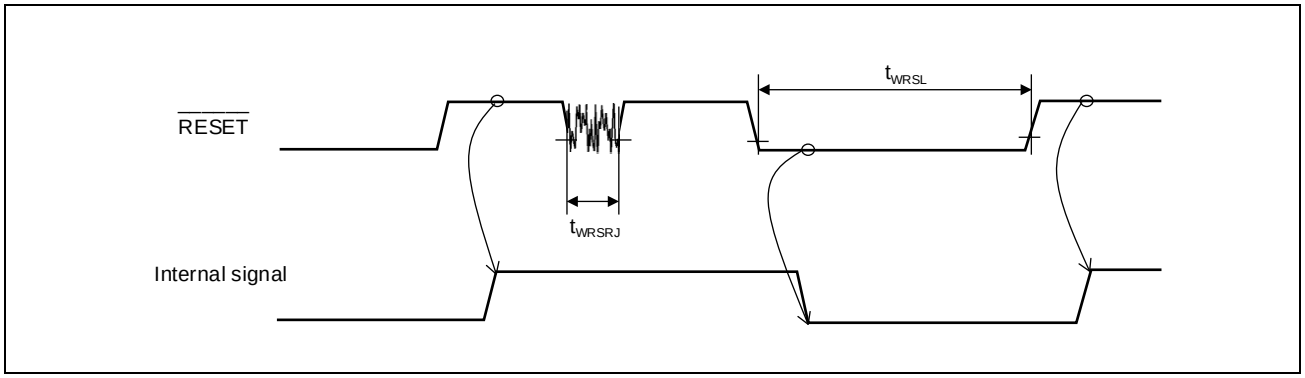
3A.5.1 $\overline{\text{RESET}}$ Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width*1	t_{WRSL}	Except power on	600			ns
$\overline{\text{RESET}}$ pulse rejection*2	t_{WRSRJ}		100			ns

Note 1. $\overline{\text{RESET}}$ input width is needed to ensure that the internal reset signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



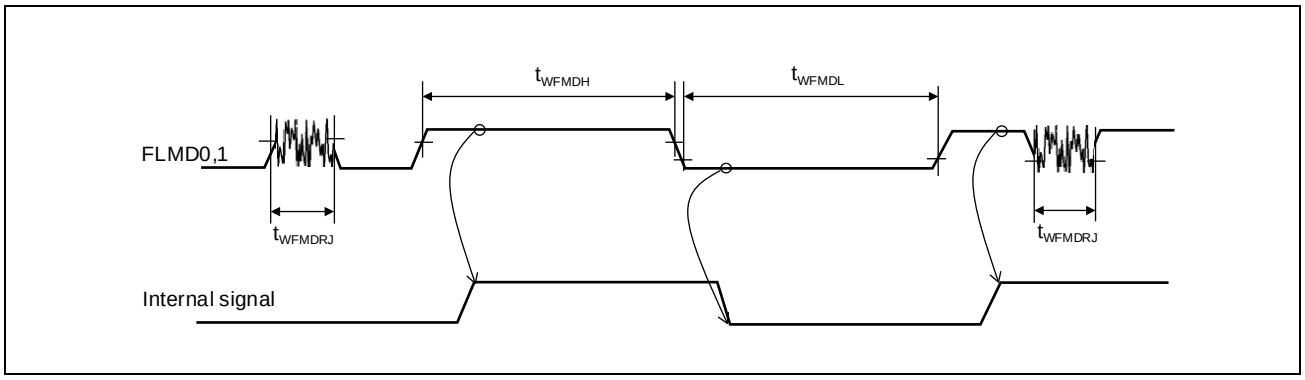
3A.5.2 Mode Timing

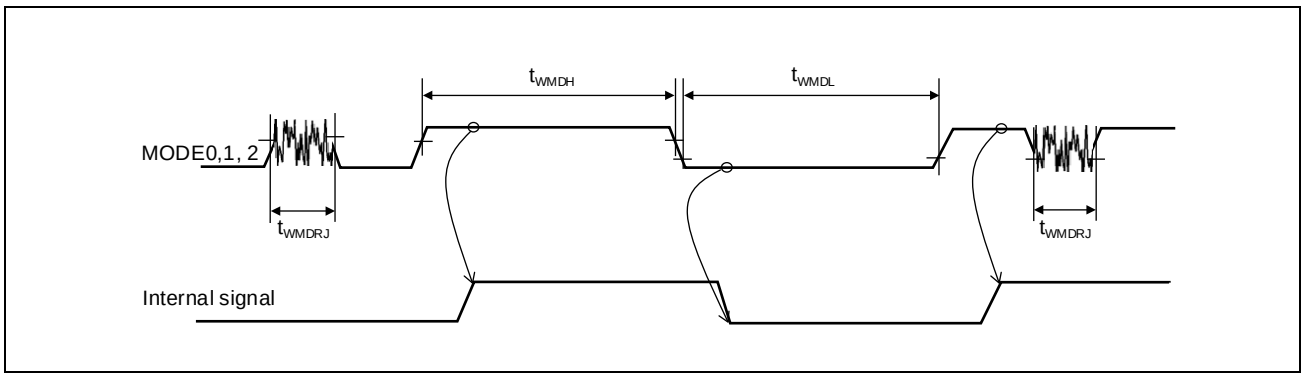
Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0, 1 input high/low level width*1	t_{WFMDH}/ t_{WFMDL}		600			ns
FLMD0, 1 pulse rejection*2	t_{WFMDRJ}		100			ns
MODE0, 1, 2 input high/low level width*1	t_{WMDH}/ t_{WMDL}		600			ns
MODE0, 1, 2 pulse rejection*2	t_{WMDRJ}		100			ns

Note 1. FLMD0, 1 and MODE0, 1, 2 input width is needed to ensure that the internal mode signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.





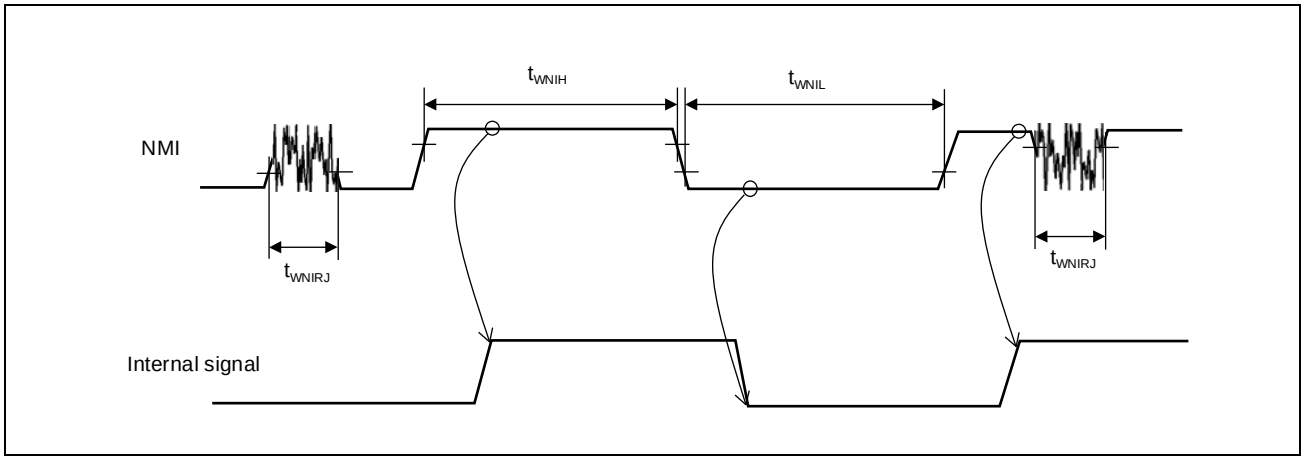
3A.5.3 Interrupt Timing

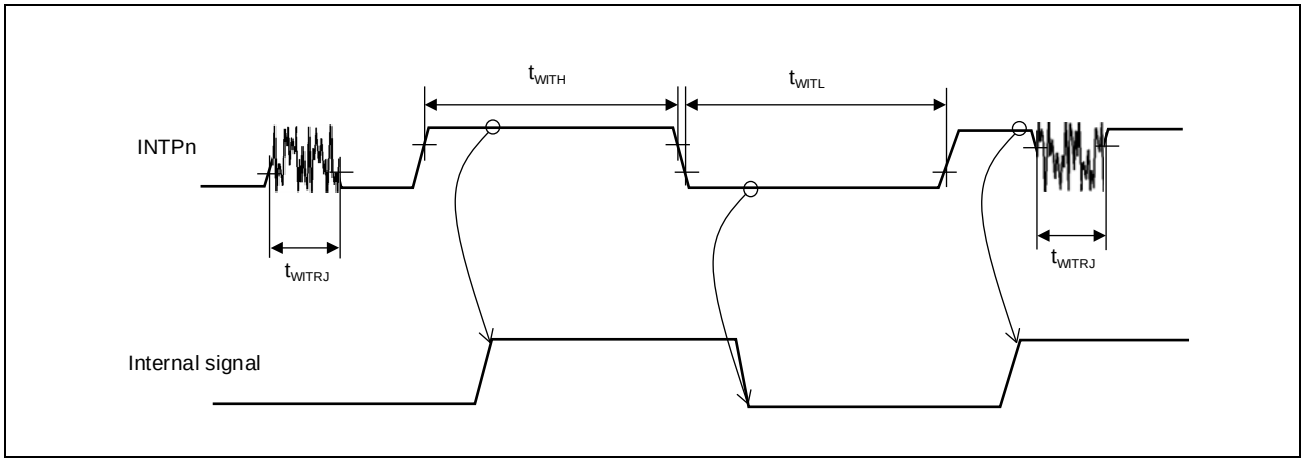
Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high/low level width*1	t_{WNIH}/ t_{WNIL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	24			µs
NMI pulse rejection*2	t_{WNIRJ}		100			ns
INTPn input high/low level width*1	t_{WITH}/ t_{WITL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	24			µs
INTPn pulse rejection*2	t_{WITRJ}		100			ns

Note 1. NMI and INTPn input width is needed to ensure that the internal interrupt signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



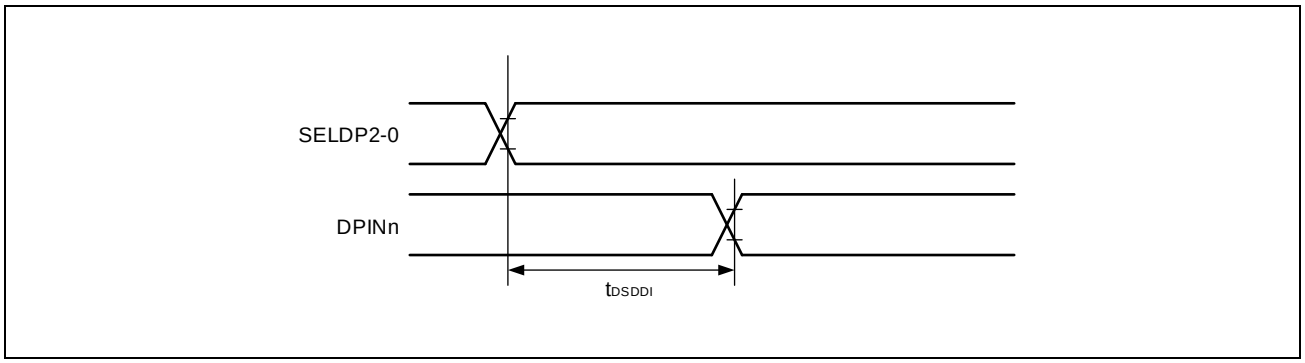


3A.5.4 Low Power Sampler (DPIN input) Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DPINn input delay time (vs SELDP2-0)	t_{DSDDI}				150	ns

Note: n = 7 to 0



3A.5.5 CSCXFOUT Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

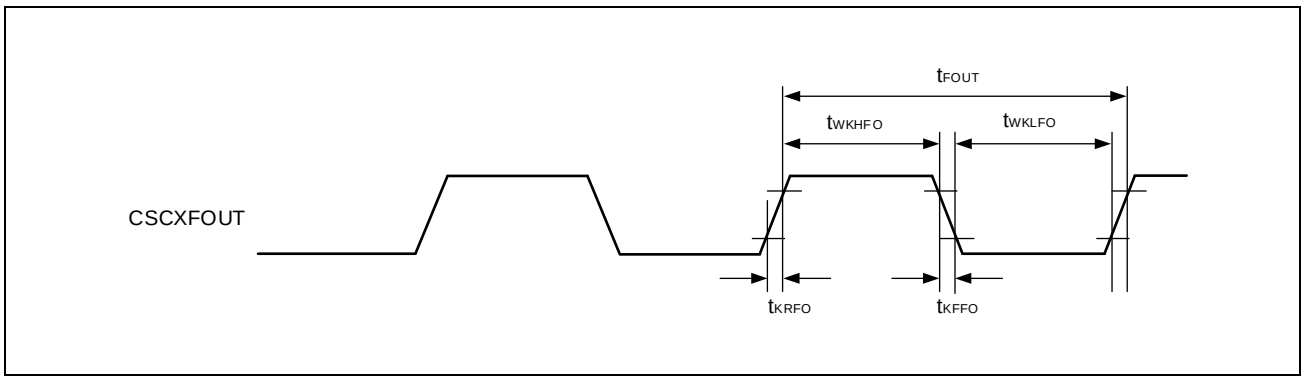
CSCXFOUT: Slow or fast mode (refer to the condition in the following table)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
CSCXFOUT output cycle	t_{FOUT}	Slow mode		100 (max. 10 MHz)			ns
		Fast mode		41.6 (max. 24 MHz)			ns
CSCXFOUT high level width	t_{WKHFO}	Slow mode	N: 1*1 or even value*2	t_{FOUT} / 2 – 37			ns
			N: Odd value (N ≥ 5)*2,*3	t_{FOUT} × (N+1) / 2N – 37			ns
		Fast mode	N: 1*1 or even value*2	t_{FOUT} / 2 – 10			ns
			N: Odd value (N ≥ 3)*2	t_{FOUT} × (N+1) / 2N – 10			ns
CSCXFOUT low level width	t_{WKLFO}	Slow mode	N: 1*1 or even value*2	t_{FOUT} / 2 – 37			ns
			N: Odd value (N ≥ 5)*2,*3	t_{FOUT} × (N–1) / 2N – 37			ns
		Fast mode	N: 1*1 or even value*2	t_{FOUT} / 2 – 10			ns
			N: Odd value (N ≥ 3)*2	t_{FOUT} × (N–1) / 2N – 10			ns
CSCXFOUT rise/ fall time	t_{KRFO}/ t_{KFFO}	Slow mode				37	ns
		Fast mode				10	ns

Note 1. When MainOSC, HS IntOSC, LS IntOSC or SubOSC is selected as source clock with the condition of N = 1, the characteristics of output signal depends on the selected source clock. It is recommended to use output signal after evaluation on an actual environment.

Note 2. “N” is the value of “Clock divisor N” defined by FOUTDIV register.

Note 3. The selection of N = 3 is prohibited when slow mode is used.



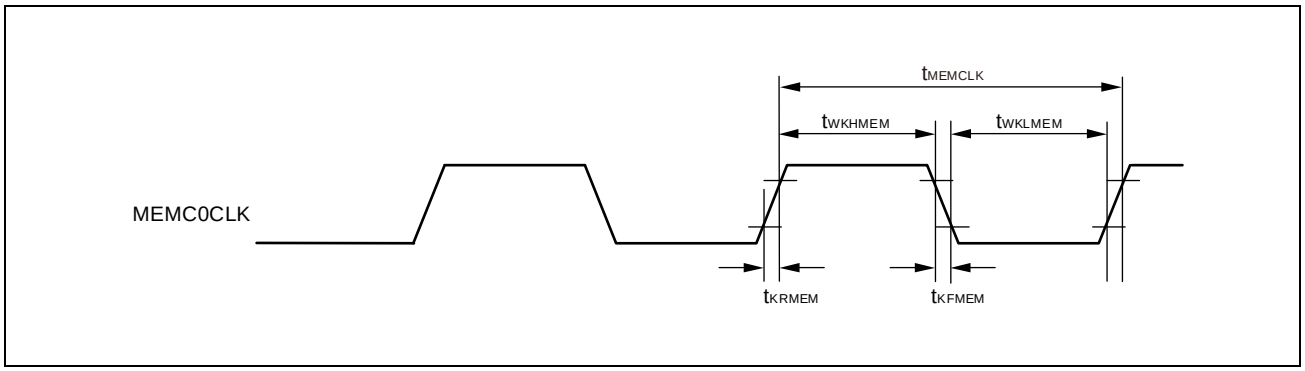
3A.5.6 MEMC0CLK Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

<Output driver strength>

MEMC0CLK pin: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MEMC0CLK output cycle	t_{MEMCLK}		33.4 (max.30 MHz)			ns
MEMC0CLK high / low level width	t_{WKHMEM} / t_{WKLMEM}		t_{MEMCLK} / 2 – 10			ns
MEMC0CLK rise / fall time	t_{KRMEM} / t_{KFMEM}				10	ns



3A.5.7 External Bus Timing

3A.5.7.1 MEMC0CLK Asynchronous

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

MEMC0AD0-15, MEMC0A16-23, $\overline{\text{MEMC0CS3-0}}$, $\overline{\text{MEMC0BEN1-0}}$, $\overline{\text{MEMC0ASTB}}$, $\overline{\text{MEMC0WR}}$, and $\overline{\text{MEMC0RD}}$ pins: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bus operational period	T		33.4 (max.30 MHz)			ns
Address*4 setup time to $\overline{\text{MEMC0ASTB}}$ ↓	t_{SAST}	<1>	(1 + ASW) × T – 15			ns
Address (MEMC0AD15-0) hold time from $\overline{\text{MEMC0ASTB}}$ ↓	t_{HSTA}	<2>	(1 + AHW) × T – 15			ns
Address (MEMC0AD15-0) float delay time from $\overline{\text{MEMC0RD}}$ ↓	t_{FRDA}*8	<3>			9	ns
Address*5 hold time from $\overline{\text{MEMC0RD}}$ ↑	t_{HRDA}	<4>	–1.5			ns
Data (MEMC0AD15-0) input delay time from $\overline{\text{MEMC0RD}}$ ↓	t_{DRDID}	<5>	9		(1 + w) × T – 35	ns
Data (MEMC0AD15-0) input hold time from $\overline{\text{MEMC0RD}}$ ↑	t_{HRDID}	<6>	0			ns
Delay time from $\overline{\text{MEMC0ASTB}}$ ↓ to $\overline{\text{MEMC0RD}}$ ↓	t_{DSTRD}	<7>	(1 + AHW) × T – 15			ns
Delay time from $\overline{\text{MEMC0ASTB}}$ ↓ to $\overline{\text{MEMC0WR}}$ ↓	t_{DSTWR}	<8>	(1 + AHW) × T – 15			ns
$\overline{\text{MEMC0RD}}$, $\overline{\text{MEMC0WR}}$ low level width	t_{WRDST}	<9>	(1 + w) × T – 10			ns
Data (MEMC0AD15-0) output delay time from $\overline{\text{MEMC0WR}}$ ↓	t_{DWROD}	<10>			11	ns
Address*5 hold time from $\overline{\text{MEMC0WR}}$ ↑	t_{HWRA}	<11>	(1 + DHW) × T – 15			ns
Data (MEMC0AD15-0) output setup time to $\overline{\text{MEMC0WR}}$ ↑	t_{SODWR}	<12>	(1 + w) × T – 15			ns
Data (MEMC0AD15-0) output hold time from $\overline{\text{MEMC0WR}}$ ↑	t_{HWROD}	<13>	(1 + DHW) × T – 15			ns
$\overline{\text{MEMC0WAIT}}$ setting delay from $\overline{\text{MEMC0ASTB}}$ ↓	t_{SSTWT1}	<14>			(AHW + DPW) × T – 24	ns
	t_{SSTWT2}	<15> DEW ≥ 1			(AHW + DPW + DEW) × T – 24	ns
$\overline{\text{MEMC0WAIT}}$ hold time from $\overline{\text{MEMC0ASTB}}$ ↓	t_{HSTWT1}	<16>	(AHW + DPW + DEW – 1) × T – 9			ns
	t_{HSTWT2}	<17> DEW ≥ 1	(AHW + DPW + DEW) × T – 9			ns

Note 1. ASW means the number of address setup wait for multiplex bus.

Note 2. AHW means the number of address hold wait for multiplex bus.

Note 3. DPW means the number of programmable data wait for multiplex bus.
DEW means the number of external data wait for multiplex bus.
"w" means the sum of DPW and DEW.

Note 4. t_{CPUCLK}: CPU clock period.

Note 5. DHW means the number of data hold wait for multiplex bus.

Note 6. Address means MEMC0AD15-0, MEMC0A23-16, $\overline{\text{MEMC0CS3-0}}$, and $\overline{\text{MEMC0BEN1-0}}$.
324-pin products support 24-bit address. 233/176-pin products support 23-bit address.

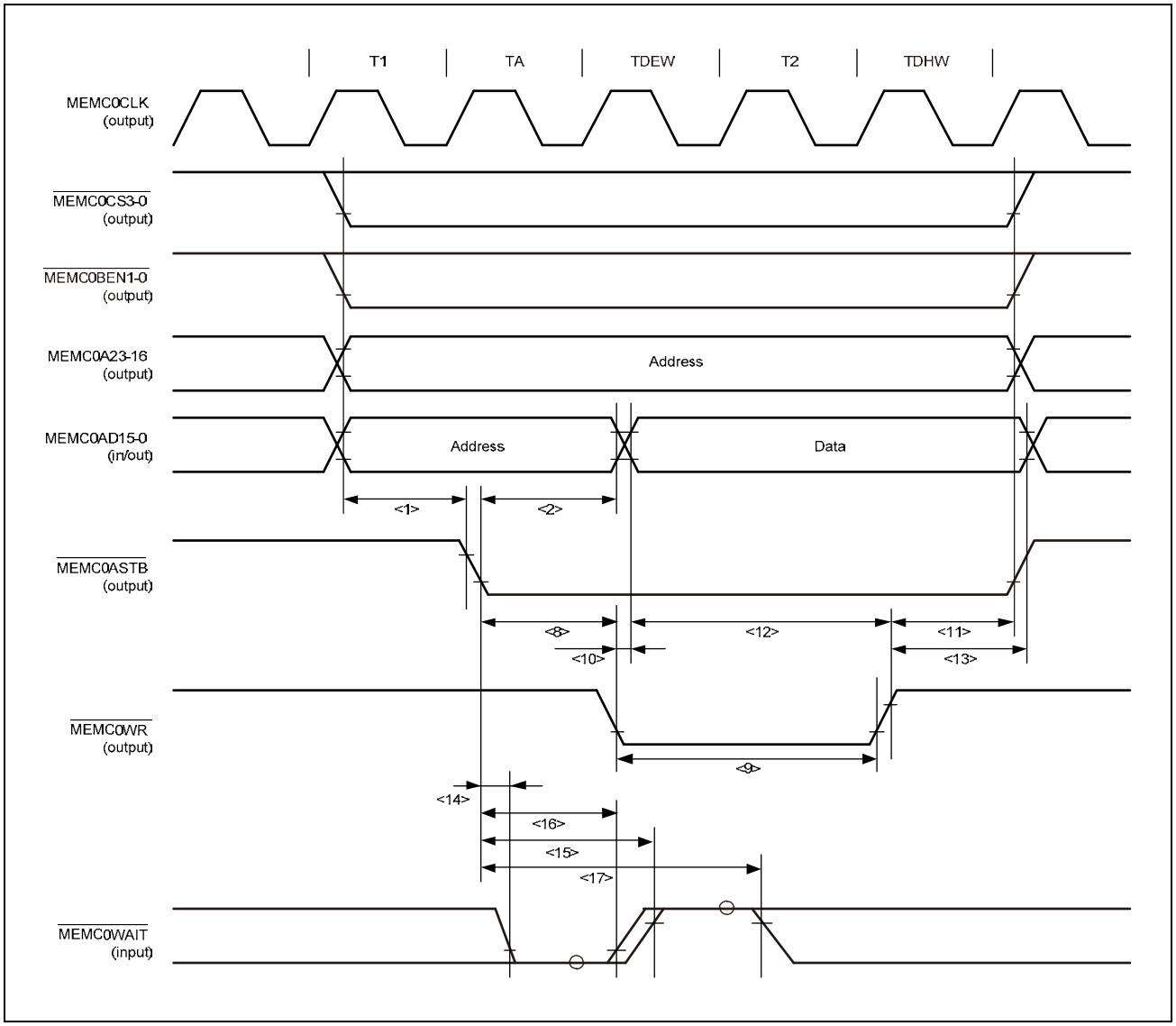
Note 7. Address means MEMC0A23-16, $\overline{\text{MEMC0CS3-0}}$, $\overline{\text{MEMC0BEN1-0}}$, and $\overline{\text{MEMC0ASTB}}$.
324-pin products support 24-bit address. 233/176-pin products support 23-bit address.

Note 8. t_{FRDA} means the period from output off to Hi-z for MEMC0AD15-0.

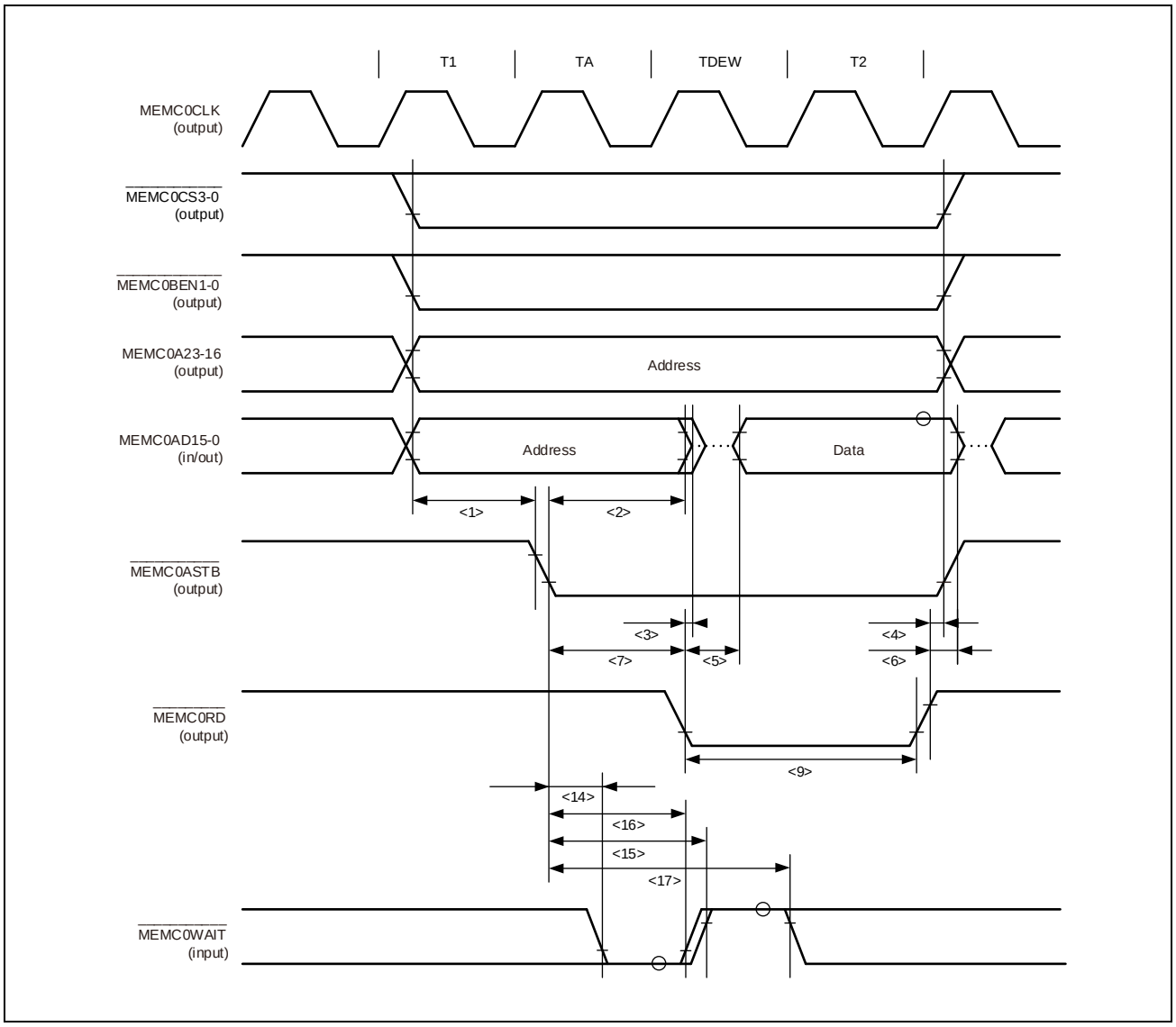
NOTE

When the bus period (T) is shorter than 44 ns, t_{DRDID} spec requires at least 1data wait. (w = 1)

(1) Multiplex Write Cycle (Asynchronous; 1 Data Wait)



(2) Multiplex Read Cycle (Asynchronous; 1 Data Wait)



3A.5.7.2 MEMC0CLK Synchronous

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

MEMC0AD0-15, MEMC0A16-23, $\overline{\text{MEMC0CS3-0}}$, $\overline{\text{MEMC0BEN1-0}}$, $\overline{\text{MEMC0ASTB}}$, $\overline{\text{MEMC0WR}}$, and $\overline{\text{MEMC0RD}}$ pins: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bus operational period	T		33.4 (max.30 MHz)			ns
Delay time from MEMC0CLK ↑ to address*1	t_{DKA}	<18>	–0.5		15	ns
Delay time from MEMC0CLK ↑ to address (MEMC0AD15-0) float	t_{FKA}*2	<19>	0		12	ns
Delay time from MEMC0CLK ↑ to $\overline{\text{MEMC0ASTB}}$	t_{DKST}	<20>	0		11	ns
Delay time from MEMC0CLK ↑ to $\overline{\text{MEMC0RD}}$ and $\overline{\text{MEMC0WR}}$	t_{DKRDWR}	<21>	–2.5		6	ns
Data (MEMC0AD15-0) input setup time (from MEMC0CLK ↑)	t_{SIDK}	<22>	29			ns
Data (MEMC0AD15-0) input hold time (from MEMC0CLK ↑)	t_{HKID}	<23>	2.5			ns
Data (MEMC0AD15-0) output delay time (from MEMC0CLK ↑)	t_{DKOD}	<24>			15	ns
$\overline{\text{MEMC0WAIT}}$ setup time (to MEMC0CLK ↑)	t_{SWTK}	<25>	T + 22			ns
$\overline{\text{MEMC0WAIT}}$ hold time (from MEMC0CLK ↑)	t_{HKWT}	<26>	–T – 5			ns

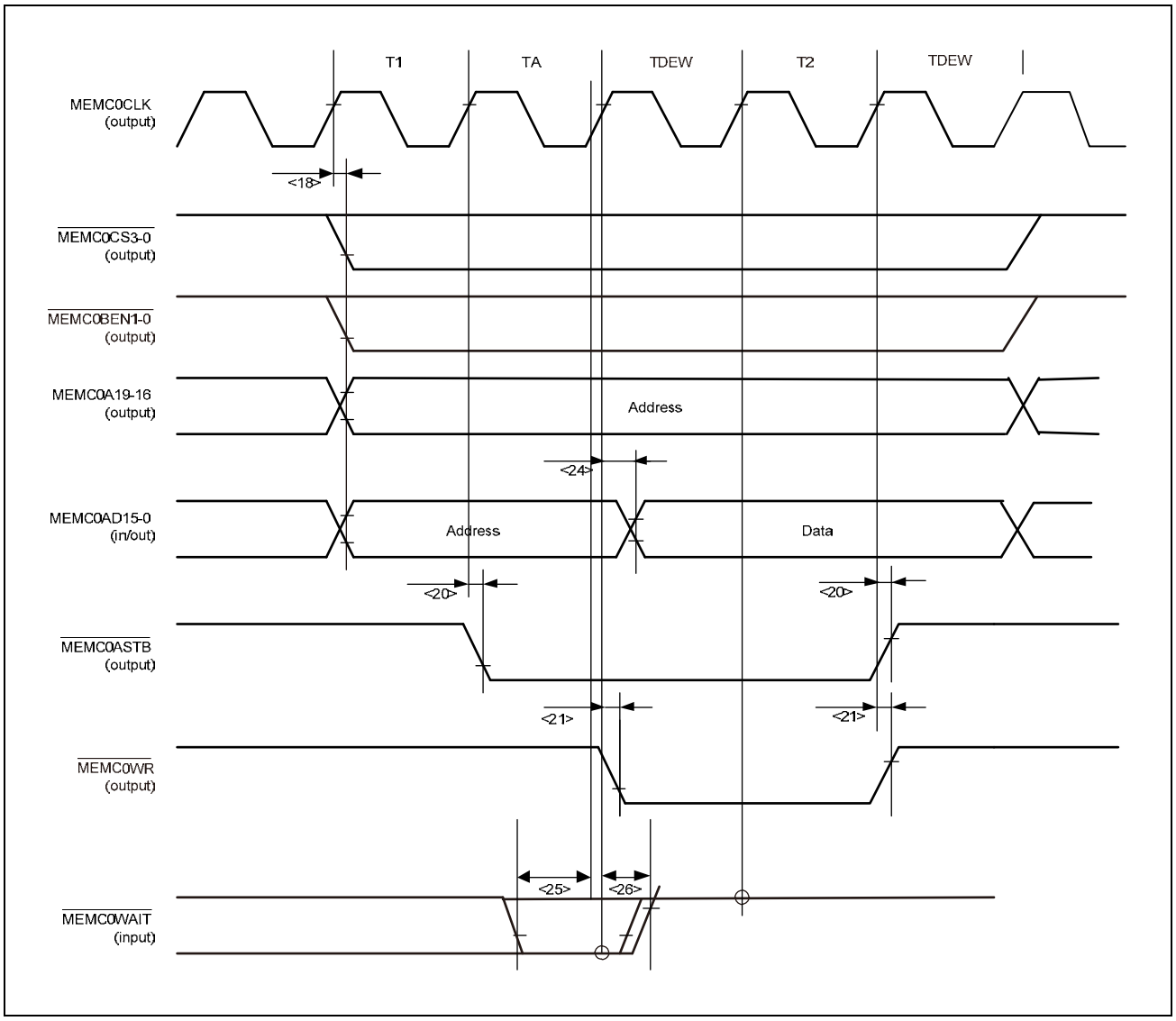
Note 1. Address means MEMC0AD15-0, MEMC0A23-16, $\overline{\text{MEMC0CS3-0}}$ and $\overline{\text{MEMC0BEN1-0}}$. 324-pin products support 24-bit address. 233/176-pin products support 23-bit address.

Note 2. t_{FKA} means the period from output off to Hi-z for MEMC0AD15-0.

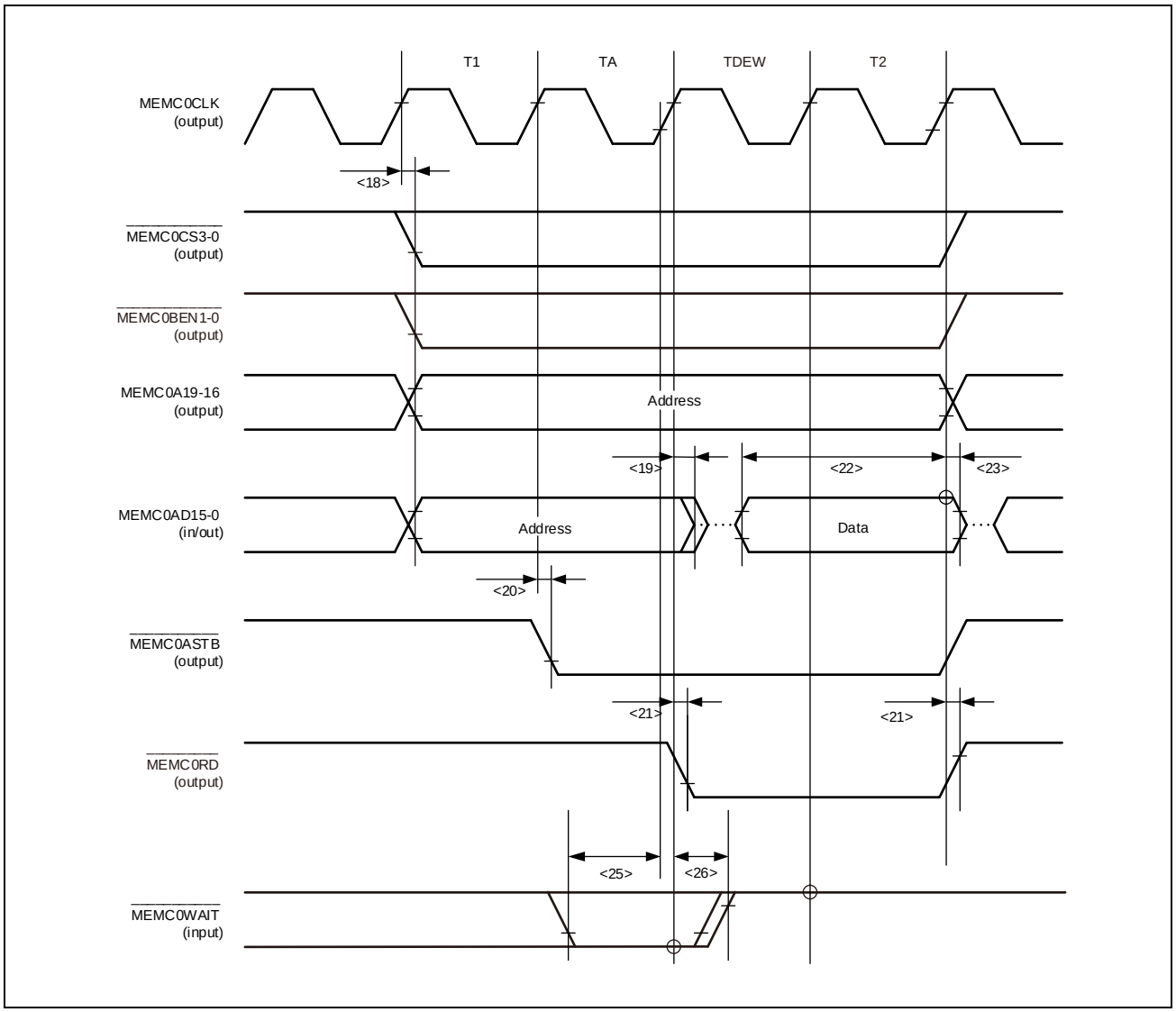
NOTE

When the bus period (T) is shorter than 44 ns, t_{DRDID} spec requires at least 1data wait. (w = 1)

(1) Multiplex Write Cycle (Synchronous; 1 Data Wait)



(2) Multiplex Read Cycle (Synchronous; 1 Data Wait)



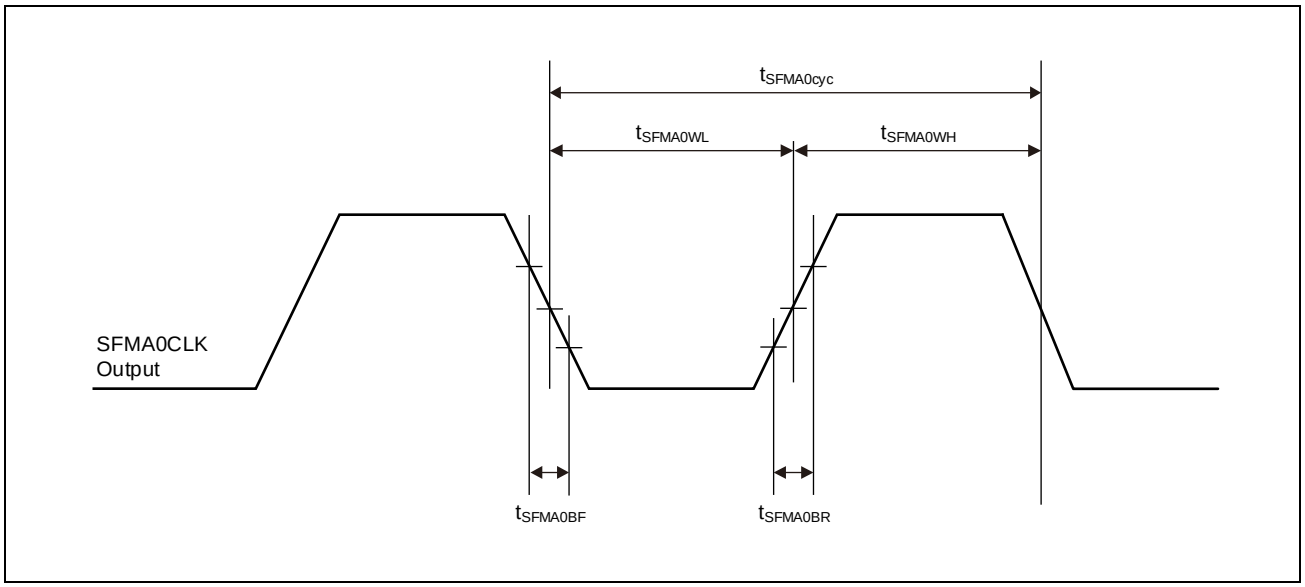
3A.5.8 SFMA Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to 3.6 V, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

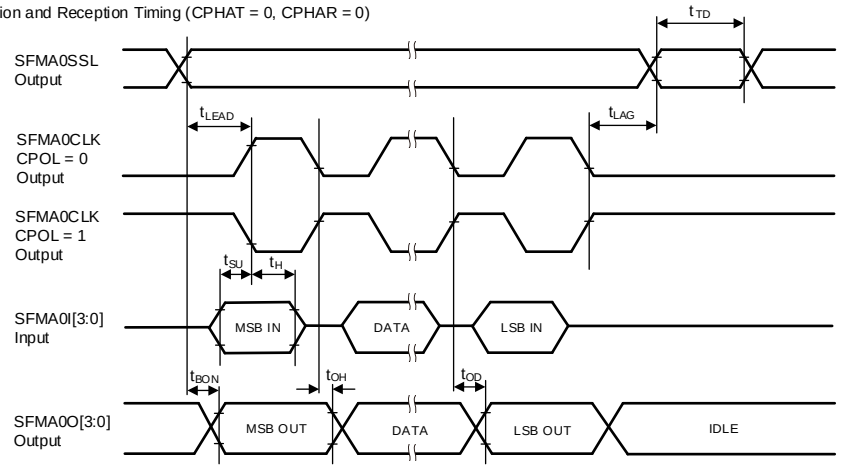
<Output driver strength>

SFMA0CLK, SFMA0SSL, and SFMA0O[3:0] pins: Fast mode

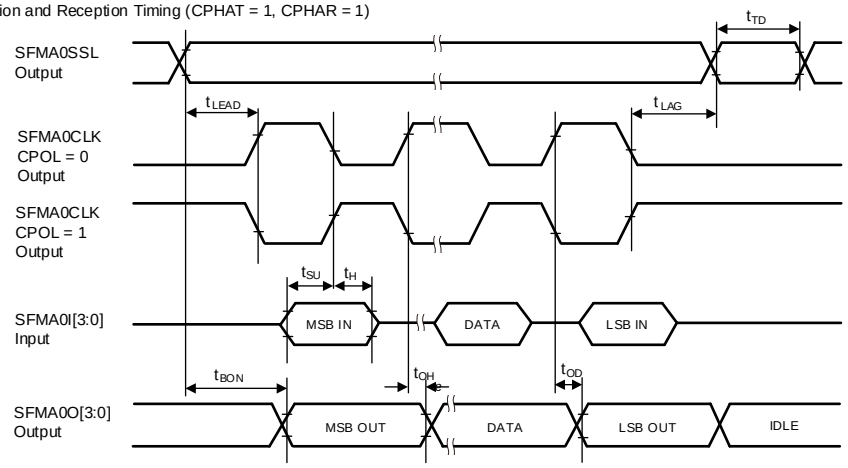
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SFMA0CLK clock cycle	$t_{SFMA0cyc}$		25			ns
SFMA0CLK high pulse width	$t_{SFMA0WH}$		0.4 × $t_{SFMA0cyc}$		0.6 × $t_{SFMA0cyc}$	ns
SFMA0CLK low pulse width	$t_{SFMA0WL}$		0.4 × $t_{SFMA0cyc}$		0.6 × $t_{SFMA0cyc}$	ns
SFMA0CLK rise time	t_{SFMA0R}				4.5	ns
SFMA0CLK fall time	t_{SFMA0F}				4.5	ns
Data input setup time	t_{SU}		13.0			ns
Data input hold time	t_{H}		0.0			ns
SFMA0SSL setup time	t_{LEAD}		1 × $t_{SFMA0cyc}$ – 5		8 × $t_{SFMA0cyc}$	ns
SFMA0SSL hold time	t_{LAG}		1.5 × $t_{SFMA0cyc}$		8.5 × $t_{SFMA0cyc}$ + 5	ns
Continuous transfer delay time	t_{TD}		1 × $t_{SFMA0cyc}$		8 × $t_{SFMA0cyc}$	ns
Data output delay time	t_{OD}				3.6	ns
Data output hold time	t_{OH}		–1.6			ns
Data output buffer on time	t_{BON}				3.6	ns
Data output buffer off time	t_{BOFF}		–7.0		0	ns



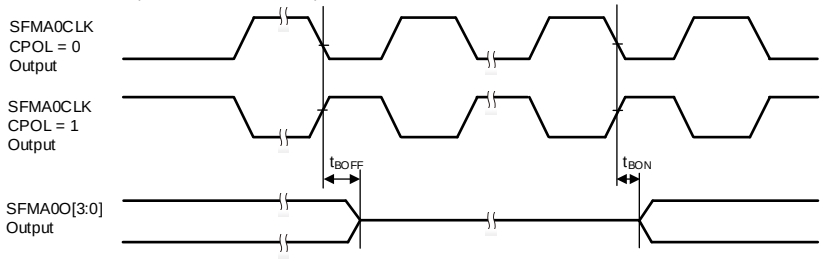
Transmission and Reception Timing (CPHAT = 0, CPHAR = 0)



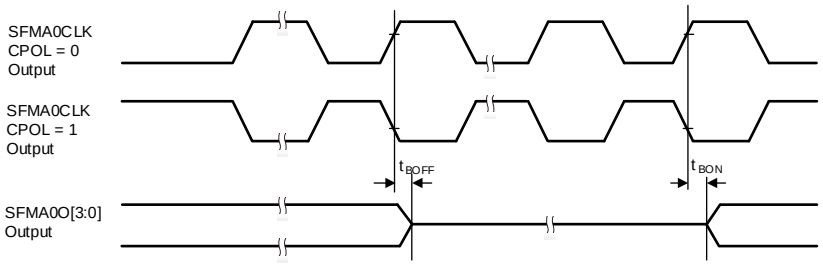
Transmission and Reception Timing (CPHAT = 1, CPHAR = 1)



Timing for Switching the Buffers on and off (CPHAT = 0, CPHAR = 0)



Timing for Switching the Buffers on and off (CPHAT = 1, CPHAR = 1)



3A.5.9 MMCA Timing

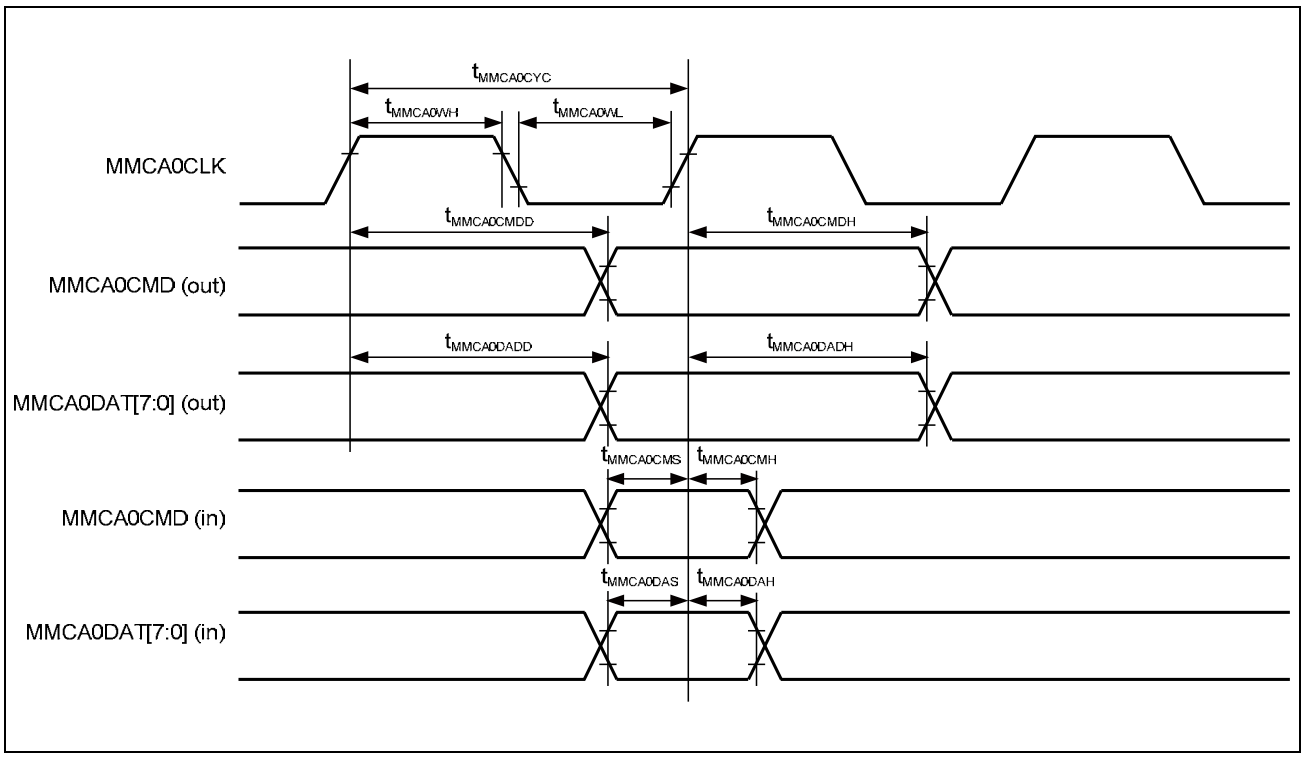
Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

MMCA0CLK, MMCA0CMD and MMCA0DAT[7:0] pin: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MMCA0CLK clock cycle	$t_{MMCA0CYC}$		2 × t_{CKSCLK_IPERI2}			ns
MMCA0CLK high time	$t_{MMCA0WH}$		10			ns
MMCA0CLK low time	$t_{MMCA0WL}$		10			ns
MMCA0CMD output data delay time	$t_{MMCA0CMDD}$				$t_{MMCA0CYC}$ × 1/2 + 19	ns
MMCA0CMD output data hold time	$t_{MMCA0CMDH}$		4			ns
Data output delay time	$t_{MMCA0DADD}$				$t_{MMCA0CYC}$ × 1/2 + 19	ns
Data output hold time	$t_{MMCA0DADH}$		4			ns
MMCA0CMD input data setup time	$t_{MMCA0CMS}$		10			ns
MMCA0CMD input data hold time	$t_{MMCA0CMH}$		7			ns
Data input setup time	$t_{MMCA0DAS}$		10			ns
Data input hold time	$t_{MMCA0DAH}$		7			ns

Note: t_{CKSCLK_IPERI2} is period of CKSCLK_IPERI2.



3A.5.10 CSI Timing

3A.5.10.1 CSIG Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3A.12 CSIG Timing (Master Mode)

<Output driver strength>

CSIGnSO, CSIGnSC (output): Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYMGn}		100			ns
CSIGnSC high level width	t_{KWHMGn}		0.5 × t_{KCYMGn} – 10			ns
CSIGnSC low level width	t_{KWLMGn}		0.5 × t_{KCYMGn} – 10			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSIMGn}		30			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSIMGn}		0			ns
CSIGnSO output delay (vs. CSIGnSC)	t_{DSOMGn}				7	ns
CSIGnRYI setup time (vs. CSIGnSC)	t_{SRYIGn}	CSIGnCTL1.CSIGnSIT = x CSIGnCTL1.CSIGnHSE = 1	2 × t_{KCYGn} + 25			ns
CSIGnRYI high level width	t_{WRYIGn}	CSIGnCTL1.CSIGnHSE = 1	t_{KCYGn} + 5			ns

Note: n = 0 to 4

Table 3A.13 CSIG Timing (Slave Mode)

<Output driver strength>

CSIGnSO: Fast mode

CSIGnRYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYSGn}		200			ns
CSIGnSC high level width	t_{KWHSGn}		0.5 × t_{KCYSGn} – 10			ns
CSIGnSC low level width	t_{KWLSGn}		0.5 × t_{KCYSGn} – 10			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSISGn}		20			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSISGn}		t_{KCYGn} + 5			ns
CSIGnSO output delay (vs. CSIGnSC)	t_{DSOSGn}				30	ns
CSIGnRYO output delay	t_{SRYOGn}				38	ns
$\overline{\text{CSIGnSSI}}$ setup time (vs. CSIGnSC)	$t_{SSSISGn}$		0.5 × t_{KCYSGn} – 5			ns
$\overline{\text{CSIGnSSI}}$ hold time (vs. CSIGnSC)	$t_{HSSISGn}$		t_{KCYGn} + 5			ns

Note: n = 0 to 4

3A.5.10.2 CSIH Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

Table 3A.14 CSIH Timing (Master Mode: 10 Mbps)

<Output driver strength>

CSIHnSO, CSIHnSC (output): Fast mode (CL = 100pF@n = 0 / 50pF@n = 1-4)

CSIHnCSSx: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYMHn}		100			ns
CSIHnSC high level width	t_{KWHMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSC low level width	t_{KWLMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSIMHn}	SI positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	19			ns
		SI negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	14			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSIMHn}	SI positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	0			ns
		SI negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	t_{KCYHn}/2			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOMHn}				7	ns
CSIHnRYI setup time (vs. CSIHnSC)	t_{SRYIHn}	CSIHnCTL1.CSIHnSIT = x CSIHnCTL1.CSIHnHSE = 1	2 × t_{KCYHn} + 25			ns
CSIHnRYI high level width	t_{WRYIHn}	CSIHnCTL1.CSIHnHSE = 1	t_{KCYHn} + 5			ns
CSIHnCSS0-7 inactive width	$t_{WSCSBHn}$		CSIDLE × t_{KCYMHn} – 15			ns
CSIHnCSS0-7 setup time (vs. CSIHnSC)	$t_{SSCSBHn0}$	CSIHnCFGx.CSIHnDAP = 0	CSSETUP × t_{KCYMHn} – 23			ns
	$t_{SSCSBHn1}$	CSIHnCFGx.CSIHnDAP = 1	(CSSETUP + 0.5) × t_{KCYMHn} – 23			ns
CSIHnCSS0-7 hold time (vs. CSIHnSC)	$t_{HSCSBHn0}$	CSIHnCTL1.CSIHnSIT = 0	CSSHOLD × t_{KCYMHn} – 5			ns
	$t_{HSCSBHn1}$	CSIHnCTL1.CSIHnSIT = 1	(CSSHOLD + 0.5) × t_{KCYMHn} – 5			ns

Note: n = 0 to 4

NOTE

CSIDLE: Setting value of CSIHnCFGx.CSIHnIDx[2:0]
CSSETUP: Setting value of CSIHnCFGx.CSIHnSPx[3:0]
CSSHOLD: Setting value of CSIHnCFGx.CSIHnHDx[3:0]
x: Depends on number of the chip select signals.

CAUTION

When the serial clock level is changed during the communication (CSIHnCFGx.CSIHnCKPx) and the IDLE has a setting of 0.5 transmission clock cycles, an inactive width time $t_{WSCSBHn}$ of "0.5 × t_{KCYMHn}" is added.

Table 3A.15 CSIH Timing (Slave Mode: 5 Mbps)

<Output driver strength>
CSIHnSO: Fast mode
CSIHnRYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYSHn}		200			ns
CSIHnSC high level width	t_{KWHSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSC low level width	t_{KWLSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSISHn}		20			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSISHn}		$t_{KCYHn} + 5$			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOSHn}				30	ns
CSIHnRYO output delay	t_{SRYOHn}	$t_{KCYSHn} \geq 8 \times t_{KCYHn}$			38	ns
		$t_{KCYSHn} < 8 \times t_{KCYHn}$			$38 + t_{KCYHn}$	ns
$\overline{\text{CSIHnSSI}}$ setup time (vs. CSIHnSC)	$t_{SSSISHn}$		$0.5 \times t_{KCYSHn} - 5$			ns
$\overline{\text{CSIHnSSI}}$ hold time (vs. CSIHnSC)	$t_{HSSISHn}$		$t_{KCYHn} + 5$			ns

Note: n = 0 to 4

Table 3A.16 CSIH Timing (Slave Mode: 8 Mbps)

<Output driver strength>
CSIHnSO: Fast mode
CSIHnRYO: Slow mode

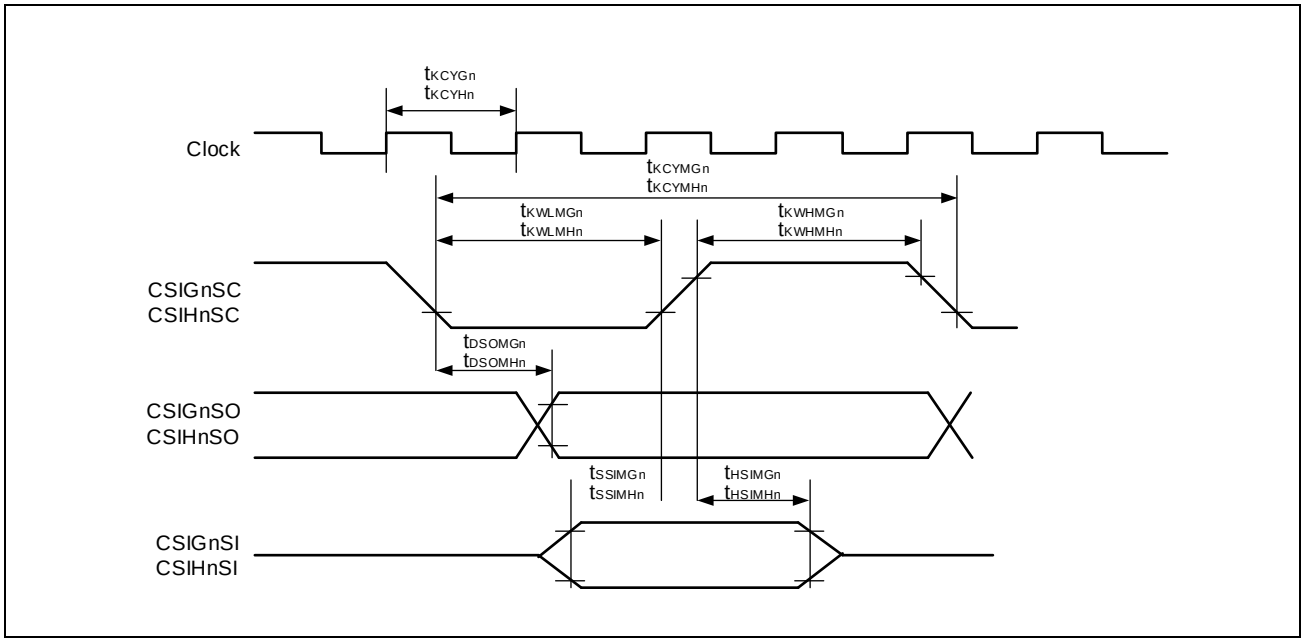
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYSHn}		125			ns
CSIHnSC high level width	t_{KWHSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSC low level width	t_{KWLSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSISHn}		12.5			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSISHn}		$t_{KCYHn} + 5$			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOSHn}				25	ns
CSIHnRYO output delay	t_{SRYOHn}	$t_{KCYSHn} \geq 8 \times t_{KCYHn}$			27	ns
		$t_{KCYSHn} < 8 \times t_{KCYHn}$			$27 + t_{KCYHn}$	ns
$\overline{\text{CSIHnSSI}}$ setup time (vs. CSIHnSC)	$t_{SSSISHn}$		$0.5 \times t_{KCYSHn} - 5$			ns
$\overline{\text{CSIHnSSI}}$ hold time (vs. CSIHnSC)	$t_{HSSISHn}$		$t_{KCYHn} + 5$			ns

Note: n = 2 (Only for CSIH2)

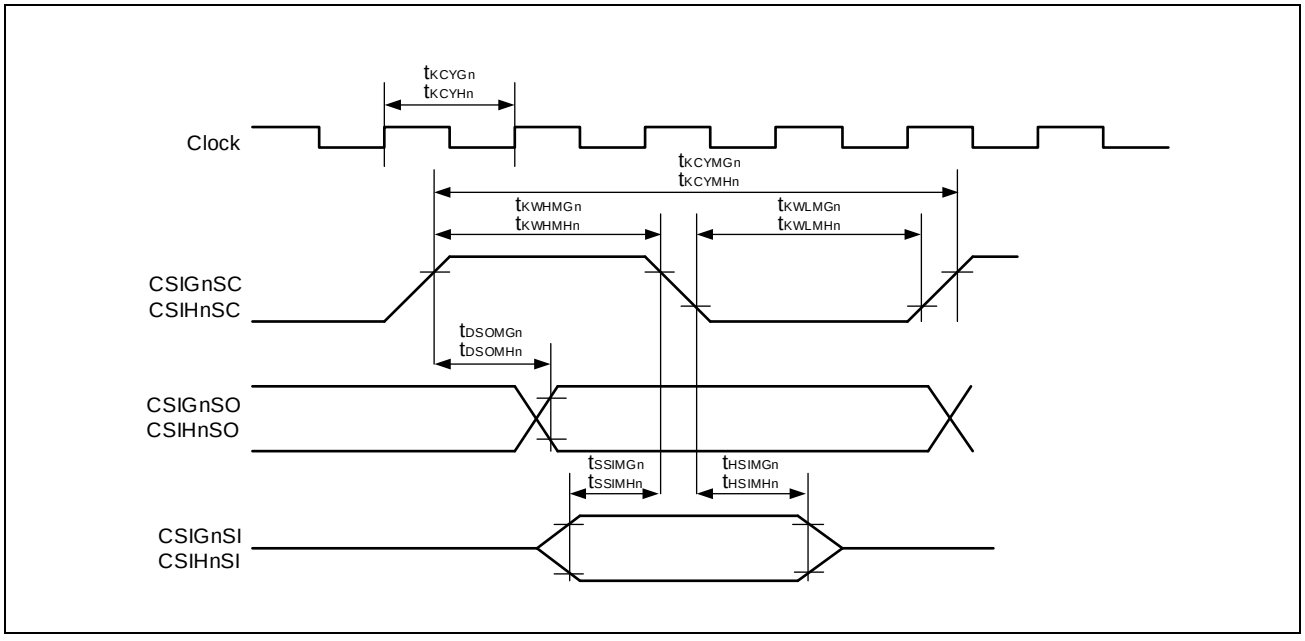
(1) SC/SI/SO

Master mode:

- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0 or 1/1)



- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0 or 0/1)



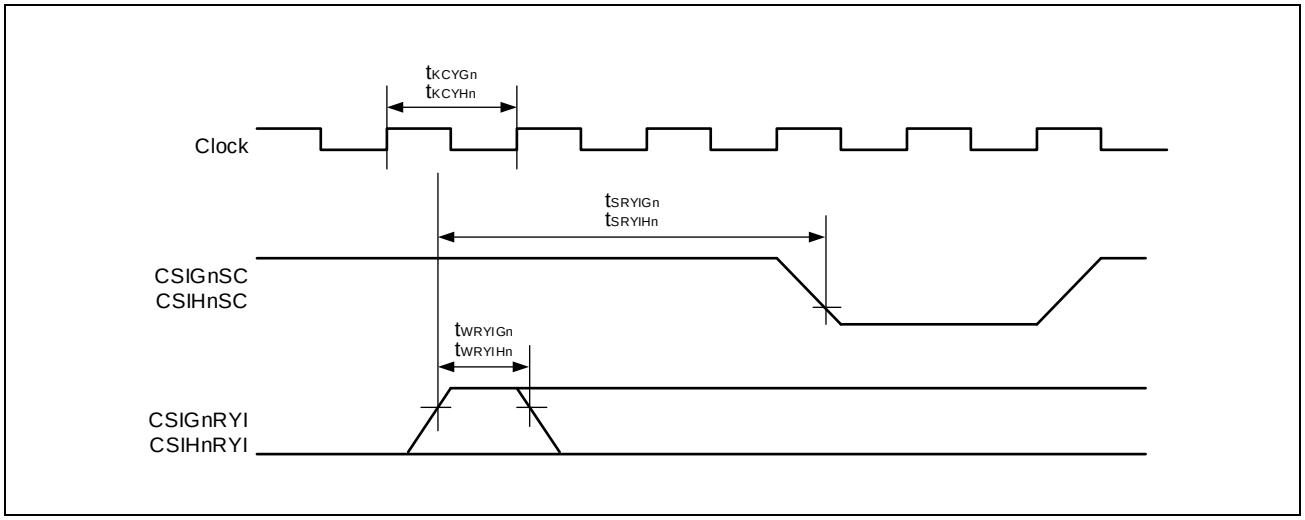
(2) RYI

Master mode:

- CSIG: Only master mode (CSIGnCTL1: CSIGnHSE = 1, CSIGnCTL1: CSIGnSIT = 0)
- CSIH: Only master mode (CSIHnCTL1: CSIHnHSE = 1, CSIHnCTL1: CSIHnSIT = 0)

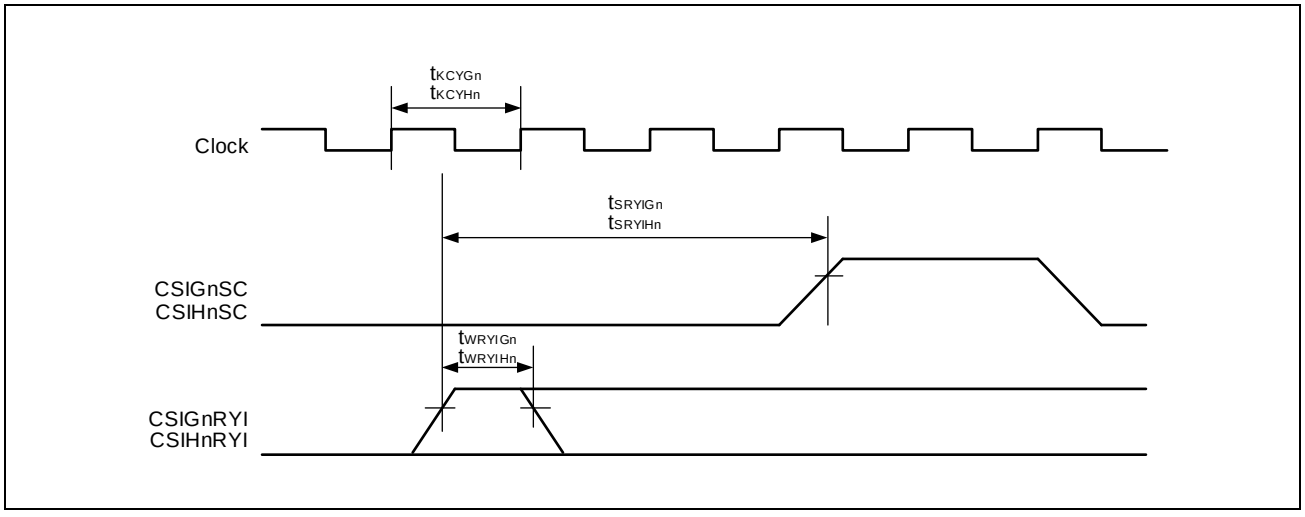
  – CSIG (CSIGnCTL1: CSIGnCKR = 0)

  – CSIH (CSIHnCFGx: CSIHnCKPx = 0)



  – CSIG (CSIGnCTL1: CSIGnCKR = 1)

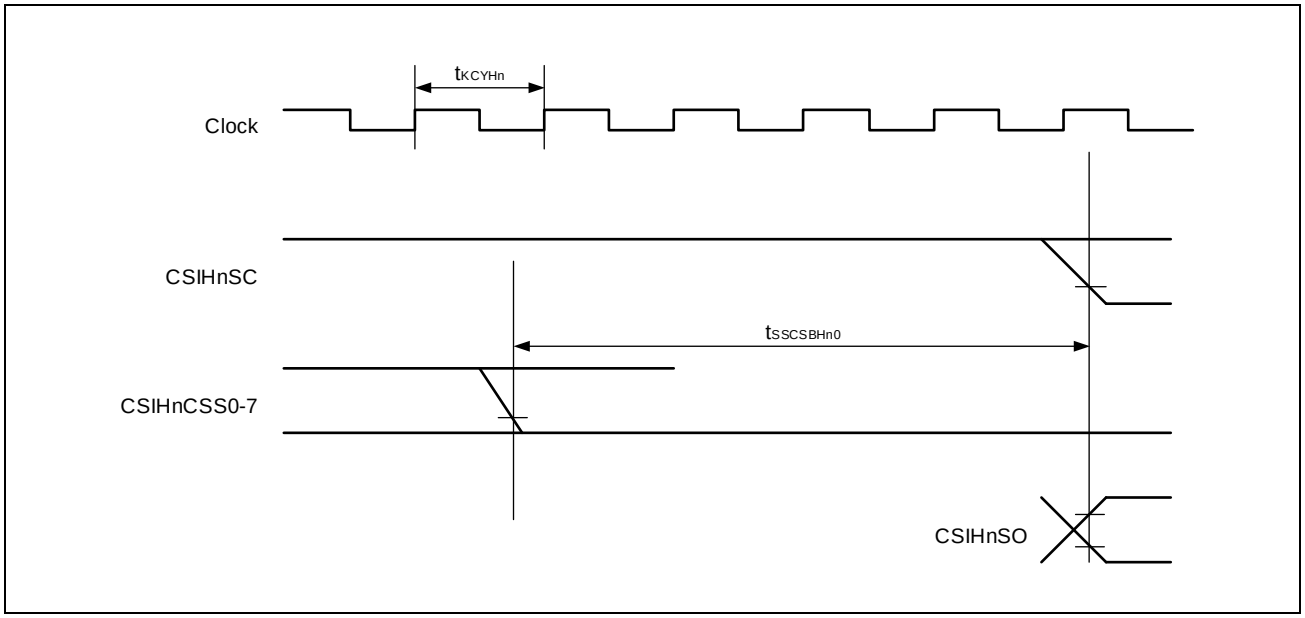
  – CSIH (CSIHnCFGx: CSIHnCKPx = 1)



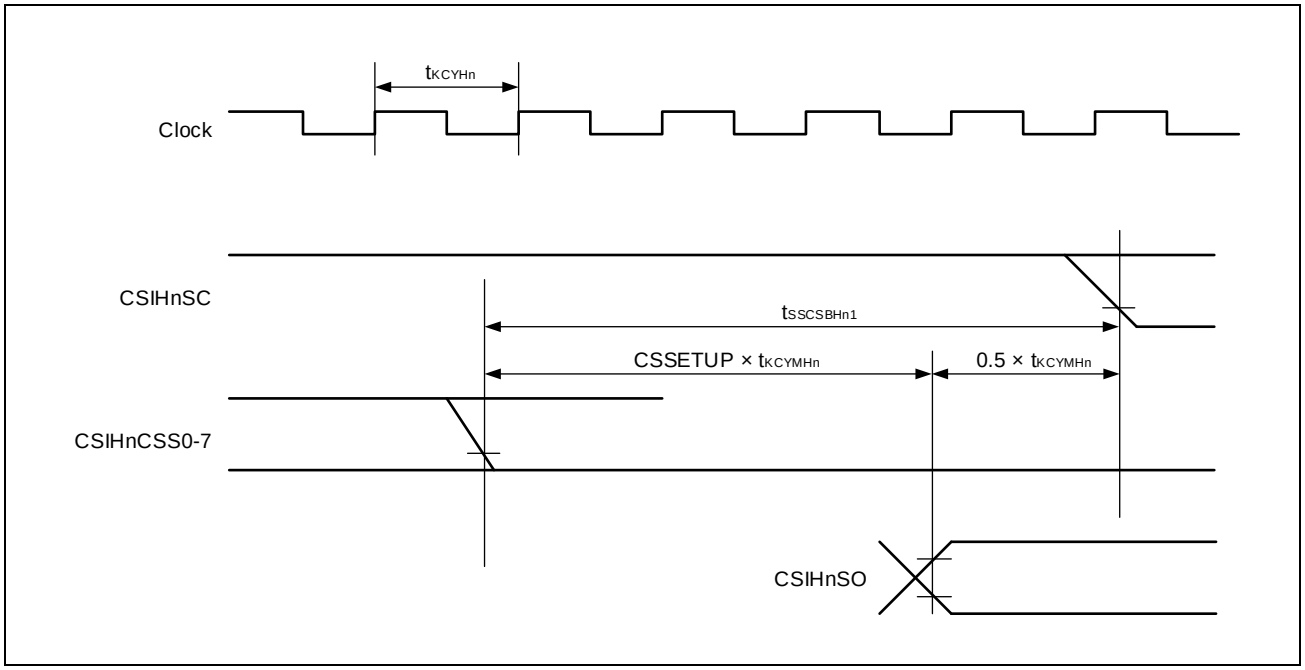
(3) CSSx

Only master mode (setup time):

- CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0

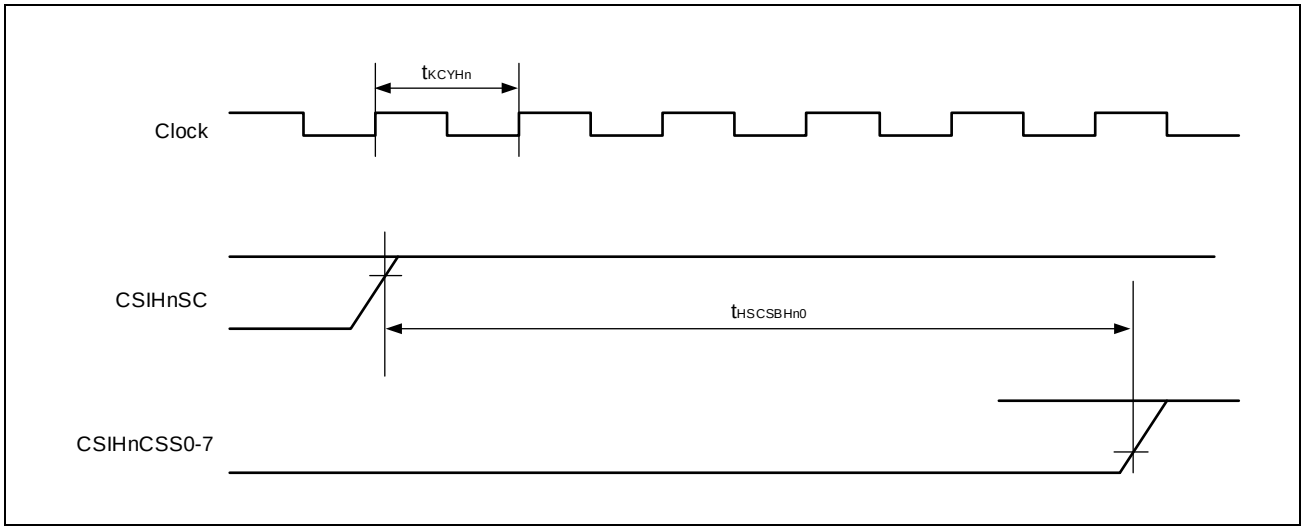


- CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 1

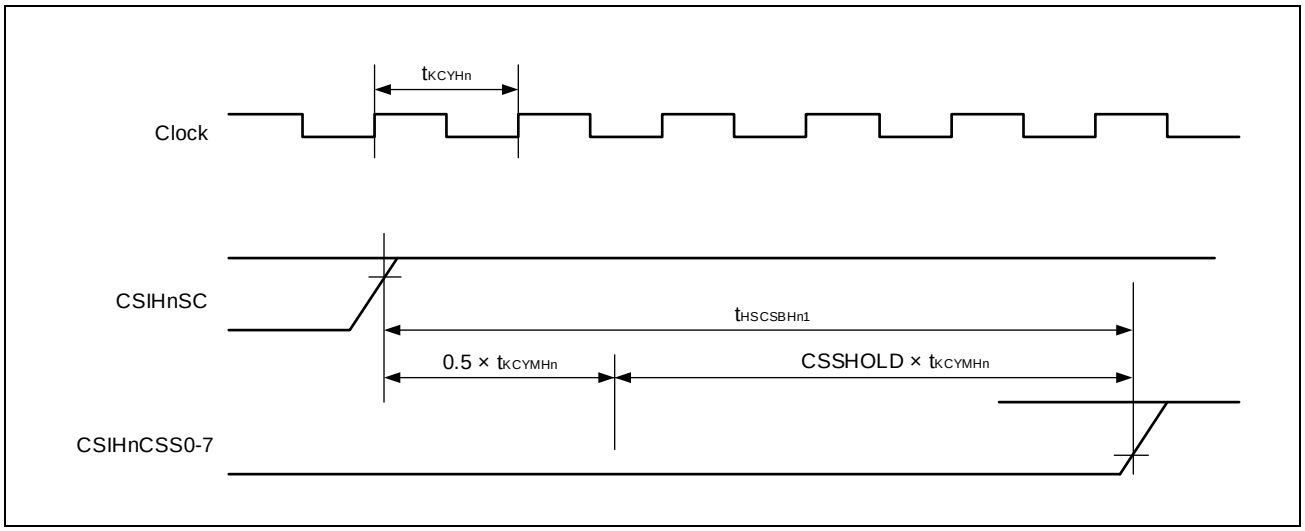


Only master mode (hold time):

- CSIHnCTL1: CSIHnSIT = 0, CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0



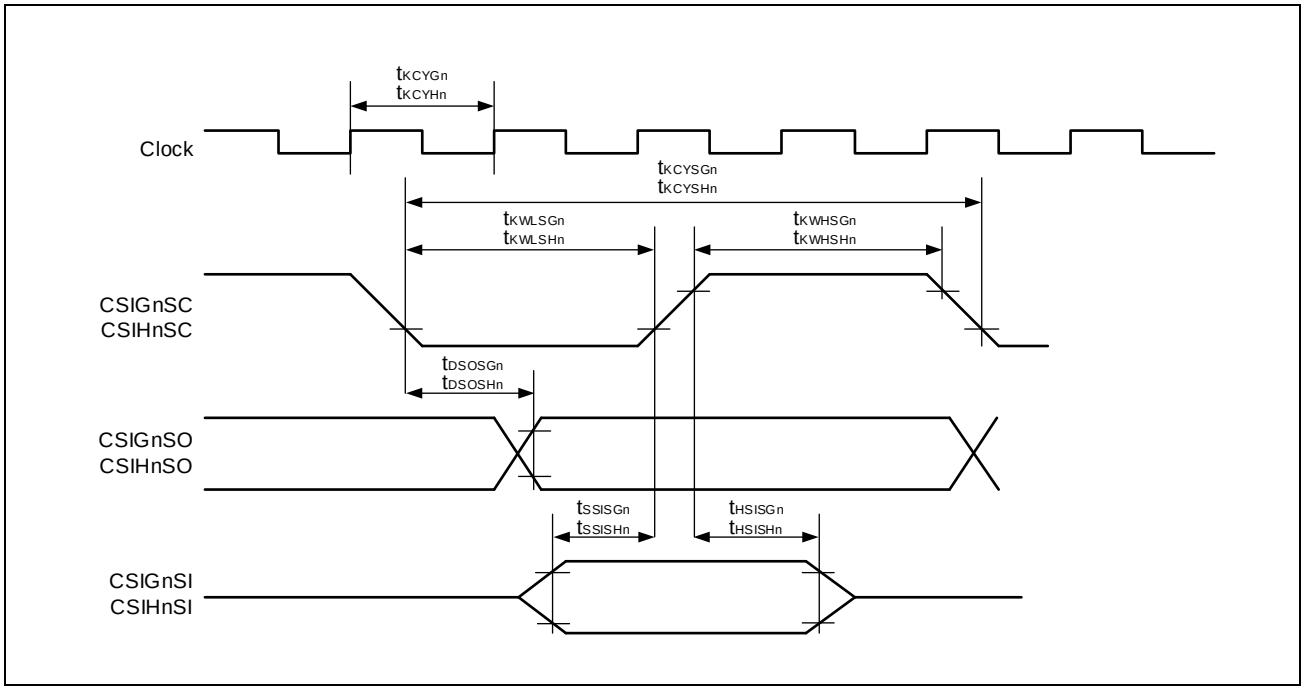
- CSIHnCTL1: CSIHnSIT = 1, CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0



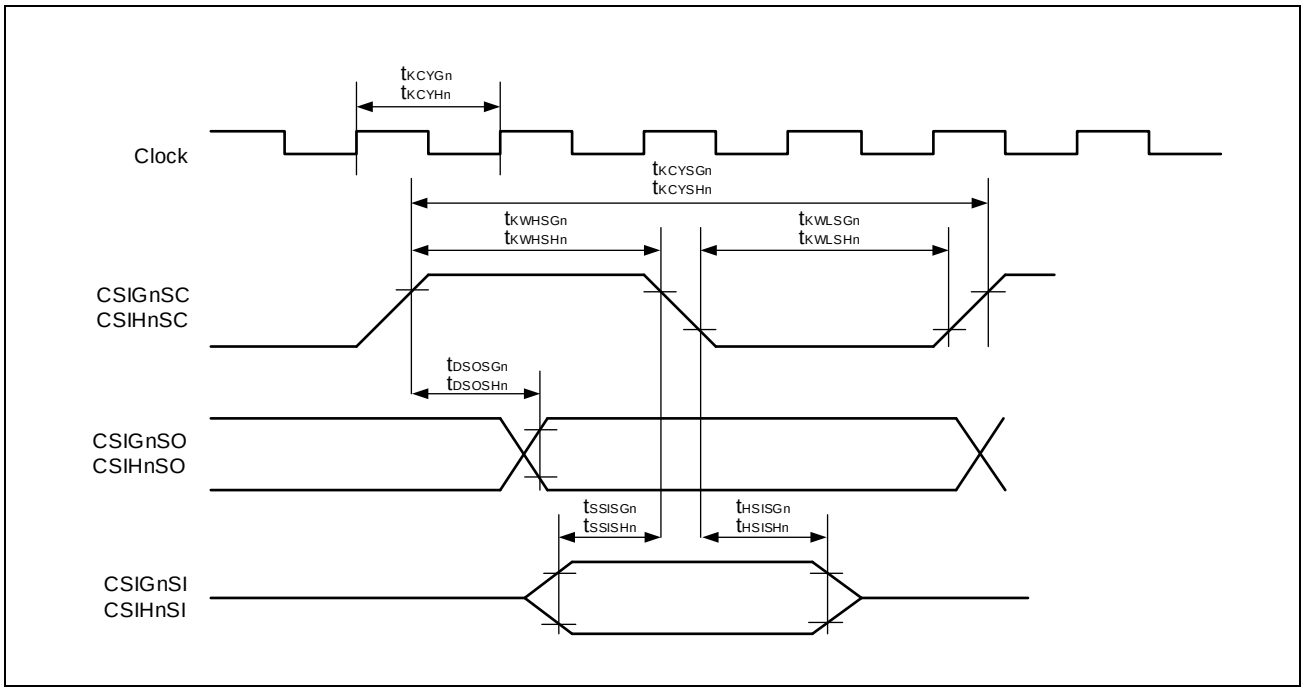
(4) SC/SI/SO

Slave mode:

- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0 or 1/1)

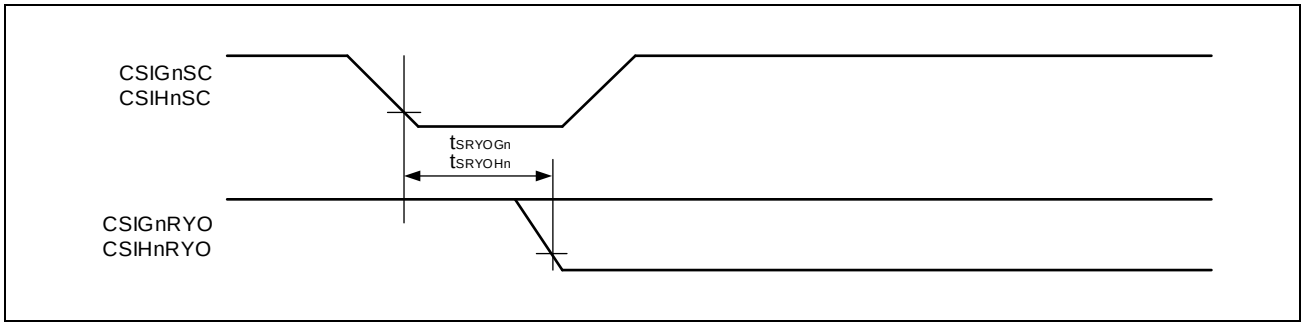


- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0 or 0/1)

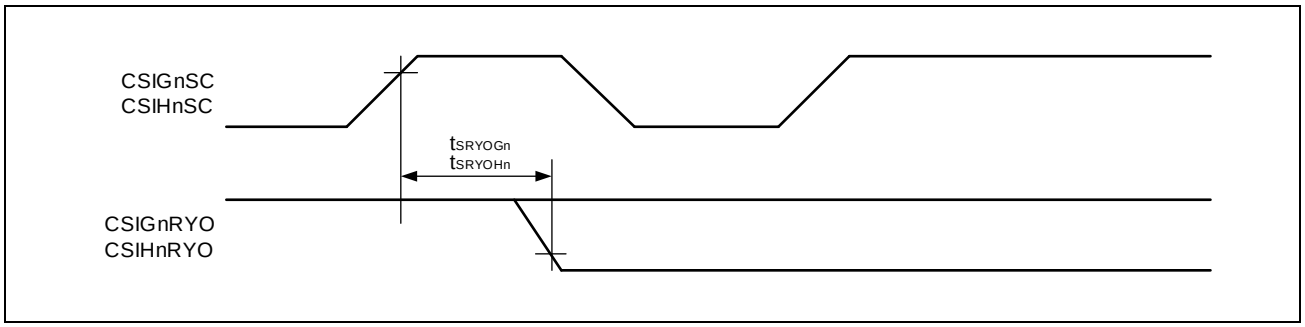


(5) RYO

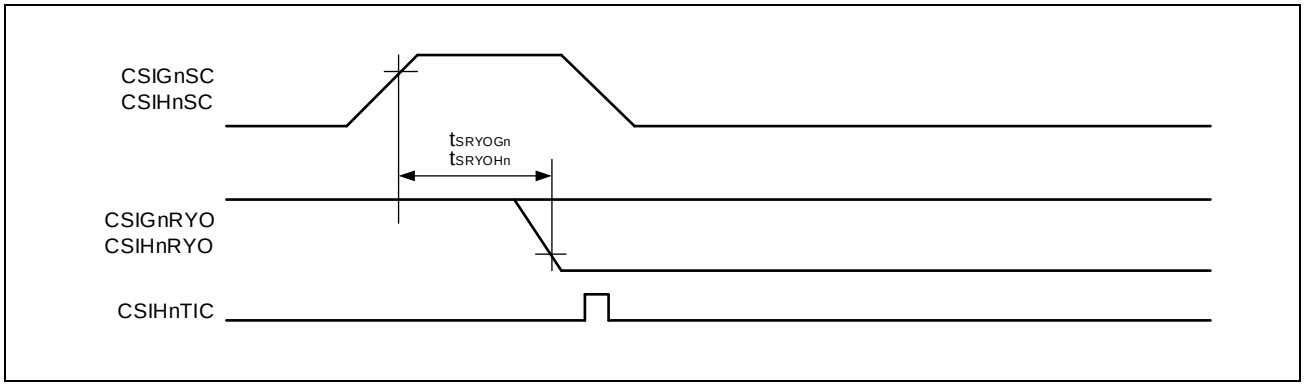
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0)



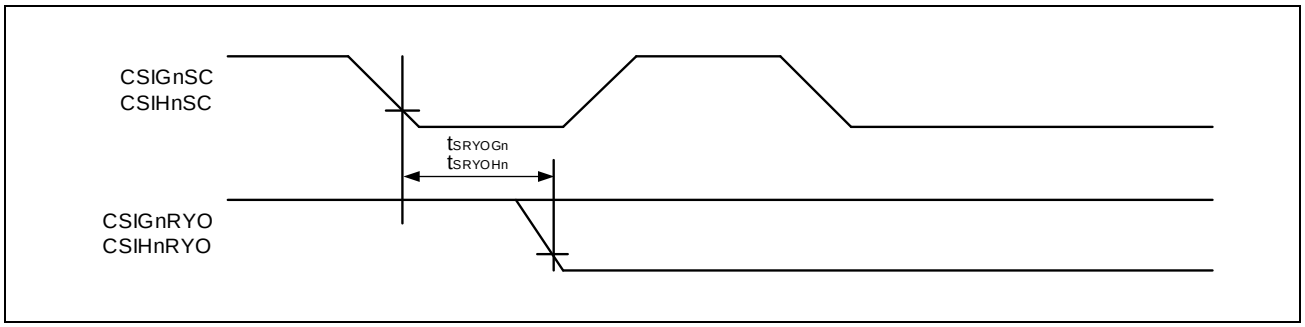
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/1)



- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0)



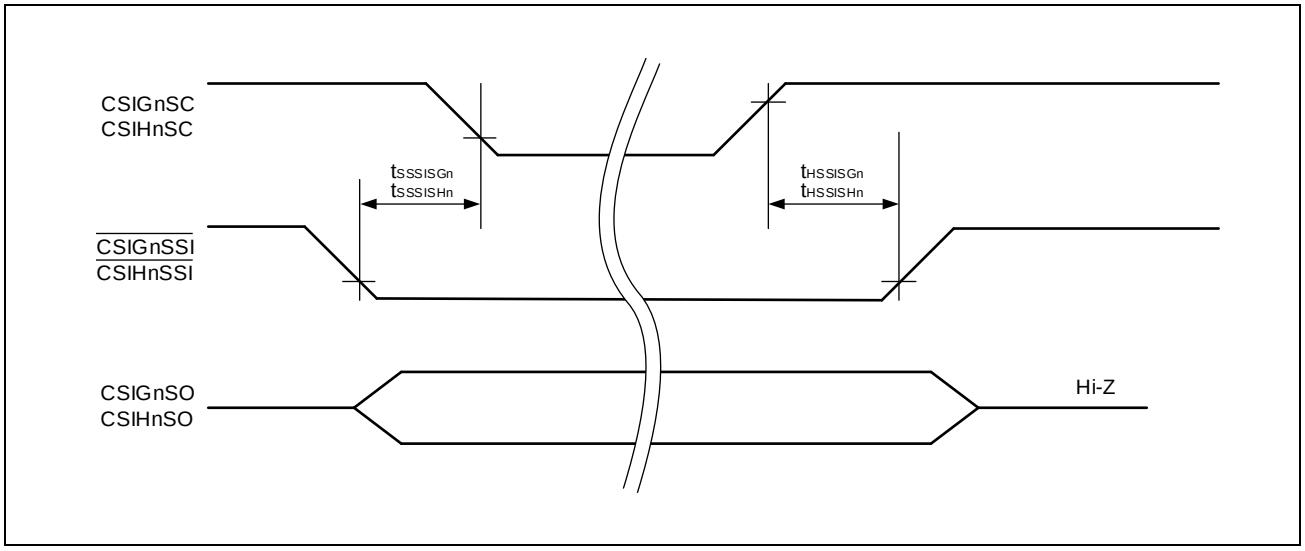
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/1)



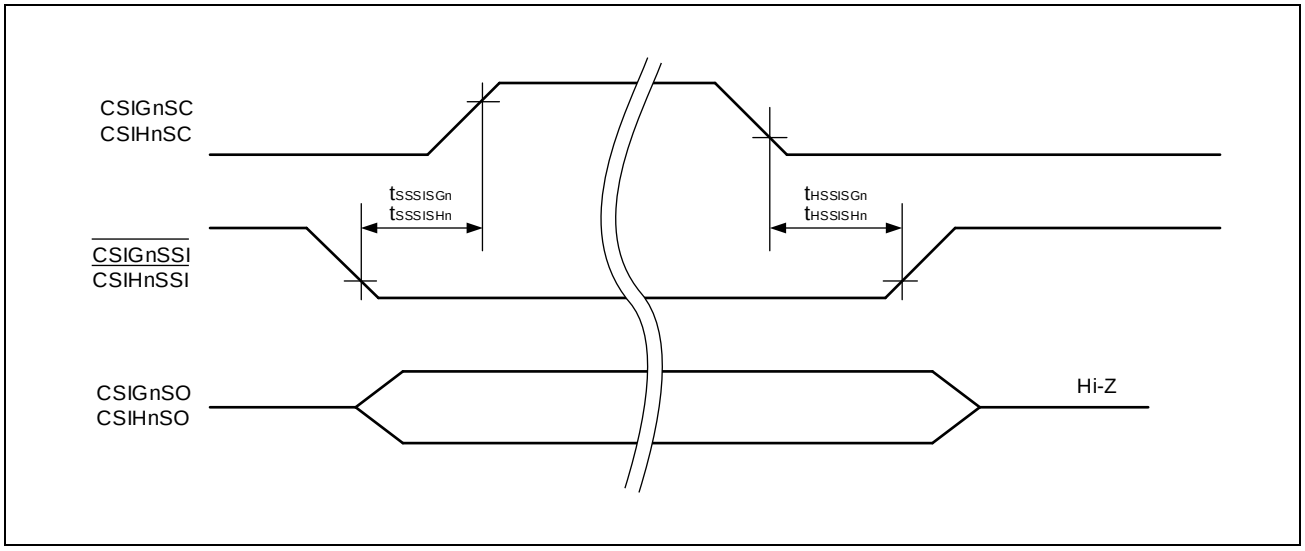
(6) SSI

Slave mode:

- CSIG (CSIGnCTL1: CSIGnSSE = 1, CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCTL1: CSIHnSSE = 1, CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0 or 1/1)



- CSIG (CSIGnCTL1: CSIGnSSE = 1, CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCTL1: CSIHnSSE = 1, CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0 or 0/1)



3A.5.11 RLIN2/RLIN3 Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate		LIN specification	1		20	kbps
		LIN extended baud rate	1		115.2*1	kbps
		UART function			1.5	Mbps
RLIN2 transfer rate		LIN specification	1		20	kbps

Note 1. The LIN extended baud rate is not part of the LIN standard specification.

3A.5.12 RIIC Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C

Table 3A.17 RIIC Timing (Normal Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIICnSCL clock period	f_{CLK}				100	kHz
Bus free time (between stop/start condition)	t_{BUF}		4.7			µs
Hold time*1	t_{HD}: STA		4.0			µs
RIICnSCL clock low-level width	t_{LOW}		4.7			µs
RIICnSCL clock high-level time	t_{HIGH}		4.0			µs
Setup time for start/restart condition	t_{SU}: STA		4.7			µs
Data hold time	t_{HD}: DAT	CBUS compatible master	5.0			µs
		I^2C mode	0*2			µs
Data setup time	t_{SU}: DAT		250			ns
Stop condition setup time	t_{SU}: STO		4.0			µs
Capacitance load of each bus line	Cb				400	pF

Remark: n = 0, 1

Note: If the system does not extend the RIICnSCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIICnSDA signal (at VIH min. of RIICnSCL signal). In order to occupy the undefined area at the falling edge of RIICnSCL.

Table 3A.18 RIIC Timing (Fast Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIICnSCL clock period	f_{CLK}				400	kHz
Bus free time (between stop/start condition)	t_{BUF}		1.3			µs
Hold time*1	t_{HD}: STA		0.6			µs
RIICnSCL clock low-level width	t_{LOW}		1.3			µs
RIICnSCL clock high-level time	t_{HIGH}		0.6			µs
Setup time for start/restart condition	t_{SU}: STA		0.6			µs
Data hold time	t_{HD}: DAT	I^2C mode	0*2			µs
Data setup time	t_{SU}: DAT		100*3			ns
Stop condition setup time	t_{SU}: STO		0.6			µs
Pulse width with spike suppressed by input filter	t_{SP}		0		50	ns
Capacitance load of each bus line	Cb				400	pF

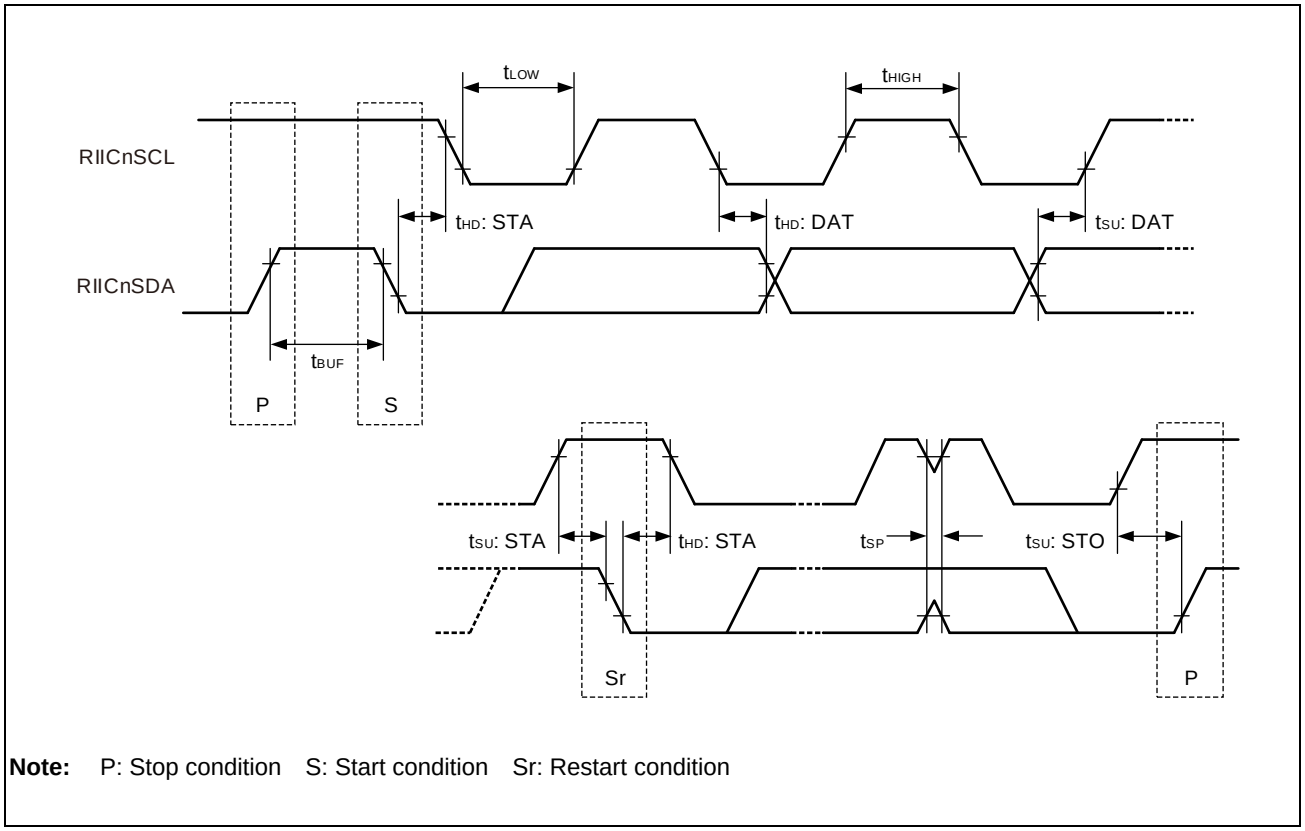
Remark: n = 0, 1

Note: If the system does not extend the RIICnSCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIICnSDA signal (at VIH min. of RIICnSCL signal). In order to occupy the undefined area at the falling edge of RIICnSCL.

Note 3. The fast mode I^2C bus can be used in normal mode I^2C bus system. In this case, set the fast mode I^2C bus so that it meets the following conditions.
- If the system does not extend the RIICnSCL signal's low state hold time: t_{SU}: DAT ≥ 250 ns
- If the system extends the RIICnSCL signal's low state hold time:
Transmit the following data bit to the RIICnSDA line prior to releasing the RIICnSCL line
(1250 ns: Normal mode I^2C bus specification).



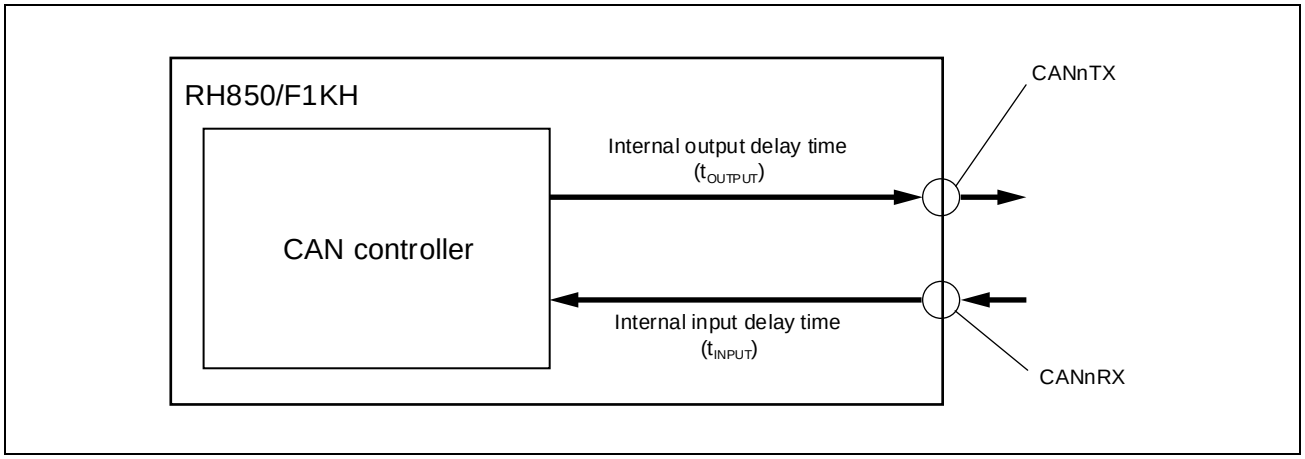
Note: P: Stop condition S: Start condition Sr: Restart condition

3A.5.13 RS-CANFD Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate		Classical CAN mode			1	Mbps
Data bit rate (CAN FD mode)		Nominal bit rate ≤ 500 kbps			5	Mbps
		Nominal bit rate > 500 kbps			2	Mbps
Internal delay time*1	t_{NODE}				50	ns

Note 1. t_{NODE} = Internal input delay time (t_{INPUT}) + Internal output delay time (t_{OUTPUT})



3A.5.14 FlexRay Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

Products of CPU frequency 240 MHz max.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					10	Mbps

Products of CPU frequency 160 MHz max.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					5	Mbps

3A.5.15 Ethernet Timing

3A.5.15.1 MII Interface

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to 3.6 V, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 15 pF

<Output driver strength>

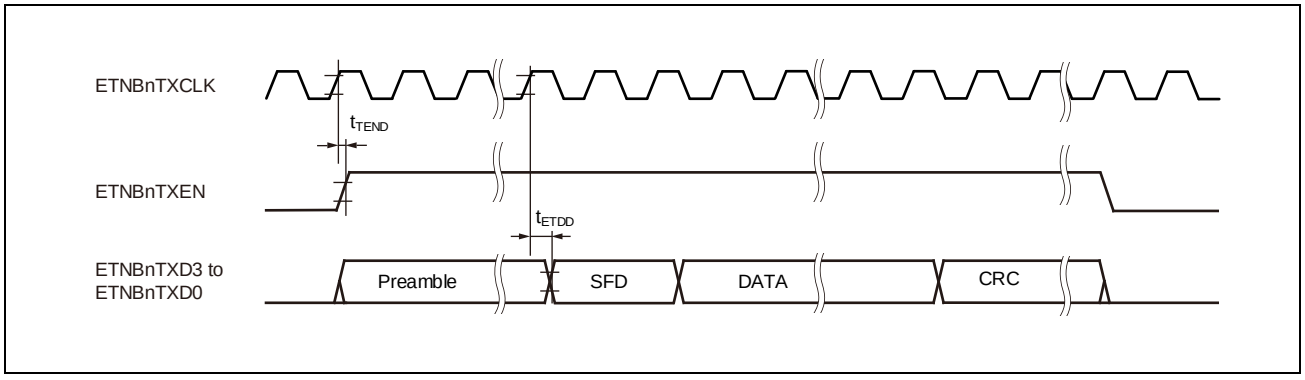
ETNBnTXD3-0 and ETNBnTXEN pins: Fast mode

ETNBnTXCLK pin: TTL type

Table 3A.19 MII Interface (Transmission Interface)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNBnTXCLK clock period	t_{Tcyc}	100 Mbps	40 – 100 ppm	40	40 + 100 ppm	ns
		10 Mbps	400 – 100 ppm	400	400 + 100 ppm	ns
ETNBnTXEN delay vs ETNBnTXCLK ↑	t_{TEND}	CL = 15 pF			18	ns
ETNBnTXD[3:0] delay vs ETNBnTXCLK ↑	t_{ETDD}	CL = 15 pF			18	ns

Note: n = 0, 1

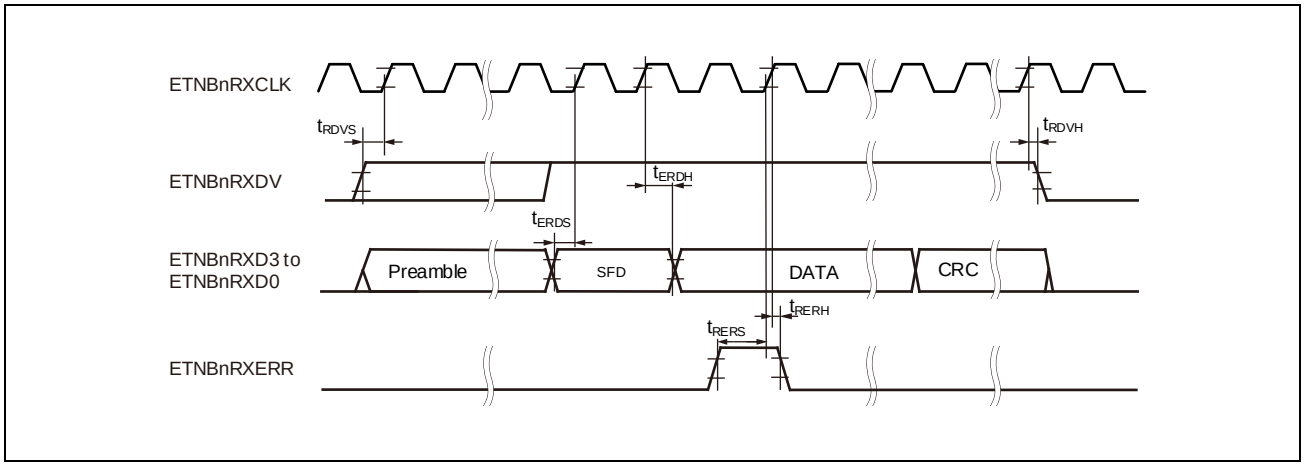


<Input buffer>
ETNBnRXCLK, ETNBnRXDV, ETNBnRXD[3:0], and ETNBnRXER pins: TTL type

Table 3A.20 MII Interface (Reception Interface)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNBnRXCLK clock period	t_{Rcyc}	100 Mbps	40 – 100 ppm	40	40 + 100 ppm	ns
		10 Mbps	400 – 100 ppm	400	400 + 100 ppm	ns
ETNBnRXDV hold time vs ETNBnRXCLK ↑	t_{RDVH}		10			ns
ETNBnRXDV setup time vs ETNBnRXCLK ↑	t_{RDVS}		10			ns
ETNBnRXD[3:0] hold time vs ETNBnRXCLK ↑	t_{ERDH}		10			ns
ETNBnRXD[3:0] setup time vs ETNBnRXCLK ↑	t_{ERDS}		10			ns
ETNBnRXERR hold time vs ETNBnRXCLK ↑	t_{RERH}		10			ns
ETNBnRXERR setup time vs ETNBnRXCLK ↑	t_{RERS}		10			ns

Note: n = 0, 1



3A.5.15.2 Management Interface

Timing of management interface (ETNBnMDC and ETNBnMDIO) depends on software. It is necessary to adjust wait time according to AC specification of PHY.

3A.5.16 RSENT Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Tick Time			1		90	µs

3A.5.17 Timer Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

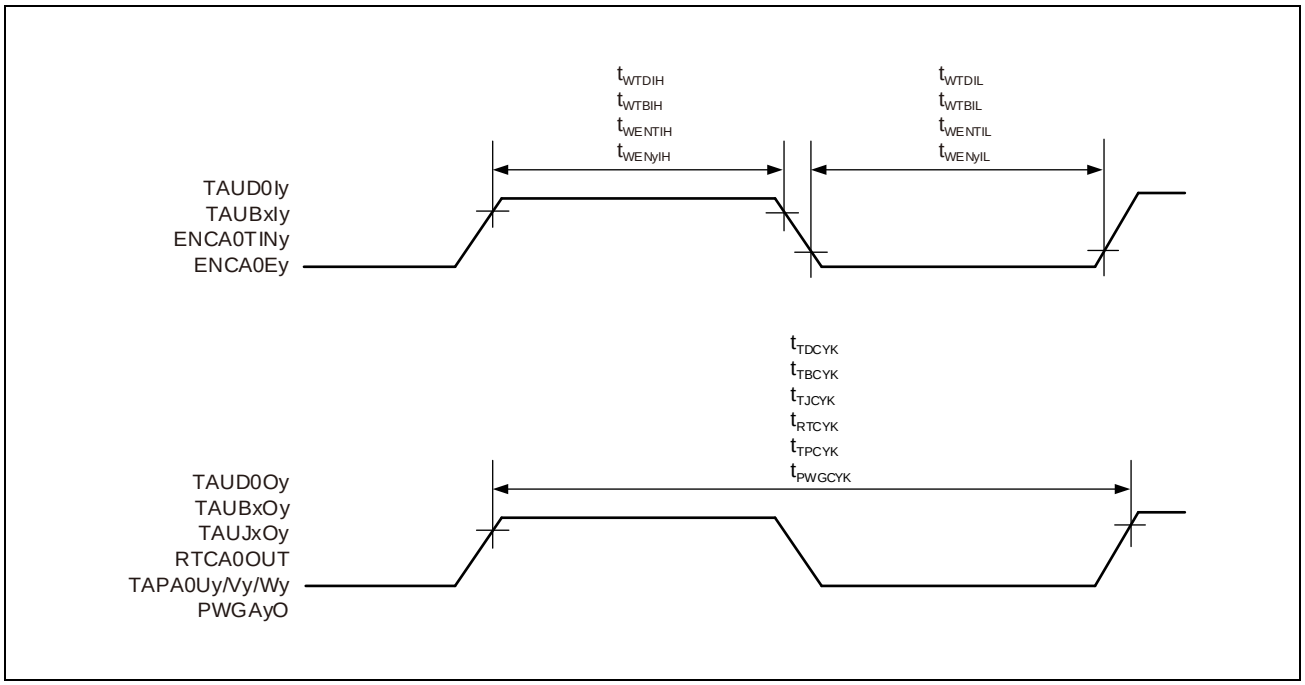
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUD0Iy input high/low level width (y = 0 to 15)	t_{WTDIH}/ t_{WTDIL}		n × Tsamp + 20*1,*2			ns
TAUD0Oy output cycle (y = 0 to 15)	t_{TDCYK}	Slow mode			10	MHz
TAUBxIy input high/low level width (x = 0, 1, y = 0 to 15)	t_{WTBIH}/ t_{WTBIL}		n × Tsamp + 20*1,*2			ns
TAUBxOy output cycle (x = 0, 1, y = 0 to 15)	t_{TBCYK}	Slow mode			10	MHz
TAUJxIy input high/low level width*3 (x = 0 to 3, y = 0 to 3)	t_{WTJIH}/ t_{WTJIL}		600			ns
TAUJxIy pulse rejection*4	t_{WTIJRJ}		100			ns
TAUJxOy output cycle (x = 0 to 3, y = 0 to 3)	t_{TJCYK}	Slow mode			10	MHz
RTCA0OUT output cycle	t_{RTCYK}			1		Hz
TAPA0ESO input high/low level width*3	t_{WESIH}/ t_{WESIL}		600			ns
TAPA0ESO pulse rejection*4	t_{WESIRJ}		100			ns
TAPA0Uy/Vy/Wy output cycle (y = P, N)	t_{TPCYK}	Slow mode			10	MHz
ENCA0TINy input high/low level width (y = 0, 1)	t_{WENTIH}/ t_{WENTIL}		n × Tsamp + 20*1			ns
ENCA0Ey input high/low level width (y = 0, 1, C)	t_{WENyIH}/ t_{WENyIL}		n × Tsamp + 20*1			ns
PWGAyO output cycle (y = 0 to 95)	t_{PWGCYK}	Slow mode			10	MHz

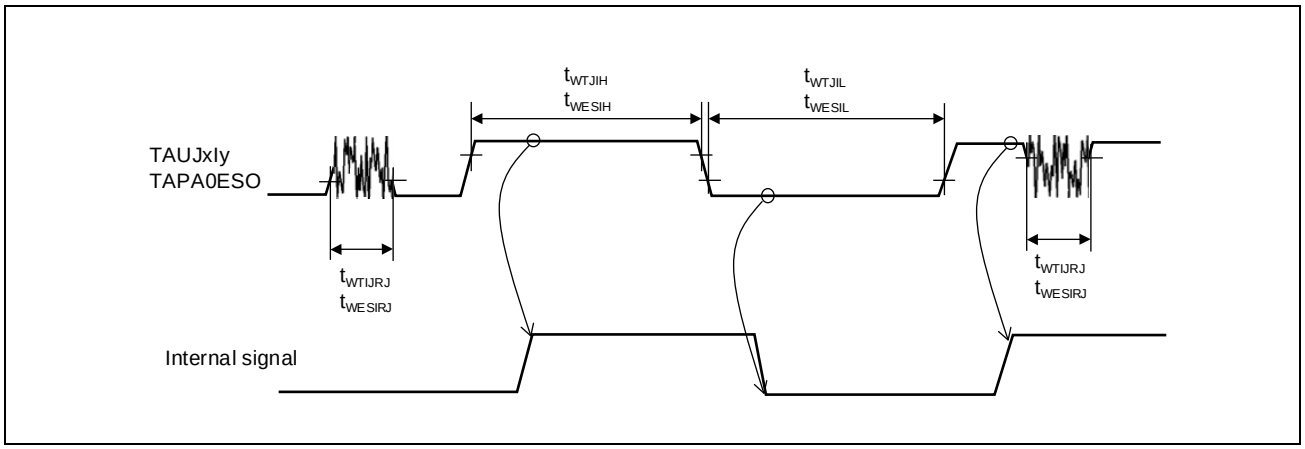
Note 1. n: Sampling number of the digital noise filter for each input.
Tsamp: Sampling time of the digital noise filter for each input.

Note 2. Input more than 1 count clock width of each timer counter channel.

Note 3. TAUJxIy and TAPA0ESO input width is needed to ensure that the internal timer input signal is activated.

Note 4. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.


t_{WTDIH}
t_{WTBIH}
t_{WENTIH}
t_{WENyIH}
t_{WTDIL}
t_{WTBIL}
t_{WENTIL}
t_{WENyIL}
TAUD0Iy
TAUBxIy
ENCA0TINy
ENCA0Ey
t_{TDCYK}
t_{TBCYK}
t_{TJCYK}
t_{RTCYK}
t_{TPCYK}
t_{PWGCYK}
TAUD0Oy
TAUBxOy
TAUJxOy
RTCA0OUT
TAPA0Uy/Vy/Wy
PWGAyO

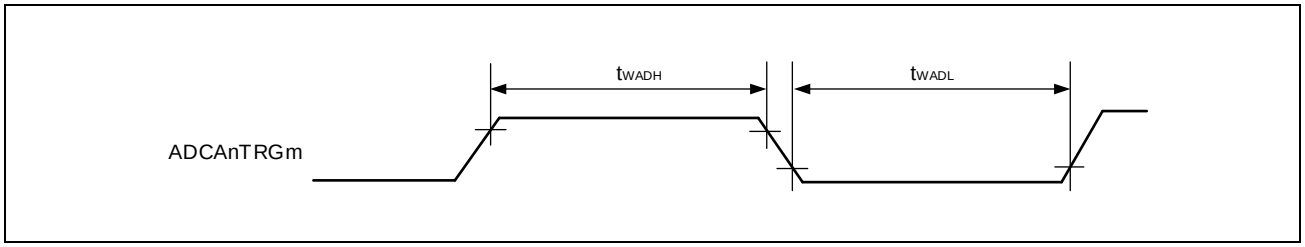

t_{WTJIH}
t_{WESIH}
t_{WTJIL}
t_{WESIL}
TAUJxIy
TAPA0ESO
t_{WTIJRJ}
t_{WESIRJ}
t_{WTIJRJ}
t_{WESIRJ}
Internal signal

3A.5.18 ADTRG Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCAnTRGm input high/ low level width	t_{WADH}/t_{WADL}		k × Tsamp + 20*1			ns

Note 1. k: Sampling number of the digital noise filter for each input.
Tsamp: Sampling time of the digital noise filter for each input.



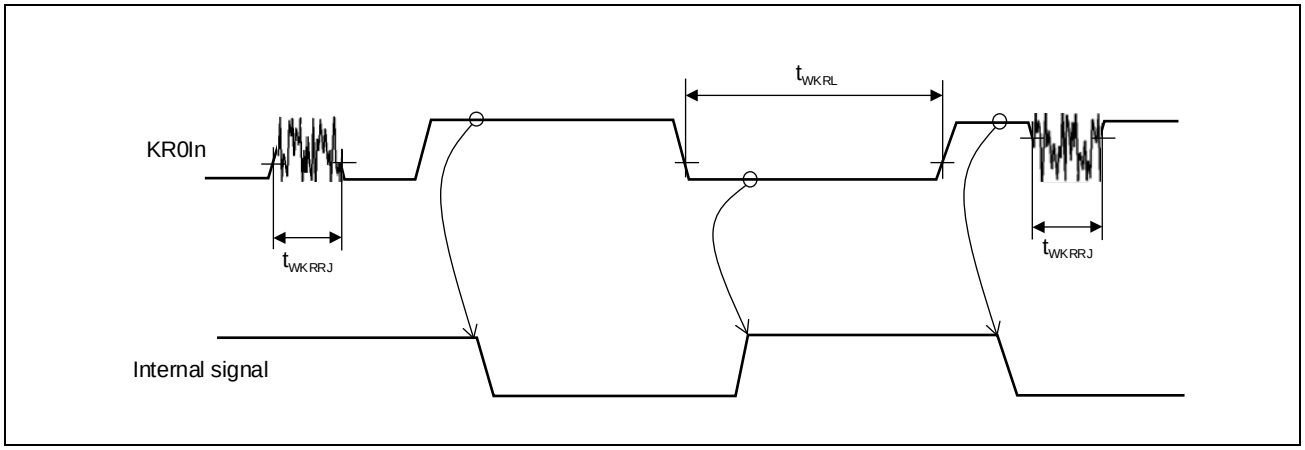
3A.5.19 Key Return Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
KR0In input low level width*1	t_{WKRL}		600			ns
KR0In pulse rejection*2	t_{WKRRJ}		100			ns

Note 1. KR0In input width is needed to ensure that the internal key input signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value.
Noise such as the figure can be filtered.



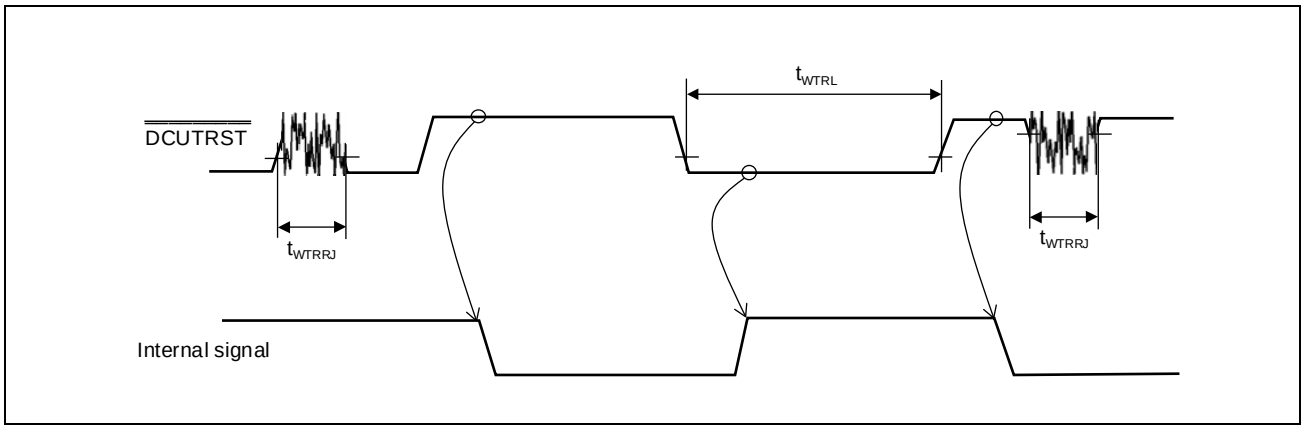
3A.5.20 $\overline{\text{DCUTRST}}$ Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{DCUTRST}}$ input low level width*1	t_{WTRL}		600			ns
$\overline{\text{DCUTRST}}$ pulse rejection*2	t_{WTRRJ}		100			ns

Note 1. $\overline{\text{DCUTRST}}$ input width is needed to ensure that the internal DCU reset input signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value.
Noise such as the figure can be filtered.



3A.5.21 Debug Interface Characteristics

3A.5.21.1 Nexus Interface Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

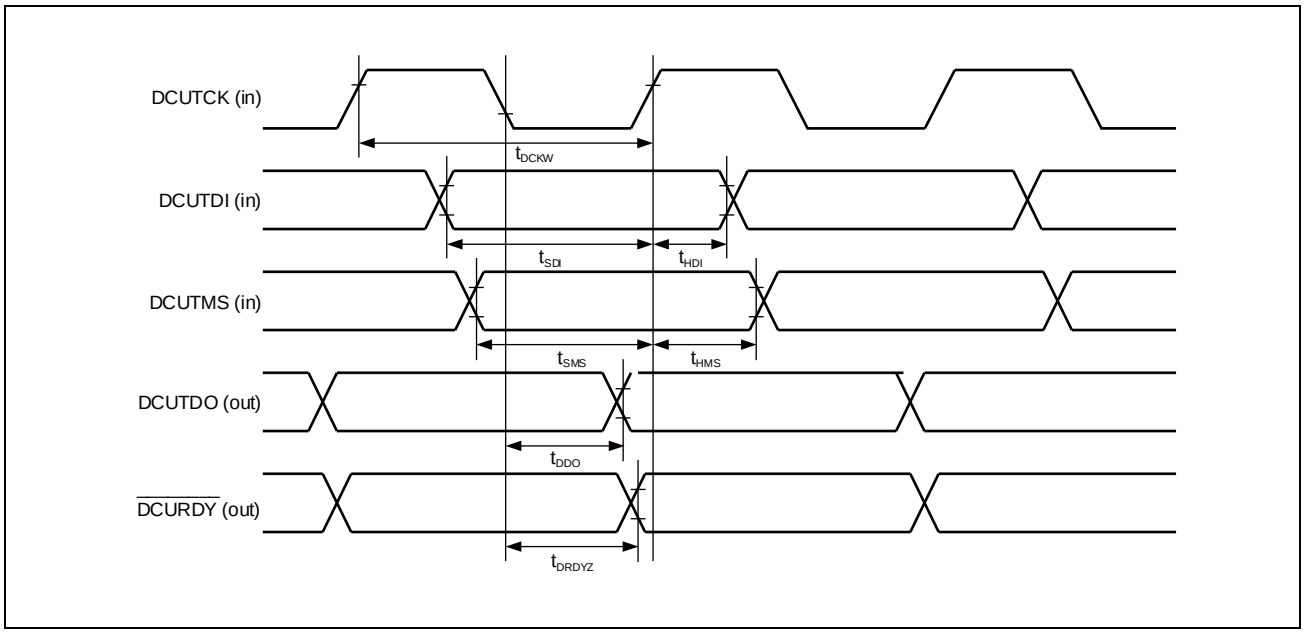
<Input buffer>

DCUTDI, DCUTCK, DCUTMS, $\overline{\text{DCUTRST}}$: TTL

<Output driver strength>

DCUTDO, $\overline{\text{DCURDY}}$: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DCUTCK cycle width	t_{DCKW}		50			ns
DCUTDI setup time (vs DCUTCK ↑)	t_{SDI}		12			ns
DCUTDI hold time (vs DCUTCK ↑)	t_{HDI}		3			ns
DCUTMS setup time (vs DCUTCK ↑)	t_{SMS}		12			ns
DCUTMS hold time (vs DCUTCK ↑)	t_{HMS}		3			ns
DCUTDO delay time (↓ DCUTCK)	t_{DDO}		0		20	ns
$\overline{\text{DCURDY}}$ delay time (↓ DCUTCK)	t_{RDYZ}		0		20	ns



3A.5.21.2 LPD (4 Pins) Interface Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 100 pF

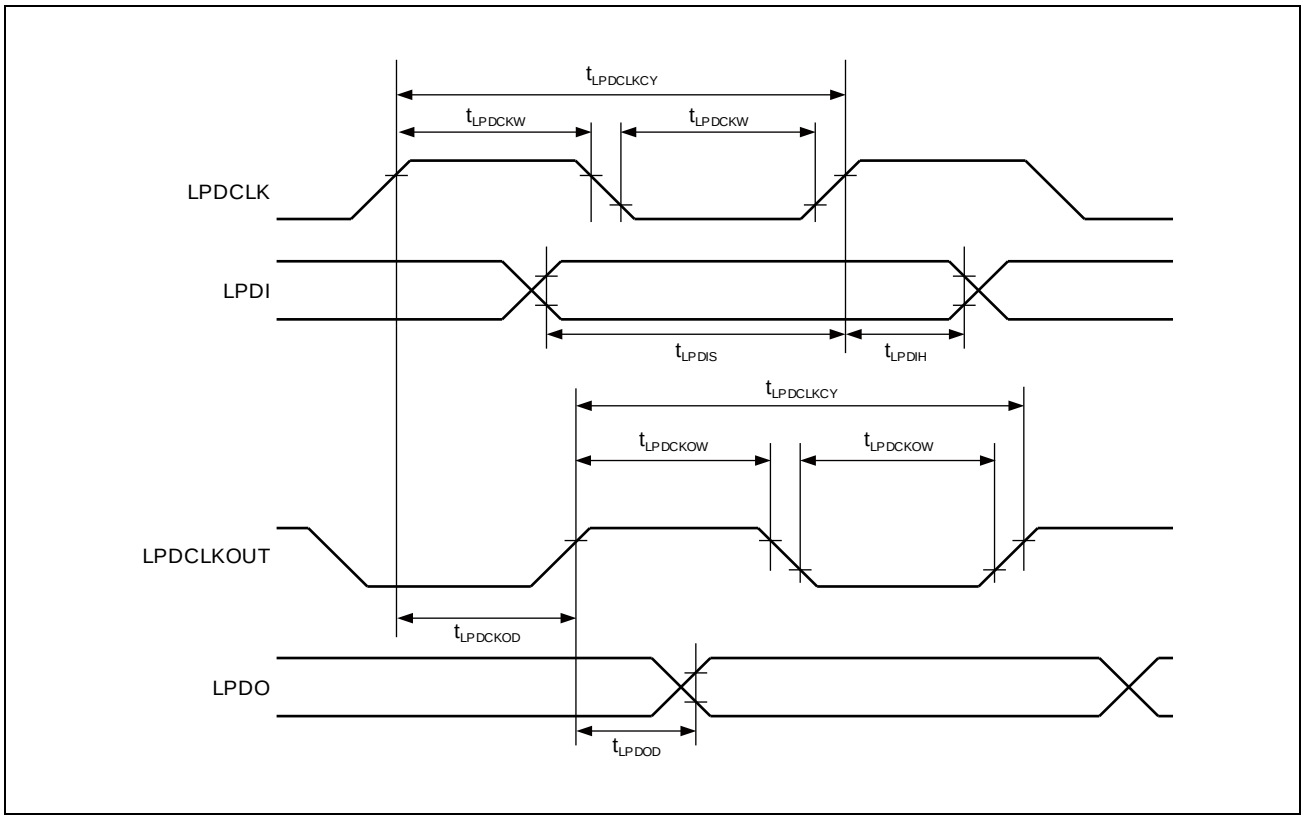
<Input buffer>

LPDCLK, LPDI: TTL

<Output driver strength>

LPDCLKOUT, LPDO: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPDCLK cycle time/ LPDCLKOUT cycle time	$t_{LPDCLKCY}$		83.3 (max.12 MHz)			ns
LPDCLK High-level width/ LPDCLK Low-level width	t_{LPDCKW}		0.5 × $t_{LPDCLKCY}$ – 10			ns
LPDCLKOUT High-level width/ LPDCLKOUT low-level width	$t_{LPDCKOW}$		t_{LPDCKW} – 10			ns
LPDI setup time (LPDCLK ↑)	t_{LPDIS}		41			ns
LPDI hold time (LPDCLK ↑)	t_{LPDIH}		3			ns
LPDCLK to LPDCLKOUT delay time	$t_{LPDCKOD}$				44	ns
LPDO delay time (LPDCLKOUT ↑)	t_{LPDOD}		0		15	ns



3A.5.21.3 LPD (1 Pin) Interface Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 50 pF

<Input buffer>
LPDIO: TTL

<Output driver strength>
LPDIO: Fast mode

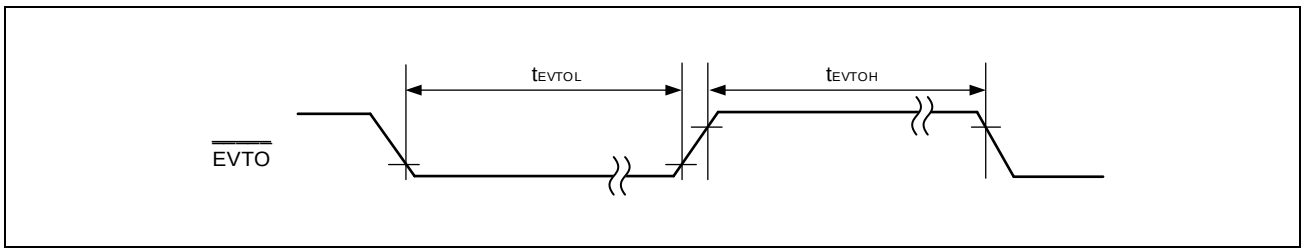
<External pull-up resistor>
LPDIO: 1 kΩ to 10 kΩ

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPD (1 pin) baud rate					2.0	Mbps

3A.5.21.4 Debug Event Interface Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 50 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{EVTO}}$ high/low level width	t_{EVTOH}/t_{EVTOL}		50			ns



3A.6 A/D Converter Characteristics

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

(1/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Conversion clock	ADCLKn				8*3		40	MHz
Resolution	RESn	12-bit mode			12	12	12	bit
		10-bit mode			10	10	10	bit
Conversion time	t_{CONn}	ADCAnSMPCR.SMPT[7:0] = 12 H (40 cycle) (8M Hz*3 ≤ ADCLKn ≤ 32 MHz), External MPX is not used			1.25		5	µs
		ADCAnSMPCR.SMPT[7:0] = 18 H (46 cycle) (8 MHz*3 ≤ ADCLKn ≤ 40 MHz), External MPX is not used			1.15		5.75	µs
		ADCAnSMPCR.SMPT[7:0]=12 H (80 cycle) (8 MHz*3 ≤ ADCLKn ≤ 32 MHz), External MPX is used			2.5*4		10	µs
		ADCAnSMPCR.SMPT[7:0] = 18 H (92 cycle) (8 MHz*3 ≤ ADCLKn ≤ 40 MHz), External MPX is used			2.3*4		11.5	µs
Sampling time	t_{SMP}	ADCAnSMPCR.SMPT[7:0] = 12 H (18 cycle) (8 MHz*3 ≤ ADCLKn ≤ 32 MHz)			0.56		2.25	µs
		ADCAnSMPCR.SMPT[7:0] = 18 H (24cycle) (8 MHz*3 ≤ ADCLKn ≤ 40 MHz)			0.6		3	µs
Overall error*1	TOEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±4.0	LSB
				ADCA0I0-5 (T&H used)			±6.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±6.0	LSB
				ADCA0I0-5 (T&H used)			±8.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB
Analog input voltage	VAIN0SN	ADCAnIm	T&H not used		AnVSS		AnVREF	V
		ADCA0I0-5	T&H used		0.2		A0VREF – 0.2	V
		ADCA0ImS	A0VREF ≥ EVCC		A0VSS		EVCC	V
			A0VREF < EVCC		A0VSS		A0VREF	V
		ADCA1ImS	A1VREF ≥ BVCC		A1VSS		BVCC	V
			A1VREF < BVCC		A1VSS		A1VREF	V
Operation current	IA0VREF IA1VREF	T&H not used				1.1	3.0	mA
		T&H used (max. 6 pins)					*2	mA
STOP, DeepSTOP, Cyclic STOP current (@LPS is stopped)	IA0VREFS IA1VREFS					1	10	µA
T&H current	ITH					0.5	1.3	mA/ch
T&H sampling time	t_{THSMP}				450			ns
T&H hold time	t_{THHOLD}						10	µs
Set up time of self diagnosis voltage circuit	t_{BOOT}				500			ns
Set up time of self diagnosis voltage level	t_{OUT}				500			ns
Pull-down resistor for diagnosis of open pins		ADCnIm pins	VI = AnVREF		350	500	650	kΩ
		ADCnImS pins	A0VREF ≥ EVCC: VI = EVCC A0VREF < EVCC: VI = A0VREF		100	215	800	kΩ
			A1VREF ≥ BVCC: VI = BVCC A1VREF < BVCC: VI = A1VREF					

(2/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Accuracy of self-diagnosis function (except diagnosis of open pins)	TESH0SN	12-bit mode	Self-diagnosis voltage level = AnVREF		4015-|TOEn|		4095	—
			Self-diagnosis voltage level = 2/3AnVREF		2651-|TOEn|	2731	2811+|TOEn|	—
			Self-diagnosis voltage level = 1/2AnVREF		1968-|TOEn|	2048	2128+|TOEn|	—
			Self-diagnosis voltage level = 1/3AnVREF		1285-|TOEn|	1365	1445+|TOEn|	—
			Self-diagnosis voltage level = AnVSS		0		80+|TOEn|	—
		10-bit mode	Self-diagnosis voltage level = AnVREF		1003-|TOEn|		1023	—
			Self-diagnosis voltage level = 2/3AnVREF		663-|TOEn|	683	703+|TOEn|	—
			Self-diagnosis voltage level = 1/2AnVREF		492-|TOEn|	512	532+|TOEn|	—
			Self-diagnosis voltage level = 1/3AnVREF		321-|TOEn|	341	361+|TOEn|	—
			Self-diagnosis voltage level = AnVSS		0		20+|TOEn|	—
Integral nonlinearity error*1	ILEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±2.0	LSB
				ADCA0I0-5 (T&H used)			±3.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±3.0	LSB
				ADCA0I0-5 (T&H used)			±4.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB
Differential nonlinearity error*1	DLEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±1.0	LSB
				ADCA0I0-5 (T&H used)			±2.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±3.0	LSB
				ADCA0I0-5 (T&H used)			±4.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.0V to 4.5V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
Zero scale error (offset error)*1	ZSEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±3.5	LSB
				ADCA0I0-5 (T&H used)			±5.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±5.5	LSB
				ADCA0I0-5 (T&H used)			±7.5	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±0.5	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
Full scale error*1	FSEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±3.5	LSB
				ADCA0I0-5 (T&H used)			±5.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±5.5	LSB
				ADCA0I0-5 (T&H used)			±7.5	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±0.5	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB

Note: Conversion accuracy when ADCA0ImS terminal is converted in 12-bit mode: Conversion accuracy can be applied if lower 2-bit is ignored from conversion result.

Note 1. This does not include quantization error.

Note 2. 3.0 + 1.3 × (the number of used T&H)

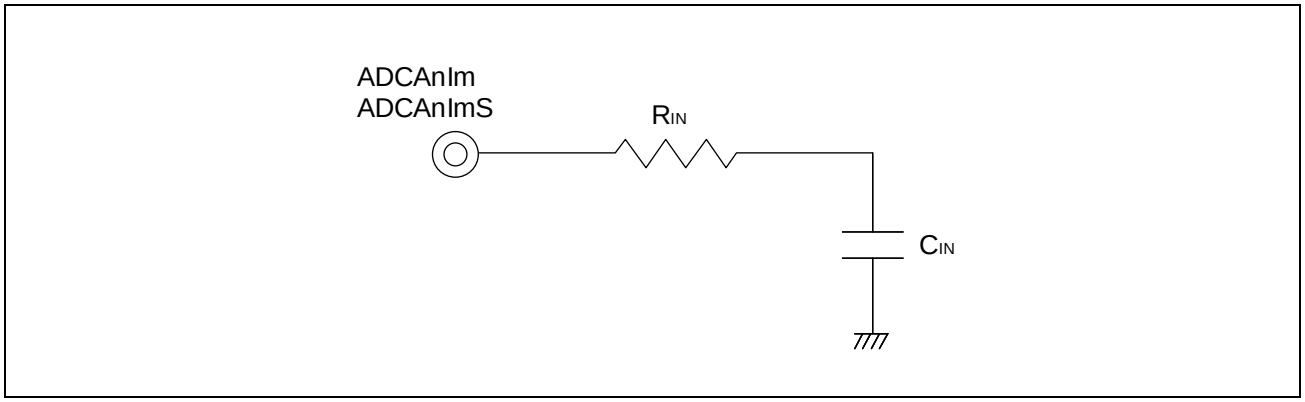
Note 3. Include the oscillation accuracy of HS IntOSC.

Note 4. When the external multiplexer is used, the detailed time of A/D conversion is MPX setup time, sampling time and successive approximation time. MPX setup time is same as “sampling time + successive approximation time”.

CAUTION

When an external digital pulse is applied to AP0, AP1, P8, P9, P18, and P19 pins during an A/D conversion this may lead to an A/D conversion result with a larger conversion error as expected due to the coupling noise of the external digital pulse.
The same behavior may apply when the digital buffer is used as an output pin. For the output port the potential degradation increases with the driven total output current of the port. In addition the conversion resolution may drop if the output current fluctuates at adjacent pins due to the coupling effect of the external circuit connected to these port pins.

3A.6.1 Equivalent Circuit of the Analog Input Block



Terminals	Condition	RIN (kΩ)	CIN (pF)
ADCA0I0 to 5	When T&H is used	14.1	2.1
	When T&H is not used	3.9	2.1
ADCA0I6 to 15	—	3.9	2.1
ADCA0I0S to 3S, 5S to 11S, 14S to 16S	—	5.7	9.2
ADCA0I4S, 17S to 19S	—	10.3	9.2
ADCA1I0 to 15	—	4	2.1
ADCA1I0S to 19S	—	5.5	7.9

CAUTION

This specification is not tested during outgoing inspection. Therefore RIN and CIN are reference values only and not guaranteed. In addition these values are specified as maximum values.

3A.7 Flash Programming Characteristics

3A.7.1 Code Flash

The code flash memory is shipped in the erased state. If the code flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: REG0VCC = EVCC = VPOC to 5.5 V, REG1VCC = VPOC to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = VPOC to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

Table 3A.21 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3		5*4		30	MHz
Number of rewrites*1	CWRT	Data retention of 20 years*2	1000			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 1000), the device can be erased “n” times for each block. For example, when a block of 32 KB is erased after 256 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Note 3. f_{PCLK} = 1/8 f_{CPUCLK_H}: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 3A.22 Programming Characteristic

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz CWRT < 100 times	256 B		0.4*1	6*1	ms
			8 KB		20	90	ms
			32 KB		80	360	ms
			256 KB		0.6	2.7	s
			384 KB		0.9	4.1	s
			512 KB		1.2	5.4	s
			768 KB		1.7	8.1	s
			1 MB		2.3	10.8	s
			1.5 MB		3.4	16.2	s
			2 MB		4.5	21.5	s
			3 MB		6.8	32.3	s
			4 MB		9	43	s
			6 MB		13.5	64.5	s
			8 MB		18	85.9	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	256 B		0.5*1	7.2*1	ms
			8 KB		24	108	ms
			32 KB		96	432	ms
			256 KB		0.7	3.3	s
			384 KB		1.1	4.9	s
			512 KB		1.4	6.5	s
			768 KB		2.1	9.8	s
			1 MB		2.7	13	s
			1.5 MB		4.1	19.5	s
			2 MB		5.4	26	s
			3 MB		8.1	39	s
			4 MB		10.8	52	s
			6 MB		16.2	78	s
			8 MB		21.6	104	s

Table 3A.22 Programming Characteristic

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Erase time		f_{PCLK} ≥ 20 MHz CWRT < 100 times	8 KB		39	120	ms
			32 KB		141	480	ms
			256 KB		1.2	3.5	s
			384 KB		1.7	5.3	s
			512 KB		2.3	7	s
			768 KB		3.4	10.5	s
			1 MB		4.5	14	s
			1.5 MB		6.8	21	s
			2 MB		9	28	s
			3 MB		13.5	42	s
			4 MB		18	56	s
			6 MB		27	84	s
			8 MB		36	112	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	8 KB		47	144	ms
			32 KB		169	576	ms
			256 KB		1.4	4.2	s
			384 KB		2.1	6.3	s
			512 KB		2.7	8.4	s
			768 KB		4.1	12.6	s
			1 MB		5.4	16.8	s
			1.5 MB		8.1	25.2	s
			2 MB		10.8	33.6	s
			3 MB		16.2	50.4	s
			4 MB		21.6	67.2	s
			6 MB		32.4	100.8	s
			8 MB		43.2	134.4	s

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

3A.7.2 Data Flash

The data flash memory is shipped in the erased state. If the data flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: REG0VCC = EVCC = VPOC to 5.5 V, REG1VCC = VPOC to 3.6 V, REG1VCC ≤ REG0VCC,
BVCC = VPOC to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C,
CL = 30 pF

Table 3A.23 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3		5*4		30	MHz
Number of rewrites*1	CWRT	Data retention 20 years*2	125 k			times
		Data retention 3 years*2	250 k			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 125000), the device can be erased “n” times for each block. For example, when a block of 64 bytes is erased after 4 bytes of writing have been performed for different addresses 16 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the data flash memory.

Note 3. f_{PCLK} = 1/8 f_{CPUCLK_H}: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 3A.24 Programming Characteristics

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz	4 B		0.16*1	1.7*1	ms
			32 KB		1.4	6.8	s
			64 KB		2.79	13.44	s
			128 KB		5.58	26.88	s
			256 KB		11.16	53.74	s
Erase time		f_{PCLK} ≥ 20 MHz	64 B		1.7*1	10*1	ms
			32 KB		0.9	5.2	s
			64 KB		1.74	10.24	s
			128 KB		3.48	20.48	s
			256 KB		6.95	40.94	s
Blank check time		f_{PCLK} ≥ 20 MHz	4 B			30*1	µs
			64 B			100*1	µs
			32 KB			35.2	ms
			64 KB			70.4	ms
			128 KB			140.8	ms
			256 KB			281.6	ms

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

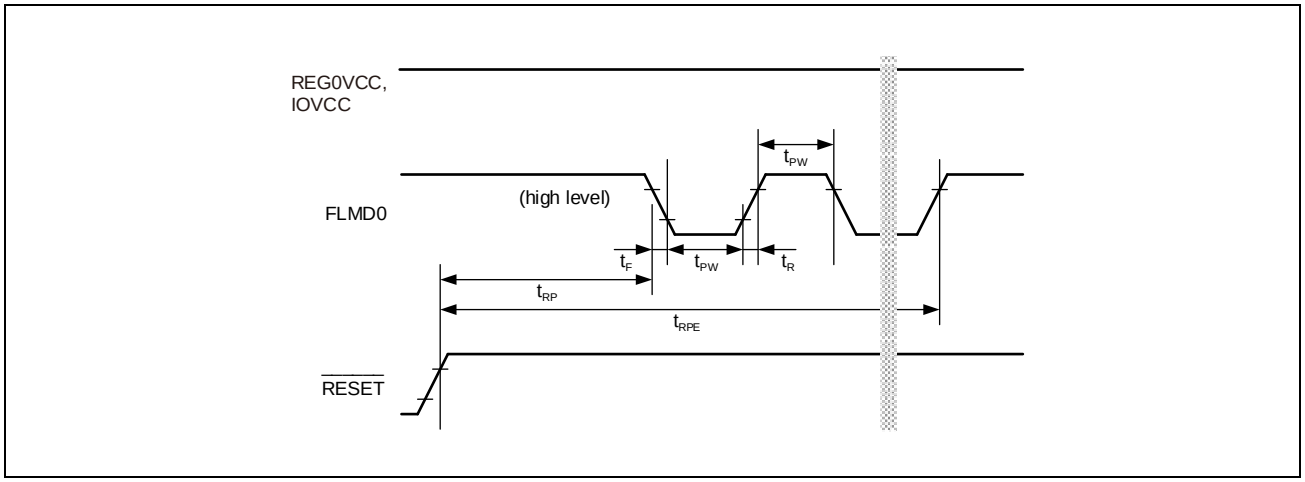
3A.7.3 Serial Programming Interface

3A.7.3.1 Serial Programmer Setup Timing

Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0 pulse input start time	t_{RP}		1.5			ms
FLMD0 pulse input end time	t_{RPE}				101.5	ms
FLMD0 low/high level width	t_{PW}		3.2			µs
FLMD0 rise time	t_R				20	ns
FLMD0 fall time	t_F				20	ns

Note: IOVCC: EVCC = BVCC = A0VREF = A1VREF



3A.7.3.2 Flash Programming Interface

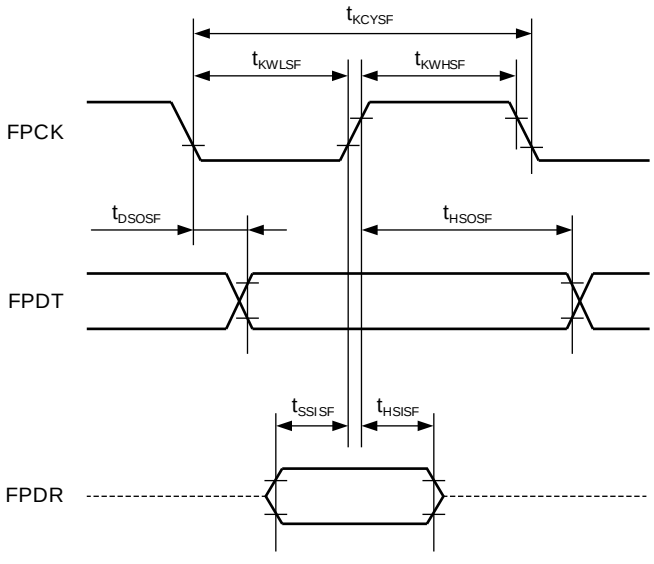
Condition: REG0VCC = EVCC = 3.0 V to 5.5 V, REG1VCC = 3.0 V to 3.6 V, REG1VCC ≤ REG0VCC, BVCC = 3.0 V to REG0VCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Flash Programming transfer rate		1-wired UART mode			1	Mbps
		2-wired UART mode (Products of CPU frequency 240 MHz max.)			1.5	Mbps
		2-wired UART mode (Products of CPU frequency 160 MHz max.)			1	Mbps
FPCK cycle time	t_{KCYSF}	3-wired clock sync mode	200*[1]			ns
FPCK high level width	t_{KWHSF}	3-wired clock sync mode	t_{KCYSF} / 2 – 15			ns
FPCK low level width	t_{KWLSF}	3-wired clock sync mode	t_{KCYSF} / 2 – 15			ns
FPDR setup time (vs. FPCK)	t_{SSISF}	3-wired clock sync mode	t_{Pcyc} × 2			ns
FPDR hold time (vs. FPCK)	t_{HSISF}	3-wired clock sync mode	t_{Pcyc} × 2			ns
FPDT output delay (vs. FPCK)	t_{DSOSF}	3-wired clock sync mode Not continuous transfer (data: 1st bit)			0	ns
		3-wired clock sync mode Not continuous transfer (data: except 1st bit)			$–t_{KWHSF}$ + 3 × t_{Pcyc} + 36	ns
FPDT hold time (vs. FPCK)	t_{HSOSF}	3-wired clock sync mode	t_{Pcyc} × 2			ns

Note 1. Input an external clock that is more than 6 clocks of PCLK.

NOTE

t_{Pcyc} is period of PCLK.



3A.8 Thermal Characteristics

3A.8.1 Parameters

Package	Item	Symbol	Estimate	Unit	Note
324-pin FPBGA	Thermal Resistance	Θja	17.4	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	9.8		
233-pin FPBGA	Thermal Resistance	Θja	17.9	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	9.9		
176-pin LQFP	Thermal Resistance	Θja	31.9	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	23.8		

NOTE

The thermal resistance and characterization parameters depend on the usage environment.

3A.8.2 Board

Conforming to JESD51-7 (4 layers)

	Board Size (mm)		
	X	Y	Area (mm^2)
Board	76.2	114.3	8709.66
Remaining copper rates	Thickness of conductors		
50-95-95-50%	70-35-35-70 µm		

Section 3B Electrical Characteristics of RH850/F1KM-S4, RH850/F1KM-S2

3B.1 Overview

The electrical spec of this device is guaranteed by the following operational condition. But, this condition is different depends on each characteristics, so refer to each chapter for more detail.

3B.1.1 Pin Groups

3B.1.1.1 272-Pin Version (RH850/F1KM-S4)

Symbol	Pin Group Supplied by	Related Pins/Ports
PgR	REGVCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
PgE	EVCC, EVSS	Related ports: JP0, P0, P1, P2, P3, P8, P9, P20 Related pins: $\overline{\text{RESET}}$, FLMD0
PgB	BVCC, BVSS	Related ports: P10, P11, P12, P13, P18, P19, P21, P22
PgA0	A0VREF, A0VSS	Related port: AP0
PgA1	A1VREF, A1VSS	Related port: AP1

3B.1.1.2 233-Pin Version (RH850/F1KM-S4)

Symbol	Pin Group Supplied by	Related Pins/Ports
PgR	REGVCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
PgE	EVCC, EVSS	Related ports: JP0, P0, P1, P2, P3, P8, P9, P20 Related pins: $\overline{\text{RESET}}$, FLMD0
PgB	BVCC, BVSS	Related ports: P10, P11, P12, P13, P18, P19
PgA0	A0VREF, A0VSS	Related port: AP0
PgA1	A1VREF, A1VSS	Related port: AP1

3B.1.1.3 176-Pin Version (RH850/F1KM-S4, RH850/F1KM-S2)

Symbol	Pin Group Supplied by	Related Pins/Ports
PgR	REGVCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
PgE	EVCC, EVSS	Related ports: JP0, P0, P1, P2, P8, P9, P20 Related pins: $\overline{\text{RESET}}$, FLMD0
PgB	BVCC, BVSS	Related ports: P10, P11, P12, P18
PgA0	A0VREF, A0VSS	Related port: AP0
PgA1	A1VREF, A1VSS	Related port: AP1

3B.1.1.4 144-Pin Version (RH850/F1KM-S4, RH850/F1KM-S2)

Symbol	Pin Group Supplied by	Related Pins/Ports
PgR	REGVCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
PgE	EVCC, EVSS	Related ports: JP0, P0, P1, P8, P9, P20 Related pins: $\overline{\text{RESET}}$, FLMD0
PgB	BVCC, BVSS	Related ports: P10, P11, P12, P18
PgA0	A0VREF, A0VSS	Related port: AP0
PgA1	A1VREF, A1VSS	Related port: AP1

3B.1.1.5 100-Pin Version (RH850/F1KM-S4, RH850/F1KM-S2)

Symbol	Pin Group Supplied by	Related Pins/Ports
PgR	REGVCC, AWOVSS	X1, X2
PgE	EVCC, EVSS	Related ports: JP0, P0, P8, P9, P10, P11 Related pins: $\overline{\text{RESET}}$, FLMD0
PgA0	A0VREF, A0VSS	Related port: AP0

3B.1.2 General Measurement Conditions

3B.1.2.1 Common Conditions

- Power supply
  - REGVCC = EVCC = VPOC*[1] to 5.5 V
  - BVCC = VPOC*[1] to REGVCC
  - A0VREF = 3.0 V to 5.5 V
  - A1VREF = 3.0 V to 5.5 V
  - AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V
- Capacitance of the internal regulator
  - CAWOVCL: 0.1 µF ±30%
  - CISOVCL: 0.1 µF ±30% per pin
- Operating temperature
  - Tj = –40 to +130°C@R7F7016xx3ABG*[2]
  - Tj = –40 to +150°C@R7F7016xx4ABG*[2]
    @R7F7016yy3AFP*[2]
    @R7F7017zz3AFP*[2]

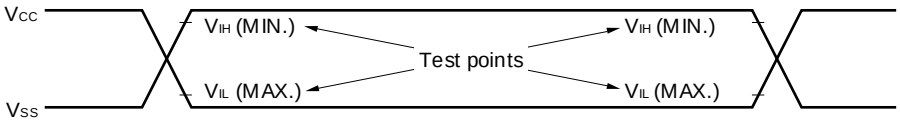
  xx = 50, 51, 52, 53
  yy = 44, 45, 46, 47, 48, 49
  zz = 60, 62, 64
- Load conditions
  - CL = 30 pF

Note 1. “VPOC” means POC (power-on clear) detection voltage. For more detail, see **Section 3B.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.

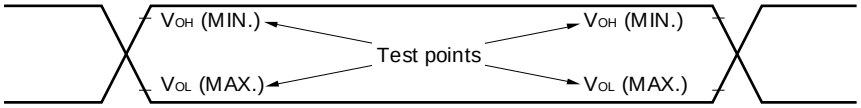
Note 2. Regarding operation temperature of each product, see **Section 1B.3, RH850/F1KM Product Lineup**.

3B.1.2.2 AC Characteristic Measurement Condition

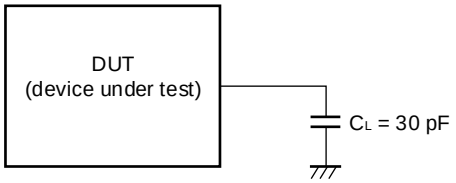
(1) AC Test Input Measurement Points



(2) AC Test Output Measurement Points



(3) Load Conditions



CAUTION

If the load capacitance exceeds 30pF due to the circuit configuration, it is recommended to insert a buffer in order to reduce capacitance to less than 30pF.

3B.2 Absolute Maximum Ratings

CAUTIONS

1. Do not directly connect outputs (or input/outputs) to each other, power supply and ground.
2. Even momentarily exceeding the absolute maximum rating for just one item creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings. The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.
3. When designing an external circuit ensure that the connections don't conflict with the port state of this device.

3B.2.1 Supply Voltages

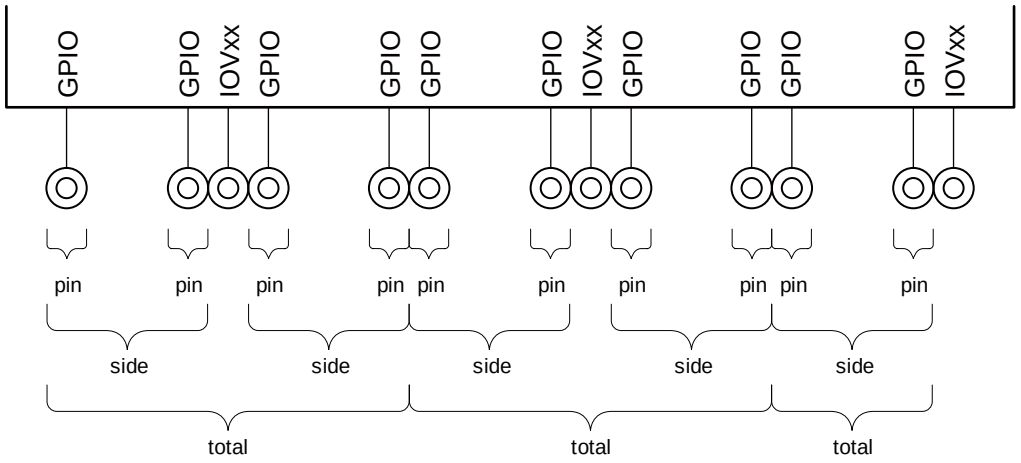
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System supply voltage	REGVCC		–0.5		6.5	V
	AWOVSS		–0.5		0.5	V
	ISOVSS		–0.5		0.5	V
Port supply voltage	EVCC		–0.5		6.5	V
	BVCC		–0.5		6.5	V
	EVSS		–0.5		0.5	V
	BVSS		–0.5		0.5	V
A/D-converter supply voltage	A0VREF		–0.5		6.5	V
	A1VREF		–0.5		6.5	V
	A0VSS		–0.5		0.5	V
	A1VSS		–0.5		0.5	V

3B.2.2 Port Voltages

Item	Pin Group*1	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	PgR	VI		–0.5		REGVCC + 0.5 (Do not exceed 6.5 V)	V
	PgE			–0.5		EVCC + 0.5 (Do not exceed 6.5 V)	V
	PgB			–0.5		BVCC + 0.5 (Do not exceed 6.5 V)	V
	PgA0			–0.5		A0VREF + 0.5 (Do not exceed 6.5 V)	V
	PgA1			–0.5		A1VREF + 0.5 (Do not exceed 6.5 V)	V

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

3B.2.3 Port Current



Definition of the condition:

- Per pin: Output current of one GPIO
- Per side: Total output current of all GPIO pins on one side of one IOVxx
- Total: Total output current of both sides of one IOVxx

Note:

- GPIO: General-purpose I/O pin (JP0, P0, P1, P2, P3, P8, P9, P10, P11, P12, P13, P18, P19, P20, P21, P22, AP0, AP1)
- IOVxx: Power supply pin for I/O pins (EVCC/EVSS, BVCC/BVSS, A0VREF/A0VSS, A1VREF/A1VSS)

3B.2.3.1 272-Pin Version (RH850/F1KM-S4)

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (total of P9_0 to P9_4, P20_10 to P20_14)			–48	mA
			Per side (total of P20_0 to P20_9)			–48	mA
			Per side (total of P0_0 to P0_3)			–40	mA
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12)			–48	mA
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0)			–48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P1_4,P1_5, P1_14, P1_15, P2_2 to P2_5, P8_0, P8_1, P8_3 to P8_9)			–48	mA
			Per side (total of P3_1 to P3_10)			–48	mA
			Total (EVCC)			–60	mA
		PgB	Per pin			–10	mA
			Per side (total of P18_0 to P18_7)			–48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)			–48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1)			–48	mA
			Per side (total of P10_0 to P10_2)			–30	mA
			Per side (total of P10_3 to P10_5)			–30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7)			–48	mA
			Per side (total of P21_0, P21_2 to P21_4, P22_0 to P22_2)			–48	mA
			Per side (total of P22_3 to P22_8)			–48	mA
			Per side (total of P21_1, P22_9 to P22_15)			–48	mA
			Total (BVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
		PgA1	Per pin			–10	mA
			Total (A1VREF)			–48	mA

(272-pin version)

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0 to P9_4, P20_10 to P20_14)			48	mA
			Per side (total of P20_0 to P20_9)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12)			48	mA
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0, P8_2, P8_10 to P8_12)			48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P2_2, P2_3)			48	mA
			Per side (total of P1_4, P1_5, P1_14, P1_15, P2_4, P2_5, P8_0, P8_1, P8_3 to P8_9)			48	mA
			Per side (total of P3_1 to P3_10)			48	mA
			Total (EVCC)			60	mA
		PgB	Per pin			10	mA
			Per side (total of P18_0 to P18_7)			48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)			48	mA
			Per side (total of P10_6 to P10_14, P11_1, P11_2)			48	mA
			Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1)			48	mA
			Per side (total of P10_0 to P10_2)			30	mA
			Per side (total of P10_3 to P10_5)			30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7)			48	mA
			Per side (total of P21_0, P21_2 to P21_4, P22_0 to P22_6)			48	mA
			Per side (total of P21_1, P22_7 to P22_15)			48	mA
			Total (BVCC)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VREF)			48	mA
		PgA1	Per pin			10	mA
			Total (A1VREF)			48	mA

3B.2.3.2 233-Pin Version (RH850/F1KM-S4)

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			–48	mA
			Per side (total of P0_0 to P0_3)			–40	mA
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12)			–48	mA
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0)			–48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P1_4, P1_5, P1_14, P1_15, P2_2 to P2_5, P8_0, P8_1, P8_3 to P8_9)			–48	mA
			Total (EVCC)			–60	mA
		PgB	Per pin			–10	mA
			Per side (total of P18_0 to P18_7)			–48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)			–48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1)			–48	mA
			Per side (total of P10_0 to P10_2)			–30	mA
			Per side (total of P10_3 to P10_5)			–30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7)			–48	mA
			Total (BVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
		PgA1	Per pin			–10	mA
			Total (A1VREF)			–48	mA

(233-pin version)

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12)			48	mA
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0, P8_2, P8_10 to P8_12)			48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P2_2, P2_3)			48	mA
			Per side (total of P1_4, P1_5, P1_14, P1_15, P2_4, P2_5, P8_0, P8_1, P8_3 to P8_9)			48	mA
			Total (EVCC)			60	mA
		PgB	Per pin			10	mA
			Per side (total of P18_0 to P18_7)			48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)			48	mA
			Per side (total of P10_6 to P10_14, P11_1, P11_2)			48	mA
			Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1)			48	mA
			Per side (total of P10_0 to P10_2)			30	mA
			Per side (total of P10_3 to P10_5)			30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7)			48	mA
			Total (BVCC)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VREF)			48	mA
		PgA1	Per pin			10	mA
			Total (A1VREF)			48	mA

3B.2.3.3 176-Pin Version (RH850/F1KM-S4, RH850/F1KM-S2)

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			–48	mA
			Per side (total of P0_0 to P0_3)			–40	mA
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6, P8_2, P8_10 to P8_12)			–48	mA
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11, P2_0, P2_1)			–48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P1_4, P1_5, P1_14, P1_15, P2_2 to P2_5, P8_0, P8_1, P8_3 to P8_9)			–48	mA
			Total (EVCC)			–60	mA
		PgB	Per pin			–10	mA
			Per side (total of P10_6 to P10_9, P18_0 to P18_7)			–48	mA
			Per side (total of P10_10 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2)			–48	mA
			Per side (total of P10_0 to P10_2)			–30	mA
			Per side (total of P10_3 to P10_5)			–30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5)			–48	mA
			Total (BVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
		PgA1	Per pin			–10	mA
			Total (A1VREF)			–48	mA
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6)			48	mA
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P2_0, P2_1, P8_2, P8_10 to P8_12)			48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P2_2, P2_3)			48	mA
			Per side (total of P1_4, P1_5, P1_14, P1_15, P2_4, P2_5, P8_0, P8_1, P8_3 to P8_9)			48	mA
			Total (EVSS)			60	mA
		PgB	Per pin			10	mA
			Per side (total of P18_0 to P18_7)			48	mA
			Per side (total of P10_6 to P10_14, P11_1, P11_2)			48	mA
			Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2)			48	mA
			Per side (total of P10_0 to P10_2)			30	mA
			Per side (total of P10_3 to P10_5)			30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5)			48	mA
			Total (BVSS)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA
		PgA1	Per pin			10	mA
			Total (A1VSS)			48	mA

3B.2.3.4 144-Pin Version (RH850/F1KM-S4, RH850/F1KM-S2)

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (total of P9_0 to P9_4, P20_4, P20_5)			–48	mA
			Per side (total of P0_0 to P0_3)			–40	mA
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P8_2, P8_10 to P8_12)			–48	mA
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11)			–48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P1_4, P1_5, P8_0, P8_1, P8_3 to P8_9)			–48	mA
			Total (EVCC)			–60	mA
		PgB	Per pin			–10	mA
			Per side (total of P10_6 to P10_9, P18_0 to P18_3)			–48	mA
			Per side (total of P10_10 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2)			–48	mA
			Per side (total of P10_0 to P10_5, P10_15, P11_0, P11_8 to P11_12)			–48	mA
			Total (BVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
		PgA1	Per pin			–10	mA
			Total (A1VREF)			–48	mA
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0 to P9_4, P20_4, P20_5)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3)			48	mA
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P8_2, P8_10 to P8_12)			48	mA
			Per side (total of JP0_6, P0_7 to P0_10)			48	mA
			Per side (total of P1_4, P1_5, P8_0, P8_1, P8_3 to P8_9)			48	mA
			Total (EVSS)			60	mA
		PgB	Per pin			10	mA
			Per side (total of P18_0 to P18_3)			48	mA
			Per side (total of P10_6 to P10_14, P11_1, P11_2)			48	mA
			Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2)			48	mA
			Per side (total of P10_0 to P10_5, P10_15, P11_0, P11_8 to P11_12)			48	mA
			Total (BVSS)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA
		PgA1	Per pin			10	mA
			Total (A1VSS)			48	mA

3B.2.3.5 100-Pin Version (RH850/F1KM-S4, RH850/F1KM-S2)

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (Total of P9_0 to P9_4)			–48	mA
			Per side (Total of P0_0 to P0_3, P10_3 to P10_5)			–48	mA
			Per side (Total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P8_2, P8_10 to P8_12)			–48	mA
			Per side (Total of JP0_0 to JP0_2)			–30	mA
			Per side (Total of P0_7 to P0_10, P8_3 to P8_9)			–48	mA
			Per side (Total of P10_6 to P10_9)			–40	mA
			Per side(Total of P10_10 to P10_14, P11_1 to P11_7)			–48	mA
			Per side (Total of P10_0 to P10_2)			–30	mA
			Total (EVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (Total of P9_0 to P9_4)			48	mA
			Per side (Total of P0_0 to P0_6, P0_11 to P0_14, P10_3 to P10_5)			48	mA
			Per side (Total of JP0_0 to JP0_5, P8_2, P8_10 to P8_12)			48	mA
			Per side (Total of P0_7 to P0_10)			40	mA
			Per side (Total of P8_3 to P8_9)			48	mA
			Per side(Total of P10_6 to P10_14, P11_1, P11_2)			48	mA
			Per side (Total of P11_3 to P11_7)			48	mA
			Per side (Total of P10_0 to P10_2)			30	mA
			Total (EVCC)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA

3B.2.4 Temperature Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Storage temperature	Tstg		–55		150	°C
Junction temperature	Tj	R7F7016xx3ABG	–40		130	°C
		R7F7016xx4ABG R7F7016yy3AFP R7F7017zz3AFP	–40		150	°C

Note: xx = 50, 51, 52, 53
yy = 44, 45, 46, 47, 48, 49
zz = 60, 62, 64

Regarding operation temperature of each product, see **Section 1B.3, RH850/F1KM Product Lineup**.

3B.3 Operational Condition

3B.3.1 Recommended Operating Conditions

Products of CPU frequency 240 MHz max.

(1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f_{CPUCLK_H}	CKDIVMD = 1			240	MHz
		CKDIVMD = 0			120	MHz
	f_{CPUCLK_M}				120	MHz
	f_{CPUCLK_L}	for OSTMn			60	MHz
		for MEMC*5				
	f_{CPUCLK_UL}				30	MHz
Peripheral clock (clock domain) frequency*1	f_{CKSCLK_AWDTA}	for WDTA0			240*2	kHz
	f_{CKSCLK_ATAUJ}	for TAUJ0			40	MHz
		for TAUJ2				
	f_{CKSCLK_ARTCA}	for RTCA0			4	MHz
	f_{CKSCLK_AADCA}	for ADCA0			40	MHz
	f_{CKSCLK_AFOUT}	for FOUT			24	MHz
	$f_{CKSCLK\_ICPUCLK}$	for CPU subsystem			240 / 120	MHz
	f_{CKSCLK_IPERI1}	for TAUD0			80	MHz
		for TAUJ1				
		for TAUJ3				
		for ENCA0				
		for TAPA0				
		for PIC0				
		for SFMA0				
	f_{CKSCLK_IPERI2}	for TAUBn			40	MHz
		for RCFDCn (clkc)				
		for RSENTn				
		for PWBAn				
		for PWGAn				
		for PWSAn				
	f_{CKSCLK_ILIN}	for RLIN24n			40	MHz
		for RLIN3n				
	f_{CKSCLK_IADCA}	for ADCA1			40	MHz
	f_{CKSCLK_ICAN}	for RCFDCn (PCLK)			80	MHz
	$f_{CKSCLK\_ICANOSC}$	for RCFDCn (clk_xincan)			24	MHz
	f_{CKSCLK_ICSI}	for CSIGn			80	MHz
		for CSIHn				
	f_{CKSCLK_IIIC}	for RIICn			40	MHz
	$f_{LS\ IntOSC}$	for WDTA1			240*2	kHz
	f_{EMCLK}	for LPSn			8	MHz

(2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply	REGVCC	REGVCC = EVCC	VPOC*3		5.5	V
	EVCC					
	BVCC		VPOC*3		REGVCC	V
	A0VREF		3.0		5.5	V
	A1VREF					
Normal operation voltage	AWOVCL		1.1	1.25	1.35	V
	ISOVCL					
Limited operation voltage*4	AWOVCL		1.35		1.43	V
	ISOVCL					

Note 1. For clock specification of peripherals, see **Section 12AB, Clock Controller of RH850/F1KH-D8, RH850/F1KM-S4, RH850/F1KM-S2** of the ***RH850/F1KH, RH850/F1KM User's Manual: Hardware***.

Note 2. This frequency depends on the internal oscillator (LS IntOSC).

Note 3. "VPOC" means POC (power-on clear) detection voltage (TYP. 2.85 V). For detail, see **Section 3B.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.
In addition, the guaranteed operation in DC characteristic.
And AC characteristic is guaranteed when more than 3.0 V.
When the power supply voltage is VPOC to 3.0 V, the device does not malfunction.

Note 4. Reliability restrictions from 1.35 V to 1.43 V.

Note 5. Devided by 2 on MEMC internal.

Products of CPU frequency 160 MHz max.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f_{CPUCLK_H}				160	MHz
	f_{CPUCLK_M}				80	MHz
	f_{CPUCLK_L}	for OSTMn			40	MHz
		for MEMC*5				
	f_{CPUCLK_UL}				20	MHz
Peripheral clock (clock domain) frequency*1	f_{CKSCLK_AWDTA}	for WDTA0			240*2	kHz
	f_{CKSCLK_ATAUJ}	for TAUJ0			40	MHz
		for TAUJ2				
	f_{CKSCLK_ARTCA}	for RTCA0			4	MHz
	f_{CKSCLK_AADCA}	for ADCA0			40	MHz
	f_{CKSCLK_AFOUT}	for FOUT			24	MHz
	$f_{CKSCLK\_ICPUCLK}$	for CPU subsystem			160	MHz
	f_{CKSCLK_IPERI1}	for TAUD0			80	MHz
		for TAUJ1				
		for TAUJ3				
		for ENCA0				
		for TAPA0				
		for PIC0				
		for SFMA0				
	f_{CKSCLK_IPERI2}	for TAUBn			40	MHz
		for RCFDCn (clkc)				
		for RSENTn				
		for PWBAn				
		for PWGAn				
		for PWSAn				
	f_{CKSCLK_ILIN}	for RLIN24n			40	MHz
		for RLIN3n				
	f_{CKSCLK_IADCA}	for ADCA1			40	MHz
	f_{CKSCLK_ICAN}	for RCFDCn (pclk)			80	MHz
	$f_{CKSCLK\_ICANOSC}$	for RCFDCn (clk_xincan)			24	MHz
	f_{CKSCLK_ICSI}	for CSIGn			80	MHz
		for CSIHn				
	f_{CKSCLK_IIIC}	for RIICn			40	MHz
	$f_{LS\ IntOSC}$	for WDTA1			240*2	kHz
	f_{EMCLK}	for LPSn			8	MHz
Power supply	REGVCC	REGVCC = EVCC	VPOC*3		5.5	V
	EVCC					
	BVCC		VPOC*3		REGVCC	V
	A0VREF		3.0		5.5	V
	A1VREF					
Normal operation voltage	AWOVCL		1.1	1.25	1.35	V
	ISOVCL					
Limited operation voltage*4	AWOVCL		1.35		1.43	V

Note 1. For clock specification of peripherals, see **Section 12AB, Clock Controller of RH850/F1KH-D8, RH850/F1KM-S4, RH850/F1KM-S2** of the ***RH850/F1KH, RH850/F1KM User's Manual: Hardware***.

Note 2. This frequency depends on the internal oscillator (LS IntOSC).

Note 3. "VPOC" means POC (power-on clear) detection voltage (TYP. 2.85 V). For detail, see **Section 3B.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.
In addition, the guaranteed operation in DC characteristic.
And AC characteristic is guaranteed when more than 3.0 V.
When the power supply voltage is VPOC to 3.0 V, the device does not malfunction.

Note 4. Reliability restrictions from 1.35 V to 1.43 V.

Note 5. Devided by 2 on MEMC internal.

3B.3.2 Oscillator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C

(1) MainOSC (In Case of Using a Crystal/Ceramic)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MainOSC frequency*3	f_{MOSC}		8		24	MHz
MainOSC current consumption	I_{MOSC}	After stabilization		1.9*2	2.3*2	mA
MainOSC oscillation start point	V_{MOSCSP}		VPOC			V
MainOSC oscillation operating point	V_{MOSCOP}			0.5 × REGVCC*2		V
MainOSC oscillation amplitude	$V_{MOSCAMP}$		0.4 × REGVCC – 0.2*2			V
MainOSC oscillation stabilization time	t_{MSTB}			2*1,*2		ms
MainOSC transconductance	g_{m_MOSC}	MOSCS.MOSCCLKACT = 0, MOSCC.MOSCAMPSEL[1:0] = 00		11.1*2		mA/V
		MOSCS.MOSCCLKACT = 0, MOSCC.MOSCAMPSEL[1:0] = 01		10.6*2		mA/V
		MOSCS.MOSCCLKACT = 0, MOSCC.MOSCAMPSEL[1:0] = 10		9.3*2		mA/V
		MOSCS.MOSCCLKACT = 0, MOSCC.MOSCAMPSEL[1:0] = 11		7.8*2		mA/V
		MOSCS.MOSCCLKACT = 1, MOSCC.MOSCAMPSEL[1:0] = 00		8.6*2		mA/V
		MOSCS.MOSCCLKACT = 1, MOSCC.MOSCAMPSEL[1:0] = 01		7.8*2		mA/V
		MOSCS.MOSCCLKACT = 1, MOSCC.MOSCAMPSEL[1:0] = 10		6.1*2		mA/V
		MOSCS.MOSCCLKACT = 1, MOSCC.MOSCAMPSEL[1:0] = 11		4.0*2		mA/V

Note 1. Oscillator stabilization time is time until being set (“1”) in MOSCS.MOSCCLKACT bit after MOSCE.MOSCENTRG bit is written “1”, and depends on the setting value of MOSCST register. Please decide appropriate oscillation stabilization time by matching test with resonator and oscillation circuit.

Note 2. This is reference value.

Note 3. The following four crystal/ceramic resonator frequencies are supported: 8 MHz, 16 MHz, 20 MHz and 24 MHz.

(2) MainOSC (In Case of External Clock Input to X1)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
X1 clock Input frequency*1	f_{EX}		8		24	MHz
X1 clock Input cycle time	t_{EXCYC}		41.7		125	ns
X1 High level Input voltage	V_{IH}		0.7 × REGVCC		REGVCC + 0.5	V
		@Flash Programing Interface*2	0.8 × REGVCC		REGVCC + 0.5	V
X1 Low level Input voltage	V_{IL}		–0.5		0.3 × REGVCC	V
		@Flash Programing Interface*2	–0.5		0.2 × REGVCC	V
X1 Input leakage current	I_{LIH}	VI = REGVCC			0.5	µA
	I_{LIL}	VI = 0 V			–0.5	µA
X1 clock Input low-level pulse width	t_{EXL}	f_{EX} = 8 MHz	58			ns
		f_{EX} = 16 MHz	26			ns
		f_{EX} = 20 MHz	20			ns
		f_{EX} = 24 MHz	16			ns
X1 clock Input high-level pulse width	t_{EXH}	f_{EX} = 8 MHz	58			ns
		f_{EX} = 16 MHz	26			ns
		f_{EX} = 20 MHz	20			ns
		f_{EX} = 24 MHz	16			ns
X1 clock Input period jitter			–0.3		0.3	ns

Note 1. The following four external clock input frequencies are supported: 8 MHz, 16 MHz, 20 MHz and 24 MHz.

Note 2. X2 should be open and its parasitic capacitance should be less than 5 pF.

(3) SubOSC

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SubOSC frequency	f_{SOSC}	Crystal	30	32.768	38	kHz
SubOSC current consumption	I_{SOSC}	After stabilization		1.5*2	4*2	µA
SubOSC DC operating point	$V_{SOSCDCOP}$			0.65*2		V
SubOSC oscillation stabilization time	t_{SSTB}			*1		s

Note 1. Oscillator stabilization time is time until being set (“1”) in SOSCS.SOSCCLKACT bit after SOSCE.SOSCENTRG bit is written “1”, and depends on the setting value of SOSCST register. Please decide appropriate oscillation stabilization time by matching test with resonator and oscillation circuit.

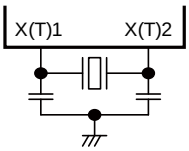
Note 2. This is reference value.

CAUTION

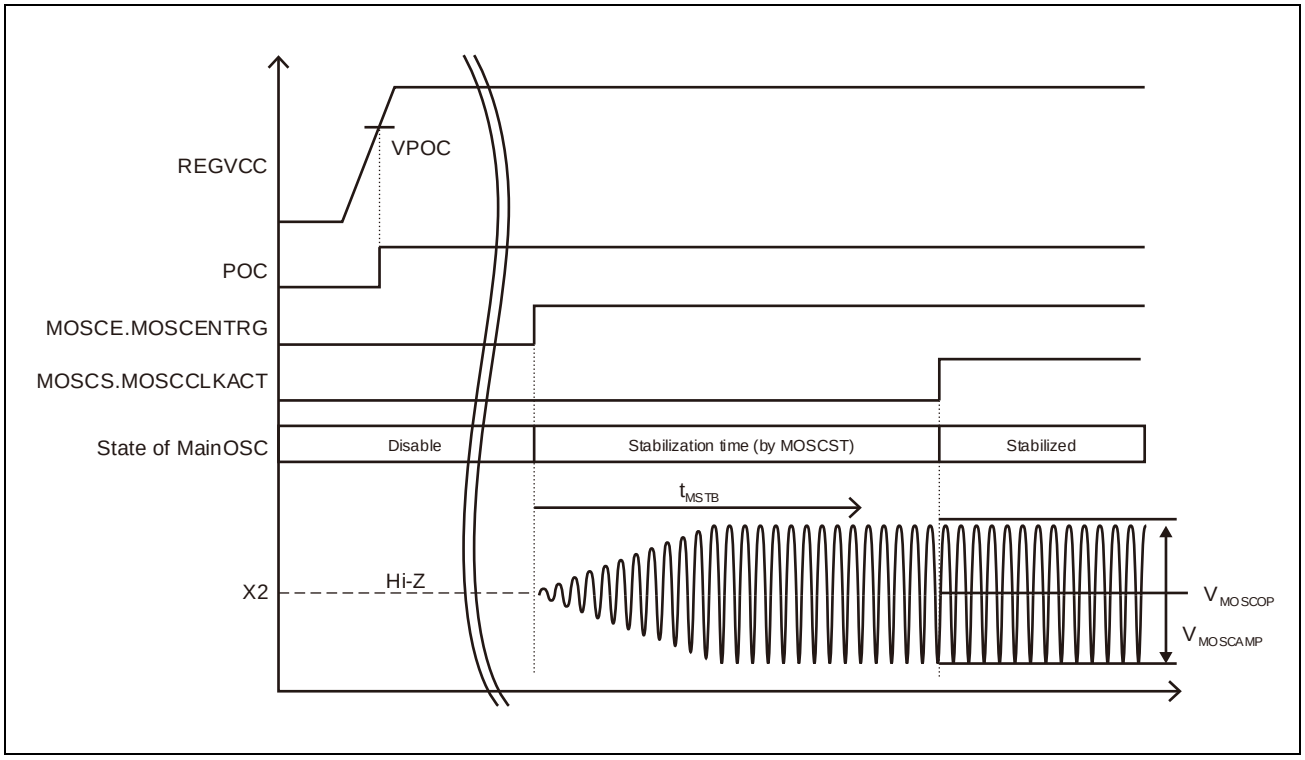
The oscillation stabilization time differs according the matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by an oscillator matching test.

NOTE

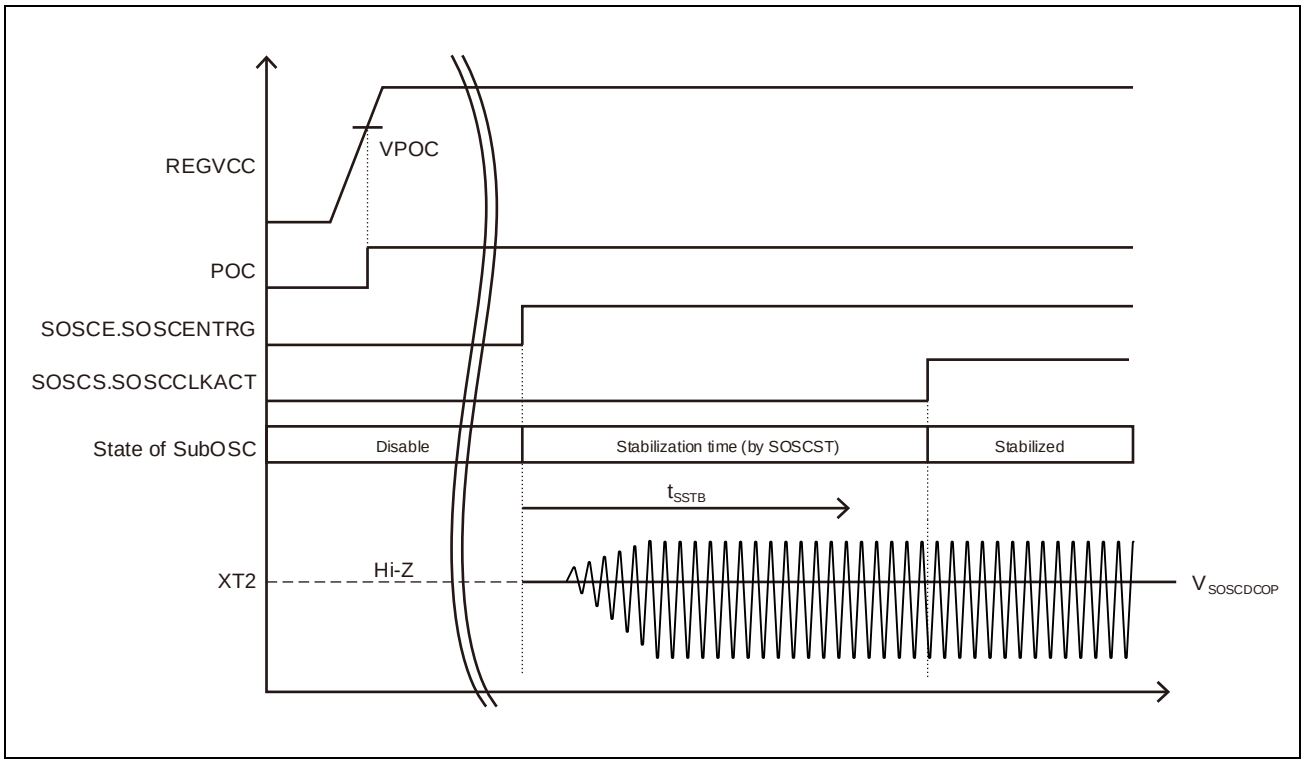
Recommended oscillator circuit is shown below.



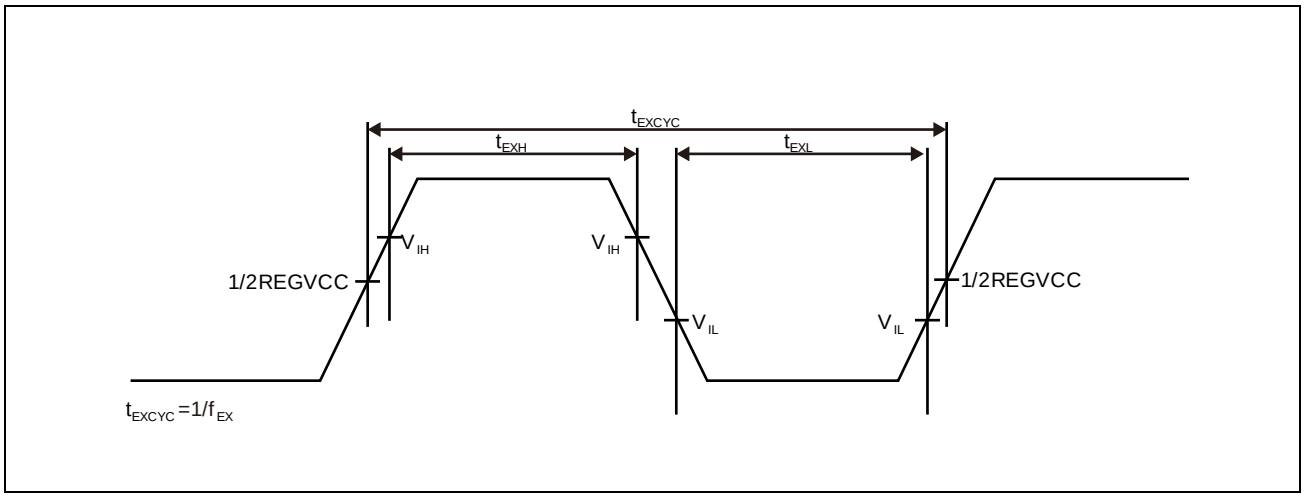
MainOSC



SubOSC



External clock



3B.3.3 Internal Oscillator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LS IntOSC frequency	f_{RL}		220.8	240	259.2	kHz
HS IntOSC frequency*3	f_{RH}		7.6	8	8.4	MHz
		After user trimming @ trimming temp*2	7.92	8	8.08	MHz
HS IntOSC current consumption	I_{RH}	After stabilization			170*1	µA
HS IntOSC oscillation stabilization time	t_{RHSTB}				54.4	µs

Note 1. This is reference value.

Note 2. The HS IntOSC frequency may not meet the specification range (8.00 MHz ±0.08 MHz after user trimming @ trimming temp) in the while writing/erasing the code/data flash.

Note 3. The HS IntOSC frequency may not meet the specification range in the Cyclic STOP/Cyclic RUN mode.

3B.3.4 PLL Characteristics

3B.3.4.1 PLL0 (for CPU, with SSCG) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Input frequency	$f_{PLL0CLKIN}$	MainOSC			8		24	MHz
		HS IntOSC*3			7.6	8.0	8.4	MHz
		HS IntOSC After user trimming @ trimming temp*3			7.92	8.0	8.08	MHz
Output frequency	$f_{CPLL0OUT}$	SSCG mode	MainOSC	Products of CPU frequency 240 MHz max.	105.8		240	MHz
				Products of CPU frequency 160 MHz max.	105.8		160	MHz
			HS IntOSC*3		67		84	MHz
			HS IntOSC After user trimming @ trimming temp*3		69.8		80.8	MHz
Modulation frequency	f_{MOD}				20		100	kHz
Frequency dithering range*2	f_{DIT}				0.82	1.0	1.18	%
					1.64	2.0	2.36	%
					2.46	3.0	3.54	%
					3.28	4.0	4.72	%
					4.10	5.0	5.90	%
					4.92	6.0	7.08	%
					6.56	8.0	9.44	%
					8.20	10.0	11.80	%
Lock time*1	t_{LCK0}	SSCG mode	PLL0ST = 0000 $1B80_H$		814.9	880	956.6	µs

Note 1. Lock time is time until being set (“1”) in PLL0S.PLL0CLKACT bit after PLL0E.PLL0ENTRG bit is written “1”.

Note 2. "Frequency dithering range” is set by PLL0ADJ[2:0] bits of PLL0C registers.

Note 3. The HS IntOSC has a frequency deviation. When the HSIntOSC is used the frequency deviation should be considered for the customer application as it affects peripheral functions (e.g. TAUx, ADCAn, etc.).

3B.3.4.2 PLL1 (for CPU/Peripheral) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input frequency	$f_{PLL1CLKIN}$	MainOSC	8		24	MHz
		HS IntOSC*3	7.6	8.0	8.4	MHz
		HS IntOSC After user trimming @ trimming temp*3	7.92	8.0	8.08	MHz
Output frequency	$f_{CPLL1OUT}$	MainOSC	80		120	MHz
		HS IntOSC*3	76	80	84	MHz
	$f_{PPLLOUT}$		76	80	84	MHz
Output period jitter*1	t_{CPJ1}		–100		100	ps
Long term jitter*1	t_{LTJ}	term = 1 µs	–500		500	ps
		term = 10 µs	–1		1	ns
		term = 20 µs	–2		2	ns
Lock time*2	t_{LCK1}		104	112.3	122.1	µs

Note 1. This is reference value.

Note 2. Lock time is time until being set (“1”) in PLL1S.PLL1CLKACT bit after PLL1E.PLL1ENTRG bit is written “1”.

Note 3. The HS IntOSC has a frequency deviation. When the HSIntOSC is used the frequency deviation should be considered for the customer application as it affects peripheral functions (e.g. TAUx, ADCAn, etc.).

3B.4 DC Characteristics

3B.4.1 Capacitance

Condition: REGVCC = EVCC = BVCC = A0VREF = A1VREF = AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, Ta = 25°C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI*1	f = 1 MHz			10	pF
Input/output capacitance	CIO*2	0 V for non measurement pins			10	pF

Note 1. CI: Capacitance between the input pin and ground

Note 2. CIO: Capacitance between the input/output pin and ground

3B.4.2 Pin Characteristics

Condition: Some of the conditions mentioned in this chapter can be selected by software and described in the hardware user's manual.

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Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
$\overline{\text{RESET}}$	—	—	✓	—	—	—	—	—	—
FLMD0	—	✓	—	—	—	—	—	✓	✓
AP0_0	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_1	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_2	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_3	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_4	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_5	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_6	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_7	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_8	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_9	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_10	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_11	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_12	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_13	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_14	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_15	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_0	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_1	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_2	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_3	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_4	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_5	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_6	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_7	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_8	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_9	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_10	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_11	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_12	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_13	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_14	✓	—	—	—	—	✓	Slow	—	✓*1
AP1_15	✓	—	—	—	—	✓	Slow	—	✓*1
IP0_0	—	—	—	—	—	—	—	—	—
JP0_0	—	✓	—	✓	✓	—	Slow	✓	✓
JP0_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
JP0_2	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
JP0_3	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
JP0_4	—	—	—	✓	—*5	—	Slow	✓	✓
JP0_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓

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Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
JP0_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_2	—	✓	—	✓	—	—	Slow/Fast*2	✓	✓
P0_3	—	✓	—	✓	—	—	Slow/Fast*2	✓	✓
P0_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_5	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P0_6	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P0_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P1_15	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_0	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P10_1	—	✓	—	✓	✓*6	—	Slow/Fast*3	✓	✓
P10_2	—	✓	—	✓	✓*6	—	Slow/Fast*3	✓	✓
P10_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_4	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P10_5	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P10_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓

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Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P10_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_15	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_2	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P11_3	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P11_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_6	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P11_7	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P11_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_10	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P11_11	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P11_12	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P11_15	—	✓	—	✓	✓*6	—	Slow/Fast	✓	✓
P12_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P12_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P12_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P12_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P12_4	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P12_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P13_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P13_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P13_2	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P13_3	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P13_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P13_5	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
P13_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P13_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P18_0	—	✓	—	✓	✓*6	✓	Slow/Fast	✓	✓*4
P18_1	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_2	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_3	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_4	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_5	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_6	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_7	—	✓	—	✓	✓	✓	Slow/Fast	✓	✓*4
P18_8	—	✓	—	✓	✓	✓	Slow/Fast	✓	✓*4
P18_9	—	✓	—	✓	✓	✓	Slow/Fast	✓	✓*4
P18_10	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_11	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_12	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_13	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4

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Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P18_14	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P18_15	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P19_0	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P19_1	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P19_2	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P19_3	—	✓	—	✓	—	✓	Slow/Fast	✓	✓*4
P2_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P2_15	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P20_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P21_0	—	✓	—	✓	—	—	Slow	✓	✓
P21_1	—	✓	—	✓	—	—	Slow	✓	✓
P21_2	—	✓	—	✓	—	—	Slow	✓	✓
P21_3	—	✓	—	✓	—	—	Slow	✓	✓
P21_4	—	✓	—	✓	—	—	Slow	✓	✓
P22_0	—	✓	—	✓	—	—	Slow	✓	✓
P22_1	—	✓	—	✓	—	—	Slow	✓	✓

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Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P22_2	—	✓	—	✓	—	—	Slow	✓	✓
P22_3	—	✓	—	✓	—	—	Slow	✓	✓
P22_4	—	✓	—	✓	—	—	Slow	✓	✓
P22_5	—	✓	—	✓	—	—	Slow	✓	✓
P22_6	—	✓	—	✓	—	—	Slow	✓	✓
P22_7	—	✓	—	✓	—	—	Slow	✓	✓
P22_8	—	✓	—	✓	—	—	Slow	✓	✓
P22_9	—	✓	—	✓	—	—	Slow	✓	✓
P22_10	—	✓	—	✓	—	—	Slow	✓	✓
P22_11	—	✓	—	✓	—	—	Slow	✓	✓
P22_12	—	✓	—	✓	—	—	Slow	✓	✓
P22_13	—	✓	—	✓	—	—	Slow	✓	✓
P22_14	—	✓	—	✓	—	—	Slow	✓	✓
P22_15	—	✓	—	✓	—	—	Slow	✓	✓
P3_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_2	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P3_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P8_0	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_1	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_2	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_3	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_4	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_5	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_6	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_7	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_8	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_9	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_10	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_11	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_12	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_0	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_1	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_2	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_3	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_4	—	✓	—	✓	—	✓	Slow	✓	✓*4

Note 1. Pull-down resistor for ADC diagnostic purpose. Control via ADC self-diagnostic register.

Note 2. Supports Cload: 100 pF

Note 3. Supports Cload: 50 pF

Note 4. Pull-down resistors for ADC diagnostic and internal pull-down purposes. For ADC diagnostic, control via ADC self-diagnostic register. For internal pull-down, control via PD register.

Note 5. TTL is selected for Boundary scan mode or Nexus in normal operating mode.

Note 6. Only available for 176-pin, 233-pin and 272-pin devices.

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

(1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH	CMOS		0.65 × IOVCC		IOVCC + 0.3	V
		SHMT1*3		0.65 × IOVCC		IOVCC + 0.3	V
		SHMT2		0.75 × IOVCC		IOVCC + 0.3	V
		SHMT4		0.8 × IOVCC		IOVCC + 0.3	V
		TTL	IOVCC = VPOC to 3.6 V	2.0		IOVCC + 0.3	V
			IOVCC = 3.6 V to 5.5 V	2.2		IOVCC + 0.3	V
		IP0_0 pin		0.7 × REGVCC		REGVCC	V
Low level input voltage	VIL	CMOS		–0.3		0.35 × IOVCC	V
		SHMT1		–0.3		0.35 × IOVCC	V
		SHMT2		–0.3		0.25 × IOVCC	V
		SHMT4		–0.3		0.5 × IOVCC	V
		TTL		–0.3		0.8	V
		IP0_0 pin		0		0.3 × REGVCC	V
Input hysteresis for Schmitt	VH	SHMT1		0.3			V
		SHMT2		0.2 × IOVCC			V
		SHMT4		0.1			V
Input leakage current	ILIH	IP0_0 pin, VI = REGVCC				0.5	µA
		$\overline{\text{RESET}}$, FLMD0, JP0, P0, P1, P2, P3, P8, P9, P20 pin, VI = EVCC*2				0.5	µA
		P10, P11, P12, P13, P18, P19, P21, P22 pin, VI = BVCC*2				0.5	µA
		AP0 pin, VI = A0VREF*2, Tj ≤ 130°C				0.3	µA
		AP0 pin, VI = A0VREF*2				0.5	µA
		AP1 pin, VI = A1VREF*2, Tj ≤ 130°C				0.3	µA
		AP1 pin, VI = A1VREF*2				0.5	µA
	ILIL	IP0_0 pin, VI = 0 V				–0.5	µA
		$\overline{\text{RESET}}$, FLMD0, JP0, P0, P1, P2, P3, P8, P9, P20 pin, VI = 0 V*2				–0.5	µA
		P10, P11, P12, P13, P18, P19, P21, P22 pin, VI = 0V*2				–0.5	µA
		AP0 pin, VI = 0 V*2, Tj ≤ 130°C				–0.3	µA
		AP0 pin, VI = 0 V*2				–0.5	µA
		AP1 pin, VI = 0 V*2, Tj ≤ 130°C				–0.3	µA
		AP1 pin, VI = 0 V*2				–0.5	µA
Internal pull-up resistance	RU	except FLMD0 pin, VI = 0 V		20 (275 µA)	40	100	kΩ
		FLMD0 pin, VI = 0V*3		4 (1375 µA)		36	kΩ
Internal pull-down resistance	RD	except FLMD0 pin, VI = IOVCC		20 (275 µA)	40	100	kΩ
		FLMD0 pin, VI = EVCC		4 (1375 µA)		36	kΩ

(2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High level output voltage	VOH	Fast mode	IOH = –5 mA (6 pins)*4	IOVCC – 1.0			V
			IOH = –3 mA (10 pins)*4	IOVCC – 1.0			V
			IOH = –1 mA (16 pins)*4	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins)*4	IOVCC – 0.5			V
		Slow mode	IOH = –1 mA (16 pins)*4	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins)*4	IOVCC – 0.5			V
Low level output voltage	VOL	Fast mode	IOL = 5 mA (6 pins)*4			0.4	V
			IOL = 3 mA (10 pins)*4			0.4	V
			IOL = 1 mA (16 pins)*4			0.4	V
		Slow mode	IOL = 1 mA (16 pins)*4			0.4	V
Rise/Fall time	t_{KRP}/t_{KFP}	Fast mode (except below pins)*5	CL = 30 pF			7	ns
			CL = 50 pF			12	ns
			CL = 100 pF			24	ns
		Fast mode (P0_5, P0_6, P10_1, P10_2, P11_2, P11_3, P11_6, P11_7)*6	CL = 50 pF			6	ns
		Fast mode (P0_2, P0_3)*6	CL = 100 pF			6.15	ns
		Slow mode*5	CL = 30 pF			37	ns
			CL = 50 pF			62	ns
			CL = 100 pF			124	ns
Output frequency	f_O	Fast mode	CL = 30 pF			40	MHz
		Slow mode	CL = 30 pF			10	MHz
			CL = 50 pF			6	MHz
			CL = 100 pF			3	MHz

Note 1. “IOVCC” means the pins are assigned to the power supply (EVCC, BVCC, A0VREF and A1VREF).

Note 2. Not select the analog input function of ADCn.

Note 3. When the internal pull-up resistor of FLMD0 pin is applied by FLMDCNT register, please connect 86 kΩ or more as external pull-down resistor.

Note 4. The number of pin indicates simultaneous ON.

Note 5. Measurement point: 0.1 × IOVCC to 0.9 × IOVCC

Note 6. Measurement point: 0.2 × IOVCC to 0.8 × IOVCC

3B.4.2.1 Output Current

(1) 272-Pin Version (RH850/F1KM-S4)

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_10 to P20_14			–30	mA
				P20_0 to P20_9			–30	mA
				P0_0 to P0_3			–20	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0			–30	mA
				JP0_6, P0_7 to P0_10, P1_4, P1_5, P1_14, P1_15, P2_2 to P2_5, P8_0, P8_1, P8_3 to P8_9			–30	mA
				P3_1 to P3_10			–30	mA
			Total (EVCC)				–60	mA
		PgB	Per side	P18_0 to P18_7			–30	mA
				P18_8 to P18_15, P19_0 to P19_3			–30	mA
				P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1			–30	mA
				P10_0 to P10_2			–15	mA
				P10_3 to P10_5			–15	mA
				P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7			–30	mA
				P21_0, P21_2 to P21_4, P22_0 to P22_2			–7	mA
				P22_3 to P22_8			–4	mA
				P21_1, P22_9 to P22_15			–8	mA
			Total (BVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
		PgA1	Total (A1VREF)				–16	mA

(272-pin version)

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_10 to P20_14			30	mA
				P20_0 to P20_9			30	mA
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12			30	mA
				JP0_0 to JP0_5, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0, P8_2, P8_10 to P8_12			30	mA
				JP0_6, P0_7 to P0_10, P2_2, P2_3			30	mA
				P1_4, P1_5, P1_14, P1_15, P2_4, P2_5, P8_0, P8_1, P8_3 to P8_9			30	mA
				P3_1 to P3_10			30	mA
			Total (EVCC)				60	mA
		PgB	Per side	P18_0 to P18_7			30	mA
				P18_8 to P18_15, P19_0 to P19_3			30	mA
				P10_6 to P10_14, P11_1, P11_2			30	mA
				P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1			30	mA
				P10_0 to P10_2			15	mA
				P10_3 to P10_5			15	mA
				P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7			30	mA
				P21_0, P21_2 to P21_4, P22_0 to P22_6			11	mA
				P21_1, P22_7 to P22_15			10	mA
			Total (BVCC)				60	mA
		PgA0	Total (A0VREF)				16	mA
		PgA1	Total (A1VREF)				16	mA

Note: For detail of the definition of “side” and “total”, see **Section 3B.2.3, Port Current**.

(2) 233-Pin Version (RH850/F1KM-S4)

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5			–30	mA
				P0_0 to P0_3			–20	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15, P3_0			–30	mA
				JP0_6, P0_7 to P0_10, P1_4, P1_5, P1_14, P1_15, P2_2 to P2_5, P8_0, P8_1, P8_3 to P8_9			–30	mA
			Total (EVCC)				–60	mA
		PgB	Per side	P18_0 to P18_7			–30	mA
				P18_8 to P18_15, P19_0 to P19_3			–30	mA
				P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1			–30	mA
				P10_0 to P10_2			–15	mA
				P10_3 to P10_5			–15	mA
				P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7			–30	mA
			Total (BVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
		PgA1	Total (A1VREF)				–16	mA
Low-level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5			30	mA
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6 to P2_12			30	mA
				JP0_0 to JP0_5, P1_8 to P1_11, P2_0, P2_1, P2_13 to P2_15 P3_0, P8_2, P8_10 to P8_12			30	mA
				JP0_6, P0_7 to P0_10, P2_2, P2_3			30	mA
				P1_4, P1_5, P1_14, P1_15, P2_4, P2_5, P8_0, P8_1, P8_3 to P8_9			30	mA
			Total (EVCC)				60	mA
		PgB	Per side	P18_0 to P18_7			30	mA
				P18_8 to P18_15, P19_0 to P19_3			30	mA
				P10_6 to P10_14, P11_1, P11_2			30	mA
				P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0, P13_1			30	mA
				P10_0 to P10_2			15	mA
				P10_3 to P10_5			15	mA
				P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5, P13_2 to P13_7			30	mA
			Total (BVCC)				60	mA
		PgA0	Total (A0VREF)				16	mA
		PgA1	Total (A1VREF)				16	mA

Note: For detail of the definition of “side” and “total”, see **Section 3B.2.3, Port Current**.

(3) 176-Pin Version (RH850/F1KM-S4, RH850/F1KM-S2)

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5			–30	mA
				P0_0 to P0_3			–20	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2, P1_8 to P1_11, P2_0, P2_1			–30	mA
				JP0_6, P0_7 to P0_10, P1_4, P1_5, P1_14, P1_15, P2_2 to P2_5, P8_0, P8_1, P8_3 to P8_9			–30	mA
			Total (EVCC)				–60	mA
		PgB	Per side	P10_6 to P10_9, P18_0 to P18_7			–30	mA
				P10_10 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2			–30	mA
				P10_0 to P10_2			–15	mA
				P10_3 to P10_5			–15	mA
				P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5			–30	mA
			Total (BVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
		PgA1	Total (A1VREF)				–16	mA
Low-level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5			11	mA
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12, P1_13, P2_6			30	mA
				JP0_0 to JP0_5, P1_8 to P1_11, P2_0, P2_1, P8_2, P8_10 to P8_12			30	mA
				JP0_6, P0_7 to P0_10, P2_2, P2_3			30	mA
				P1_4, P1_5, P1_14, P1_15, P2_4, P2_5, P8_0, P8_1, P8_3 to P8_9			30	mA
			Total (EVCC)				60	mA
		PgB	Per side	P18_0 to P18_7			30	mA
				P10_6 to P10_14, P11_1, P11_2			30	mA
				P11_3 to P11_7, P11_15, P12_0 to P12_2			30	mA
				P10_0 to P10_2			15	mA
				P10_3 to P10_5			15	mA
				P10_15, P11_0, P11_8 to P11_12, P12_3 to P12_5			30	mA
			Total (BVCC)				60	mA
		PgA0	Total (A0VREF)				16	mA
		PgA1	Total (A1VREF)				16	mA

Note: For detail of the definition of “side” and “total”, see **Section 3B.2.3, Port Current**.

(4) 144-Pin Version (RH850/F1KM-S4, RH850/F1KM-S2)

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_4, P20_5			–15	mA
				P0_0 to P0_3			–20	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2, P1_8 to P1_11			–30	mA
				JP0_6, P0_7 to P0_10, P1_4, P1_5, P8_0 to P8_1, P8_3 to P8_9			–30	mA
			Total (EVCC)				–60	mA
		PgB	Per side	P10_6 to P10_9, P18_0 to P18_3			–30	mA
				P10_10 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2			–30	mA
				P10_0 to P10_5, P10_15, P11_0, P11_8 to P11_12			–30	mA
			Total (BVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
		PgA1	Total (A1VREF)				–8	mA
Low-level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_4 to P20_5			15	mA
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3			30	mA
				JP0_0 to JP0_5, P1_8 to P1_11, P8_2, P8_10 to P8_12			30	mA
				JP0_6, P0_7 to P0_10			25	mA
				P1_4 to P1_5, P8_0, P8_1, P8_3 to P8_9			19	mA
			Total (EVCC)				60	mA
		PgB	Per side	P18_0 to P18_3			20	mA
				P10_6 to P10_14, P11_1, P11_2			30	mA
				P11_3 to P11_7, P11_15, P12_0 to P12_2			30	mA
				P10_0 to P10_5, P10_15, P11_0, P11_8 to P11_12			30	mA
			Total (BVCC)				60	mA
		PgA0	Total (A0VREF)				16	mA
		PgA1	Total (A1VREF)				8	mA

Note: For detail of the definition of “side” and “total”, see **Section 3B.2.3, Port Current**.

(5) 100-Pin Version (RH850/F1KM-S4, RH850/F1KM-S2)

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_4			–5	mA
				P0_0 to P0_3, P10_3 to P10_5			–25	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2			–11	mA
				P0_7 to P0_10, P8_3 to P8_9			–27	mA
				P10_6 to P10_9			–20	mA
				P10_10 to P10_14, P11_1 to P11_7			–30	mA
				P10_0 to P10_2			–15	mA
			Total (EVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
Low-level output current	IOL	PgE	Per side	P9_0 to P9_4			5	mA
				P0_0 to P0_6, P0_11 to P0_14, P10_3 to P10_5			30	mA
				JP0_0 to JP0_5, P8_2, P8_10 to P8_12			26	mA
				P0_7 to P0_10			20	mA
				P8_3 to P8_9			7	mA
				P10_6 to P10_14, P11_1, P11_2			30	mA
				P11_3 to P11_7			25	mA
				P10_0 to P10_2			15	mA
			Total (EVCC)				60	mA
		PgA0	Total (A0VREF)				16	mA

Note: For detail of the definition of “side” and “total”, see **Section 3B.2.3, Port Current**.

3B.4.3 Power Supply Currents

Condition: REGVCC, EVCC, BVCC, A0VREF and A1VREF total current. But the I/O buffer is stopped.

Products of CPU frequency 240 MHz max. (RH850/F1KM-S4)

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2				
RUN mode current	IDDR	Run (240 MHz)	Run	–40 to 150°C	Run (#1)		70	185	mA
				25°C	Stop (#1)		64		mA
RUN mode current (During data/code flash programming)	IDDR3	Run (240 MHz)	Run	–40 to 150°C	Run (#2)		90	205	mA
RUN mode current (With code flash background operation)	IDDRBGO	Run (240 MHz)	Run	–40 to 150°C	Run (#6)		90	205	mA
RUN mode current (HALT state)	IDDH	Run (240 MHz)	Run	–40 to 150°C	Run (#3)		67	183	mA

Products of CPU frequency 240 MHz max. (RH850/F1KM-S2)

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2				
RUN mode current	IDDR	Run (240 MHz)	Run	–40 to 150°C	Run (#1)		60	154	mA
				25°C	Stop (#1)		46		mA
RUN mode current (During data/code flash programming)	IDDR3	Run (240 MHz)	Run	–40 to 150°C	Run (#2)		80	174	mA
RUN mode current (With code flash background operation)	IDDRBGO	Run (240 MHz)	Run	–40 to 150°C	Run (#6)		80	174	mA
RUN mode current (HALT state)	IDDH	Run (240 MHz)	Run	–40 to 150°C	Run (#3)		58	152	mA

Products of CPU frequency 160 MHz max. (RH850/F1KM-S4)

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2				
RUN mode current	IDDR	Run (160 MHz)	Run	–40 to 150°C	Run (#1)		60	173	mA
				25°C	Stop (#1)		54		mA
RUN mode current (During data/code flash programming)	IDDR3	Run (160 MHz)	Run	–40 to 150°C	Run (#2)		80	193	mA
RUN mode current (With code flash background operation)	IDDRBGO	Run (160 MHz)	Run	–40 to 150°C	Run (#6)		80	193	mA
RUN mode current (HALT state)	IDDH	Run (160 MHz)	Run	–40 to 150°C	Run (#3)		57	171	mA

Products of CPU frequency 240 MHz max., 160 MHz max. (RH850/F1KM-S4)

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2				
STOP mode current	IDDS	Stop	Stop	–40 to 90°C	Stop (#2)		1.3	22	mA
				110°C	Stop (#2)			42	mA
				135°C	Stop (#2)			66	mA
DeepSTOP mode current	IDDDS	Power off	Power off	–40 to 85°C	Stop (#3)		50	700	µA
				105°C	Stop (#3)			1280	µA
				125°C	Stop (#3)			1840	µA
Cyclic RUN mode current	IDDCR	Run (HS IntOSC)	Stop	–40 to 90°C	Run (#4)		6.1	28	mA
				115°C	Run (#4)			47	mA
				135°C	Run(#4)			71	mA
Cyclic STOP mode current	IDDCS	Stop	Stop	–40 to 90°C	Run (#5)		1.4	23	mA
				110°C	Run (#5)			42	mA
				135°C	Run (#5)			66	mA

Products of CPU frequency 240 MHz max. (RH850/F1KM-S2)

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2				
STOP mode current	IDDS	Stop	Stop	–40 to 90°C	Stop (#2)		1.0	21	mA
				110°C	Stop (#2)			38	mA
DeepSTOP mode current	IDDDS	Power off	Power off	–40 to 85°C	Stop (#3)		50	670	µA
				105°C	Stop (#3)			1100	µA
Cyclic RUN mode current	IDDCR	Run (HS IntOSC)	Stop	–40 to 90°C	Run (#4)		4.4	25	mA
				115°C	Run (#4)			43	mA
Cyclic STOP mode current	IDDCS	Stop	Stop	–40 to 90°C	Run (#5)		1.2	21	mA
				110°C	Run (#5)			39	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- REGVCC = EVCC = BVCC = A0VREF = A1VREF = 5.0 V
- AWOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V

Note 2. Operating condition of each peripheral function is shown in the table of next page.

Caution: It must be ensured that the junction temperature in the Ta range remains below Tj ≤ 150°C and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

Function		Run						Stop		
		(#1)	(#2)	(#3)	(#4)	(#5)	(#6)	(#1)	(#2)	(#3)
AWO	MainOSC	Run	Run	Run	Stop	Stop	Run	Run	Stop	Stop
	SubOSC	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	HS IntOSC	Run	Run	Run	Run	Stop	Run	Run	Stop	Stop
	FOUT	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	LPS	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	RRAM	Read/Write	Read/Write	No access	Fetch	No access	Read/Write	Read/Write	No access	No access
	WDTA0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	TAUJ0, TAUJ2	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Run	Stop	Stop	Stop
	RTCA0	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Run	Stop	Stop	Stop
	CLMA0	Run	Run	Run	Run	Stop	Run	Stop	Stop	Stop
	CLMA1	Run	Run	Run	Stop	Stop	Run	Stop	Stop	Stop
	ADCA0	Run*1	Run*1	Run*1	Stop	Stop	Run*1	Stop	Stop	Stop
ISO	CPU	Run (PLL0)	Run (PLL0)	HALT (PLL0)	Run (HS IntOSC)	Stop	Run (PLL0)	Run (PLL0)	Stop	Power off
	ICUMD	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	DMA	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	PLL0	Run	Run	Run	Stop	Stop	Run	Run	Stop	
	PLL1	Run	Run	Run	Stop	Stop	Run	Run	Stop	
	Code flash (FLI0)	Fetch	Fetch	No access	No access	No access	Fetch	Fetch	No access	
	Code flash (FLI1)	Fetch	Fetch	No access	No access	No access	Write/Erase	Fetch	No access	
	Data flash	Read	Write/Erase	No access	No access	No access	No access	Read	No access	
	LRAM	Read/Write	Read/Write	No access	No access	No access	Read/Write	Read/Write	No access	
	GRAM	Read/Write*2	Read/Write*2	No access	No access	No access	Read/Write*2	Read/Write*2	No access	
	OSTMn	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	WDTA1	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	TAUD0	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	TAUBn	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	TAUJ1, TAUJ3	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	TAPA, PIC	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	ENCA0	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	PWM-diag	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	RLIN3n	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	RLIN24n	Wait	Wait	Wait	Stop	Stop	Wait	Stop	Stop	
	RCFDCn	Wait	Wait	Wait	Stop	Stop	Wait	Stop	Stop	
	CSIGn	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	CSIHn	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	RIICn	Wait	Wait	Wait	Stop	Stop	Wait	Stop	Stop	
	FlexRay	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	ETNBn	Wait	Wait	Wait	Stop	Stop	Wait	Stop	Stop	
	SFMA0	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	KR	Wait	Wait	Wait	Stop	Stop	Wait	Stop	Stop	
	RSENTn	Run	Run	Run	Stop	Stop	Wait	Stop	Stop	
	CLMA2	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	CLMA3	Run	Run	Run	Stop	Stop	Run	Stop	Stop	
	ADCA1	Run	Run	Run	Stop	Stop	Run	Stop	Stop	

Note 1. T&H used.

Note 2. GRZF not used.

3B.4.4 Injection Currents

Table 3B.1 Definition of Pin Group (RH850/F1KM-S4 272-Pin Version)

Symbol	Power Supply for Pin Group	Pin
PgR	REGVCC, AWOVSS	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P2, P3, P20
PgB	BVCC, BVSS	P10, P11, P12, P13, P21, P22
PgE’	EVCC, EVSS	P8, P9
PgB’	BVCC, BVSS	P18, P19
PgA0	A0VREF, A0VSS	AP0
PgA1	A1VREF, A1VSS	AP1

Table 3B.2 Definition of Pin Group (RH850/F1KM-S4 233-Pin Version)

Symbol	Power Supply for Pin Group	Pin
PgR	REGVCC, AWOVSS	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P2, P3, P20
PgB	BVCC, BVSS	P10, P11, P12, P13
PgE’	EVCC, EVSS	P8, P9
PgB’	BVCC, BVSS	P18, P19
PgA0	A0VREF, A0VSS	AP0
PgA1	A1VREF, A1VSS	AP1

Table 3B.3 Definition of Pin Group (RH850/F1KM-S4, RH850/F1KM-S2 176-Pin Version)

Symbol	Power Supply for Pin Group	Pin
PgR	REGVCC, AWOVSS	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P2, P20
PgB	BVCC, BVSS	P10, P11, P12
PgE’	EVCC, EVSS	P8, P9
PgB’	BVCC, BVSS	P18
PgA0	A0VREF, A0VSS	AP0
PgA1	A1VREF, A1VSS	AP1

Table 3B.4 Definition of Pin Group (RH850/F1KM-S4, RH850/F1KM-S2 144-Pin Version)

Symbol	Power Supply for Pin Group	Pin
PgR	REGVCC, AWOVSS	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P20
PgB	BVCC, BVSS	P10, P11, P12
PgE’	EVCC, EVSS	P8, P9
PgB’	BVCC, BVSS	P18
PgA0	A0VREF, A0VSS	AP0
PgA1	A1VREF, A1VSS	AP1

Table 3B.5 Definition of Pin Group (RH850/F1KM-S4, RH850/F1KM-S2 100-Pin Version)

Symbol	Power Supply for Pin Group	Pin
PgE	EVCC, EVSS	JP0, P0, P10, P11
PgE’	EVCC, EVSS	P8, P9
PgA0	A0VREF, A0VSS	AP0

3B.4.4.1 Absolute Maximum Ratings

(1) 272/233/176/144-Pin Versions (RH850/F1KM-S4), 176/144-Pin Versions (RH850/F1KM-S2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJPM}	PgE	Per pin			10	mA
			Total			60	mA
		PgB	Per pin			10	mA
			Total			60	mA
		PgE’	Per pin			10	mA
			Total			60	mA
		PgB’	Per pin			10	mA
			Total			60	mA
		PgA0	Per pin			10	mA
			Total			60	mA
		PgA1	Per pin			10	mA
			Total			60	mA
		PgR	Per pin			10	mA
Negative overload current VIN < VSS	I_{INJNM}	PgE	Per pin			–10	mA
			Total			–60	mA
		PgB	Per pin			–10	mA
			Total			–60	mA
		PgE’	Per pin			–10	mA
			Total			–60	mA
		PgB’	Per pin			–10	mA
			Total			–60	mA
		PgA0	Per pin			–10	mA
			Total			–60	mA
		PgA1	Per pin			–10	mA
			Total			–60	mA
		PgR	Per pin			–10	mA

CAUTIONS

1. The DC injection current (Total) must satisfy the specifications of the injection current per pin.
2. In case of an injected current condition for PgA0 and PgA1, TESH0SN is kept when the injected current is applied to an adjacent pin where the ADC self-diagnosis is executed. When an injected current is applied to the same pin where the ADC self-diagnosis is executed the TESH0SN deviating value will increase sharply with increasing absolute value of injection current.

(2) 100-Pin Version (RH850/F1KM-S4, RH850/F1KM-S2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJPM}	PgE	Per pin			10	mA
			Total			60	mA
		PgE'	Per pin			10	mA
			Total			60	mA
		PgA0	Per pin			10	mA
			Total			60	mA
Negative overload current VIN < VSS	I_{INJNM}	PgE	Per pin			–10	mA
			Total			–60	mA
		PgE'	Per pin			–10	mA
			Total			–60	mA
		PgA0	Per pin			–10	mA
			Total			–60	mA

CAUTIONS

1. The DC injection current (Total) must satisfy the specifications of the injection current per pin.
2. In case of an injected current condition for PgA0, TESH0SN is kept when the injected current is applied to an adjacent pin where the ADC self-diagnosis is executed. When an injected current is applied to the same pin where the ADC self-diagnosis is executed the TESH0SN deviating value will increase sharply with increasing absolute value of injection current.

3B.4.4.2 DC Characteristics for Overload Current

(1) 272/233/176/144-Pin Versions (RH850/F1KM-S4), 176/144-Pin Versions (RH850/F1KM-S2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJP}	PgE	Per pin			2	mA
			Total			50	mA
		PgB	Per pin			2	mA
			Total			50	mA
		PgE’	Per pin			3	mA
			Total			20	mA
		PgB’	Per pin			3	mA
			Total			20	mA
		PgA0	Per pin			3	mA
			Total			20	mA
		PgA1	Per pin			3	mA
			Total			20	mA
		PgR	Per pin			2	mA
Negative overload current VIN < VSS	I_{INJN}	PgE	Per pin			–2	mA
			Total			–50	mA
		PgB	Per pin			–2	mA
			Total			–50	mA
		PgE’	Per pin			–3	mA
			Total			–20	mA
		PgB’	Per pin			–3	mA
			Total			–20	mA
		PgA0	Per pin			–3	mA
			Total			–20	mA
		PgA1	Per pin			–3	mA
			Total			–20	mA
		PgR	Per pin			–2	mA

NOTE

These specifications are not tested on sorting and are specified based on the device characterization.

(2) 100-Pin Version (RH850/F1KM-S4, RH850/F1KM-S2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJP}	PgE	Per pin			2	mA
			Total			50	mA
		PgE’	Per pin			3	mA
			Total			20	mA
		PgA0	Per pin			3	mA
			Total			20	mA
Negative overload current VIN < VSS	I_{INJN}	PgE	Per pin			–2	mA
			Total			–50	mA
		PgE’	Per pin			–3	mA
			Total			–20	mA
		PgA0	Per pin			–3	mA
			Total			–20	mA

NOTE

These specifications are not tested on sorting and are specified based on the device characterization.

3B.4.5 Power Management Characteristics

3B.4.5.1 Regulator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	REGVCC		VPOC*1		5.5	V
Output voltage	AWOVCL	AWOVCL pin	1.15	1.25	1.35	V
	ISOVCL	ISOVCL pin	1.15	1.25	1.35	V
Capacitance	CAWOVCL	AWOVCL pin	0.07	0.10	0.13	µF
	CISOVCL	ISOVCL pin	0.07	0.10	0.13	µF
Equivalent series resistance for load capacitance	RVRAWO	for CAWOVCL			40*2	mΩ
	RVRISO	for CISOVCL			40*2	mΩ
Inrush current during power-on (RH850/F1KM-S4)					250	mA
Inrush current during power-on (RH850/F1KM-S2)					250	mA

Note 1. “VPOC” means POC (power-on clear) detection voltage (typ. 2.85 V). For detail, see **Section 3B.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.

Note 2. This is reference value.

3B.4.5.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Detection voltage (REGVCC)	VPOC	POC			2.7	2.85	3.0	V
	VLVI0	LVI	Rise		3.87	4.0	4.13	V
			Fall		3.9	4.0	4.1	V
	VLVI1		Rise		3.57	3.7	3.83	V
			Fall		3.6	3.7	3.8	V
	VLVI2		Rise		3.37	3.5	3.63	V
			Fall		3.4	3.5	3.6	V
	VVLVI	VLVI			1.8	1.9	2.0	V
Detection voltage (ISOVCL)	VCVMH	CVM	High voltage[Caution]		1.35	1.39	1.43	V
	VCVML*8		Low voltage[Caution]		1.10	1.15	1.20	V
Response time	t_{D_POC1}*6	POC	At power-on (Rise)	*1			2	ms
				*2			6.3	ms
			After power-on (Rise)	*3			2	ms
				*4			5	ms
	t_{D_POC2}*7		After power-on (Fall)	*5			5	µs
	t_{D_LVI}	LVI					2	ms
	t_{D_VLVI}	VLVI		*3			2	ms
				*4			5	ms
	t_{D_CVM}	CVM			0.2		10	µs
Setup time	t_{S_LVI}	LVI	LVICNT0,1 bits are set to 1 (except 00_B), then LVI is ready to operate				80	µs
REGVCC minimum width	t_{W_POC}	POC			0.2			ms
	t_{W_LVI}	LVI			0.2			ms
	t_{W_VLVI}	VLVI			0.2			ms

Note 1. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms

Note 2. Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms

Note 3. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 20 V/ms

Note 4. Voltage slope (t_{VS}): 20 V/ms < t_{VS} ≤ 500 V/ms

Note 5. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 500 V/ms

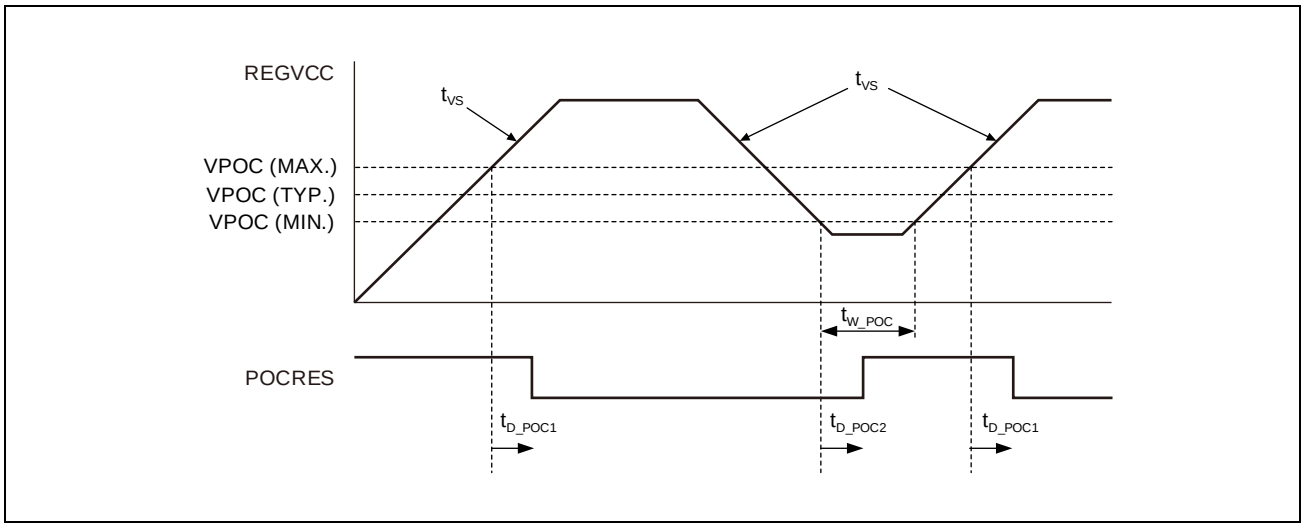
Note 6. t_{D_POC1} is the time from detection voltage to release of reset signal.

Note 7. t_{D_POC2} is the time from detection voltage to occurrence of reset signal.

Note 8. The CVM monitors the internal voltage regulator output to ensure that ISOVCL is upper than specified minimum level.

Caution: A detection of the voltage ISOVCL outside the specified level of VCVMH and VCVML is not ensured by CVM.

POC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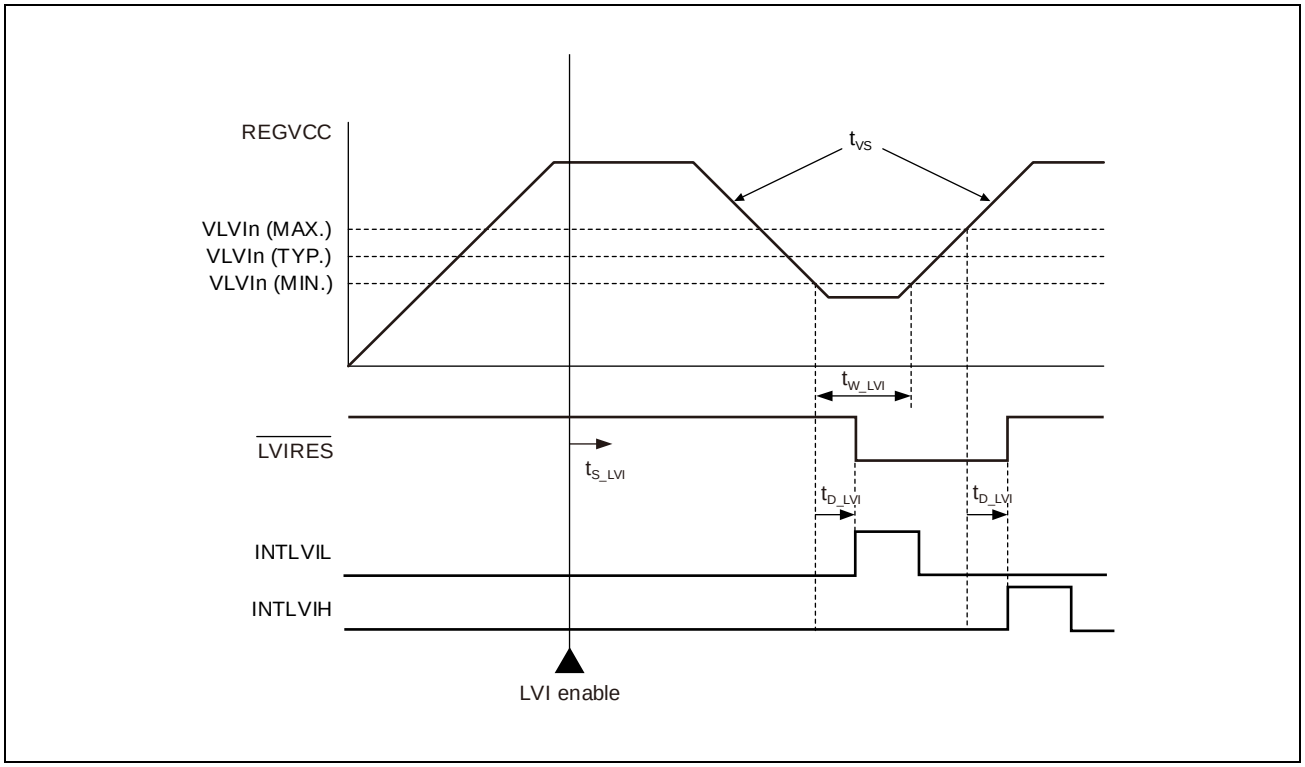
VPOC (MAX.)
VPOC (TYP.)
VPOC (MIN.)
POCRES
tVS
tVS
tW_POC
tD_POC1
tD_POC2
tD_POC1

LVI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VLVIn (TYP.)
VLVIn (MIN.)
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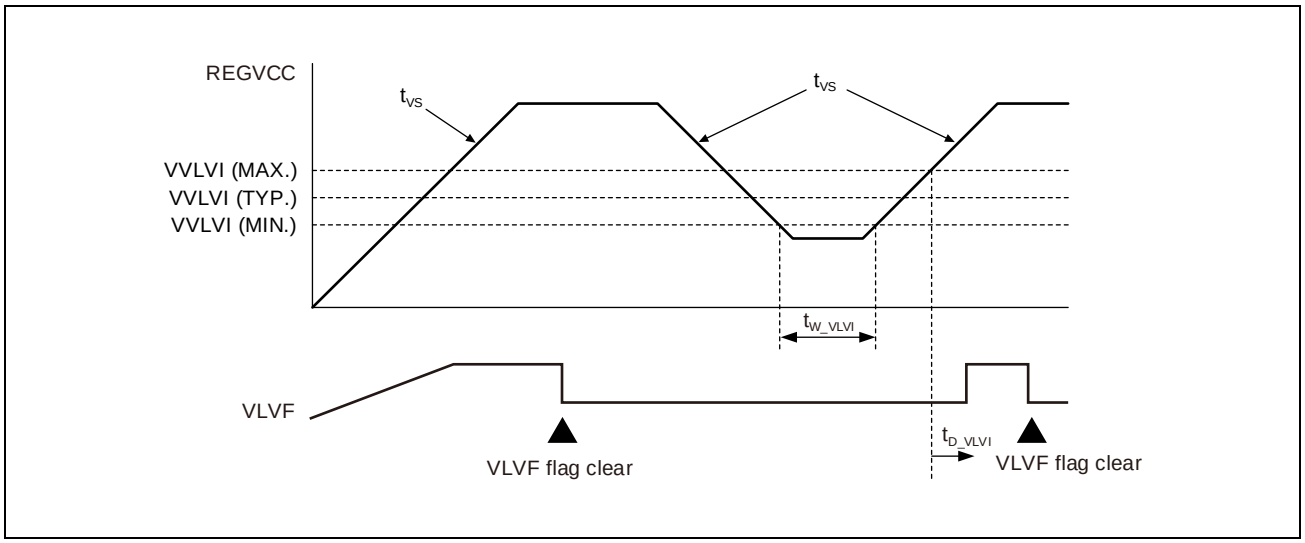
tVS
tW_LVI
tS_LVI
tD_LVI
tD_LVI
LVI enable

VLVI


REGVCC
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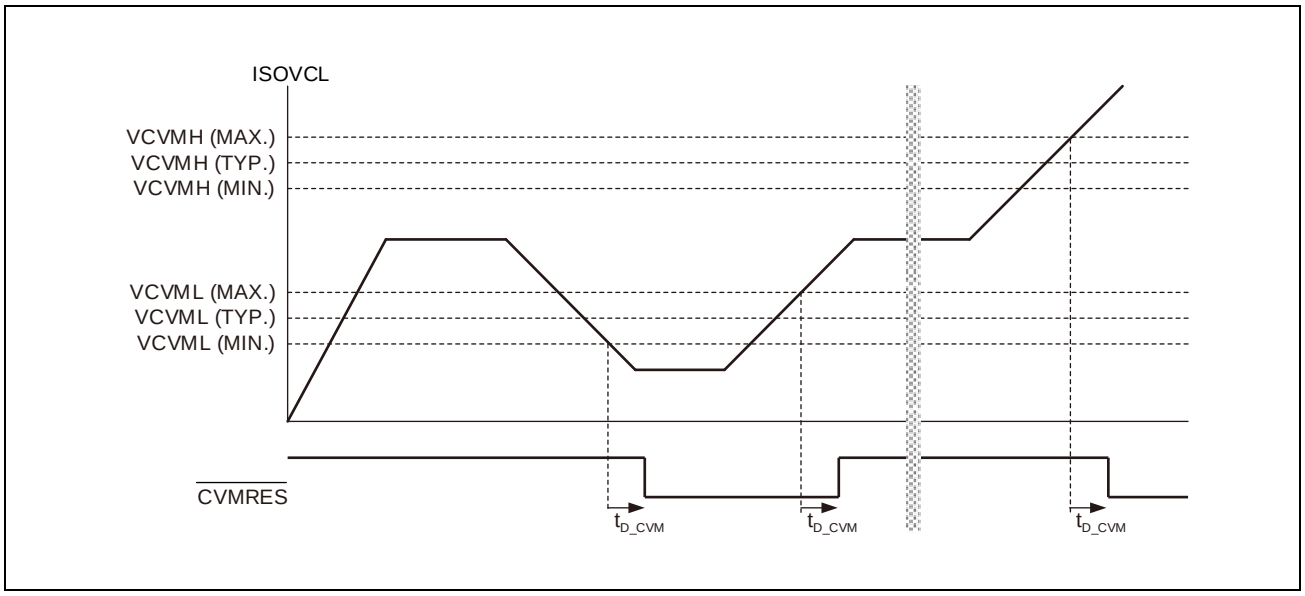
tVS
VVLVI (MAX.)
VVLVI (TYP.)
VVLVI (MIN.)
tW_VLVI
VLVF
VLVF flag clear
tD_VLVI
VLVF flag clear

CVM


ISOVCL
VCVMH (MAX.)
VCVMH (TYP.)
VCVMH (MIN.)
VCVML (MAX.)
VCVML (TYP.)
VCVML (MIN.)
CVMRES
tD_CVM
tD_CVM
tD_CVM

3B.4.5.3 Power Up/Down Timing

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3B.6 In Case the $\overline{\text{RESET}}$ Pin is Used (for Normal Operating Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 hold time (vs $\overline{\text{RESET}}$ ↑)	t_{HMDR}		1			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↓)	t_{SMDF}		0			µs
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms

Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

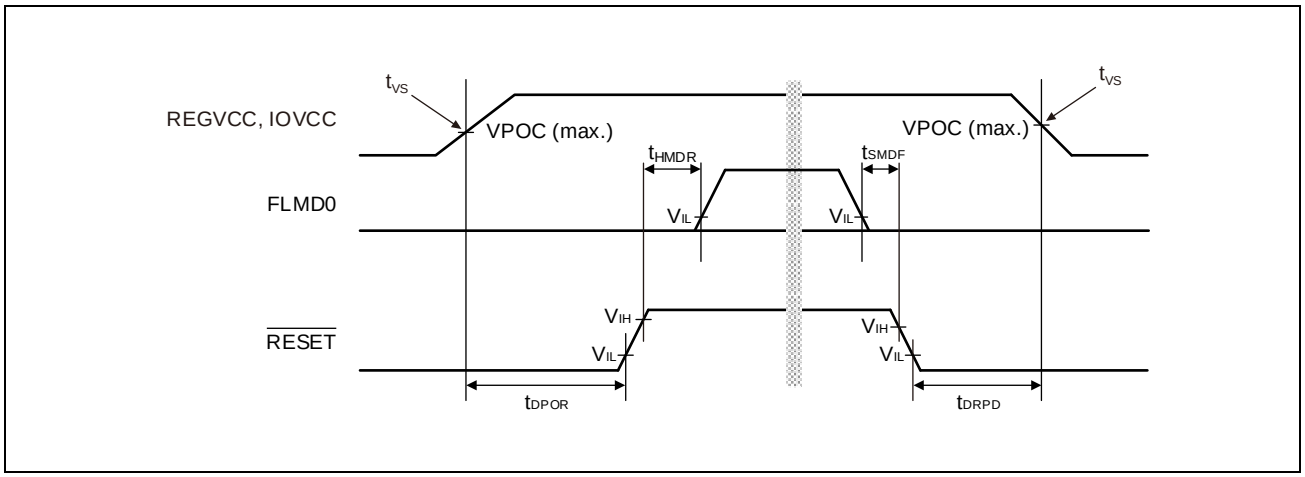


Table 3B.7 In Case the $\overline{\text{RESET}}$ Pin is Used (for Serial Programming Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms

Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

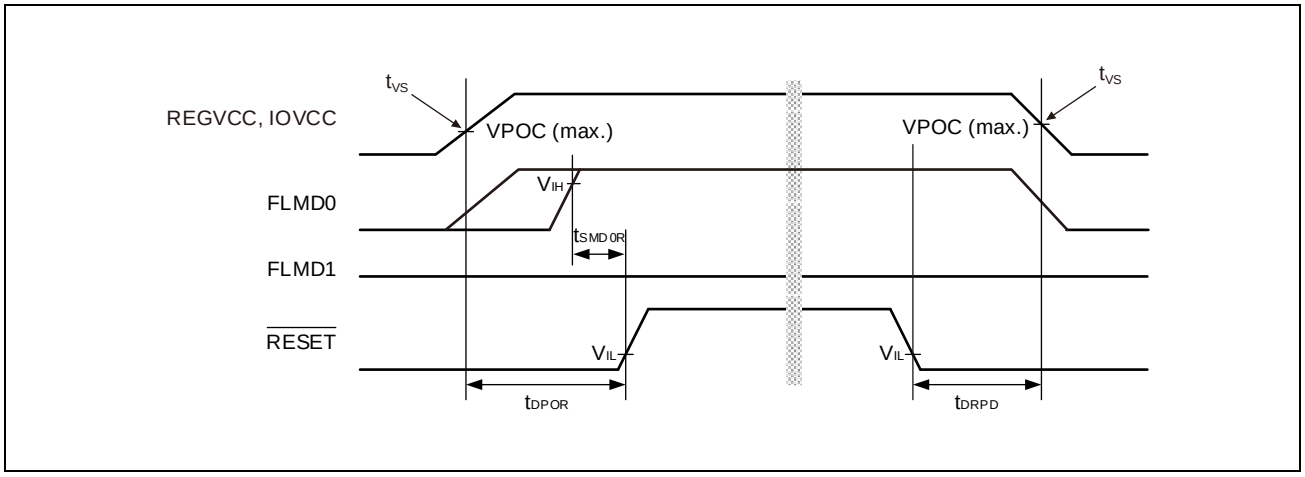


Table 3B.8 In Case the $\overline{\text{RESET}}$ Pin is Used (for Boundary Scan Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
FLMD1,MODE0,MODE1 setup time (vs FLMD0 ↑)	t_{SMD1R}		1			µs
FLMD0 hold time (vs $\overline{\text{RESET}}$ ↓)	t_{HMD0F}		1			µs
FLMD1, MODE0, MODE1, MODE2 hold time (vs FLMD0 ↓)	t_{HMD1F}		1			µs
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms
$\overline{\text{DCUTRST}}$ input delay time (vs $\overline{\text{RESET}}$ ↑)	t_{DRTRST}		1			ms
$\overline{\text{RESET}}$ hold time (vs $\overline{\text{DCUTRST}}$ ↓)	t_{HRTRST}		0			ms

Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

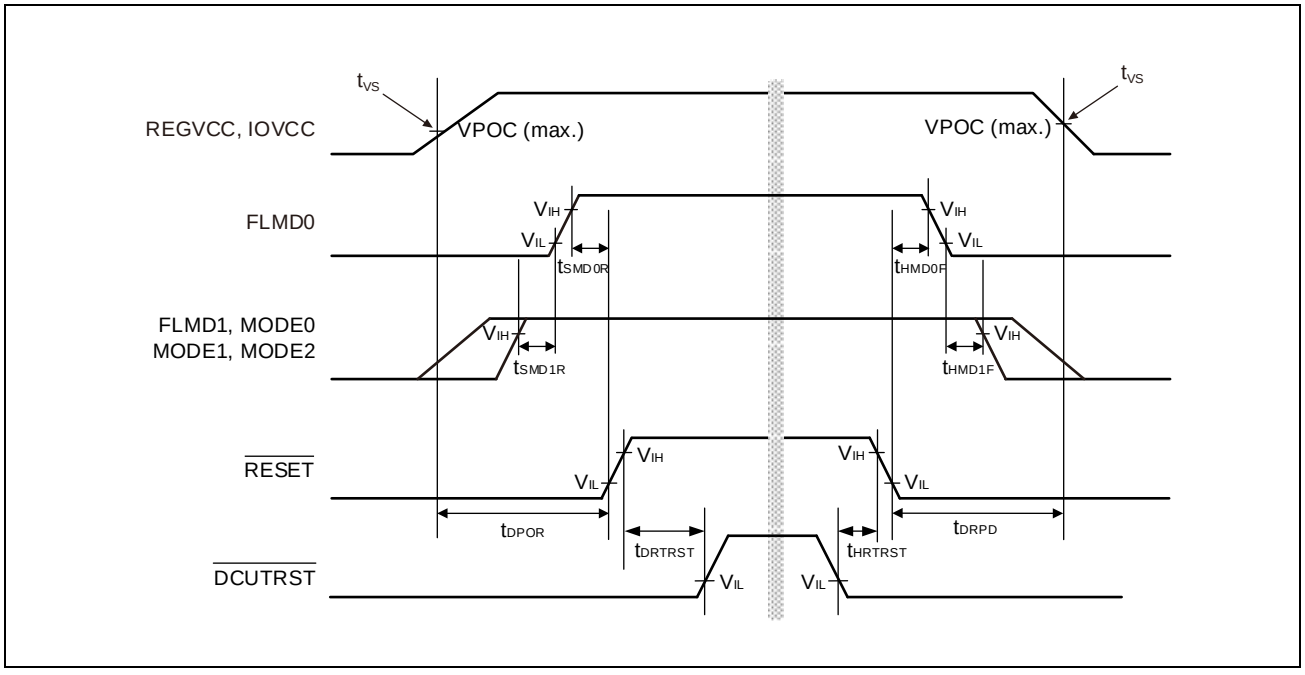


Table 3B.9 In Case the $\overline{\text{RESET}}$ Pin is Used (for User Boot Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
FLMD1, MODE0, MODE1, MODE2 setup time (vs FLMD0 ↑)	t_{SMD1R}		1			µs
FLMD0 hold time (vs $\overline{\text{RESET}}$ ↓)	t_{HMD0F}		1			µs
FLMD1, MODE0, MODE1, MODE2 hold time (vs FLMD0 ↓)	t_{HMD1F}		1			µs
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC ↓ delay time	t_{DRPD}		0			ms

Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

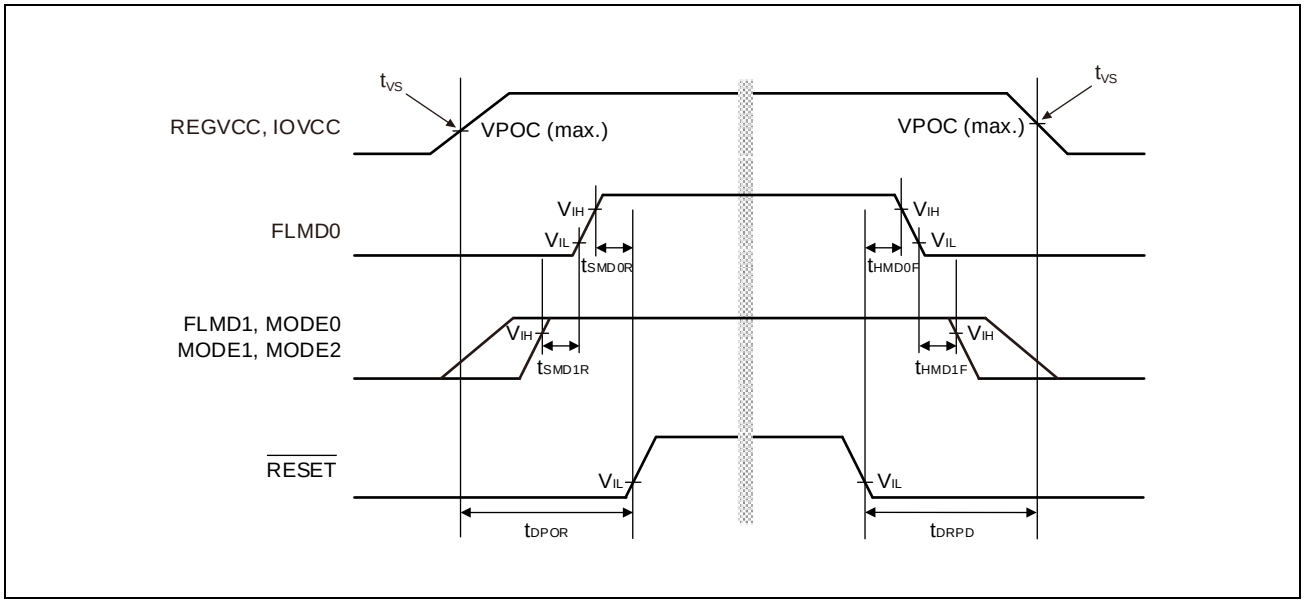
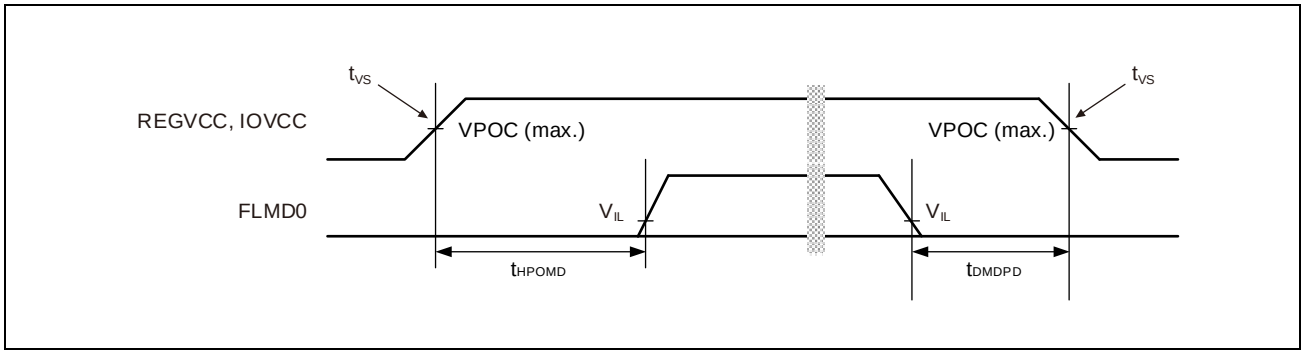


Table 3B.10 In Case the $\overline{\text{RESET}}$ Pin is Not Used and Fixed to High Level by Pull-up*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*2)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*2 ↑ to FLMD0 hold time	t_{HPOMD}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 ↓ to REGVCC ↓ and IOVCC*2 ↓ delay time	t_{DMDPD}		1			µs

Note 1. This operating condition is available only in normal operation mode (include self-programming mode). When the device is used in except normal operation mode, please use the $\overline{\text{RESET}}$ pin.

Note 2. IOVCC means EVCC, BVCC, A0VREF and A1VREF.



3B.4.5.4 CPU Reset Release Timing

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3B.11 In Case the $\overline{\text{RESET}}$ Pin is Not Used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REGVCC ↑ to CPU reset release*1	t_{DPCRR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms			2.58	ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms			8.3	ms

Note 1. This is reference value.

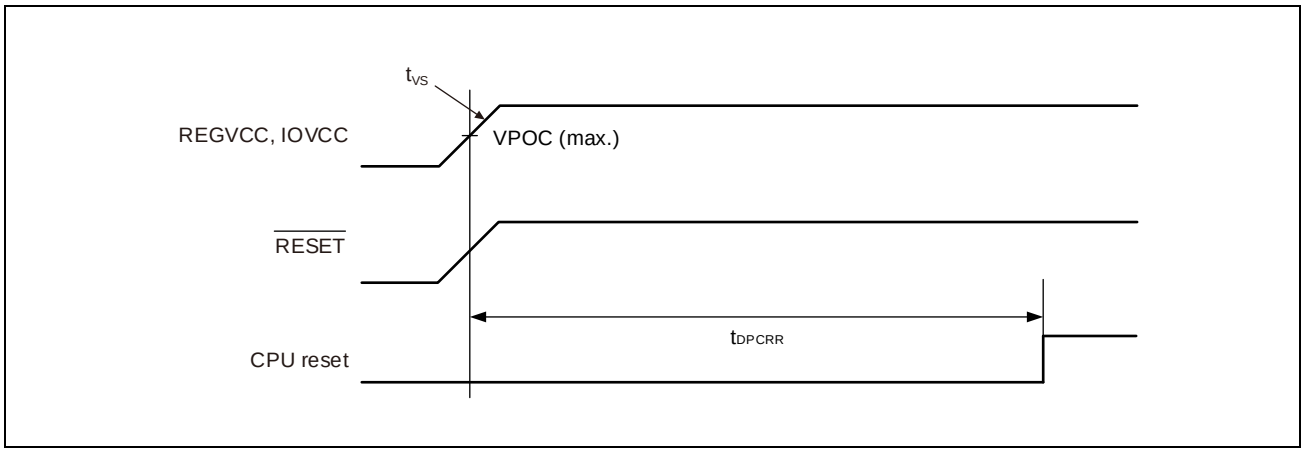
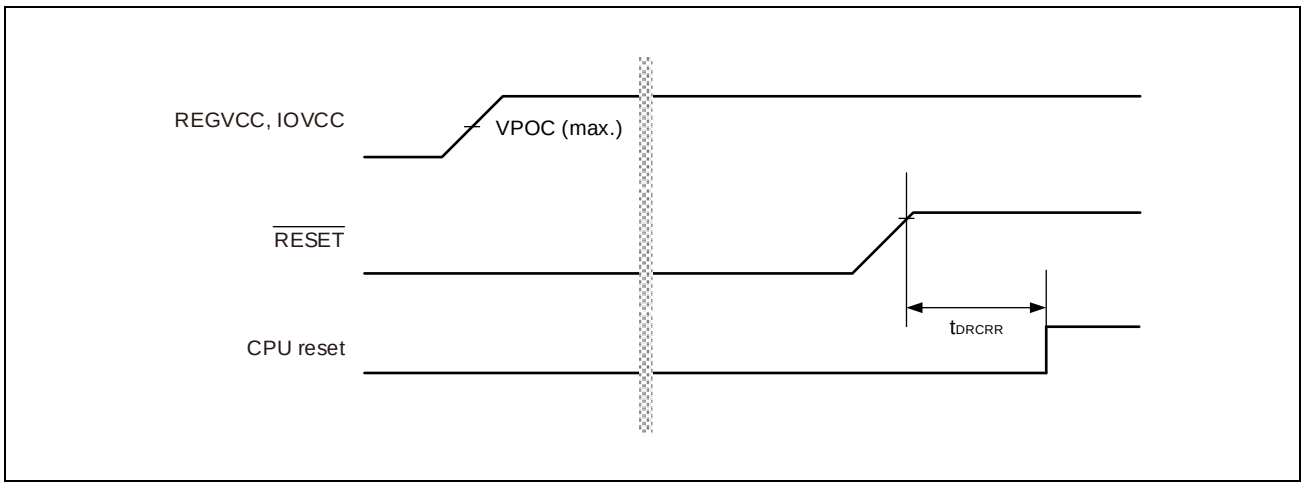


Table 3B.12 In Case the $\overline{\text{RESET}}$ Pin is Used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ ↑ to CPU reset release*1	t_{DRCRR}				32*2	µs

Note 1. This is reference value.

Note 2. In case the time until releasing the $\overline{\text{RESET}}$ pin is longer than t_{DPCRR}.



3B.5 AC Characteristics

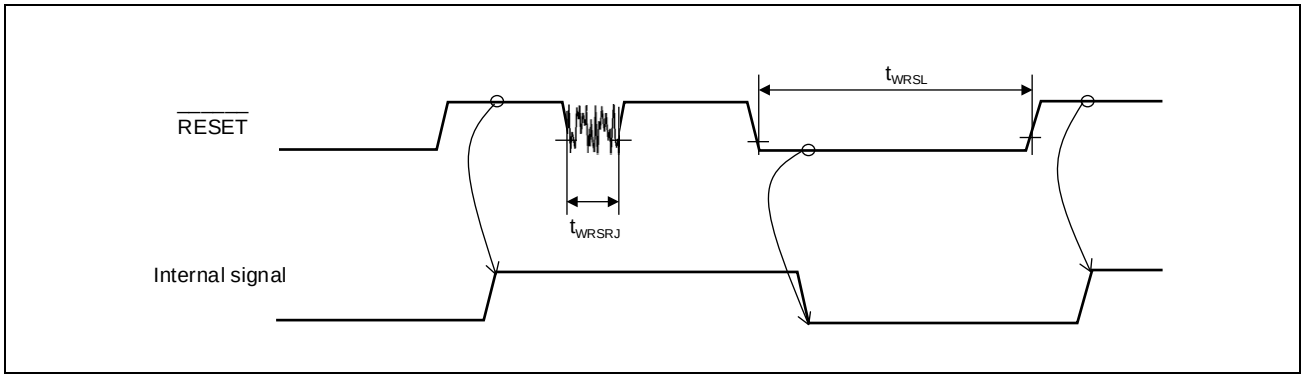
3B.5.1 $\overline{\text{RESET}}$ Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width*1	t_{WRSL}	Except power on	600			ns
$\overline{\text{RESET}}$ pulse rejection*2	t_{WRSRJ}		100			ns

Note 1. $\overline{\text{RESET}}$ input width is needed to ensure that the internal reset signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



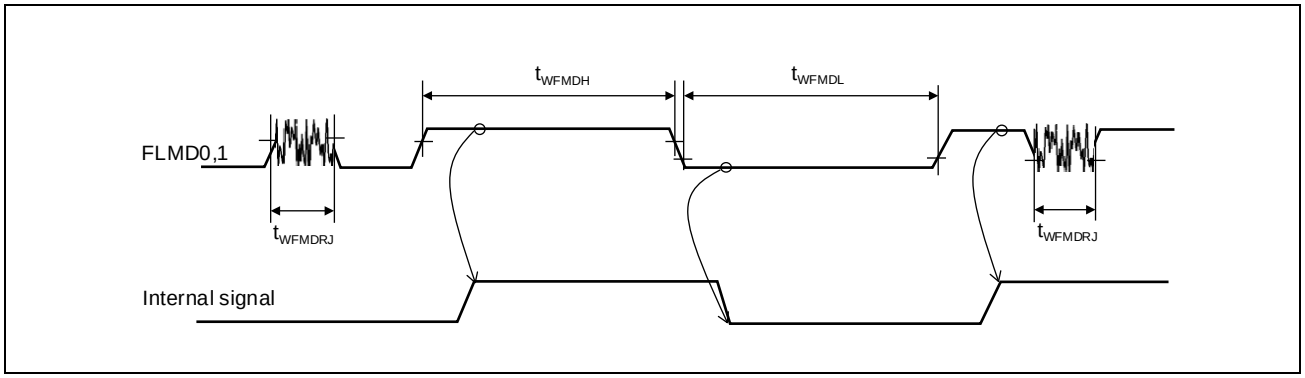
3B.5.2 Mode Timing

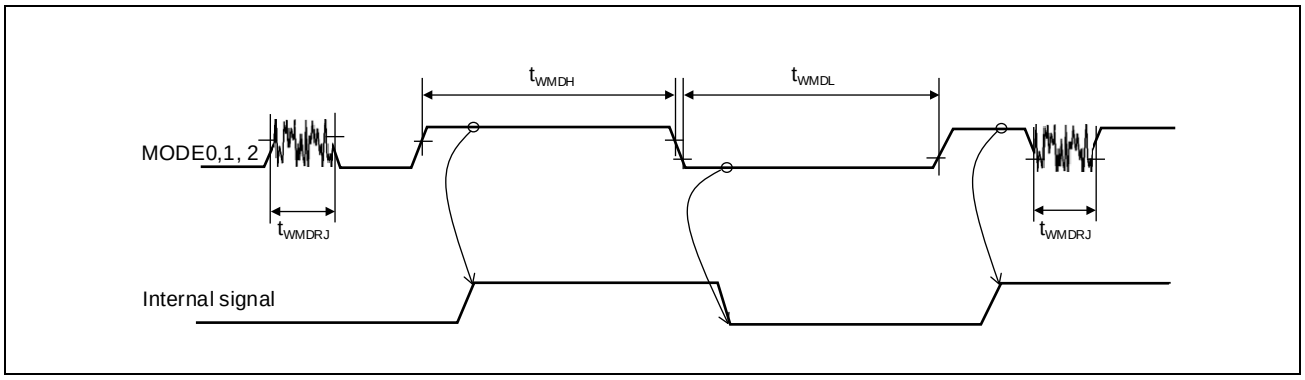
Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0, 1 input high/low level width*1	t_{WFMDH}/ t_{WFMDL}		600			ns
FLMD0, 1 pulse rejection*2	t_{WFMDRJ}		100			ns
MODE0, 1, 2 input high/low level width*1	t_{WMDH}/ t_{WMDL}		600			ns
MODE0, 1, 2 pulse rejection*2	t_{WMDRJ}		100			ns

Note 1. FLMD0, 1 and MODE0, 1, 2 input width is needed to ensure that the internal mode signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.





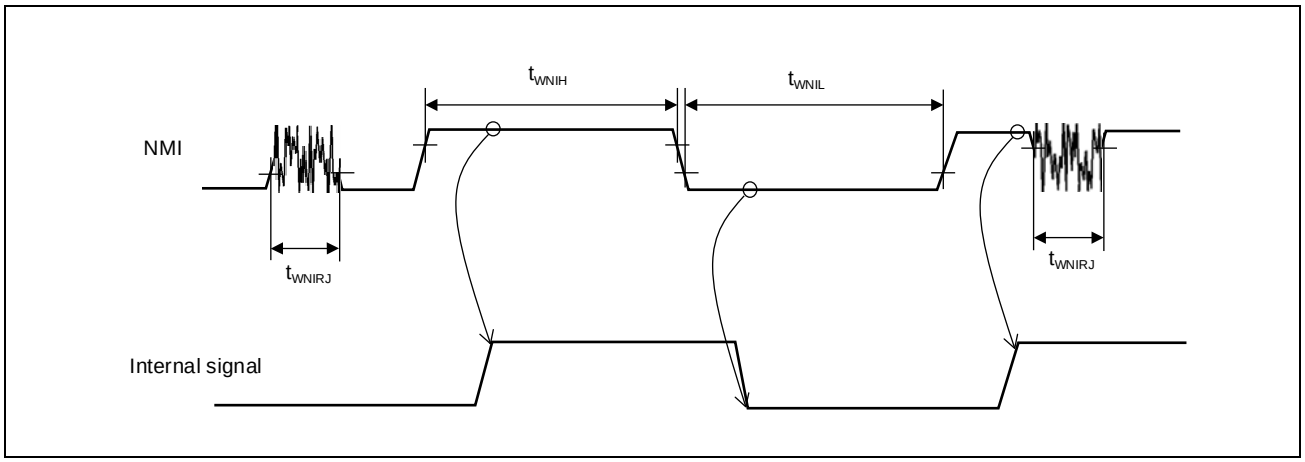
3B.5.3 Interrupt Timing

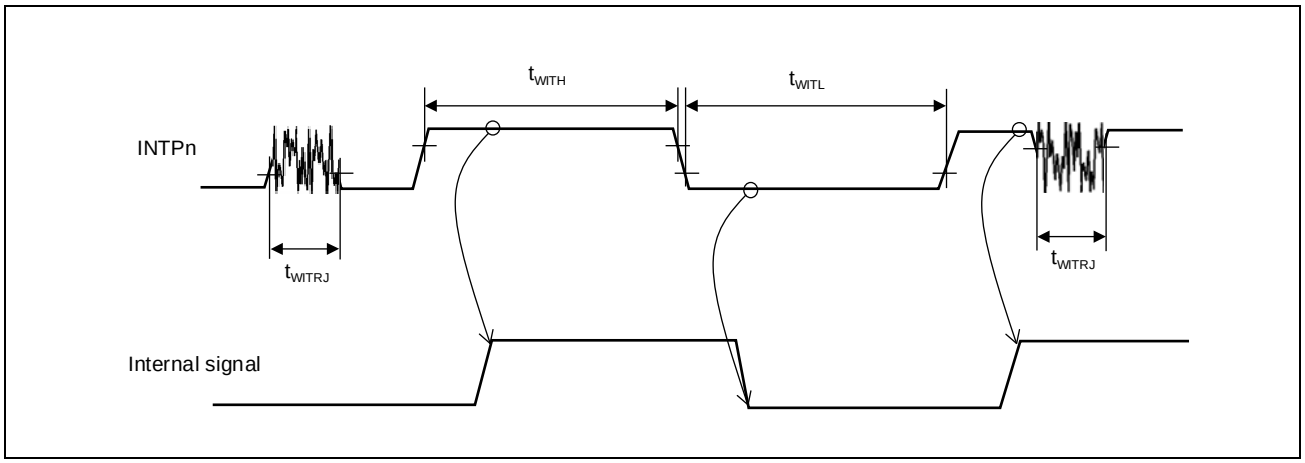
Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high/low level width*1	t_{WNIH}/ t_{WNIL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	24			µs
NMI pulse rejection*2	t_{WNIRJ}		100			ns
INTPn input high/low level width*1	t_{WITH}/ t_{WITL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	24			µs
INTPn pulse rejection*2	t_{WITRJ}		100			ns

Note 1. NMI and INTPn input width is needed to ensure that the internal interrupt signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



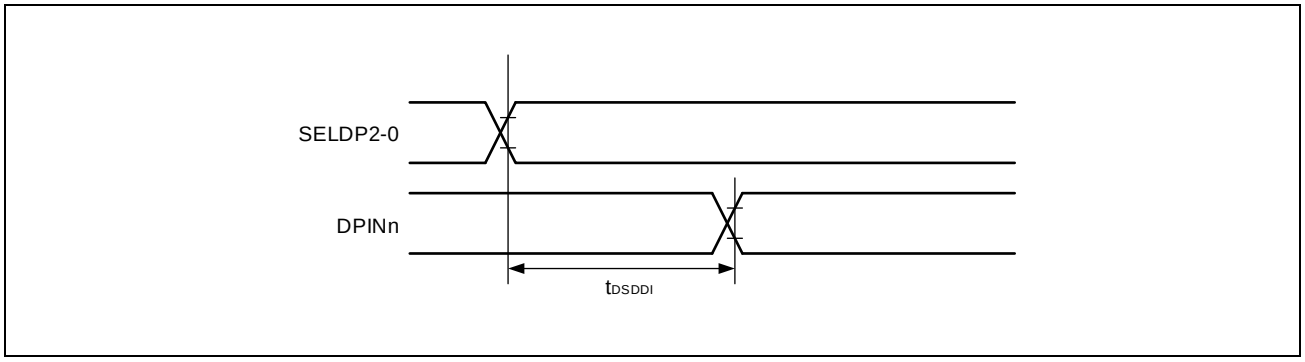


3B.5.4 Low Power Sampler (DPIN input) Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DPINn input delay time (vs SELDP2-0)	t_{DSDDI}				150	ns

Note: n = 7 to 0



3B.5.5 CSCXFOUT Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

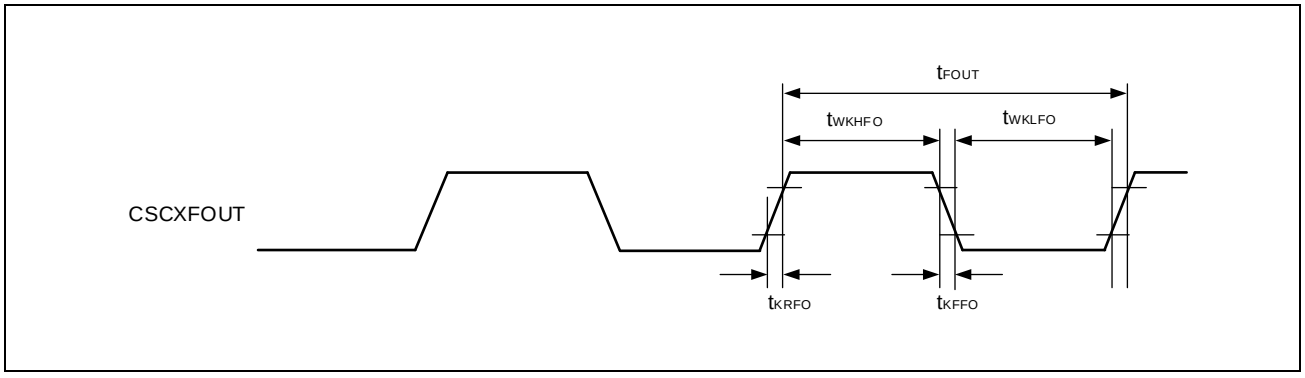
CSCXFOUT: Slow or fast mode (refer to the condition in the following table)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
CSCXFOUT output cycle	t_{FOUT}	Slow mode		100 (max. 10 MHz)			ns
		Fast mode		41.6 (max. 24 MHz)			ns
CSCXFOUT high level width	t_{WKHFO}	Slow mode	N: 1*1 or even value*2	t_{FOUT} / 2 – 37			ns
			N: Odd value (N ≥ 5)*2,*3	t_{FOUT} × (N+1) / 2N – 37			ns
		Fast mode	N: 1*1 or even value*2	t_{FOUT} / 2 – 10			ns
			N: Odd value (N ≥ 3)*2	t_{FOUT} × (N+1) / 2N – 10			ns
CSCXFOUT low level width	t_{WKLFO}	Slow mode	N: 1*1 or even value*2	t_{FOUT} / 2 – 37			ns
			N: Odd value (N ≥ 5)*2,*3	t_{FOUT} × (N–1) / 2N – 37			ns
		Fast mode	N: 1*1 or even value*2	t_{FOUT} / 2 – 10			ns
			N: Odd value (N ≥ 3)*2	t_{FOUT} × (N–1) / 2N – 10			ns
CSCXFOUT rise/ fall time	t_{KRFO}/ t_{KFFO}	Slow mode				37	ns
		Fast mode				10	ns

Note 1. When MainOSC, HS IntOSC, LS IntOSC or SubOSC is selected as source clock with the condition of N=1, the characteristics of output signal depends on the selected source clock. It is recommended to use output signal after evaluation on an actual environment.

Note 2. “N” is the value of “Clock divisor N” defined by FOUTDIV register.

Note 3. The selection of N = 3 is prohibited when slow mode is used.



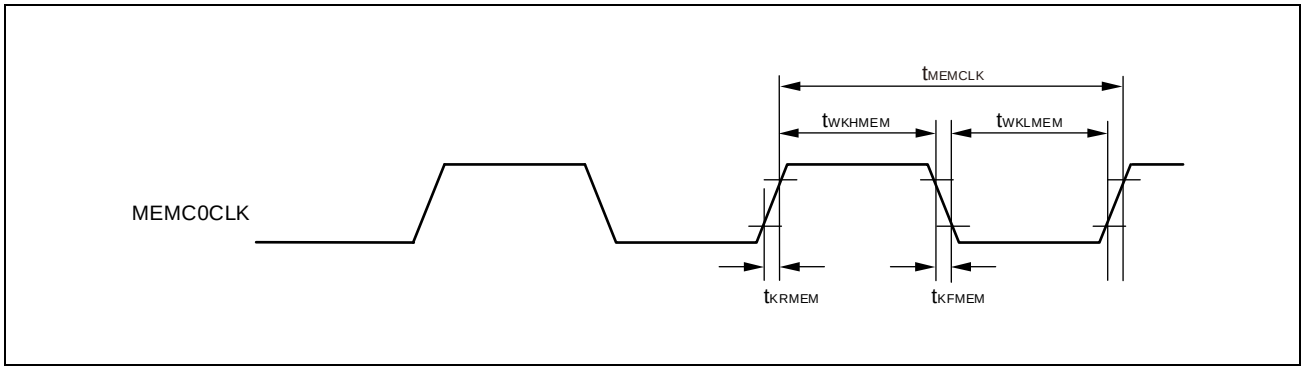
3B.5.6 MEMC0CLK Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

MEMC0CLK pin: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MEMC0CLK output cycle	t_{MEMCLK}		33.4 (max.30 MHz)			ns
MEMC0CLK high / low level width	t_{WKHMEM} / t_{WKLMEM}		t_{MEMCLK} / 2 – 10			ns
MEMC0CLK rise / fall time	t_{KRMEM} / t_{KFMEM}				10	ns



3B.5.7 External Bus Timing

3B.5.7.1 MEMC0CLK Asynchronous

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

MEMC0AD0-15, MEMC0A16-23, $\overline{\text{MEMC0CS3-0}}$, $\overline{\text{MEMC0BEN1-0}}$, $\overline{\text{MEMC0ASTB}}$, $\overline{\text{MEMC0WR}}$, and $\overline{\text{MEMC0RD}}$ pins: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bus operational period	T		33.4 (max.30 MHz)			ns
Address*4 setup time to $\overline{\text{MEMC0ASTB}}$ ↓	t_{SAST}	<1>	(1 + ASW) × T – 15			ns
Address (MEMC0AD15-0) hold time from $\overline{\text{MEMC0ASTB}}$ ↓	t_{HSTA}	<2>	(1 + AHW) × T – 15			ns
Address (MEMC0AD15-0) float delay time from $\overline{\text{MEMC0RD}}$ ↓	t_{FRDA}*8	<3>			9	ns
Address*5 hold time from $\overline{\text{MEMC0RD}}$ ↑	t_{HRDA}	<4>	–1.5			ns
Data (MEMC0AD15-0) input delay time from $\overline{\text{MEMC0RD}}$ ↓	t_{DRDID}	<5>	9		(1 + w) × T – 35	ns
Data (MEMC0AD15-0) input hold time from $\overline{\text{MEMC0RD}}$ ↑	t_{HRDID}	<6>	0			ns
Delay time from $\overline{\text{MEMC0ASTB}}$ ↓ to $\overline{\text{MEMC0RD}}$ ↓	t_{DSTRD}	<7>	(1 + AHW) × T – 15			ns
Delay time from $\overline{\text{MEMC0ASTB}}$ ↓ to $\overline{\text{MEMC0WR}}$ ↓	t_{DSTWR}	<8>	(1 + AHW) × T – 15			ns
$\overline{\text{MEMC0RD}}$, $\overline{\text{MEMC0WR}}$ low level width	t_{WRDST}	<9>	(1 + w) × T – 10			ns
Data (MEMC0AD15-0) output delay time from $\overline{\text{MEMC0WR}}$ ↓	t_{DWROD}	<10>			11	ns
Address*5 hold time from $\overline{\text{MEMC0WR}}$ ↑	t_{HWRA}	<11>	(1 + DHW) × T – 15			ns
Data (MEMC0AD15-0) output setup time to $\overline{\text{MEMC0WR}}$ ↑	t_{SODWR}	<12>	(1 + w) × T – 15			ns
Data (MEMC0AD15-0) output hold time from $\overline{\text{MEMC0WR}}$ ↑	t_{HWROD}	<13>	(1 + DHW) × T – 15			ns
$\overline{\text{MEMC0WAIT}}$ setting delay from $\overline{\text{MEMC0ASTB}}$ ↓	t_{SSTWT1}	<14>			(AHW + DPW) × T – 24	ns
	t_{SSTWT2}	<15> DEW ≥ 1			(AHW + DPW + DEW) × T – 24	ns
$\overline{\text{MEMC0WAIT}}$ hold time from $\overline{\text{MEMC0ASTB}}$ ↓	t_{HSTWT1}	<16>	(AHW + DPW + DEW – 1) × T – 9			ns
	t_{HSTWT2}	<17> DEW ≥ 1	(AHW + DPW + DEW) × T – 9			ns

Note 1. ASW means the number of address setup wait for multiplex bus.

Note 2. AHW means the number of address hold wait for multiplex bus.

Note 3. DPW means the number of programmable data wait for multiplex bus.
DEW means the number of external data wait for multiplex bus.
"w" means the sum of DPW and DEW.

Note 4. t_{CPUCLK}: CPU clock period.

Note 5. DHW means the number of data hold wait for multiplex bus.

Note 6. Address means MEMC0AD15-0, MEMC0A23-16, $\overline{\text{MEMC0CS3-0}}$, and $\overline{\text{MEMC0BEN1-0}}$.
272-pin product supports 24-bit address. 233/176-pin products support 23-bit address.

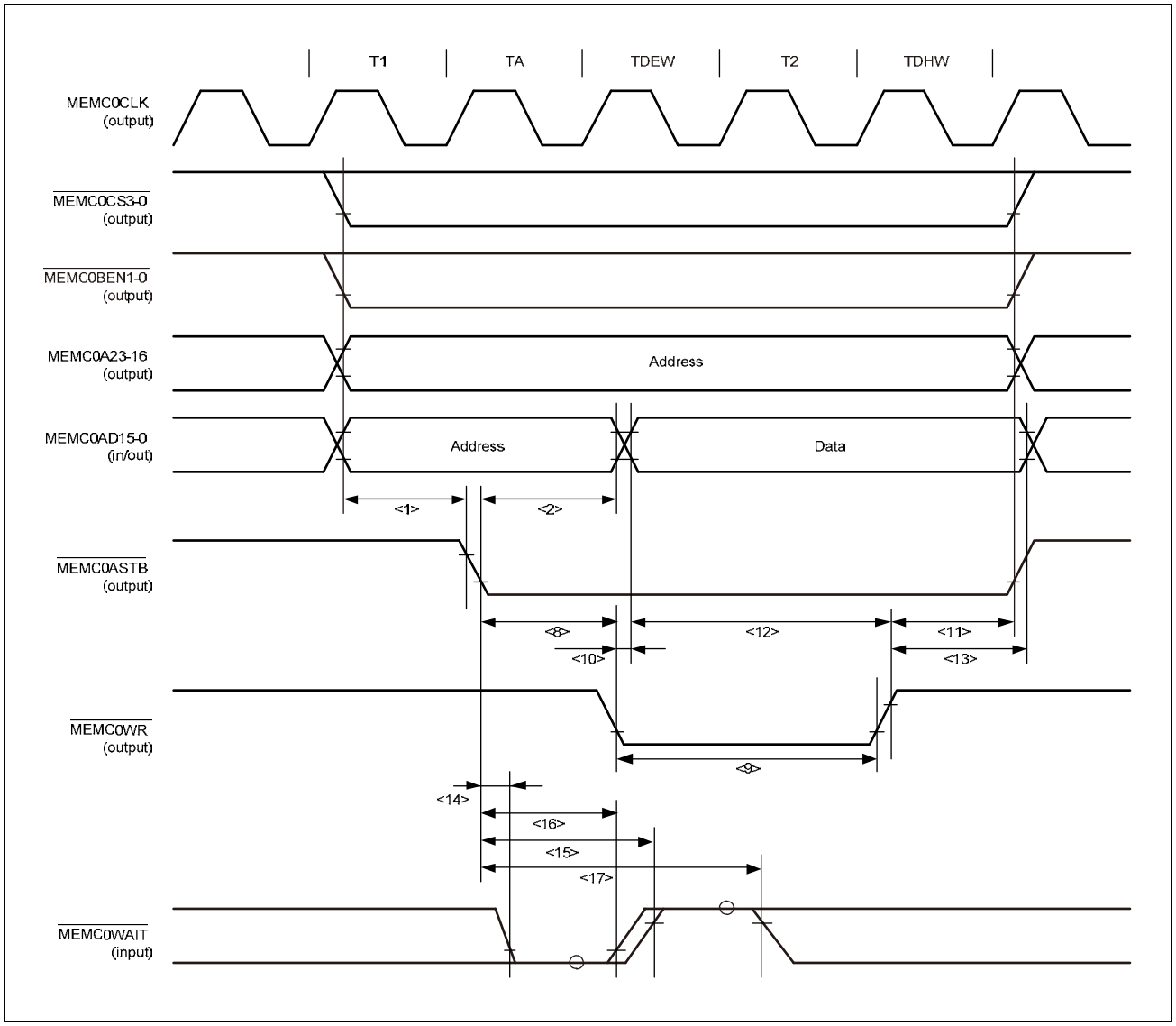
Note 7. Address means MEMC0A23-16, $\overline{\text{MEMC0CS3-0}}$, $\overline{\text{MEMC0BEN1-0}}$, and $\overline{\text{MEMC0ASTB}}$.
272-pin product supports 24-bit address. 233/176-pin products support 23-bit address.

Note 8. t_{FRDA} means the period from output off to Hi-z for MEMC0AD15-0.

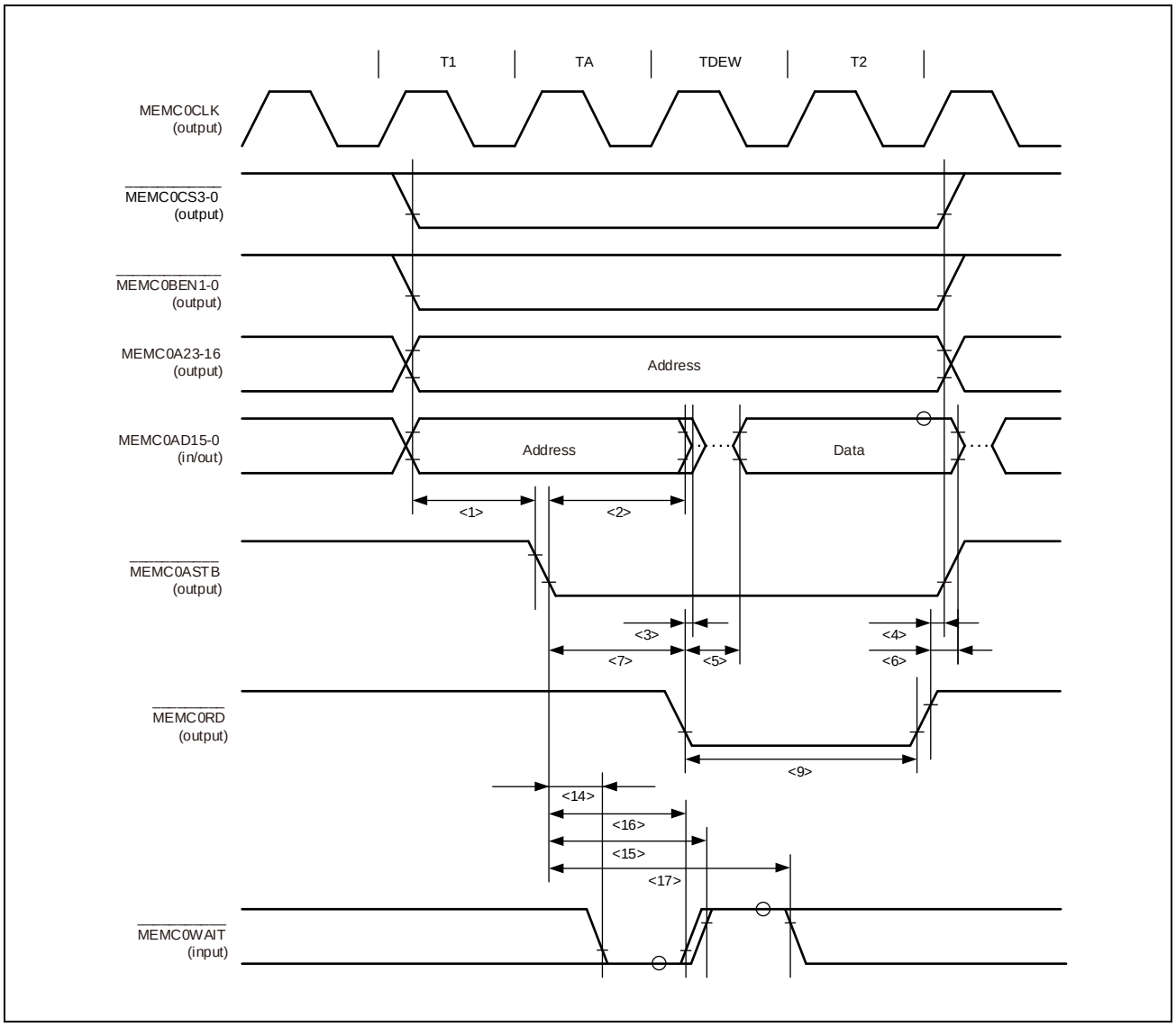
NOTE

When the bus period (T) is shorter than 44 ns, t_{DRDID} spec requires at least 1data wait. (w = 1)

(1) Multiplex Write Cycle (Asynchronous; 1 Data Wait)



(2) Multiplex Read Cycle (Asynchronous; 1 Data Wait)



3B.5.7.2 MEMC0CLK Synchronous

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

MEMC0AD0-15, MEMC0A16-23, $\overline{\text{MEMC0CS3-0}}$, $\overline{\text{MEMC0BEN1-0}}$, $\overline{\text{MEMC0ASTB}}$, $\overline{\text{MEMC0WR}}$, and $\overline{\text{MEMC0RD}}$ pins: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bus operational period	T		33.4 (max.30MHz)			ns
Delay time from MEMC0CLK ↑ to address*1	t_{DKA}	<18>	–0.5		15	ns
Delay time from MEMC0CLK ↑ to address (MEMC0AD15-0) float	t_{FKA}*2	<19>	0		12	ns
Delay time from MEMC0CLK ↑ to $\overline{\text{MEMC0ASTB}}$	t_{DKST}	<20>	0		11	ns
Delay time from MEMC0CLK ↑ to $\overline{\text{MEMC0RD}}$ and $\overline{\text{MEMC0WR}}$	t_{DKRDWR}	<21>	–2.5		6	ns
Data (MEMC0AD15-0) input setup time (from MEMC0CLK ↑)	t_{SIDK}	<22>	29			ns
Data (MEMC0AD15-0) input hold time (from MEMC0CLK ↑)	t_{HKID}	<23>	2.5			ns
Data (MEMC0AD15-0) output delay time (from MEMC0CLK ↑)	t_{DKOD}	<24>			15	ns
$\overline{\text{MEMC0WAIT}}$ setup time (to MEMC0CLK ↑)	t_{SWTK}	<25>	T + 22			ns
$\overline{\text{MEMC0WAIT}}$ hold time (from MEMC0CLK ↑)	t_{HKWT}	<26>	–T – 5			ns

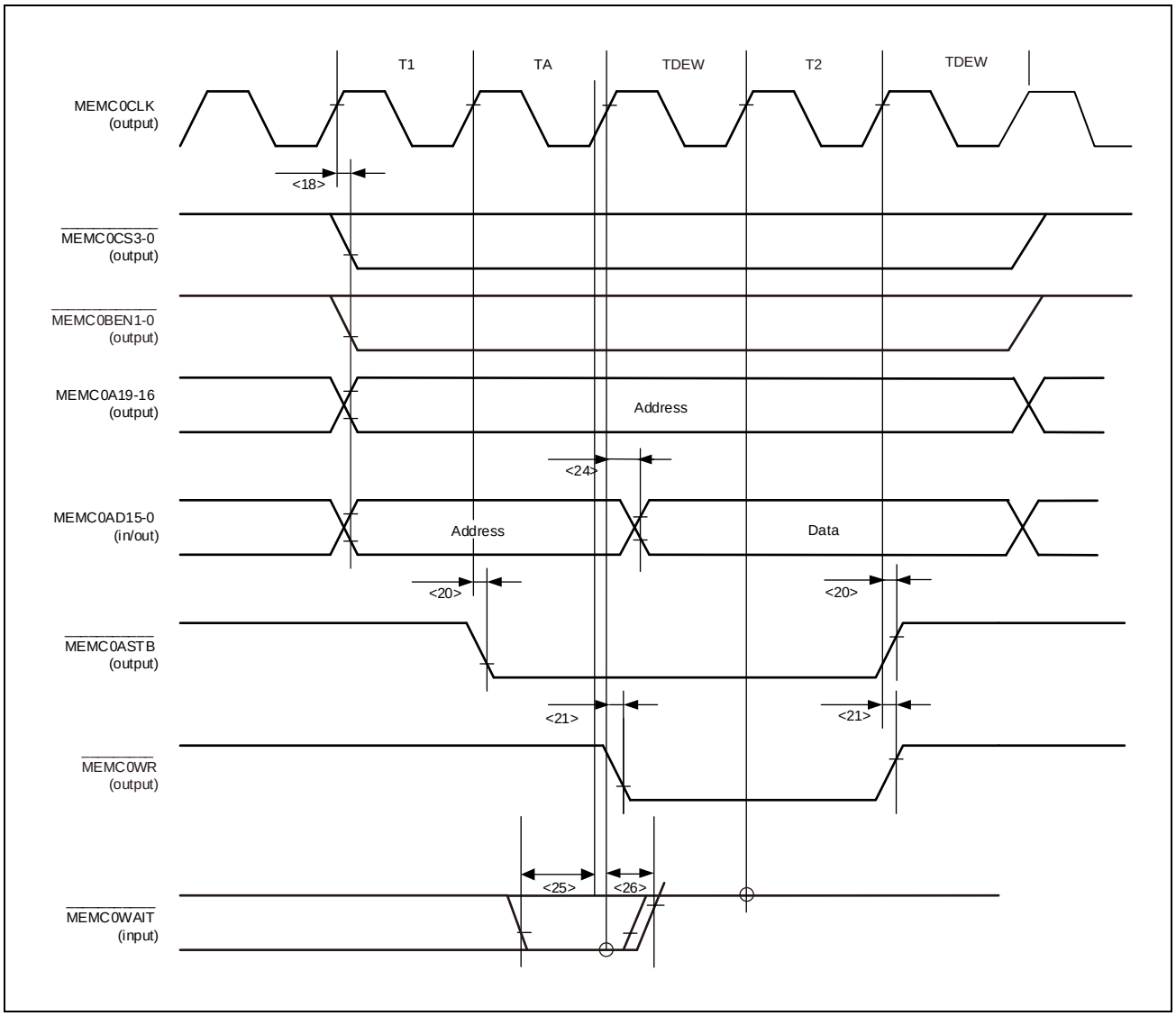
Note 1. Address means MEMC0AD15-0, MEMC0A23-16, $\overline{\text{MEMC0CS3-0}}$ and $\overline{\text{MEMC0BEN1-0}}$. 272-pin product supports 24-bit address. 233/176-pin products support 23-bit address.

Note 2. t_{FKA} means the period from output off to Hi-z for MEMC0AD15-0.

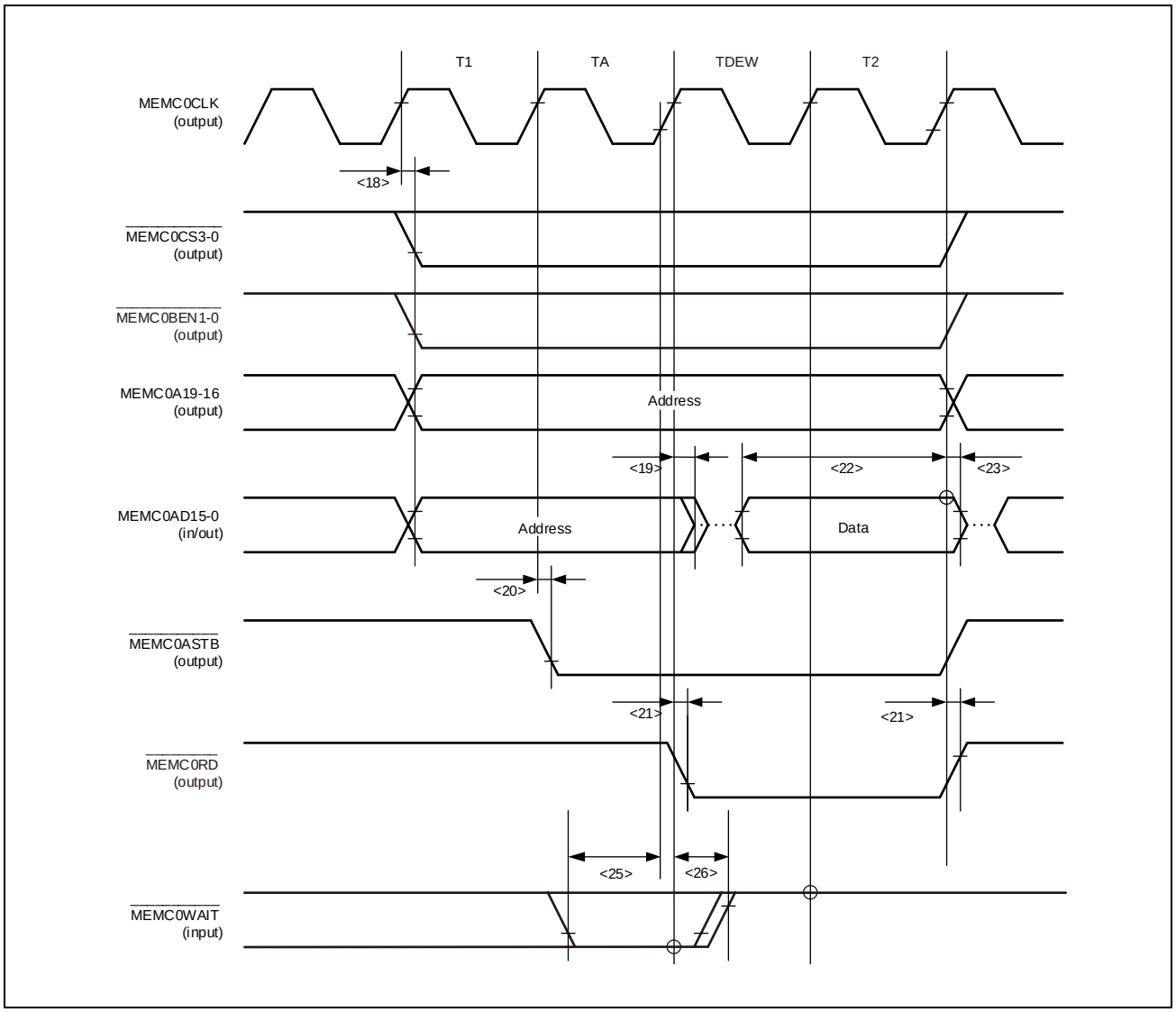
NOTE

When the bus period (T) is shorter than 44 ns, t_{DRDID} spec requires at least 1data wait. (w = 1)

(1) Multiplex Write Cycle (Synchronous; 1 Data Wait)



(2) Multiplex Read Cycle (Synchronous; 1 Data Wait)



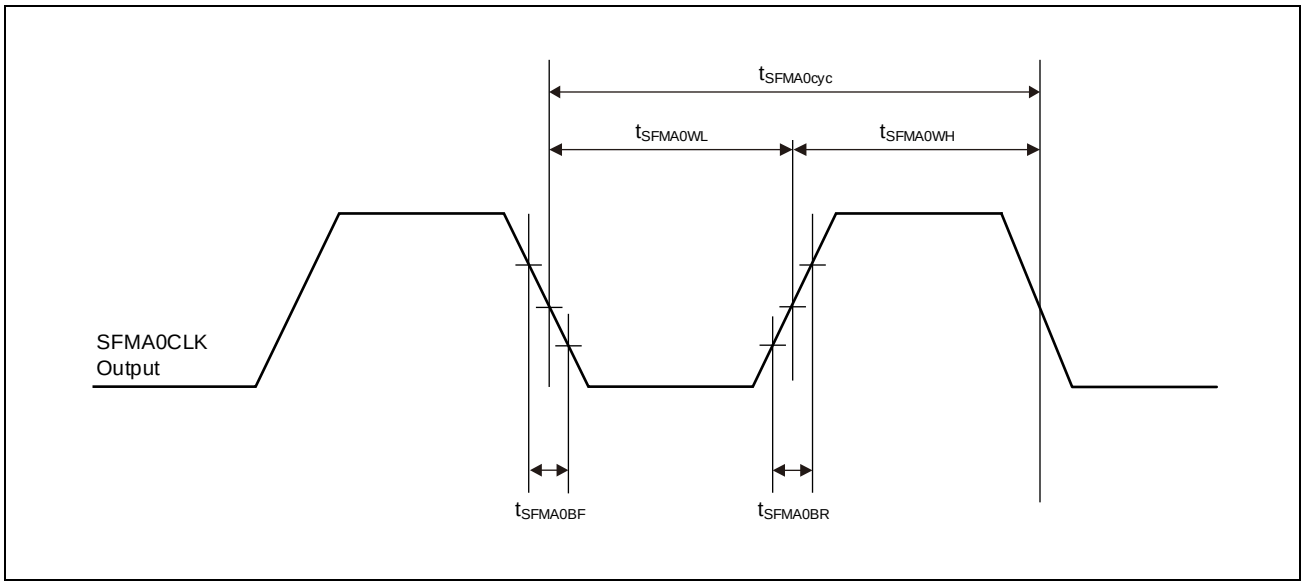
3B.5.8 SFMA Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to 3.6 V, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

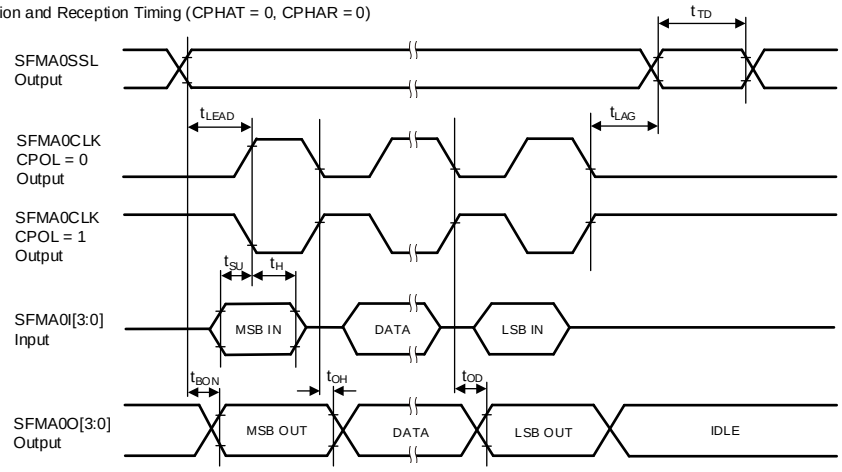
<Output driver strength>

SFMA0CLK, SFMA0SSL, and SFMA0O[3:0] pins: Fast mode

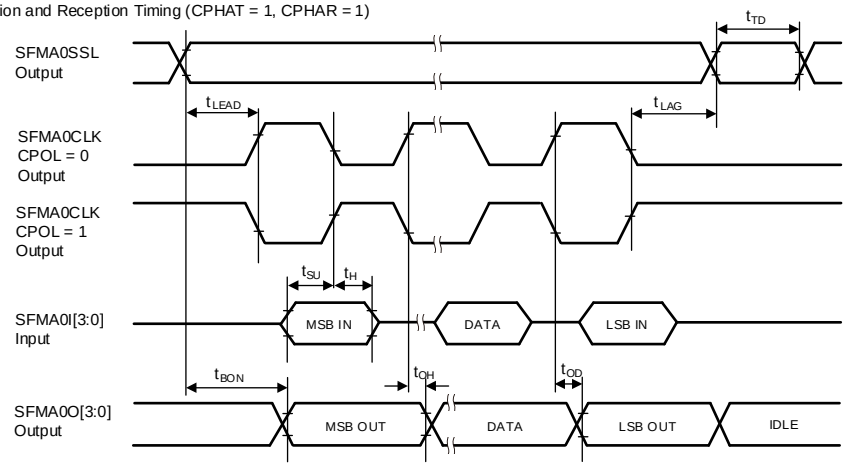
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SFMA0CLK clock cycle	$t_{SFMA0cyc}$		25			ns
SFMA0CLK high pulse width	$t_{SFMA0WH}$		0.4 × $t_{SFMA0cyc}$		0.6 × $t_{SFMA0cyc}$	ns
SFMA0CLK low pulse width	$t_{SFMA0WL}$		0.4 × $t_{SFMA0cyc}$		0.6 × $t_{SFMA0cyc}$	ns
SFMA0CLK rise time	t_{SFMA0R}				4.5	ns
SFMA0CLK fall time	t_{SFMA0F}				4.5	ns
Data input setup time	t_{SU}		13.0			ns
Data input hold time	t_{H}		0.0			ns
SFMA0SSL setup time	t_{LEAD}		1 × $t_{SFMA0cyc}$ – 5		8 × $t_{SFMA0cyc}$	ns
SFMA0SSL hold time	t_{LAG}		1.5 × $t_{SFMA0cyc}$		8.5 × $t_{SFMA0cyc}$ + 5	ns
Continuous transfer delay time	t_{TD}		1 × $t_{SFMA0cyc}$		8 × $t_{SFMA0cyc}$	ns
Data output delay time	t_{OD}				3.6	ns
Data output hold time	t_{OH}		–1.6			ns
Data output buffer on time	t_{BON}				3.6	ns
Data output buffer off time	t_{BOFF}		–7.0		0	ns

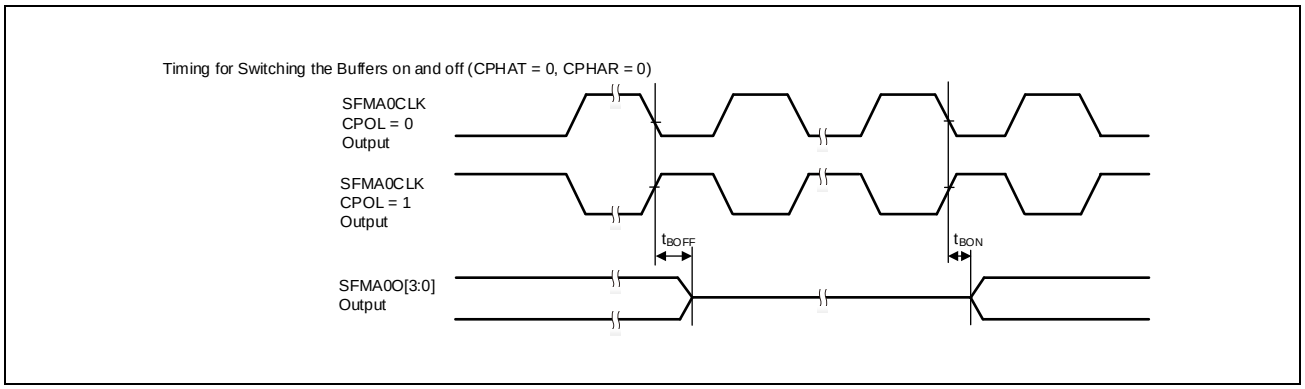


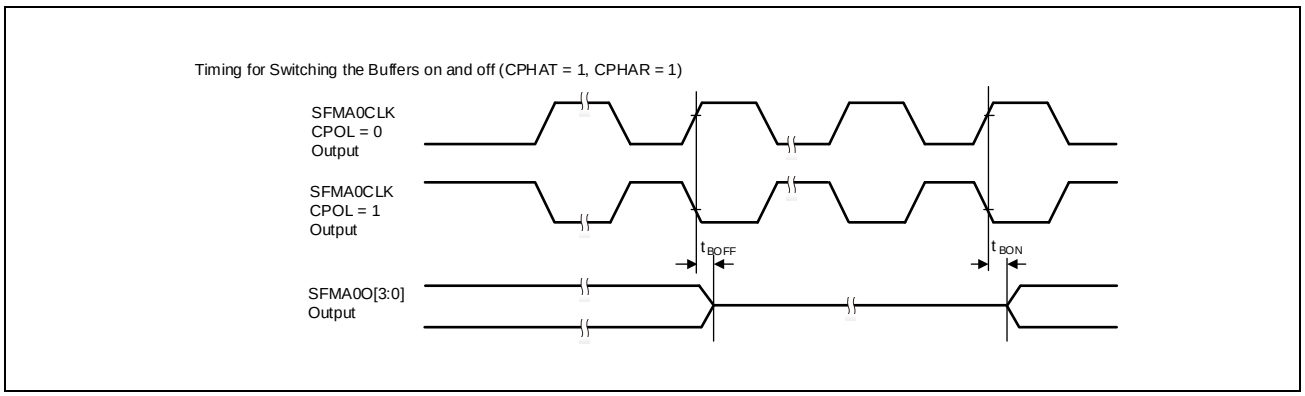
Transmission and Reception Timing (CPHAT = 0, CPHAR = 0)



Transmission and Reception Timing (CPHAT = 1, CPHAR = 1)







3B.5.9 **Reserved**

3B.5.10 CSI Timing

3B.5.10.1 CSIG Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3B.13 CSIG Timing (Master Mode)

<Output driver strength>

CSIGnSO, CSIGnSC (output): Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYMGn}		100			ns
CSIGnSC high level width	t_{KWHMGn}		0.5 × t_{KCYMGn} – 10			ns
CSIGnSC low level width	t_{KWLMGn}		0.5 × t_{KCYMGn} – 10			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSIMGn}		30			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSIMGn}		0			ns
CSIGnSO output delay (vs. CSIGnSC)	t_{DSOMGn}				7	ns
CSIGnRYI setup time (vs. CSIGnSC)	t_{SRYIGn}	CSIGnCTL1.CSIGnSIT = x CSIGnCTL1.CSIGnHSE = 1	2 × t_{KCYGn} + 25			ns
CSIGnRYI high level width	t_{WRYIGn}	CSIGnCTL1.CSIGnHSE = 1	t_{KCYGn} + 5			ns

Note: n = 0 to 3

Table 3B.14 CSIG Timing (Slave Mode)

<Output driver strength>

CSIGnSO: Fast mode

CSIGnRYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYSGn}		200			ns
CSIGnSC high level width	t_{KWHSGn}		0.5 × t_{KCYSGn} – 10			ns
CSIGnSC low level width	t_{KWLSGn}		0.5 × t_{KCYSGn} – 10			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSISGn}		20			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSISGn}		t_{KCYGn} + 5			ns
CSIGnSO output delay (vs. CSIGnSC)	t_{DSOSGn}				30	ns
CSIGnRYO output delay	t_{SRYOGn}				38	ns
$\overline{\text{CSIGnSSI}}$ setup time (vs. CSIGnSC)	$t_{SSSISGn}$		0.5 × t_{KCYSGn} – 5			ns
$\overline{\text{CSIGnSSI}}$ hold time (vs. CSIGnSC)	$t_{HSSISGn}$		t_{KCYGn} + 5			ns

Note: n = 0 to 3

3B.5.10.2 CSIH Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3B.15 CSIH Timing (Master Mode: 10 Mbps)

<Output driver strength>

CSIHnSO, CSIHnSC (output): Fast mode (CL = 100pF@n=0 / 50pF@n=1-3)

CSIHnCSSx: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYMHn}		100			ns
CSIHnSC high level width	t_{KWHMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSC low level width	t_{KWLMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSIMHn}	SI positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	19			ns
		SI negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	14			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSIMHn}	SI positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	0			ns
		SI negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	t_{KCYHn}/2			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOMHn}				7	ns
CSIHnRYI setup time (vs. CSIHnSC)	t_{SRYIHn}	CSIHnCTL1.CSIHnSIT = x CSIHnCTL1.CSIHnHSE = 1	2 × t_{KCYHn} + 25			ns
CSIHnRYI high level width	t_{WRYIHn}	CSIHnCTL1.CSIHnHSE = 1	t_{KCYHn} + 5			ns
CSIHnCSS0-7 inactive width	$t_{WSCSBHn}$		CSIDLE × t_{KCYMHn} – 15			ns
CSIHnCSS0-7 setup time (vs. CSIHnSC)	$t_{SSCSBHn0}$	CSIHnCFGx.CSIHnDAP = 0	CSSETUP × t_{KCYMHn} – 23			ns
	$t_{SSCSBHn1}$	CSIHnCFGx.CSIHnDAP = 1	(CSSETUP + 0.5) × t_{KCYMHn} – 23			ns
CSIHnCSS0-7 hold time (vs. CSIHnSC)	$t_{HSCSBHn0}$	CSIHnCTL1.CSIHnSIT = 0	CSSHOLD × t_{KCYMHn} – 5			ns
	$t_{HSCSBHn1}$	CSIHnCTL1.CSIHnSIT = 1	(CSSHOLD + 0.5) × t_{KCYMHn} – 5			ns

Note: n = 0 to 3

NOTE

CSIDLE: Setting value of CSIHnCFGx.CSIHnIDx[2:0]
CSSETUP: Setting value of CSIHnCFGx.CSIHnSPx[3:0]
CSSHOLD: Setting value of CSIHnCFGx.CSIHnHDx[3:0]
x: Depends on number of the chip select signals.

CAUTION

When the serial clock level is changed during the communication (CSIHnCFGx.CSIHnCKPx) and the IDLE has a setting of 0.5 transmission clock cycles, an inactive width time $t_{WSCSBHn}$ of "0.5 × t_{KCYMHn}" is added.

Table 3B.16 CSIH Timing (Slave Mode: 5 Mbps)

<Output driver strength>
CSIHnSO: Fast mode
CSIHnRYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYSHn}		200			ns
CSIHnSC high level width	t_{KWHSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSC low level width	t_{KWLSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSISHn}		20			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSISHn}		$t_{KCYHn} + 5$			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOSHn}				30	ns
CSIHnRYO output delay	t_{SRYOHn}	$t_{KCYSHn} \geq 8 \times t_{KCYHn}$			38	ns
		$t_{KCYSHn} < 8 \times t_{KCYHn}$			$38 + t_{KCYHn}$	ns
$\overline{\text{CSIHnSSI}}$ setup time (vs. CSIHnSC)	$t_{SSSISHn}$		$0.5 \times t_{KCYSHn} - 5$			ns
$\overline{\text{CSIHnSSI}}$ hold time (vs. CSIHnSC)	$t_{HSSISHn}$		$t_{KCYHn} + 5$			ns

Note: n = 0 to 3

Table 3B.17 CSIH Timing (Slave Mode: 8 Mbps)

<Output driver strength>
CSIHnSO: Fast mode
CSIHnRYO: Slow mode

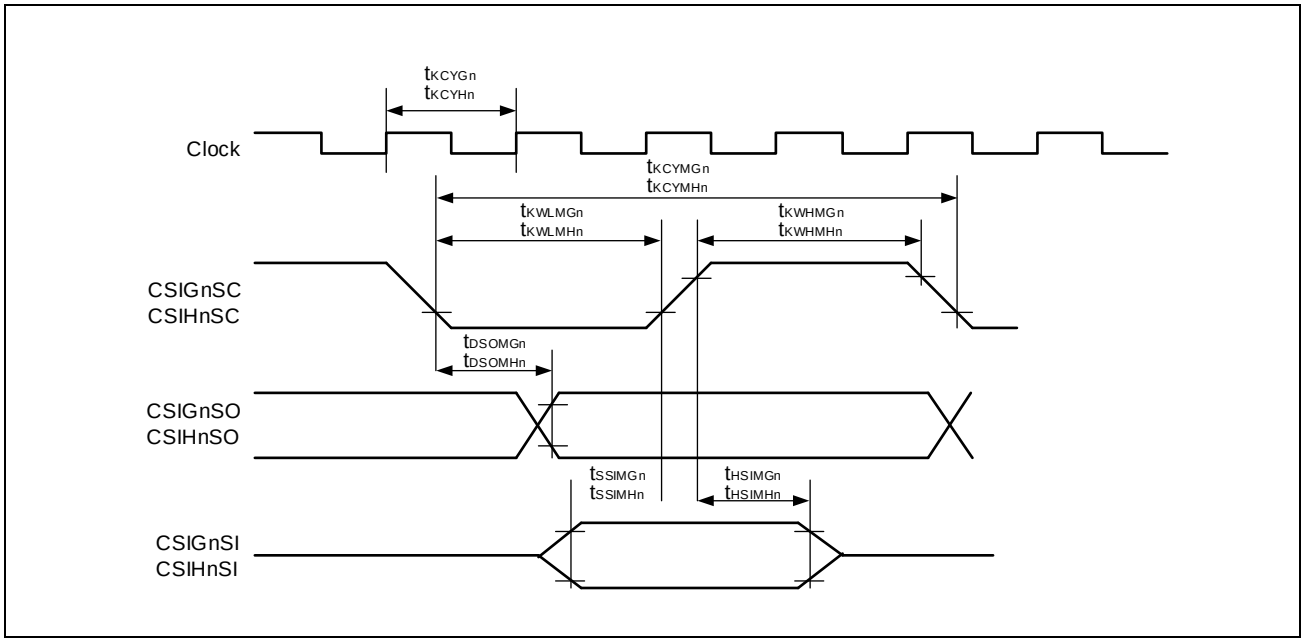
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYSHn}		125			ns
CSIHnSC high level width	t_{KWHSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSC low level width	t_{KWLSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSISHn}		12.5			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSISHn}		$t_{KCYHn} + 5$			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOSHn}				25	ns
CSIHnRYO output delay	t_{SRYOHn}	$t_{KCYSHn} \geq 8 \times t_{KCYHn}$			27	ns
		$t_{KCYSHn} < 8 \times t_{KCYHn}$			$27 + t_{KCYHn}$	ns
$\overline{\text{CSIHnSSI}}$ setup time (vs. CSIHnSC)	$t_{SSSISHn}$		$0.5 \times t_{KCYSHn} - 5$			ns
$\overline{\text{CSIHnSSI}}$ hold time (vs. CSIHnSC)	$t_{HSSISHn}$		$t_{KCYHn} + 5$			ns

Note: n = 2 (Only for CSIH2)

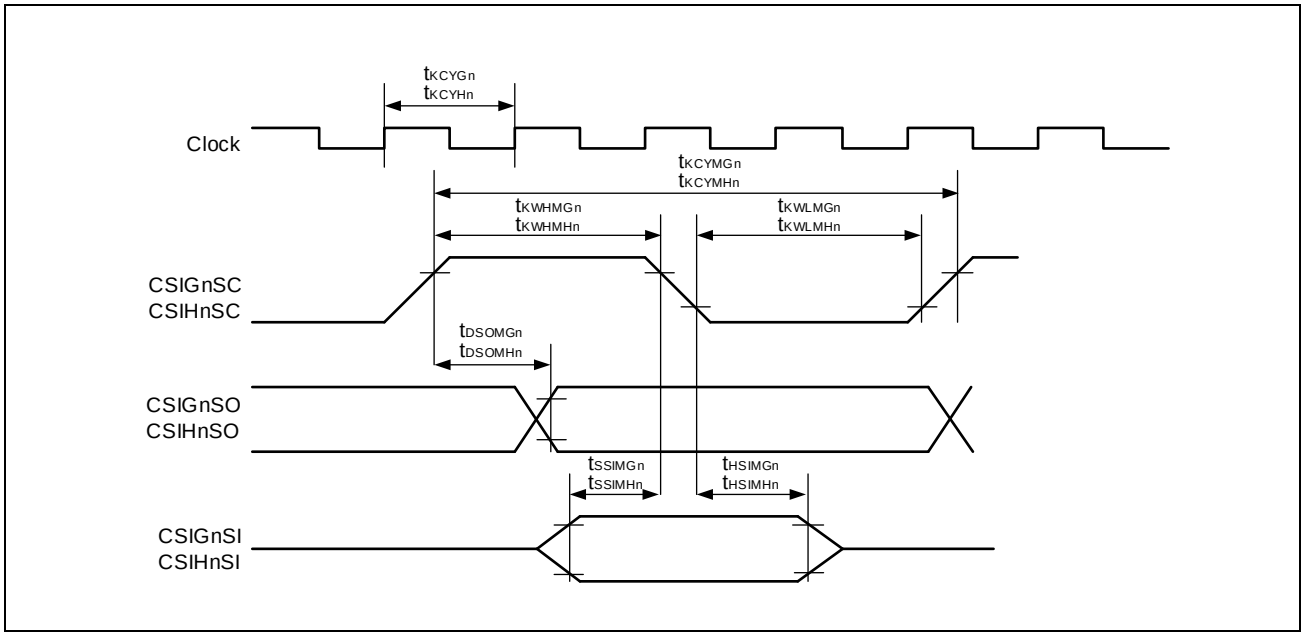
(1) SC/SI/SO

Master mode:

- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0 or 1/1)



- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0 or 0/1)



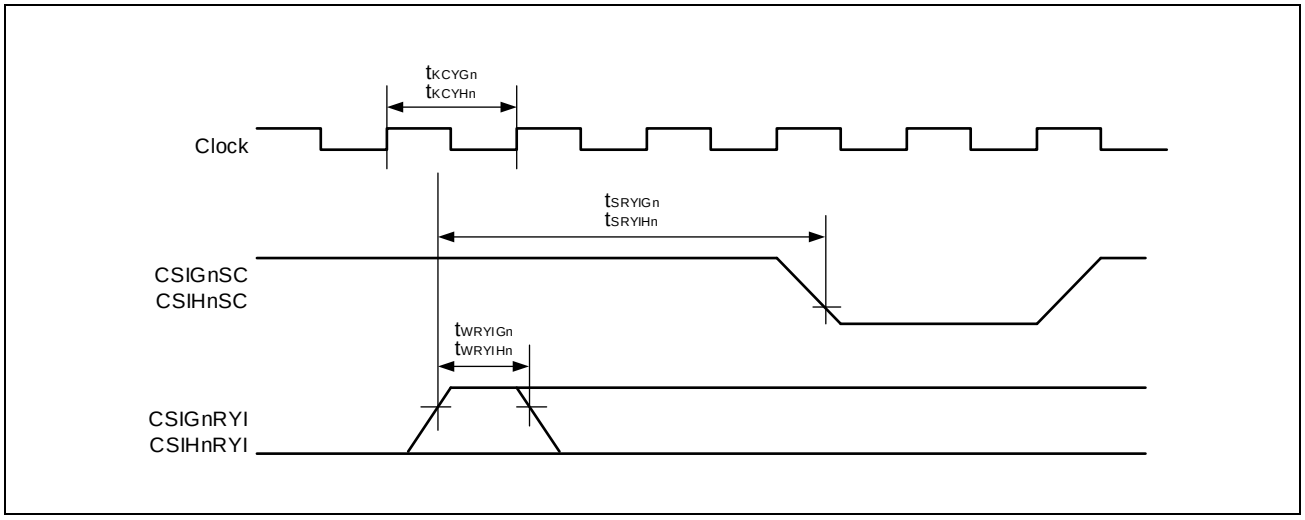
(2) RYI

Master mode:

- CSIG: Only master mode (CSIGnCTL1: CSIGnHSE = 1, CSIGnCTL1: CSIGnSIT = 0)
- CSIH: Only master mode (CSIHnCTL1: CSIHnHSE = 1, CSIHnCTL1: CSIHnSIT = 0)

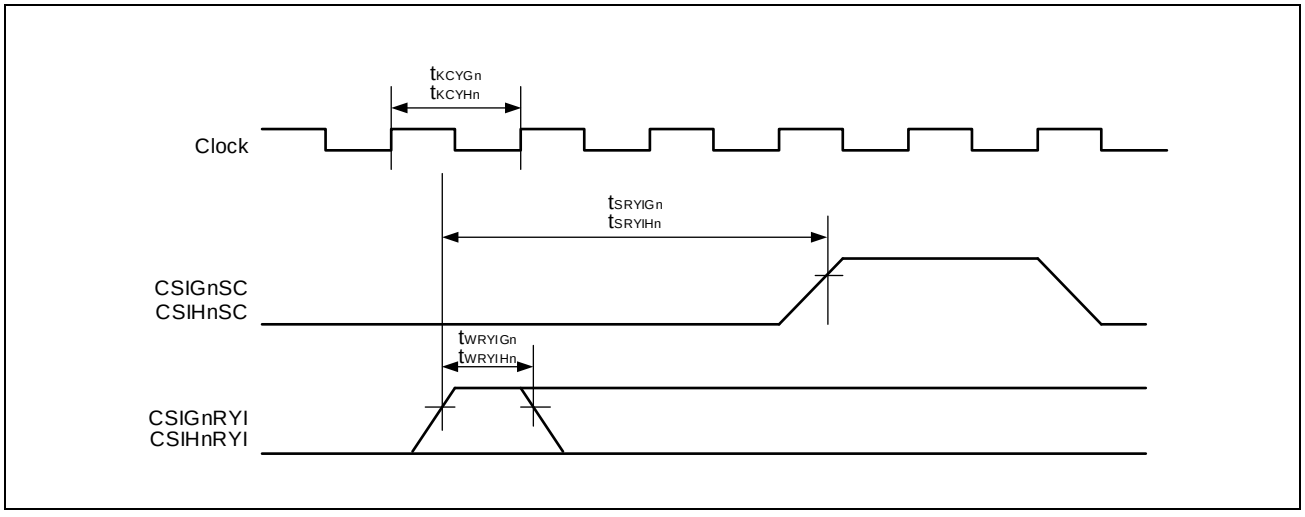
  – CSIG (CSIGnCTL1: CSIGnCKR = 0)

  – CSIH (CSIHnCFGx: CSIHnCKPx = 0)



  – CSIG (CSIGnCTL1: CSIGnCKR = 1)

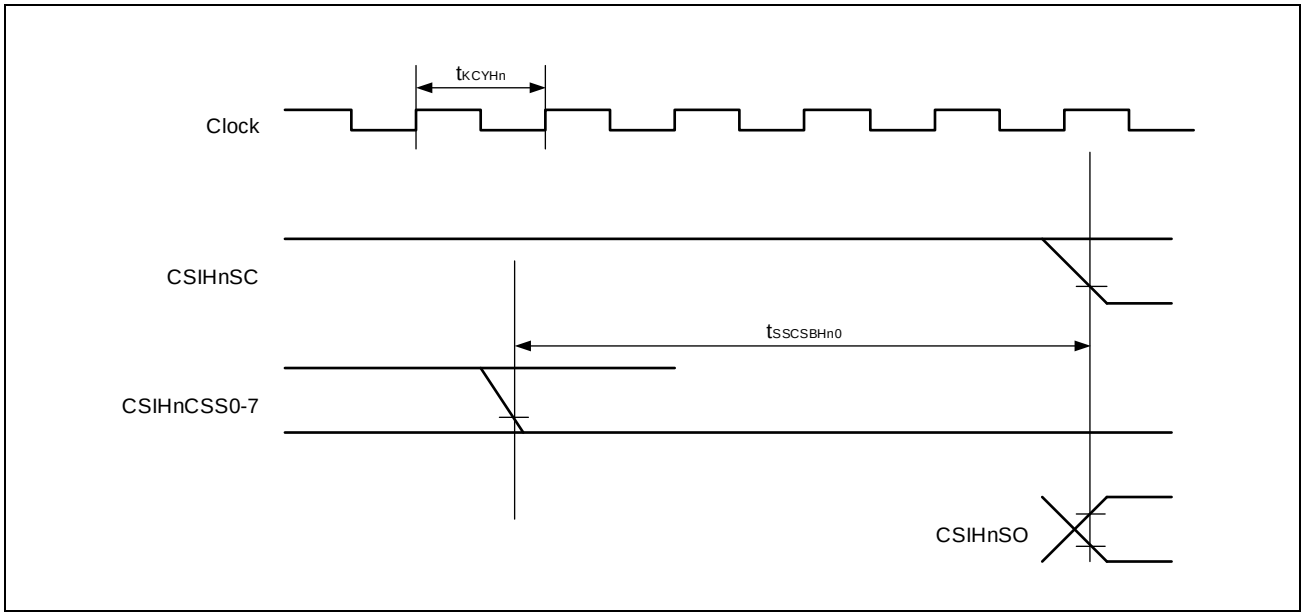
  – CSIH (CSIHnCFGx: CSIHnCKPx = 1)



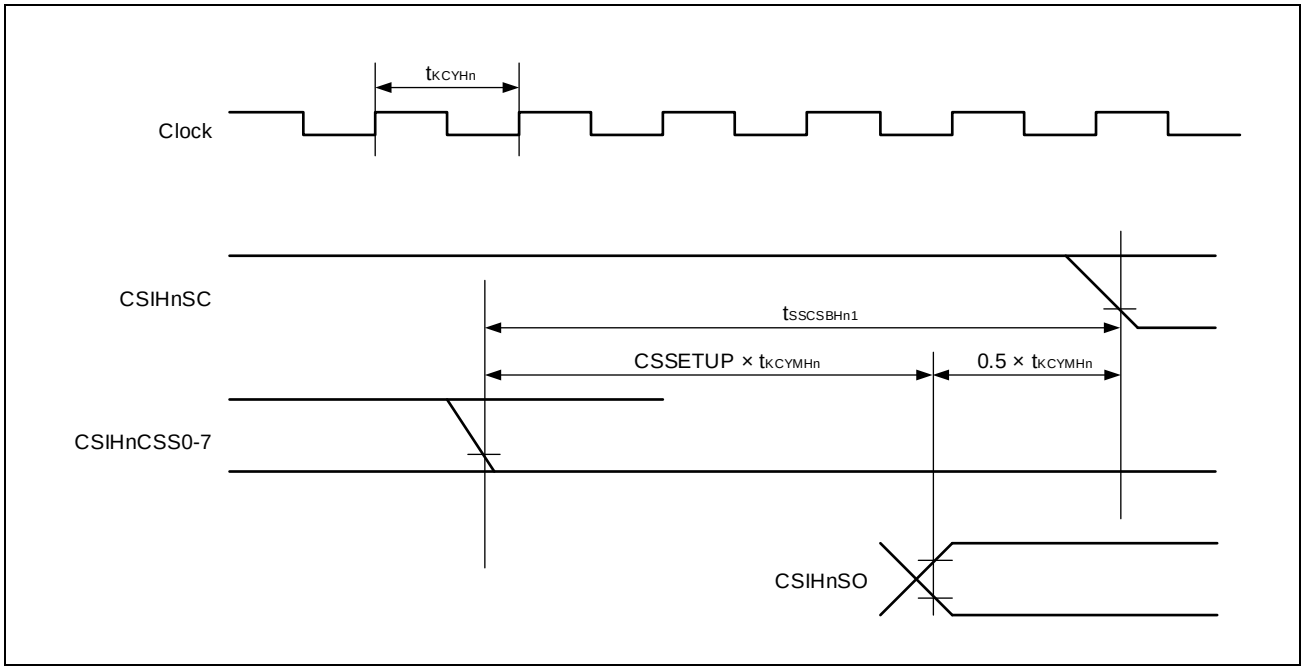
(3) CSSx

Only master mode (setup time):

- CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0

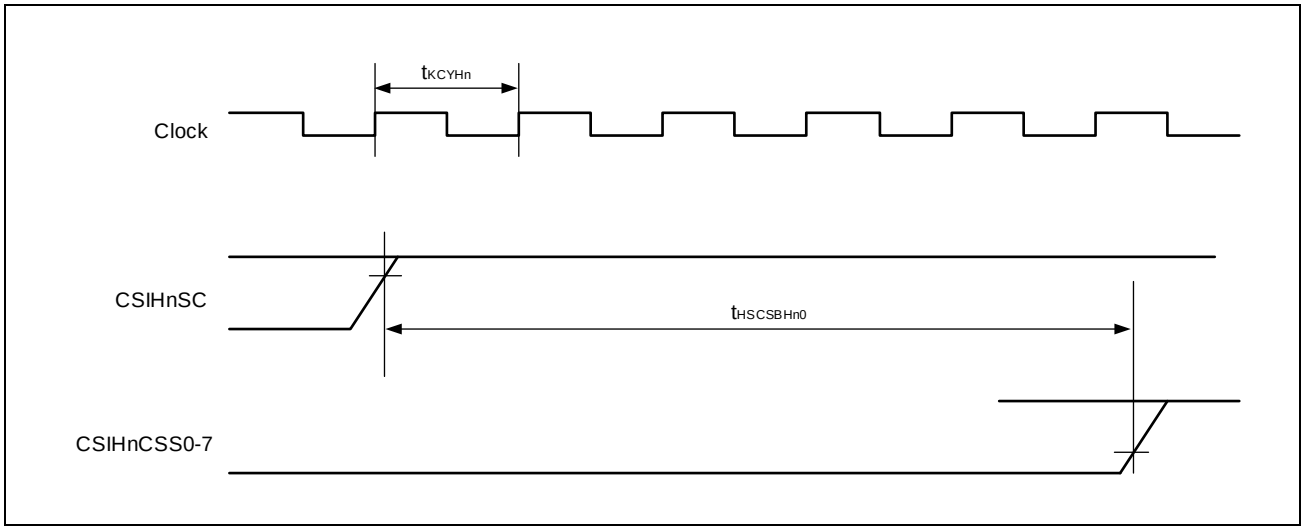


- CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 1

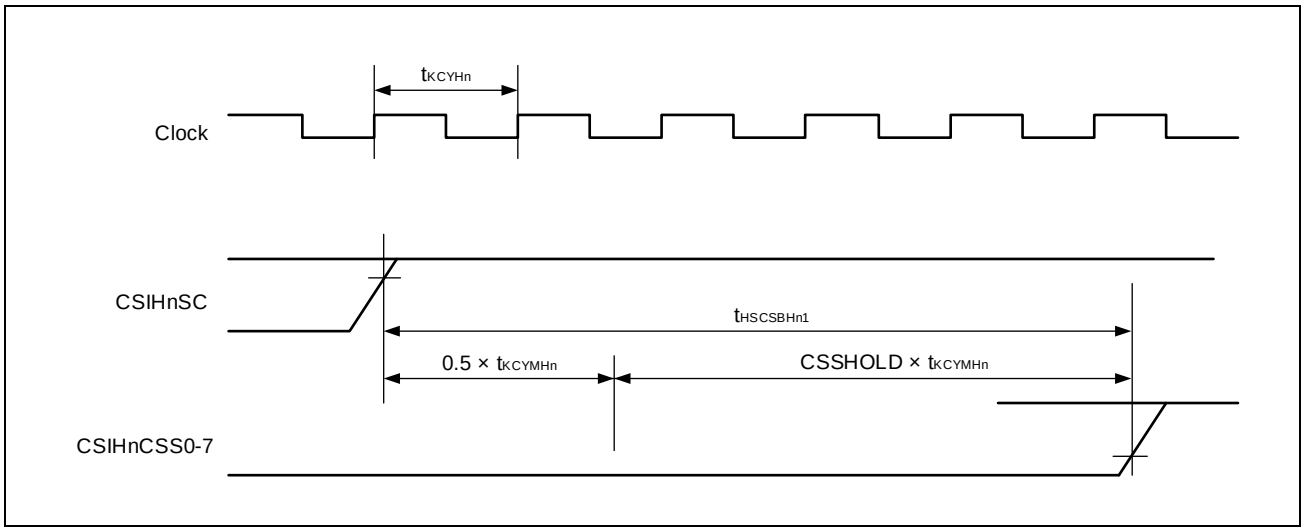


Only master mode (hold time):

- CSIHnCTL1: CSIHnSIT = 0, CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0



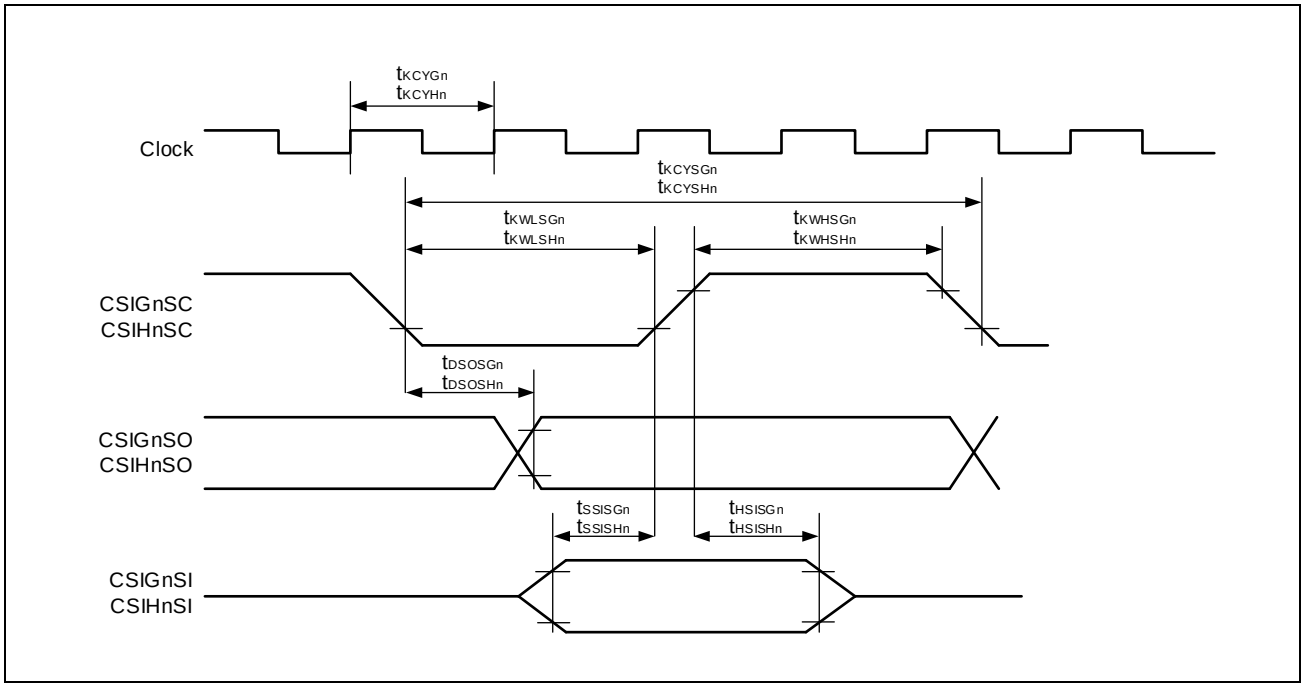
- CSIHnCTL1: CSIHnSIT = 1, CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0



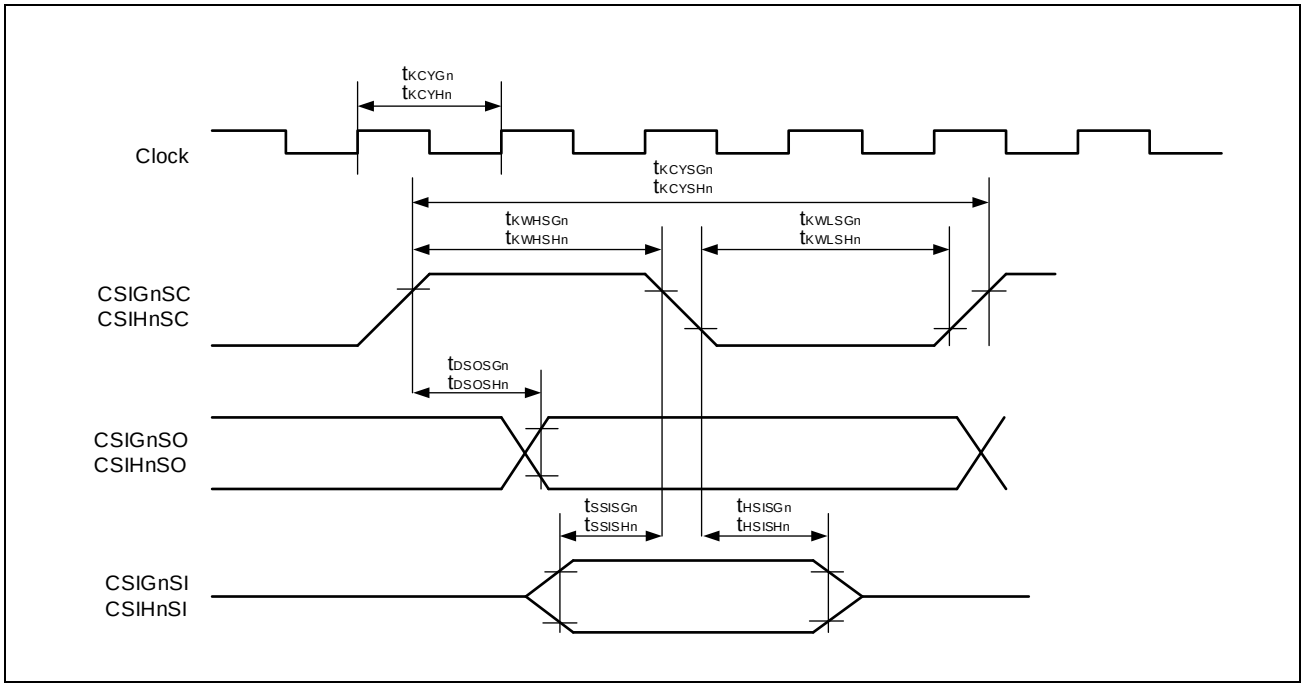
(4) SC/SI/SO

Slave mode:

- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0 or 1/1)

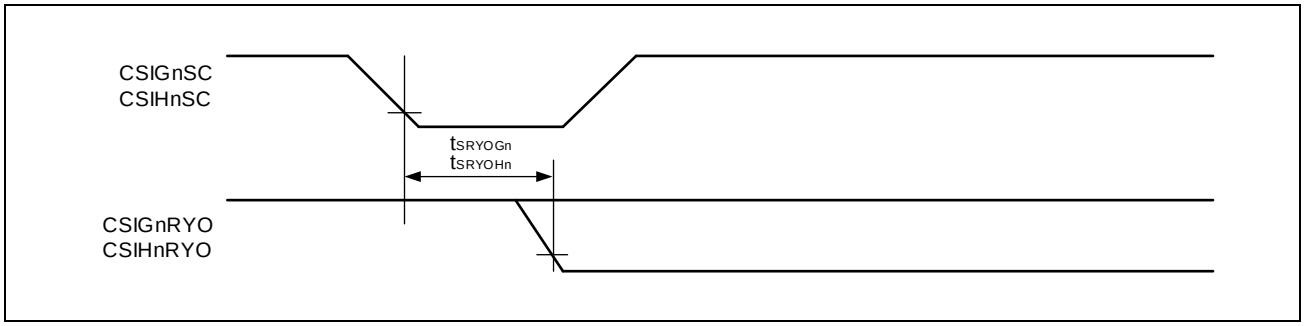


- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0 or 0/1)

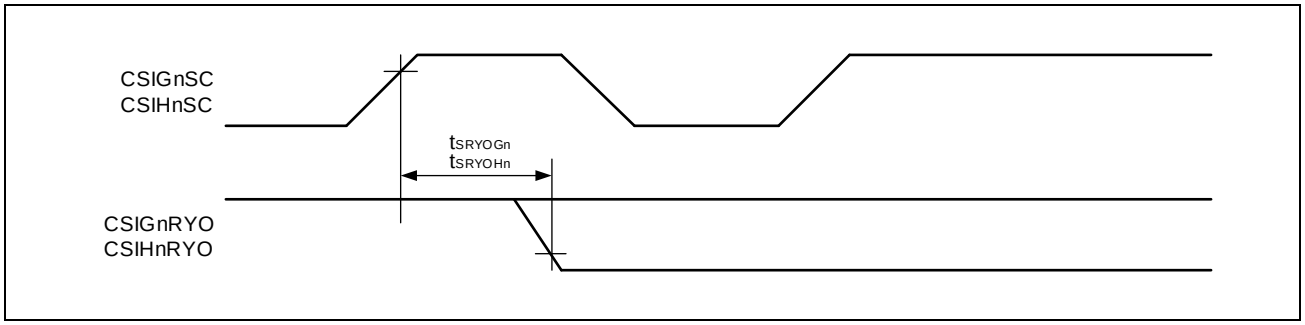


(5) RYO

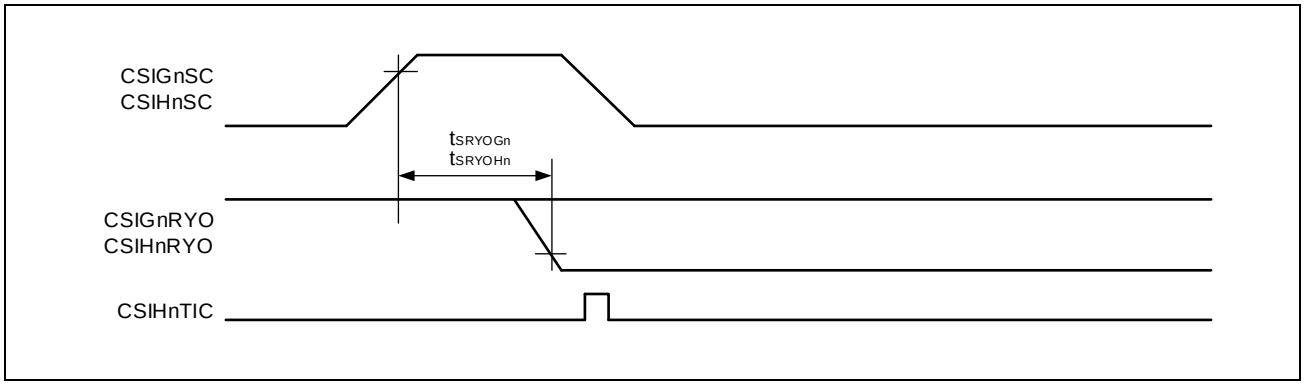
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0)



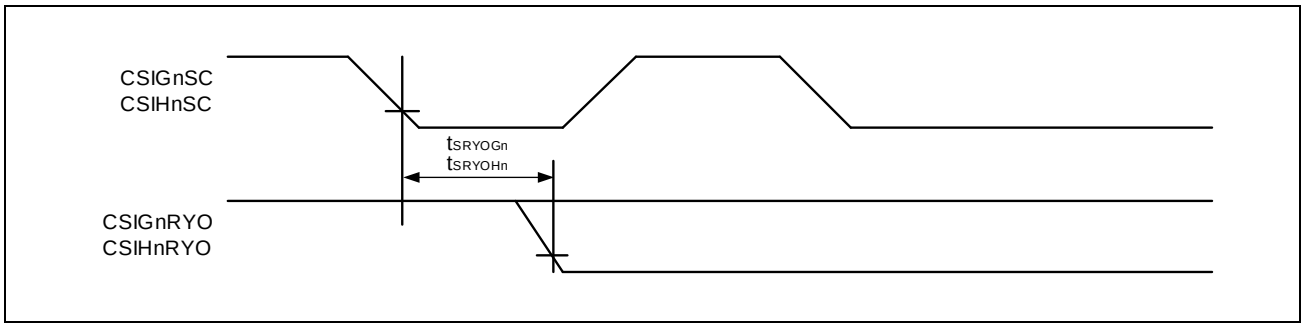
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/1)



- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0)



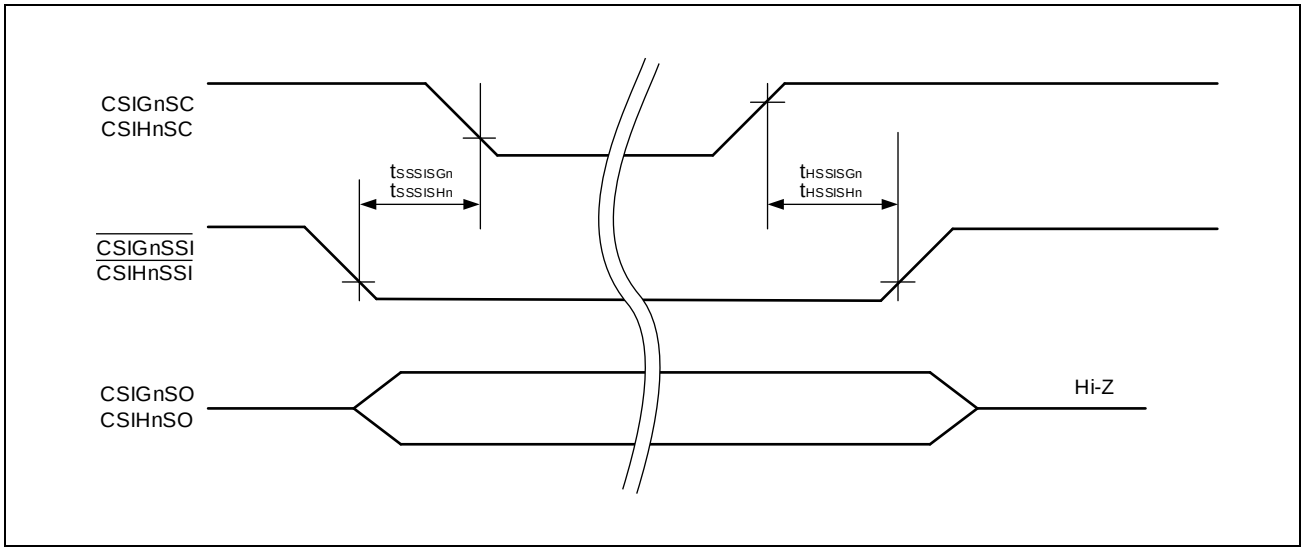
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/1)



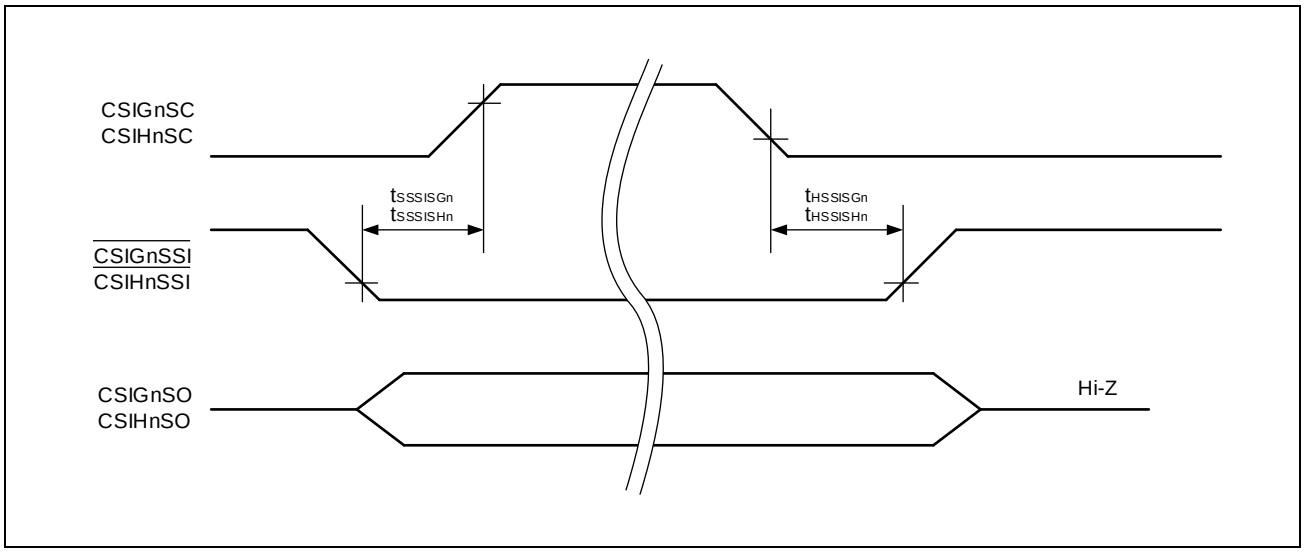
(6) SSI

Slave mode:

- CSIG (CSIGnCTL1: CSIGnSSE=1, CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0 or 1/1)



- CSIG (CSIGnCTL1: CSIGnSSE=1, CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0 or 0/1)



3B.5.11 RLIN2/RLIN3 Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate		LIN specification	1		20	kbps
		LIN extended baud rate	1		115.2*1	kbps
		UART function			1.5	Mbps
RLIN2 transfer rate		LIN specification	1		20	kbps

Note 1. The LIN extended baud rate is not part of the LIN standard specification.

3B.5.12 RIIC Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C

Table 3B.18 RIIC Timing (Normal Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIICnSCL clock period	f_{CLK}				100	kHz
Bus free time (between stop/start condition)	t_{BUF}		4.7			µs
Hold time*1	t_{HD}: STA		4.0			µs
RIICnSCL clock low-level width	t_{LOW}		4.7			µs
RIICnSCL clock high-level time	t_{HIGH}		4.0			µs
Setup time for start/restart condition	t_{SU}: STA		4.7			µs
Data hold time	t_{HD}: DAT	CBUS compatible master	5.0			µs
		I^2C mode	0*2			µs
Data setup time	t_{SU}: DAT		250			ns
Stop condition setup time	t_{SU}: STO		4.0			µs
Capacitance load of each bus line	Cb				400	pF

Remark: n = 0, 1

Note: If the system does not extend the RIICnSCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIICnSDA signal (at VIH min. of RIICnSCL signal). In order to occupy the undefined area at the falling edge of RIICnSCL.

Table 3B.19 RIIC Timing (Fast Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIICnSCL clock period	f_{CLK}				400	kHz
Bus free time (between stop/start condition)	t_{BUF}		1.3			µs
Hold time*1	t_{HD}: STA		0.6			µs
RIICnSCL clock low-level width	t_{LOW}		1.3			µs
RIICnSCL clock high-level time	t_{HIGH}		0.6			µs
Setup time for start/restart condition	t_{SU}: STA		0.6			µs
Data hold time	t_{HD}: DAT	I^2C mode	0*2			µs
Data setup time	t_{SU}: DAT		100*3			ns
Stop condition setup time	t_{SU}: STO		0.6			µs
Pulse width with spike suppressed by input filter	t_{SP}		0		50	ns
Capacitance load of each bus line	Cb				400	pF

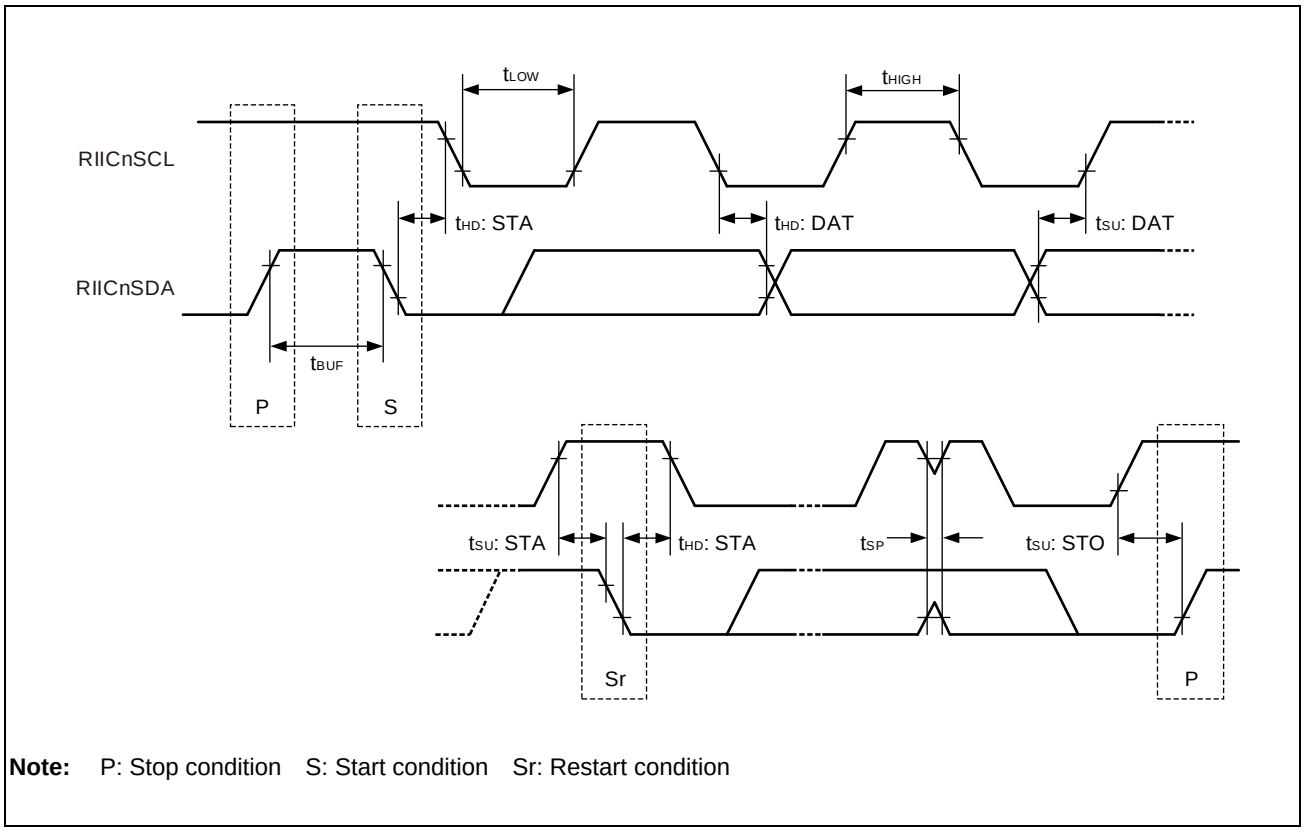
Remark: n = 0, 1

Note: If the system does not extend the RIICnSCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIICnSDA signal (at VIH min. of RIICnSCL signal). In order to occupy the undefined area at the falling edge of RIICnSCL.

Note 3. The fast mode I^2C bus can be used in normal mode I^2C bus system. In this case, set the fast mode I^2C bus so that it meets the following conditions.
- If the system does not extend the RIICnSCL signal's low state hold time: t_{SU}: DAT ≥ 250 ns
- If the system extends the RIICnSCL signal's low state hold time:
Transmit the following data bit to the RIICnSDA line prior to releasing the RIICnSCL line
(1250 ns: Normal mode I^2C bus specification).



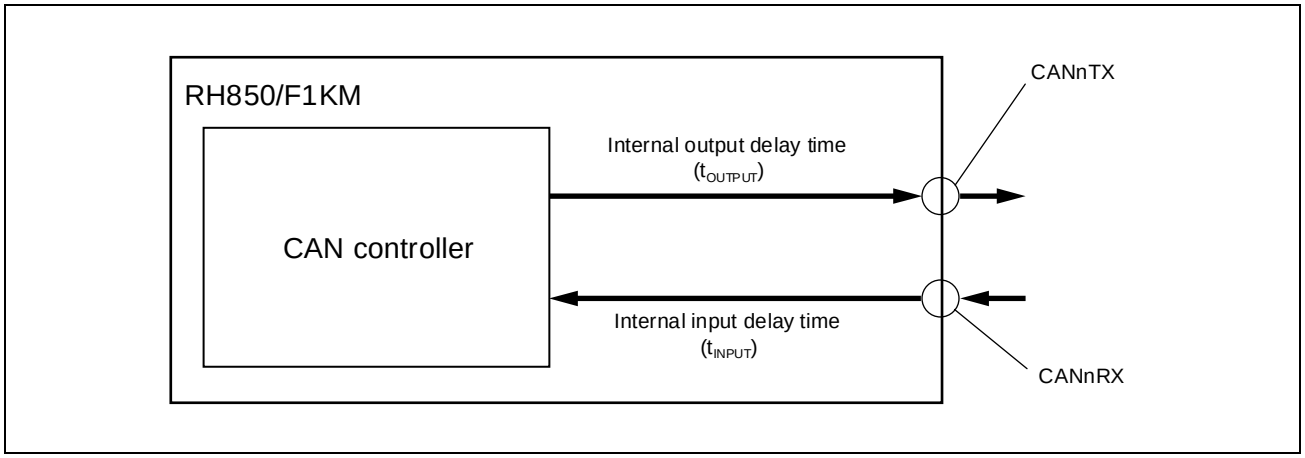
Note: P: Stop condition S: Start condition Sr: Restart condition

3B.5.13 RS-CANFD Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate		Classical CAN mode			1	Mbps
Data bit rate (CAN FD mode)		Nominal bit rate ≤ 500 kbps			5	Mbps
		Nominal bit rate > 500 kbps			2	Mbps
Internal delay time*1	t_{NODE}				50	ns

Note 1. t_{NODE} = Internal input delay time (t_{INPUT}) + Internal output delay time (t_{OUTPUT})



3B.5.14 FlexRay Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Products of CPU frequency 240 MHz max.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					10	Mbps

Products of CPU frequency 160 MHz max.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					5	Mbps

3B.5.15 Ethernet Timing

3B.5.15.1 MII Interface

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to 3.6 V, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 15 pF

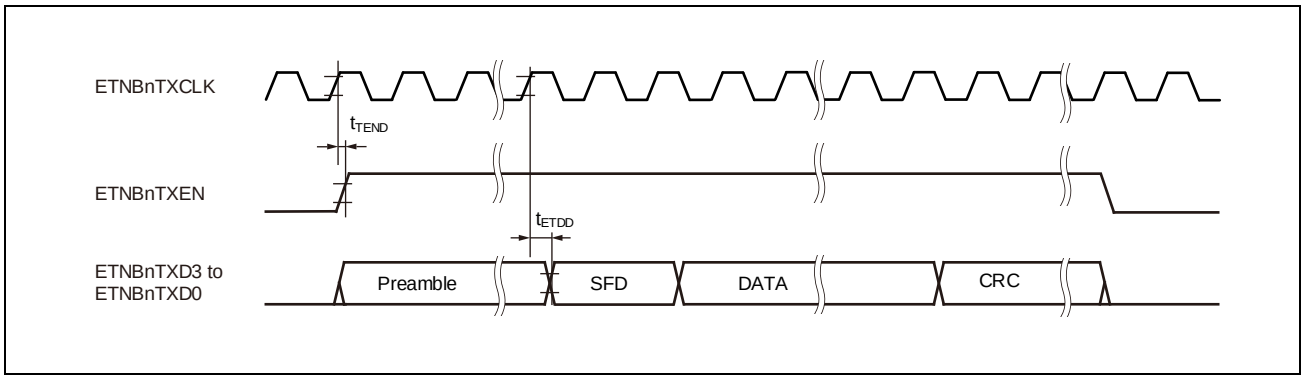
<Output driver strength>

ETNB0TXD3-0 and ETNB0TXEN pins: Fast mode

ETNB0TXCLK pin: TTL type

Table 3B.20 MII Interface (Transmission Interface)

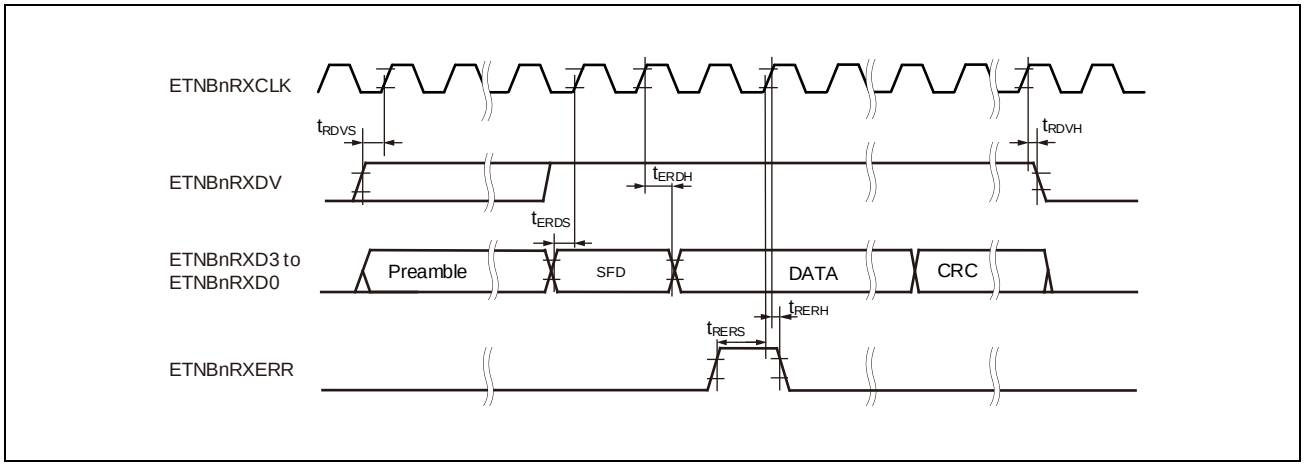
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNB0TXCLK clock period	t_{Tcyc}	100 Mbps	40 – 100 ppm	40	40 + 100 ppm	ns
		10 Mbps	400 – 100 ppm	400	400 + 100 ppm	ns
ETNB0TXEN delay vs ETNB0TXCLK ↑	t_{TEND}	CL = 15 pF			18	ns
ETNB0TXD[3:0] delay vs ETNB0TXCLK ↑	t_{ETDD}	CL = 15 pF			18	ns



<Input buffer>
ETNB0RXCLK, ETNB0RXDV, ETNB0RXD[3:0], and ETNB0RXER pins: TTL type

Table 3B.21 MII Interface (Reception Interface)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNB0RXCLK clock period	t_{Rcyc}	100 Mbps	40 – 100 ppm	40	40 + 100 ppm	ns
		10 Mbps	400 – 100 ppm	400	400 + 100 ppm	ns
ETNB0RXDV hold time vs ETNB0RXCLK ↑	t_{RDVH}		10			ns
ETNB0RXDV setup time vs ETNB0RXCLK ↑	t_{RDVS}		10			ns
ETNB0RXD[3:0] hold time vs ETNB0RXCLK ↑	t_{ERDH}		10			ns
ETNB0RXD[3:0] setup time vs ETNB0RXCLK ↑	t_{ERDS}		10			ns
ETNB0RXERR hold time vs ETNB0RXCLK ↑	t_{RERH}		10			ns
ETNB0RXERR setup time vs ETNB0RXCLK ↑	t_{RERS}		10			ns



3B.5.15.2 Management Interface

Timing of management interface (ETNB0MDC and ETNB0MDIO) depends on software. It is necessary to adjust wait time according to AC specification of PHY.

3B.5.16 RSENT Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Tick Time			1		90	µs

3B.5.17 Timer Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

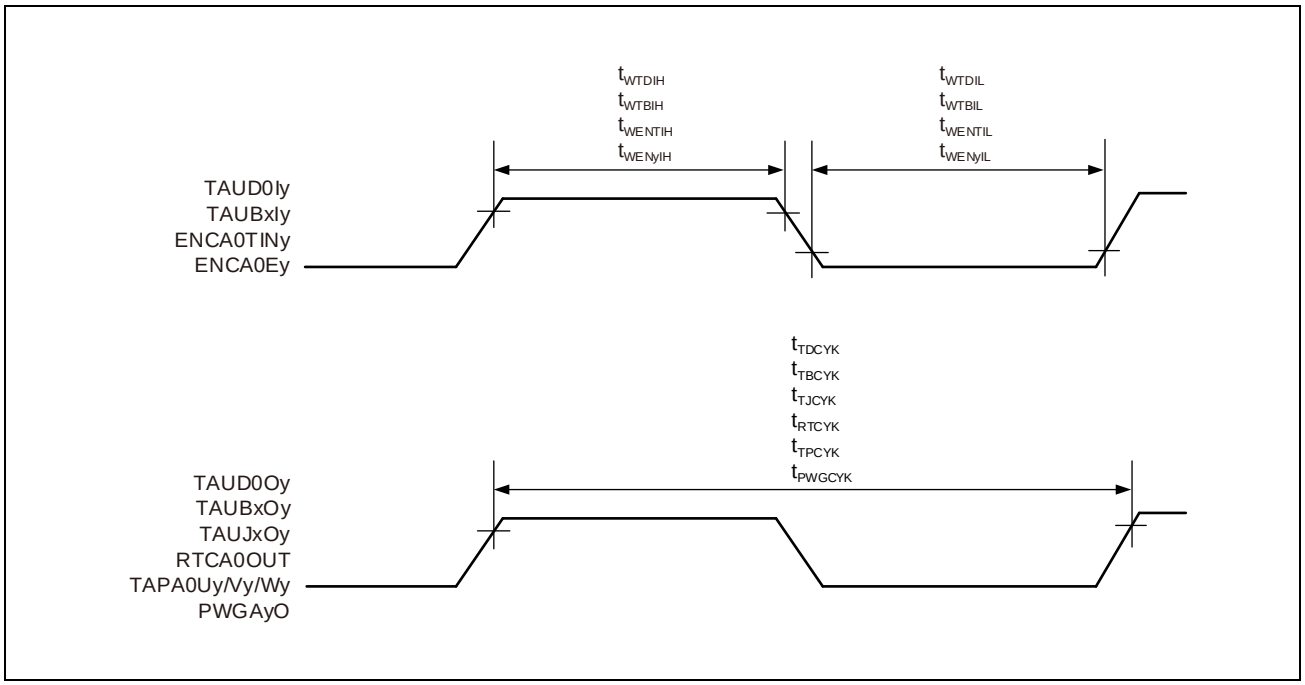
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUD0Iy input high/low level width (y = 0 to 15)	t_{WTDIH}/ t_{WTDIL}		n × Tsamp + 20*1,*2			ns
TAUD0Oy output cycle (y = 0 to 15)	t_{TDCYK}	Slow mode			10	MHz
TAUBxIy input high/low level width (x = 0, 1, y = 0 to 15)	t_{WTBIH}/ t_{WTBIL}		n × Tsamp + 20*1,*2			ns
TAUBxOy output cycle (x = 0, 1, y = 0 to 15)	t_{TBCYK}	Slow mode			10	MHz
TAUJxIy input high/low level width*3 (x = 0 to 3, y = 0 to 3)	t_{WTJIH}/ t_{WTJIL}		600			ns
TAUJxIy pulse rejection*4	t_{WTIJRJ}		100			ns
TAUJxOy output cycle (x = 0 to 3, y = 0 to 3)	t_{TJCYK}	Slow mode			10	MHz
RTCA0OUT output cycle	t_{RTCYK}			1		Hz
TAPA0ESO input high/low level width*3	t_{WESIH}/ t_{WESIL}		600			ns
TAPA0ESO pulse rejection*4	t_{WESIRJ}		100			ns
TAPA0Uy/Vy/Wy output cycle (y = P, N)	t_{TPCYK}	Slow mode			10	MHz
ENCA0TINy input high/low level width (y = 0, 1)	t_{WENTIH}/ t_{WENTIL}		n × Tsamp + 20*1			ns
ENCA0Ey input high/low level width (y = 0,1,C)	t_{WENyIH}/ t_{WENyIL}		n × Tsamp + 20*1			ns
PWGAyO output cycle (y = 0 to 95)	t_{PWGCYK}	Slow mode			10	MHz

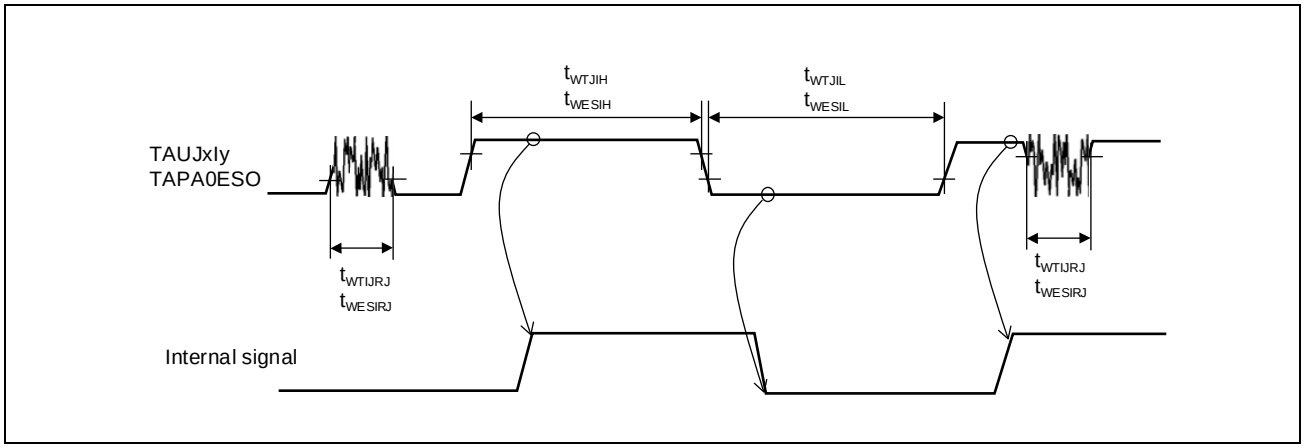
Note 1. n: Sampling number of the digital noise filter for each input.
Tsamp: Sampling time of the digital noise filter for each input.

Note 2. Input more than 1 count clock width of each timer counter channel.

Note 3. TAUJxIy and TAPA0ESO input width is needed to ensure that the internal timer input signal is activated.

Note 4. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.


t_{WTDIH}
t_{WTBIH}
t_{WENTIH}
t_{WENyIH}
t_{WTDIL}
t_{WTBIL}
t_{WENTIL}
t_{WENyIL}
TAUD0Iy
TAUBxIy
ENCA0TINy
ENCA0Ey
t_{TDCYK}
t_{TBCYK}
t_{TJCYK}
t_{RTCYK}
t_{TPCYK}
t_{PWGCYK}
TAUD0Oy
TAUBxOy
TAUJxOy
RTCA0OUT
TAPA0Uy/Vy/Wy
PWGAyO

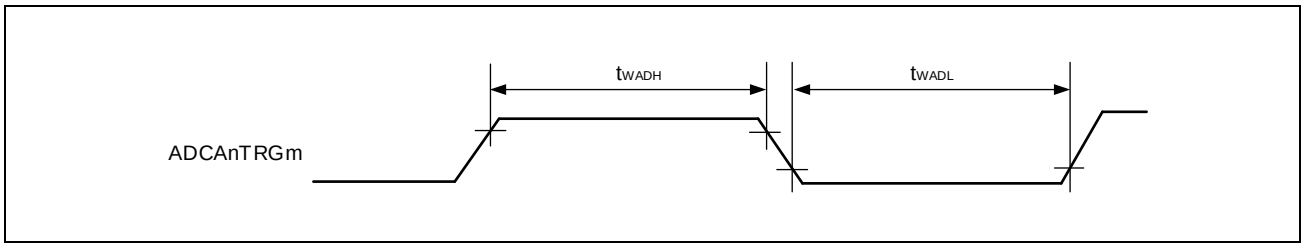

t_{WTJIH}
t_{WESIH}
t_{WTJIL}
t_{WESIL}
TAUJxIy
TAPA0ESO
t_{WTIJRJ}
t_{WESIRJ}
t_{WTIJRJ}
t_{WESIRJ}
Internal signal

3B.5.18 ADTRG Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCAnTRGm input high/ low level width	t_{WADH}/t_{WADL}		k × Tsamp + 20*1			ns

Note 1. k: Sampling number of the digital noise filter for each input.
Tsamp: Sampling time of the digital noise filter for each input.



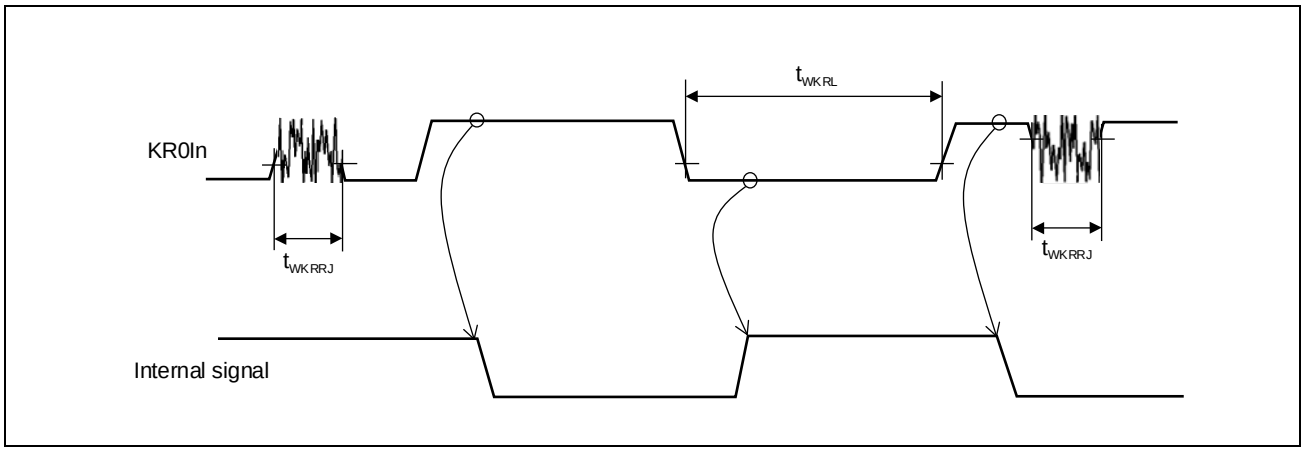
3B.5.19 Key Return Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
KR0In input low level width*1	t_{WKRL}		600			ns
KR0In pulse rejection*2	t_{WKRRJ}		100			ns

Note 1. KR0In input width is needed to ensure that the internal key input signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value.
Noise such as the figure can be filtered.



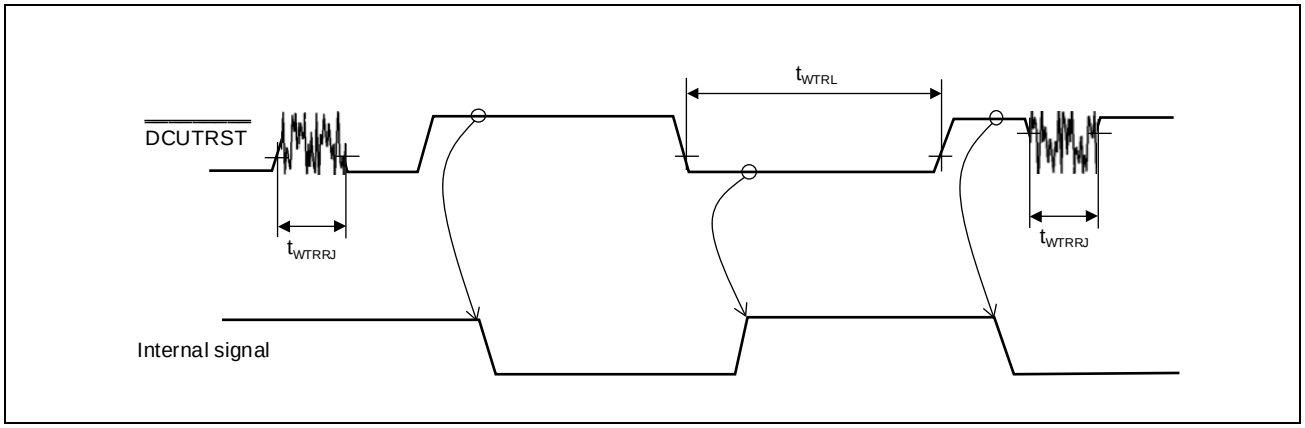
3B.5.20 $\overline{\text{DCUTRST}}$ Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{DCUTRST}}$ input low level width*1	t_{WTRL}		600			ns
$\overline{\text{DCUTRST}}$ pulse rejection*2	t_{WTRRJ}		100			ns

Note 1. $\overline{\text{DCUTRST}}$ input width is needed to ensure that the internal DCU reset input signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value.
Noise such as the figure can be filtered.



3B.5.21 Debug Interface Characteristics

3B.5.21.1 Nexus Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

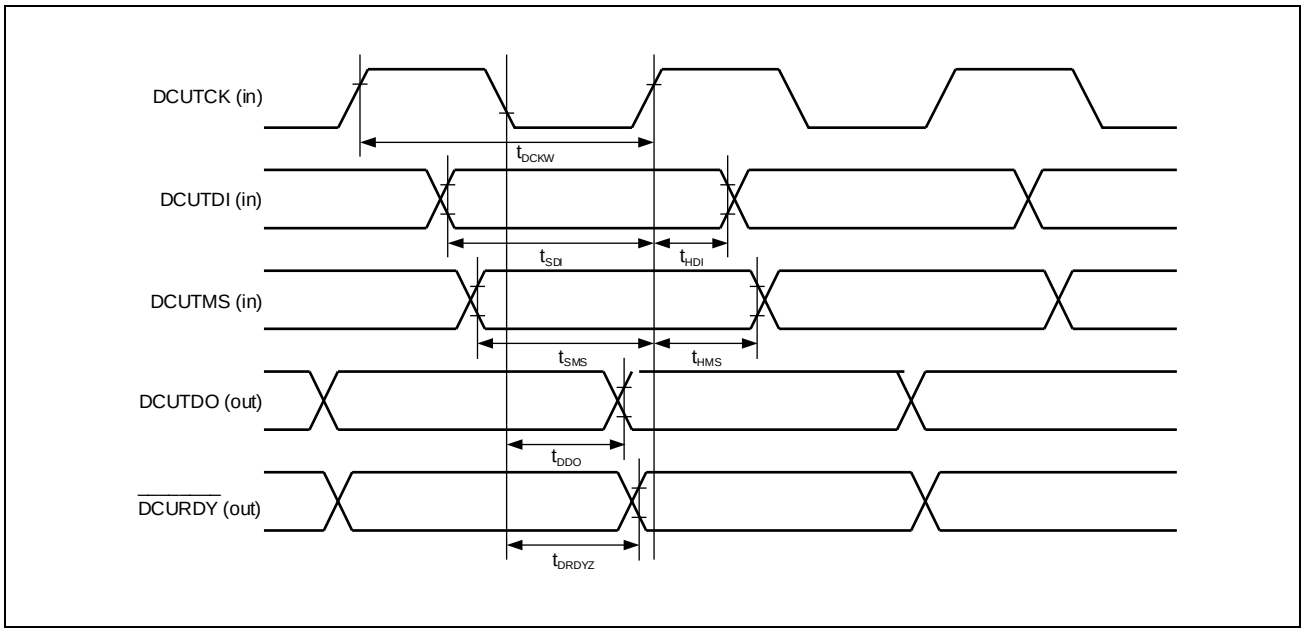
<Input buffer>

DCUTDI, DCUTCK, DCUTMS, $\overline{\text{DCUTRST}}$: TTL

<Output driver strength>

DCUTDO, $\overline{\text{DCURDY}}$: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DCUTCK cycle width	t_{DCKW}		50			ns
DCUTDI setup time (vs DCUTCK ↑)	t_{SDI}		12			ns
DCUTDI hold time (vs DCUTCK ↑)	t_{HDI}		3			ns
DCUTMS setup time (vs DCUTCK ↑)	t_{SMS}		12			ns
DCUTMS hold time (vs DCUTCK ↑)	t_{HMS}		3			ns
DCUTDO delay time (↓ DCUTCK)	t_{DDO}		0		20	ns
$\overline{\text{DCURDY}}$ delay time (↓ DCUTCK)	t_{RDYZ}		0		20	ns



3B.5.21.2 LPD (4 Pins) Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 100 pF

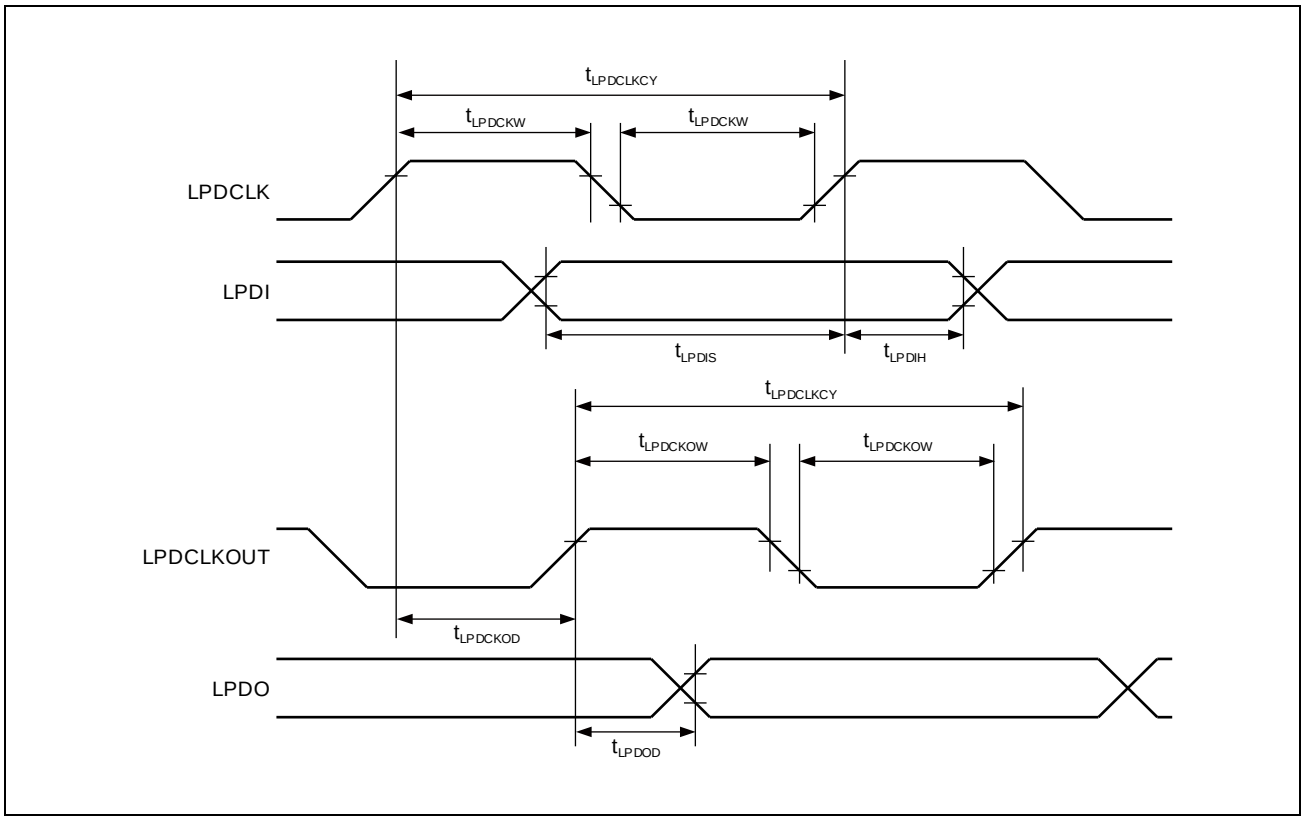
<Input buffer>

LPDCLK, LPDI: TTL

<Output driver strength>

LPDCLKOUT, LPDO: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPDCLK cycle time/ LPDCLKOUT cycle time	$t_{LPDCLKCY}$		83.3 (max.12 MHz)			ns
LPDCLK High-level width/ LPDCLK Low-level width	t_{LPDCKW}		0.5 × $t_{LPDCLKCY}$ – 10			ns
LPDCLKOUT High-level width/ LPDCLKOUT low-level width	$t_{LPDCKOW}$		t_{LPDCKW} – 10			ns
LPDI setup time (LPDCLK ↑)	t_{LPDIS}		41			ns
LPDI hold time (LPDCLK ↑)	t_{LPDIH}		3			ns
LPDCLK to LPDCLKOUT delay time	$t_{LPDCKOD}$				44	ns
LPDO delay time (LPDCLKOUT ↑)	t_{LPDOD}		0		15	ns



3B.5.21.3 LPD (1 Pin) Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 50 pF

<Input buffer>

LPDIO: TTL

<Output driver strength>

LPDIO: Fast mode

<External pull-up resistor>

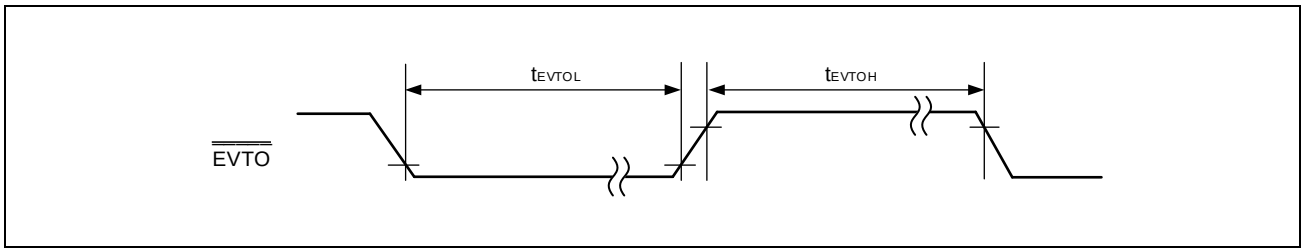
LPDIO: 1 kΩ to 10 kΩ

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPD (1 pin) baud rate					2.0	Mbps

3B.5.21.4 Debug Event Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 50 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{EVTO}}$ high/low level width	t_{EVTOH}/t_{EVTOL}		50			ns



3B.6 A/D Converter Characteristics

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

(1/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Conversion clock	ADCLKn				8*3		40	MHz
Resolution	RESn	12-bit mode			12	12	12	bit
		10-bit mode			10	10	10	bit
Conversion time	t_{CONn}	ADCAnSMPCR.SMPT[7:0] = 12 H(40 cycle) (8M Hz*3 ≤ ADCLKn ≤ 32 MHz), External MPX is not used			1.25		5	µs
		ADCAnSMPCR.SMPT[7:0] = 18 H (46 cycle) (8 MHz*3 ≤ ADCLKn ≤ 40 MHz), External MPX is not used			1.15		5.75	µs
		ADCAnSMPCR.SMPT[7:0] = 12 H (80 cycle) (8 MHz*3 ≤ ADCLKn ≤ 32 MHz), External MPX is used			2.5*4		10	µs
		ADCAnSMPCR.SMPT[7:0] = 18 H (92 cycle) (8 MHz*3 ≤ ADCLKn ≤ 40 MHz), External MPX is used			2.3*4		11.5	µs
Sampling time	t_{SMP}	ADCAnSMPCR.SMPT[7:0] = 12 H (18 cycle) (8 MHz*3 ≤ ADCLKn ≤ 32 MHz)			0.56		2.25	µs
		ADCAnSMPCR.SMPT[7:0] = 18 H (24cycle) (8 MHz*3 ≤ ADCLKn ≤ 40 MHz)			0.6		3	µs
Overall error*1	TOEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±4.0	LSB
				ADCA0I0-5 (T&H used)			±6.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±6.0	LSB
				ADCA0I0-5 (T&H used)			±8.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB
Analog input voltage	VAIN0SN	ADCAnIm	T&H not used		AnVSS		AnVREF	V
		ADCA0I0-5	T&H used		0.2		A0VREF – 0.2	V
		ADCA0ImS	A0VREF ≥ EVCC		A0VSS		EVCC	V
			A0VREF < EVCC		A0VSS		A0VREF	V
		ADCA1ImS	A1VREF ≥ BVCC		A1VSS		BVCC	V
			A1VREF < BVCC		A1VSS		A1VREF	V
Operation current	IA0VREF IA1VREF	T&H not used				1.1	3.0	mA
		T&H used (max. 6 pins)					*2	mA
STOP, DeepSTOP, Cyclic STOP current (@LPS is stopped)	IA0VREFS IA1VREFS					1	10	µA
T&H current	ITH					0.5	1.3	mA/ch
T&H sampling time	t_{THSMP}				450			ns
T&H hold time	t_{THHOLD}						10	µs
Set up time of self diagnosis voltage circuit	t_{BOOT}				500			ns
Set up time of self diagnosis voltage level	t_{OUT}				500			ns
Pull-down resistor for diagnosis of open pins		ADCnIm pins	VI = AnVREF		350	500	650	kΩ
		ADCnImS pins	A0VREF ≥ EVCC: VI = EVCC A0VREF < EVCC: VI = A0VREF		100	215	800	kΩ
			A1VREF ≥ BVCC: VI = BVCC A1VREF < BVCC: VI = A1VREF					

(2/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Accuracy of self-diagnosis function (except diagnosis of open pins)	TESH0SN	12-bit mode	Self-diagnosis voltage level = AnVREF		4015-|TOEn|		4095	—
			Self-diagnosis voltage level = 2/3AnVREF		2651-|TOEn|	2731	2811+|TOEn|	—
			Self-diagnosis voltage level = 1/2AnVREF		1968-|TOEn|	2048	2128+|TOEn|	—
			Self-diagnosis voltage level = 1/3AnVREF		1285-|TOEn|	1365	1445+|TOEn|	—
			Self-diagnosis voltage level = AnVSS		0		80+|TOEn|	—
		10-bit mode	Self-diagnosis voltage level = AnVREF		1003-|TOEn|		1023	—
			Self-diagnosis voltage level = 2/3AnVREF		663-|TOEn|	683	703+|TOEn|	—
			Self-diagnosis voltage level = 1/2AnVREF		492-|TOEn|	512	532+|TOEn|	—
			Self-diagnosis voltage level = 1/3AnVREF		321-|TOEn|	341	361+|TOEn|	—
			Self-diagnosis voltage level = AnVSS		0		20+|TOEn|	—
Integral nonlinearity error*1	ILEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±2.0	LSB
				ADCA0I0-5 (T&H used)			±3.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±3.0	LSB
				ADCA0I0-5 (T&H used)			±4.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB
Differential nonlinearity error*1	DLEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±1.0	LSB
				ADCA0I0-5 (T&H used)			±2.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±3.0	LSB
				ADCA0I0-5 (T&H used)			±4.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.0V to 4.5V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
Zero scale error (offset error)*1	ZSEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±3.5	LSB
				ADCA0I0-5 (T&H used)			±5.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±5.5	LSB
				ADCA0I0-5 (T&H used)			±7.5	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±0.5	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
Full scale error*1	FSEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±3.5	LSB
				ADCA0I0-5 (T&H used)			±5.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±5.5	LSB
				ADCA0I0-5 (T&H used)			±7.5	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±0.5	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB

Note: Conversion accuracy when ADCA0ImS terminal is converted in 12-bit mode: Conversion accuracy can be applied if lower 2-bit is ignored from conversion result.

Note 1. This does not include quantization error.

Note 2. 3.0 + 1.3 × (the number of used T&H)

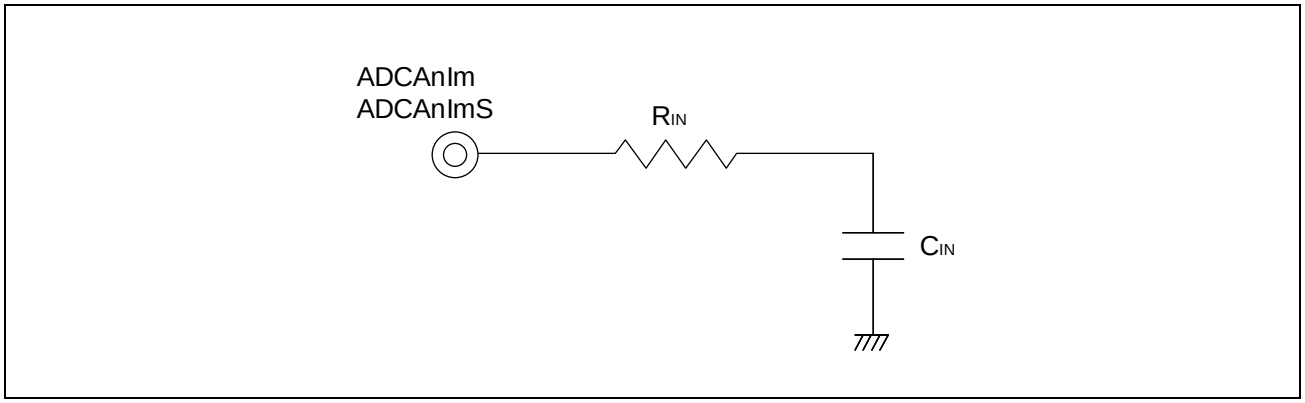
Note 3. Include the oscillation accuracy of HS IntOSC.

Note 4. When the external multiplexer is used, the detailed time of A/D conversion is MPX setup time, sampling time and successive approximation time. MPX setup time is same as “sampling time + successive approximation time”.

CAUTION

When an external digital pulse is applied to AP0, AP1, P8, P9, P18, and P19 pins during an A/D conversion this may lead to an A/D conversion result with a larger conversion error as expected due to the coupling noise of the external digital pulse.
The same behavior may apply when the digital buffer is used as an output pin. For the output port the potential degradation increases with the driven total output current of the port. In addition the conversion resolution may drop if the output current fluctuates at adjacent pins due to the coupling effect of the external circuit connected to these port pins.

3B.6.1 Equivalent Circuit of the Analog Input Block



RH850/F1KM-S4

Terminals	Condition	RIN (kΩ)	CIN (pF)
ADCA0I0 to 5	When T&H is used	14.1	2.2
	When T&H is not used	3.8	2.1
ADCA0I6 to 15	—	3.8	2.1
ADCA0I0S to 3S, 5S to 11S, 14S to 16S	—	5.3	9.3
ADCA0I4S, 17S to 19S	—	7.2	9.3
ADCA1I0 to 15	—	3.8	2
ADCA1I0S to 19S	—	5.2	7.4

RH850/F1KM-S2

Terminals	Condition	RIN (kΩ)	CIN (pF)
ADCA0I0 to 5	When T&H is used	14.2	2.0
	When T&H is not used	3.8	2.1
ADCA0I6 to 15	—	3.8	2.1
ADCA0I0S to 3S, 5S to 11S, 14S to 16S	—	5.7	8.8
ADCA0I4S, 17S to 19S	—	7.0	8.8
ADCA1I0 to 15	—	4.0	2.0
ADCA1I0S to 7S	—	5.6	5.3

CAUTION

This specification is not tested during outgoing inspection. Therefore RIN and CIN are reference values only and not guaranteed. In addition these values are specified as maximum values.

3B.7 Flash Programming Characteristics

3B.7.1 Code Flash

The code flash memory is shipped in the erased state. If the code flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3B.22 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3		5*4		30	MHz
Number of rewrites*1	CWRT	Data retention of 20 years*2	1000			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 1000), the device can be erased “n” times for each block. For example, when a block of 32 KB is erased after 256 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Note 3. f_{PCLK} = 1/8 f_{CPUCLK_H}: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 3B.23 Programming Characteristic

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz CWRT < 100 times	256 B		0.4*1	6*1	ms
			8 KB		20	90	ms
			32 KB		80	360	ms
			256 KB		0.6	2.7	s
			384 KB		0.9	4.1	s
			512 KB		1.2	5.4	s
			768 KB		1.7	8.1	s
			1 MB		2.3	10.8	s
			1.5 MB		3.4	16.2	s
			2 MB		4.5	21.5	s
			3 MB		6.8	32.3	s
			4 MB		9	43	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	256 B		0.5*1	7.2*1	ms
			8 KB		24	108	ms
			32 KB		96	432	ms
			256 KB		0.7	3.3	s
			384 KB		1.1	4.9	s
			512 KB		1.4	6.5	s
			768 KB		2.1	9.8	s
			1 MB		2.7	13	s
			1.5 MB		4.1	19.5	s
			2 MB		5.4	26	s
			3 MB		8.1	39	s
			4 MB		10.8	52	s

Table 3B.23 Programming Characteristic

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Erase time		f_{PCLK} ≥ 20 MHz CWRT < 100 times	8 KB		39	120	ms
			32 KB		141	480	ms
			256 KB		1.2	3.5	s
			384 KB		1.7	5.3	s
			512 KB		2.3	7	s
			768 KB		3.4	10.5	s
			1 MB		4.5	14	s
			1.5 MB		6.8	21	s
			2 MB		9	28	s
			3 MB		13.5	42	s
			4 MB		18	56	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	8 KB		47	144	ms
			32 KB		169	576	ms
			256 KB		1.4	4.2	s
			384 KB		2.1	6.3	s
			512 KB		2.7	8.4	s
			768 KB		4.1	12.6	s
			1 MB		5.4	16.8	s
			1.5 MB		8.1	25.2	s
			2 MB		10.8	33.6	s
			3 MB		16.2	50.4	s
			4 MB		21.6	67.2	s

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

3B.7.2 Data Flash

The data flash memory is shipped in the erased state. If the data flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3B.24 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3		5*4		30	MHz
Number of rewrites*1	CWRT	Data retention 20 years*2	125 k			times
		Data retention 3 years*2	250 k			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 125000), the device can be erased “n” times for each block. For example, when a block of 64 bytes is erased after 4 bytes of writing have been performed for different addresses 16 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the data flash memory.

Note 3. f_{PCLK} = 1/8 f_{CPUCLK_H}: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 3B.25 Programming Characteristics

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz	4 B		0.16*1	1.7*1	ms
			32 KB		1.4	6.8	s
			64 KB		2.79	13.44	s
			128 KB		5.58	26.88	s
Erase time		f_{PCLK} ≥ 20 MHz	64 B		1.7*1	10*1	ms
			32 KB		0.9	5.2	s
			64 KB		1.74	10.24	s
			128 KB		3.48	20.48	s
Blank check time		f_{PCLK} ≥ 20 MHz	4 B			30*1	µs
			64 B			100*1	µs
			32 KB			35.2	ms
			64 KB			70.4	ms
			128 KB			140.8	ms

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

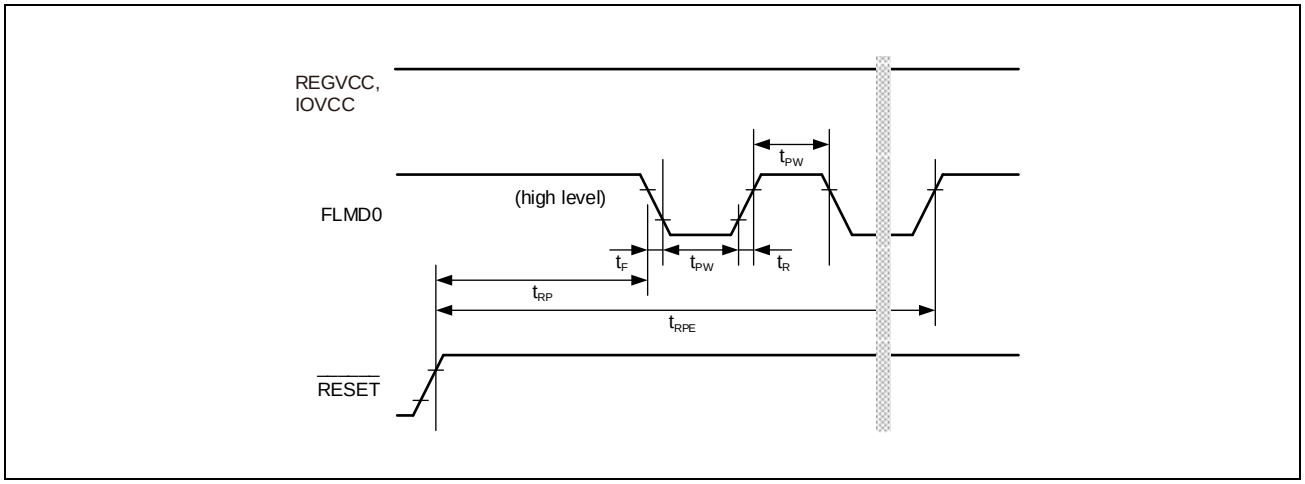
3B.7.3 Serial Programming Interface

3B.7.3.1 Serial Programmer Setup Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0 pulse input start time	t_{RP}		1.5			ms
FLMD0 pulse input end time	t_{RPE}				101.5	ms
FLMD0 low/high level width	t_{PW}		3.2			µs
FLMD0 rise time	t_R				20	ns
FLMD0 fall time	t_F				20	ns

Note: IOVCC: EVCC = BVCC = A0VREF = A1VREF



3B.7.3.2 Flash Programming Interface

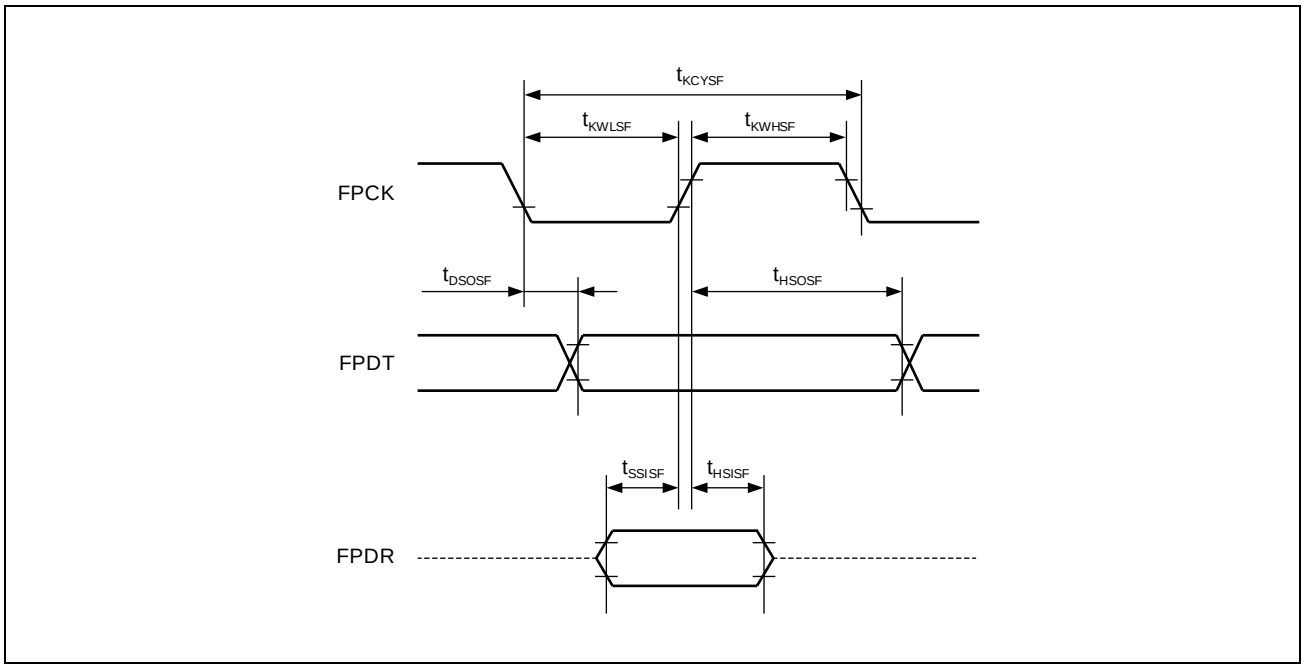
Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Flash Programming transfer rate		1-wired UART mode			1	Mbps
		2-wired UART mode (Products of CPU frequency 240 MHz max.)			1.5	Mbps
		2-wired UART mode (Products of CPU frequency 160 MHz max.)			1	Mbps
FPCK cycle time	t_{KCYSF}	3-wired clock sync mode	200*1			ns
FPCK high level width	t_{KWHSF}	3-wired clock sync mode	t_{KCYSF} / 2 – 15			ns
FPCK low level width	t_{KWLSF}	3-wired clock sync mode	t_{KCYSF} / 2 – 15			ns
FPDR setup time (vs. FPCK)	t_{SSISF}	3-wired clock sync mode	t_{Pcyc} × 2			ns
FPDR hold time (vs. FPCK)	t_{HSISF}	3-wired clock sync mode	t_{Pcyc} × 2			ns
FPDT output delay (vs. FPCK)	t_{DSOSF}	3-wired clock sync mode Not continuous transfer (data: 1st bit)			0	ns
		3-wired clock sync mode Not continuous transfer (data: except 1st bit)			$–t_{KWHSF}$ + 3 × t_{Pcyc} + 36	ns
FPDT hold time (vs. FPCK)	t_{HSOSF}	3-wired clock sync mode	t_{Pcyc} × 2			ns

Note 1. Input an external clock that is more than 6 clocks of PCLK.

NOTE

t_{Pcyc} is period of PCLK.



3B.8 Thermal Characteristics

3B.8.1 Parameters

Package	Item	Symbol	Estimate	Unit	Note
272-pin FPBGA	Thermal Resistance	Θja	21.1	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	11.8		
233-pin FPBGA	Thermal Resistance	Θja	21.2	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	11.8		
176-pin LQFP (RH850/F1KM-S4)	Thermal Resistance	Θja	35.5	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	27.6		
144-pin LQFP (RH850/F1KM-S4)	Thermal Resistance	Θja	35.5	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	26.9		
100-pin LQFP (RH850/F1KM-S4)	Thermal Resistance	Θja	38.3	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	28.1		
176-pin LQFP (RH850/F1KM-S2)	Thermal Resistance	Θja	35.5	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	27.6		
144-pin LQFP (RH850/F1KM-S2)	Thermal Resistance	Θja	35.5	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	26.9		
100-pin LQFP (RH850/F1KM-S2)	Thermal Resistance	Θja	38.3	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	28.1		

NOTE

The thermal resistance and characterization parameters depend on the usage environment.

3B.8.2 Board

Conforming to JESD51-7 (4 layers)

	Board Size (mm)		
	X	Y	Area (mm^2)
Board	76.2	114.3	8709.66
Remaining copper rates	Thickness of conductors		
50-95-95-50%	70-35-35-70 µm		

Section 3C Electrical Characteristics of RH850/F1KM-S1

3C.1 Overview

The electrical spec of this device is guaranteed by the following operational condition. But, this condition is different depends on each characteristics, so refer to each chapter for more detail.

3C.1.1 Pin Groups

3C.1.1.1 100-Pin Version

Symbol	Pin Group Supplied by	Related Pins / Ports
PgR	REGVCC, AWOVSS	X1, X2
PgE	EVCC, EVSS	Related ports: JP0, P0, P8, P9, P10, P11
		Related pins: $\overline{\text{RESET}}$, FLMD0
PgA0	A0VREF, A0VSS	Related port: AP0

3C.1.1.2 80-Pin Version

Symbol	Pin Group Supplied by	Related Pins / Ports
PgR	REGVCC, AWOVSS	X1, X2
PgE	EVCC, EVSS	Related ports: JP0, P0, P8, P9, P10, P11
		Related pins: $\overline{\text{RESET}}$, FLMD0
PgA0	A0VREF, A0VSS	Related port: AP0

3C.1.1.3 64-Pin Version

Symbol	Pin Group Supplied by	Related Pins / Ports
PgR	REGVCC, AWOVSS	X1, X2
PgE	EVCC, EVSS	Related ports: JP0, P0, P8, P9, P10
		Related pins: $\overline{\text{RESET}}$, FLMD0
PgA0	A0VREF, A0VSS	Related port: AP0

3C.1.1.4 48-Pin Version

Symbol	Pin Group Supplied by	Related Pins / Ports
PgR	REGVCC, AWOVSS	X1, X2
PgE	EVCC, EVSS	Related ports: JP0, P0, P8, P9, P10
		Related pins: $\overline{\text{RESET}}$, FLMD0
PgA0	A0VREF, A0VSS	Related port: AP0

3C.1.2 General Measurement Conditions

3C.1.2.1 Common Conditions

- Power supply
  - REGVCC = EVCC = VPOC*[1] to 5.5 V
  - A0VREF = 3.0 V to 5.5 V
  - AWOVSS = ISOVSS = EVSS = A0VSS = 0 V
- Capacitance of the internal regulator
  - CAWOVCL: 0.1 µF ±30%
  - CISOVCL: 0.1 µF ±30%
- Operating temperature
  - Tj = –40 to +130°C @ R7F7016xx3AFP*[2]
  - Tj = –40 to +150°C @ R7F7016xx4AFP*[2]

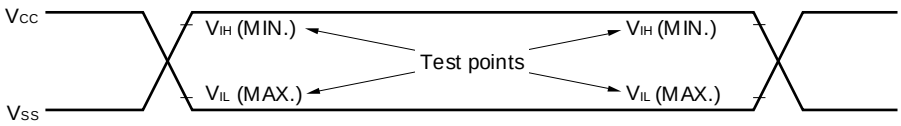
  xx = 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95
- Load conditions
  - CL = 30 pF

Note 1. "VPOC" means POC (power-on clear) detection voltage. For more detail, see **Section 3C.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.

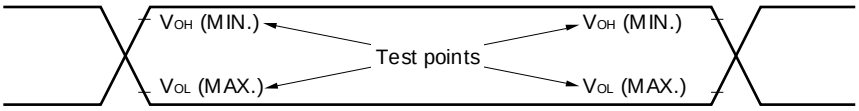
Note 2. Regarding operation temperature of each product, see **Section 1C.3, RH850/F1KM Product Lineup**.

3C.1.2.2 AC Characteristic Measurement Condition

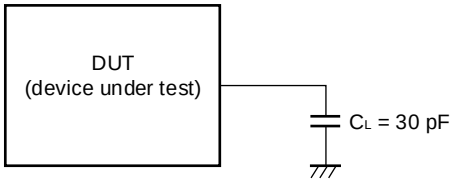
(1) AC Test Input Measurement Points



(2) AC Test Output Measurement Points



(3) Load Conditions



CAUTION

If the load capacitance exceeds 30 pF due to the circuit configuration, it is recommended to insert a buffer in order to reduce capacitance to less than 30 pF.

3C.2 Absolute Maximum Ratings

CAUTIONS

1. Do not directly connect outputs (or input/outputs) to each other, power supply and ground.
2. Even momentarily exceeding the absolute maximum rating for just one item creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings. The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.
3. When designing an external circuit ensure that the connections don't conflict with the port state of this device.

3C.2.1 Supply Voltages

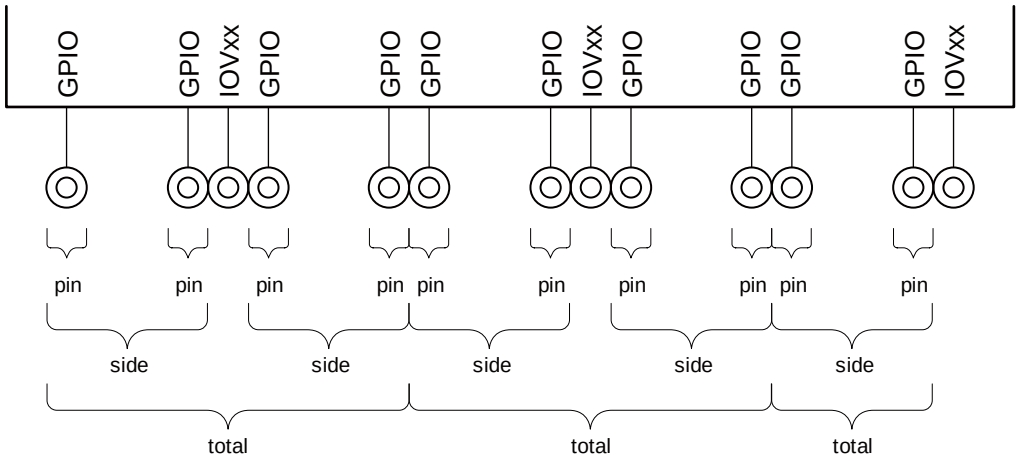
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System supply voltage	REGVCC		–0.5		6.5	V
	AWOVSS		–0.5		0.5	V
	ISOVSS		–0.5		0.5	V
Port supply voltage	EVCC		–0.5		6.5	V
	EVSS		–0.5		0.5	V
A/D-converter supply voltage	A0VREF		–0.5		6.5	V
	A0VSS		–0.5		0.5	V

3C.2.2 Port Voltages

Item	Pin Group*1	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	PgR	VI		–0.5		REGVCC + 0.5 (Do not exceed 6.5 V)	V
	PgE			–0.5		EVCC + 0.5 (Do not exceed 6.5 V)	V
	PgA0			–0.5		A0VREF + 0.5 (Do not exceed 6.5 V)	V

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

3C.2.3 Port Current



Definition of the condition:

- Per pin: Output current of one GPIO
- Per side: Total output current of all GPIO pins on one side of one IOVxx
- Total: Total output current of both sides of one IOVxx

Note:

- GPIO: General-purpose I/O pin (JP0, P0, P8, P9, P10, P11, AP0)
- IOVxx: Power supply pin for I/O pins (EVCC/EVSS, A0VREF/A0VSS)

3C.2.3.1 100-Pin Version

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (Total of P9_0 to P9_6)			–48	mA
			Per side (Total of P0_0 to P0_3, P10_3 to P10_5, P10_15, P11_0)			–48	mA
			Per side (Total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P8_2, P8_10 to P8_12)			–48	mA
			Per side (Total of JP0_0 to JP0_2)			–30	mA
			Per side (Total of P0_7 to P0_10, P8_0, P8_1, P8_3 to P8_9)			–48	mA
			Per side (Total of P10_6 to P10_9)			–40	mA
			Per side(Total of P10_10 to P10_14, P11_1 to P11_7)			–48	mA
			Per side (Total of P10_0 to P10_2)			–30	mA
			Total (EVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (Total of P9_0 to P9_6)			48	mA
			Per side (Total of P0_0 to P0_6, P0_11 to P0_14, P10_3 to P10_5, P10_15, P11_0)			48	mA
			Per side (Total of JP0_0 to JP0_5, P8_2, P8_10 to P8_12)			48	mA
			Per side (Total of P0_7 to P0_10)			40	mA
			Per side (Total of P8_0, P8_1, P8_3 to P8_9)			48	mA
			Per side(Total of P10_6 to P10_14, P11_1, P11_2)			48	mA
			Per side (Total of P11_3 to P11_7)			48	mA
			Per side (Total of P10_0 to P10_2)			30	mA
			Total (EVCC)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA

3C.2.3.2 80-Pin Version

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (Total of P9_0 to P9_6, P10_6 to P10_14, P11_1 to P11_4)			–48	mA
			Per side (Total of P10_0 to P10_2)			–30	mA
			Per side (Total of P0_0 to P0_3, P10_3 to P10_5, P10_15, P11_0)			–48	mA
			Per side (Total of JP0_0 to JP0_5, P0_4 to P0_12, P8_0 to P8_6)			–48	mA
			Total (EVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (Total of P9_0 to P9_6, P10_6 to P10_14, P11_1 to P11_4)			48	mA
			Per side (Total of P10_0 to P10_2)			30	mA
			Per side (Total of P0_0 to P0_6, P0_11, P0_12, P10_3 to P10_5, P10_15, P11_0)			48	mA
			Per side (Total of JP0_0 to JP0_5, P0_7 to P0_10, P8_0 to P8_6)			48	mA
			Total (EVSS)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA

3C.2.3.3 64-Pin Version

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (Total of P9_0 to P9_3, P10_6 to P10_14)			–48	mA
			Per side (Total of P10_0 to P10_2)			–30	mA
			Per side (Total of P0_0 to P0_3, P10_3 to P10_5)			–48	mA
			Per side (Total of JP0_0 to JP0_5, P0_4 to P0_6, P8_0 to P8_6)			–48	mA
			Total (EVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (Total of P9_0 to P9_3, P10_6 to P10_14)			48	mA
			Per side (Total of P10_0 to P10_2)			30	mA
			Per side (Total of P0_0 to P0_6, P10_3 to P10_5)			48	mA
			Per side (Total of JP0_0 to JP0_5, P8_0 to P8_6)			48	mA
			Total (EVSS)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA

3C.2.3.4 48-Pin Version

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (Total of P9_0, P9_1, P10_6 to P10_10)			–48	mA
			Per side (Total of P10_0 to P10_2)			–30	mA
			Per side (Total of P0_0 to P0_3, P10_3 to P10_5)			–48	mA
			Per side (Total of JP0_0 to JP0_5, P8_0, P8_1)			–48	mA
			Total (EVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (Total of P9_0, P9_1, P10_6 to P10_10)			48	mA
			Per side (Total of P10_0 to P10_2)			30	mA
			Per side (Total of P0_0 to P0_3, P10_3 to P10_5)			48	mA
			Per side (Total of JP0_0 to JP0_5, P8_0, P8_1)			48	mA
			Total (EVSS)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA

3C.2.4 Temperature Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Storage temperature	Tstg		–55		150	°C
Junction temperature	Tj	R7F7016xx3AFP	–40		130	°C
		R7F7016xx4AFP	–40		150	°C

Note: xx = 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95

Regarding operation temperature of each product, see **Section 1C.3, RH850/F1KM Product Lineup**.

3C.3 Operational Condition

3C.3.1 Recommended Operating Conditions

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f_{CPUCLK_M}				120	MHz
	f_{CPUCLK_L}	for OSTMn			60	MHz
Peripheral clock (clock domain) frequency*1	f_{CKSCLK_AWDTA}	for WDTA0			240*2	kHz
	f_{CKSCLK_ATAUJ}	for TAUJ0			40	MHz
		for TAUJ2				
	f_{CKSCLK_ARTCA}	for RTCA0			4	MHz
	f_{CKSCLK_AADCA}	for ADCA0			40	MHz
	f_{CKSCLK_AFOUT}	for FOUT			24	MHz
	f_{CKSCLK_IPERI1}	for TAUD0			80	MHz
		for TAUJ1				
		for TAUJ3				
		for ENCA0				
		for TAPA0				
		for PIC0				
	f_{CKSCLK_IPERI2}	for TAUB0			40	MHz
		for RCFDCn (clkc)				
		for RSENTn				
		for PWBAn				
		for PWGAn				
		for PWSAn				
	f_{CKSCLK_ILIN}	for RLIN24n			40	MHz
		for RLIN3n				
	f_{CKSCLK_ICAN}	for RCFDCn (pclk)			80	MHz
	$f_{CKSCLK\_ICANOSC}$	for RCFDCn (clk_xincan)			24	MHz
	f_{CKSCLK_ICSI}	for CSIGn			80	MHz
		for CSIHn				
	$f_{LS\ IntOSC}$	for WDTA1			240*2	kHz
	f_{CKSCLK_IIIC}	for RIICn			40	MHz
	f_{EMCLK}	for LPSn			8	MHz
Power supply	REGVCC	REGVCC = EVCC	VPOC*3		5.5	V
	EVCC					
	A0VREF		3.0		5.5	V
Normal operation voltage	AWOVCL		1.1	1.25	1.35	V
	ISOVCL					
Limited operation voltage*4	AWOVCL		1.35		1.43	V
	ISOVCL					

Note 1. For clock specification of peripherals, see **Section 12C, Clock Controller of RH850/F1KM-S1** of the ***RH850/F1KH, RH850/F1KM User's Manual: Hardware***.

Note 2. This frequency depends on the internal oscillator (LS IntOSC).

Note 3. "VPOC" means POC (power-on clear) detection voltage (TYP. 2.85 V). For detail, see **Section 3C.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.
In addition, the guaranteed operation in DC characteristic.
And AC characteristic is guaranteed when more than 3.0 V.
When the power supply voltage is VPOC to 3.0 V, the device does not malfunction.

Note 4. Reliability restrictions from 1.35 V to 1.43 V.

3C.3.2 Oscillator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C

(1) MainOSC (In Case of Using a Crystal/Ceramic)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MainOSC frequency*3	f_{MOSC}		8		24	MHz
MainOSC current consumption	I_{MOSC}	After stabilization		1.9*2	2.3*2	mA
MainOSC oscillation start point	V_{MOSCSP}		VPOC			V
MainOSC oscillation operating point	V_{MOSCOP}			0.5 × REGVCC*2		V
MainOSC oscillation amplitude	$V_{MOSCAMP}$		0.4 × REGVCC − 0.2*2			V
MainOSC oscillation stabilization time	t_{MSTB}			2*1, *2		ms
MainOSC transconductance	g_{m_MOSC}	MOSCS.MOSCCLKACT = 0, MOSCC.MOSCAMPSEL[1:0] = 00		11.1*2		mA/V
		MOSCS.MOSCCLKACT = 0, MOSCC.MOSCAMPSEL[1:0] = 01		10.6*2		mA/V
		MOSCS.MOSCCLKACT = 0, MOSCC.MOSCAMPSEL[1:0] = 10		9.3*2		mA/V
		MOSCS.MOSCCLKACT = 0, MOSCC.MOSCAMPSEL[1:0] = 11		7.8*2		mA/V
		MOSCS.MOSCCLKACT = 1, MOSCC.MOSCAMPSEL[1:0] = 00		8.6*2		mA/V
		MOSCS.MOSCCLKACT = 1, MOSCC.MOSCAMPSEL[1:0] = 01		7.8*2		mA/V
		MOSCS.MOSCCLKACT = 1, MOSCC.MOSCAMPSEL[1:0] = 10		6.1*2		mA/V
		MOSCS.MOSCCLKACT = 1, MOSCC.MOSCAMPSEL[1:0] = 11		4.0*2		mA/V

Note 1. Oscillator stabilization time is time until being set (“1”) in MOSCS.MOSCCLKACT bit after MOSCE.MOSCENTRG bit is written “1”, and depends on the setting value of MOSCST register. Please decide appropriate oscillation stabilization time by matching test with resonator and oscillation circuit.

Note 2. This is reference value.

Note 3. The following four crystal/ceramic resonator frequencies are supported: 8 MHz, 16 MHz, 20 MHz and 24 MHz.

(2) MainOSC (In Case of External Clock Input to X1)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
X1 clock Input frequency*1	f_{EX}		8		24	MHz
X1 clock Input cycle time	t_{EXCYC}		41.7		125	ns
X1 High level Input voltage	V_{IH}		0.7 × REGVCC		REGVCC + 0.5	V
		@Flash Programing Interface*2	0.8 × REGVCC		REGVCC + 0.5	V
X1 Low level Input voltage	V_{IL}		–0.5		0.3 × REGVCC	V
		@Flash Programing Interface*2	–0.5		0.2 × REGVCC	V
X1 Input leakage current	I_{LIH}	VI = REGVCC			0.5	μA
	I_{LIL}	VI = 0 V			–0.5	μA
X1 clock Input low-level pulse width	t_{EXL}	f_{EX} = 8 MHz	58			ns
		f_{EX} = 16 MHz	26			ns
		f_{EX} = 20 MHz	20			ns
		f_{EX} = 24 MHz	16			ns
X1 clock Input high-level pulse width	t_{EXH}	f_{EX} = 8 MHz	58			ns
		f_{EX} = 16 MHz	26			ns
		f_{EX} = 20 MHz	20			ns
		f_{EX} = 24 MHz	16			ns
X1 clock Input period jitter			–0.3		0.3	ns

Note 1. The following four external clock input frequencies are supported: 8 MHz, 16 MHz, 20 MHz and 24 MHz.

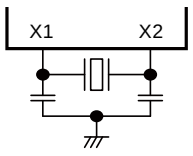
Note 2. X2 should be open and its parasitic capacitance should be less than 5 pF.

CAUTION

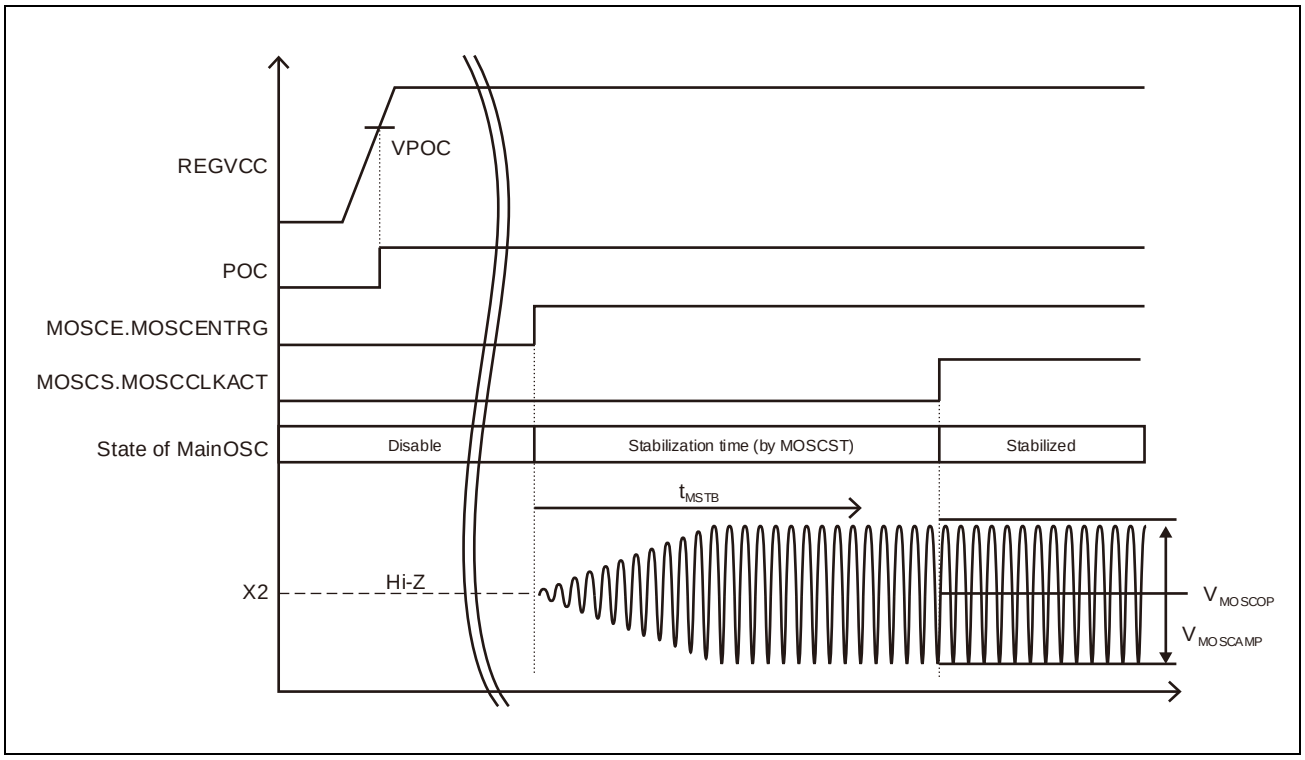
The oscillation stabilization time differs according the matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by an oscillator matching test.

NOTE

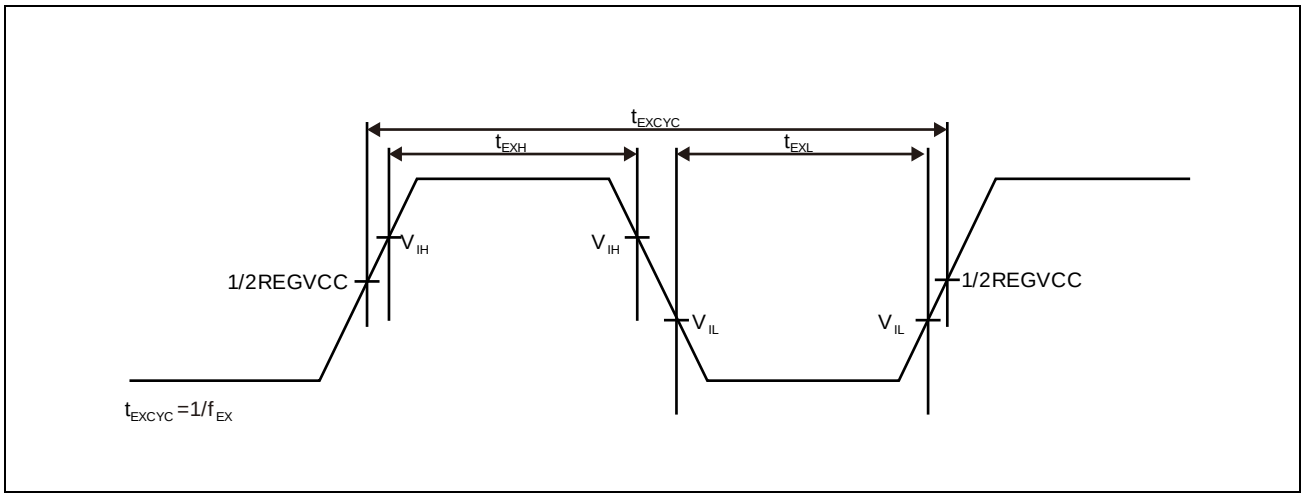
Recommended oscillator circuit is shown below.



MainOSC



External clock



3C.3.3 Internal Oscillator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LS IntOSC frequency	f_{RL}		220.8	240	259.2	kHz
HS IntOSC frequency*2, *3	f_{RH}		7.6	8	8.4	MHz
		After user trimming @ trimming temp	7.92	8	8.08	MHz
HS IntOSC current consumption	I_{RH}	After stabilization			170*1	µA
HS IntOSC oscillation stabilization time	t_{RHSTB}				54.4	µs

Note 1. This is reference value.

Note 2. The HS IntOSC frequency may not meet the specification range (8.00 MHz ±0.4 MHz, 8.00 MHz ±0.08 MHz after user trimming @ trimming temp) in the while writing/erasing the code/data flash.

Note 3. The HS IntOSC frequency may not meet the specification range in the Cyclic STOP/Cyclic RUN mode.

3C.3.4 PLL Characteristics

3C.3.4.1 PLL1 (for CPU/Peripheral) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input frequency	$f_{PLL1CLKIN}$	MainOSC		8		24	MHz
		HS IntOSC	After user trimming @ trimming temp*3, *4	7.92	8.0	8.08	MHz
Output frequency	$f_{CPLL1OUT}$	MainOSC		80		120	MHz
		HS IntOSC*3	After user trimming @ trimming temp*3	79.2	80	80.8	MHz
	$f_{PPLLOUT}$			79.2	80	80.8	MHz
Output period jitter*1	t_{CPJ1}			–100		100	ps
Long term jitter*1	t_{LTJ}	term = 1 µs		–500		500	ps
		term = 10 µs		–1		1	ns
		term = 20 µs		–2		2	ns
Lock time*2	t_{LCK1}			104	112.3	122.1	µs

Note 1. This is reference value.

Note 2. Lock time is time until being set (“1”) in PLL1S.PLL1CLKACT bit after PLL1E.PLL1ENTRG bit is written “1”.

Note 3. The HS IntOSC has a frequency deviation. When the HSIntOSC is used the frequency deviation should be considered for the customer application as it affects peripheral functions (e.g. TAUx, ADCAn, etc.).

Note 4. Do not select the PLL1 as clock source during the code/data flash write and/or erase.

3C.4 DC Characteristics

3C.4.1 Capacitance

Condition: REGVCC = EVCC = A0VREF = AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
Ta = 25°C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI*1	f = 1 MHz			10	pF
Input/output capacitance	CIO*2	0 V for non measurement pins			10	pF

Note 1. CI: Capacitance between the input pin and ground

Note 2. CIO: Capacitance between the input/output pin and ground

3C.4.2 Pin Characteristics

Condition: Some of the conditions mentioned in this chapter can be selected by software and described in the hardware user's manual.

(1/2)

Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
$\overline{\text{RESET}}$	—	—	✓	—	—	—	—	—	—
FLMD0	—	✓	—	—	—	—	—	✓	✓
AP0_0	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_1	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_2	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_3	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_4	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_5	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_6	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_7	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_8	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_9	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_10	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_11	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_12	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_13	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_14	✓	—	—	—	—	✓	Slow	—	✓*1
AP0_15	✓	—	—	—	—	✓	Slow	—	✓*1
JP0_0	—	✓	—	✓	✓	—	Slow	✓	✓
JP0_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
JP0_2	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
JP0_3	—	✓	—	✓	✓	—	Slow/Fast	✓	✓
JP0_4	—	—	—	✓	—*5	—	Slow	✓	✓
JP0_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_2	—	✓	—	✓	—	—	Slow/Fast*2	✓	✓
P0_3	—	✓	—	✓	—	—	Slow/Fast*2	✓	✓
P0_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_5	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P0_6	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P0_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P0_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_1	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓

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Port Input Buffer Function							Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P10_2	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P10_3	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_6	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_7	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_8	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_9	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_10	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_11	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_12	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_13	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_14	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P10_15	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_0	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_1	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_2	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P11_3	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P11_4	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_5	—	✓	—	✓	—	—	Slow/Fast	✓	✓
P11_6	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P11_7	—	✓	—	✓	—	—	Slow/Fast*3	✓	✓
P8_0	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_1	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_2	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_3	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_4	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_5	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_6	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_7	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_8	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_9	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_10	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_11	—	✓	—	✓	—	✓	Slow	✓	✓*4
P8_12	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_0	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_1	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_2	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_3	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_4	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_5	—	✓	—	✓	—	✓	Slow	✓	✓*4
P9_6	—	✓	—	✓	—	✓	Slow	✓	✓*4

Note 1. Pull-down resistor for ADC diagnostic purpose. Control via ADC self-diagnostic register.

Note 2. Supports Cload: 100 pF

Note 3. Supports Cload: 50 pF

Note 4. Pull-down resistors for ADC diagnostic and internal pull-down purposes. For ADC diagnostic, control via ADC self-diagnostic register. For internal pull-down, control via PD register.

Note 5. TTL is selected for Boundary scan mode or Nexus in normal operating mode.

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

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Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH	CMOS		0.65 ×IOVCC		IOVCC + 0.3	V
		SHMT1*3		0.65 × IOVCC		IOVCC + 0.3	V
		SHMT2		0.75 × IOVCC		IOVCC + 0.3	V
		SHMT4		0.8 × IOVCC		IOVCC + 0.3	V
		TTL	EVCC = VPOC to 3.6 V	2.0		IOVCC + 0.3	V
			EVCC = 3.6 V to 5.5 V	2.2		IOVCC + 0.3	V
Low level input voltage	VIL	CMOS		–0.3		0.35 × IOVCC	V
		SHMT1		–0.3		0.35 × IOVCC	V
		SHMT2		–0.3		0.25 × IOVCC	V
		SHMT4		–0.3		0.5 × IOVCC	V
		TTL		–0.3		0.8	V
Input hysteresis for Schmitt	VH	SHMT1		0.3			V
		SHMT2		0.2 × IOVCC			V
		SHMT4		0.1			V
Input leakage current	ILIH	$\overline{\text{RESET}}$, FLMD0, JP0, P0, P8, P9, P10, P11 pin, VI = EVCC*2				0.5	µA
		AP0 pin, VI = A0VREF*2, Tj ≤ 130°C				0.3	µA
		AP0 pin, VI = A0VREF*2				0.5	µA
	ILIL	$\overline{\text{RESET}}$, FLMD0, JP0, P0, P8, P9, P10, P11 pin, VI = 0 V*2				–0.5	µA
		AP0 pin, VI = 0 V*2, Tj ≤ 130°C				–0.3	µA
		AP0 pin, VI = 0 V*2				–0.5	µA
Internal pull-up resistance	RU	except FLMD0 pin, VI = 0 V		20 (275 µA)	40	100	kΩ
		FLMD0 pin, VI = 0 V*3		4 (1375 µA)		36	kΩ
Internal pull-down resistance	RD	except FLMD0 pin, VI = EVCC		20 (275 µA)	40	100	kΩ
		FLMD0 pin, VI = EVCC		4 (1375 µA)		36	kΩ
High level output voltage	VOH	Fast mode	IOH = –5 mA (6 pins) *4	IOVCC – 1.0			V
			IOH = –3 mA (10 pins) *4	IOVCC – 1.0			V
			IOH = –1 mA (16 pins) *4	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins) *4	IOVCC – 0.5			V
		Slow mode	IOH = –1 mA (16 pins) *4	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins) *4	IOVCC – 0.5			V
Low level output voltage	VOL	Fast mode	IOL = 5 mA (6 pins)*4			0.4	V
			IOL = 3 mA (10 pins)*4			0.4	V
			IOL = 1 mA (16 pins)*4			0.4	V
		Slow mode	IOL = 1 mA (16 pins)*4			0.4	V

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Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Rise/Fall time	t_{KRP}/t_{KFP}	Fast mode (except below pins)*5	CL = 30 pF			7	ns
			CL = 50 pF			12	ns
			CL = 100 pF			24	ns
		Fast mode (P0_5, P0_6, P10_1, P10_2, P11_2, P11_3, P11_6, P11_7)*6	CL = 50 pF			6	ns
		Fast mode (P0_2, P0_3)*6	CL = 100 pF			6.15	ns
		Slow mode*5	CL = 30 pF			37	ns
			CL = 50 pF			62	ns
			CL = 100 pF			124	ns
Output frequency	f_O	Fast mode	CL = 30 pF			40	MHz
		Slow mode	CL = 30 pF			10	MHz
			CL = 50 pF			6	MHz
			CL = 100 pF			3	MHz

Note 1. “IOVCC” means the pins are assigned to the power supply (EVCC, and A0VREF).

Note 2. Not select the analog input function of ADCn.

Note 3. When the internal pull-up resistor of FLMD0 pin is applied by FLMDCNT register, please connect 86 kΩ or more as external pull-down resistor.

Note 4. The number of pin indicates simultaneous ON.

Note 5. Measurement point: 0.1 × IOVCC to 0.9 × IOVCC

Note 6. Measurement point: 0.2 × IOVCC to 0.8 × IOVCC

3C.4.2.1 Output Current

(1) 100-Pin Version

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_6			–7	mA
				P0_0 to P0_3, P10_3 to P10_5, P10_15, P11_0			–30	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2			–11	mA
				P0_7 to P0_10, P8_0, P8_1, P8_3 to P8_9			–29	mA
				P10_6 to P10_9			–20	mA
				P10_10 to P10_14, P11_1 to P11_7			–30	mA
				P10_0 to P10_2			–15	mA
			Total (EVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
Low-level output current	IOL	PgE	Per side	P9_0 to P9_6			7	mA
				P0_0 to P0_6, P0_11 to P0_14, P10_3 to P10_5, P10_15, P11_0			30	mA
				JP0_0 to JP0_5, P8_2, P8_10 to P8_12			26	mA
				P0_7 to P0_10			20	mA
				P8_0, P8_1, P8_3 to P8_9			9	mA
				P10_6 to P10_14, P11_1, P11_2			30	mA
				P11_3 to P11_7			25	mA
				P10_0 to P10_2			15	mA
			Total (EVSS)				60	mA
		PgA0	Total (A0VSS)				16	mA

Note: For detail of the definition of “side” and “total”, see **Section 3C.2.3, Port Current**.

(2) 80-Pin Version

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_6, P10_6 to P10_14, P11_1 to P11_4			–30	mA
				P10_0 to P10_2			–15	mA
				P0_0 to P0_3, P10_3 to P10_5, P10_15, P11_0			–30	mA
				JP0_0 to JP0_5, P0_4 to P0_12, P8_0 to P8_6			–30	mA
			Total (EVCC)				–60	mA
		PgA0	Total (A0VREF)				–11	mA
Low-level output current	IOL	PgE	Per side	P9_0 to P9_6, P10_6 to P10_14, P11_1 to P11_4			30	mA
				P10_0 to P10_2			15	mA
				P0_0 to P0_6, P0_11, P0_12, P10_3 to P10_5, P10_15, P11_0			30	mA
				JP0_0 to JP0_5, P0_7 to P0_10, P8_0 to P8_6			21	mA
			Total (EVSS)				60	mA
		PgA0	Total (A0VSS)				11	mA

Note: For detail of the definition of “side” and “total”, see **Section 3C.2.3, Port Current**.

(3) 64-Pin Version

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_3, P10_6 to P10_14			–30	mA
				P10_0 to P10_2			–15	mA
				P0_0 to P0_3, P10_3 to P10_5			–27	mA
				JP0_0 to JP0_5, P0_4 to P0_6, P8_0 to P8_6			–24	mA
			Total (EVCC)				–60	mA
		PgA0	Total (A0VREF)				–10	mA
Low-level output current	IOL	PgE	Per side	P9_0 to P9_3, P10_6 to P10_14			30	mA
				P10_0 to P10_2			15	mA
				P0_0 to P0_6, P10_3 to P10_5			30	mA
				JP0_0 to JP0_5, P8_0 to P8_6			13	mA
			Total (EVSS)				60	mA
		PgA0	Total (A0VSS)				10	mA

Note: For detail of the definition of “side” and “total”, see **Section 3C.2.3, Port Current**.

(4) 48-Pin Version

Item	Symbol	Pin Group	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0, P9_1, P10_6 to P10_10			–27	mA
				P10_0 to P10_2			–15	mA
				P0_0 to P0_3, P10_3 to P10_5			–27	mA
				JP0_0 to JP0_5, P8_0, P8_1			–8	mA
			Total (EVCC)				–60	mA
		PgA0	Total (A0VREF)				–8	mA
Low-level output current	IOL	PgE	Per side	P9_0, P9_1, P10_6 to P10_10			27	mA
				P10_0 to P10_2			15	mA
				P0_0 to P0_3, P10_3 to P10_5			27	mA
				JP0_0 to JP0_5, P8_0, P8_1			8	mA
			Total (EVSS)				60	mA
		PgA0	Total (A0VSS)				8	mA

Note: For detail of the definition of “side” and “total”, see **Section 3C.2.3, Port Current**.

3C.4.3 Power Supply Currents

Condition: REGVCC, EVCC, A0VREF total current. But the I/O buffer is stopped.

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2				
RUN mode current	IDDR	Run (120 MHz)	Run	–40 to 150°C	Run(#1)		32	67	mA
				25°C	Stop(#1)		26		mA
RUN mode current (During data/code flash programming)	IDDR3	Run (120 MHz)	Run	–40 to 150°C	Run(#2)		43	82	mA
RUN mode current (HALT state)	IDDH	Run (120 MHz)	Run	–40 to 150°C	Run(#3)		29	63	mA

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2				
STOP mode current	IDDS	Stop	Stop	–40 to 90°C	Stop(#2)		0.7	12	mA
				110°C	Stop(#2)			17	mA
				135°C	Stop(#2)			31	mA
DeepSTOP mode current	IDDDS	Power off	Power off	–40 to 85°C	Stop(#3)		50	470	µA
				105°C	Stop(#3)			830	µA
				125°C	Stop(#3)			1370	µA
Cyclic RUN mode current	IDDCR	Run (HS IntOSC)	Stop	–40 to 90°C	Run(#4)		3.6	21	mA
				115°C	Run(#4)			28	mA
				135°C	Run(#4)			40	mA
Cyclic STOP mode current	IDDCS	Stop	Stop	–40 to 90°C	Run(#5)		1.1	13	mA
				110°C	Run(#5)			18	mA
				135°C	Run(#5)			32	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- REGVCC = EVCC = A0VREF = 5.0 V
- AWOVSS = EVSS = A0VSS = 0 V

Note 2. Operating condition of each peripheral function is shown in the table of next page.

Caution: It must be ensured that the junction temperature in the Ta range remains below Tj ≤ 150°C and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

Function		Run					Stop		
		(#1)	(#2)	(#3)	(#4)	(#5)	(#1)	(#2)	(#3)
AWO	MainOSC	Run	Run	Run	Stop	Stop	Run	Stop	Stop
	HS IntOSC	Run	Run	Run	Run	Stop	Run	Stop	Stop
	FOUT	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	LPS	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	RRAM	Read/Write	Read/Write	No access	Fetch	No access	Read/Write	No access	No access
	WDTA0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	TAUJ0, TAUJ2	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Stop	Stop	Stop
	RTCA0	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Stop	Stop	Stop
	CLMA0	Run	Run	Run	Run	Stop	Stop	Stop	Stop
	CLMA1	Run	Run	Run	Stop	Stop	Stop	Stop	Stop
	ADCA0	Run*1	Run*1	Run*1	Stop	Stop	Stop	Stop	Stop
ISO	CPU	Run (PLL1)	Run (PLL1)	HALT (PLL1)	Run (HS IntOSC)	Stop	Run (PLL1)	Stop	Power off
	DMA	Run	Run	Run	Stop	Stop	Stop	Stop	
	PLL1	Run	Run	Run	Stop	Stop	Run	Stop	
	Code flash	Fetch	Fetch	No access	No access	No access	Fetch	No access	
	Data flash	Read	Write/Erase	No access	No access	No access	Read	No access	
	LRAM	Read/Write	Read/Write	No access	No access	No access	Read/Write	No access	
	OSTM0	Run	Run	Run	Stop	Stop	Stop	Stop	
	WDTA1	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	TAUD0	Run	Run	Run	Stop	Stop	Stop	Stop	
	TAUBn	Run	Run	Run	Stop	Stop	Stop	Stop	
	TAUJ1, TAUJ3	Run	Run	Run	Stop	Stop	Stop	Stop	
	TAPA, PIC	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	ENCA0	Run	Run	Run	Stop	Stop	Stop	Stop	
	PWM-diag	Run	Run	Run	Stop	Stop	Stop	Stop	
	RLIN3n	Run	Run	Run	Stop	Stop	Stop	Stop	
	RLIN24n	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	RCFDCn	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	CSIGn	Run	Run	Run	Stop	Stop	Stop	Stop	
	CSIHn	Run	Run	Run	Stop	Stop	Stop	Stop	
	RIICn	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	KR	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	RSENTn	Run	Run	Run	Stop	Stop	Stop	Stop	
	CLMA3	Run	Run	Run	Stop	Stop	Stop	Stop	

Note 1. T&H used.

3C.4.4 Injection Currents

Table 3C.1 Definition of Pin Group (100-Pin Version)

Symbol	Power Supply for Pin Group	Pin
PgE	EVCC, EVSS	JP0, P0, P10, P11
PgE’	EVCC, EVSS	P8, P9
PgA0	A0VREF, A0VSS	AP0

Table 3C.2 Definition of Pin Group (80-Pin Version)

Symbol	Power Supply for Pin Group	Pin
PgE	EVCC, EVSS	JP0, P0, P10, P11
PgE’	EVCC, EVSS	P8, P9
PgA0	A0VREF, A0VSS	AP0

Table 3C.3 Definition of Pin Group (64-Pin Version)

Symbol	Power Supply for Pin Group	Pin
PgE	EVCC, EVSS	JP0, P0, P10
PgE’	EVCC, EVSS	P8, P9
PgA0	A0VREF, A0VSS	AP0

Table 3C.4 Definition of Pin Group (48-Pin Version)

Symbol	Power Supply for Pin Group	Pin
PgE	EVCC, EVSS	JP0, P0, P10
PgE’	EVCC, EVSS	P8, P9
PgA0	A0VREF, A0VSS	AP0

3C.4.4.1 Absolute Maximum Ratings

(1) 100-Pin Version

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJPM}	PgE	Per pin			10	mA
			Total			60	mA
		PgE'	Per pin			10	mA
			Total			60	mA
		PgA0	Per pin			10	mA
			Total			60	mA
Negative overload current VIN < VSS	I_{INJNM}	PgE	Per pin			–10	mA
			Total			–60	mA
		PgE'	Per pin			–10	mA
			Total			–60	mA
		PgA0	Per pin			–10	mA
			Total			–60	mA

CAUTIONS

1. The DC injection current (Total) must satisfy the specifications of the injection current per pin.
2. In case of an injected current condition for PgA0, TESH0SN is kept when the injected current is applied to an adjacent pin where the ADC self-diagnosis is executed. When an injected current is applied to the same pin where the ADC self-diagnosis is executed the TESH0SN deviating value will increase sharply with increasing absolute value of injection current.

(2) 80-Pin Version

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJPM}	PgE	Per pin			10	mA
			Total			60	mA
		PgE'	Per pin			10	mA
			Total			60	mA
		PgA0	Per pin			10	mA
			Total			60	mA
Negative overload current VIN < VSS	I_{INJNM}	PgE	Per pin			–10	mA
			Total			–60	mA
		PgE'	Per pin			–10	mA
			Total			–60	mA
		PgA0	Per pin			–10	mA
			Total			–60	mA

CAUTIONS

1. The DC injection current (Total) must satisfy the specifications of the injection current per pin.
2. In case of an injected current condition for PgA0, TESH0SN is kept when the injected current is applied to an adjacent pin where the ADC self-diagnosis is executed. When an injected current is applied to the same pin where the ADC self-diagnosis is executed the TESH0SN deviating value will increase sharply with increasing absolute value of injection current.

(3) 64-Pin Version

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJPM}	PgE	Per pin			10	mA
			Total			60	mA
		PgE'	Per pin			10	mA
			Total			60	mA
		PgA0	Per pin			10	mA
			Total			60	mA
Negative overload current VIN < VSS	I_{INJNM}	PgE	Per pin			–10	mA
			Total			–60	mA
		PgE'	Per pin			–10	mA
			Total			–60	mA
		PgA0	Per pin			–10	mA
			Total			–60	mA

CAUTIONS

1. The DC injection current (Total) must satisfy the specifications of the injection current per pin.
2. In case of an injected current condition for PgA0, TESH0SN is kept when the injected current is applied to an adjacent pin where the ADC self-diagnosis is executed. When an injected current is applied to the same pin where the ADC self-diagnosis is executed the TESH0SN deviating value will increase sharply with increasing absolute value of injection current.

(4) 48-Pin Version

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJPM}	PgE	Per pin			10	mA
			Total			60	mA
		PgE'	Per pin			10	mA
			Total			60	mA
		PgA0	Per pin			10	mA
			Total			60	mA
Negative overload current VIN < VSS	I_{INJNM}	PgE	Per pin			–10	mA
			Total			–60	mA
		PgE'	Per pin			–10	mA
			Total			–60	mA
		PgA0	Per pin			–10	mA
			Total			–60	mA

CAUTIONS

1. The DC injection current (Total) must satisfy the specifications of the injection current per pin.
2. In case of an injected current condition for PgA0, TESH0SN is kept when the injected current is applied to an adjacent pin where the ADC self-diagnosis is executed. When an injected current is applied to the same pin where the ADC self-diagnosis is executed the TESH0SN deviating value will increase sharply with increasing absolute value of injection current.

3C.4.4.2 DC Characteristics for Overload Current

(1) 100-Pin Version

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJP}	PgE	Per pin			2	mA
			Total			50	mA
		PgE'	Per pin			3	mA
			Total			20	mA
		PgA0	Per pin			3	mA
			Total			20	mA
Negative overload current VIN < VSS	I_{INJN}	PgE	Per pin			–2	mA
			Total			–50	mA
		PgE'	Per pin			–3	mA
			Total			–20	mA
		PgA0	Per pin			–3	mA
			Total			–20	mA

NOTE

These specifications are not tested on sorting and are specified based on the device characterization.

(2) 80-Pin Version

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJP}	PgE	Per pin			2	mA
			Total			50	mA
		PgE'	Per pin			3	mA
			Total			20	mA
		PgA0	Per pin			3	mA
			Total			20	mA
Negative overload current VIN < VSS	I_{INJN}	PgE	Per pin			–2	mA
			Total			–50	mA
		PgE'	Per pin			–3	mA
			Total			–20	mA
		PgA0	Per pin			–3	mA
			Total			–20	mA

NOTE

These specifications are not tested on sorting and are specified based on the device characterization.

(3) 64-Pin Version

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJP}	PgE	Per pin			2	mA
			Total			50	mA
		PgE’	Per pin			3	mA
			Total			20	mA
		PgA0	Per pin			3	mA
			Total			20	mA
Negative overload current VIN < VSS	I_{INJN}	PgE	Per pin			–2	mA
			Total			–50	mA
		PgE’	Per pin			–3	mA
			Total			–20	mA
		PgA0	Per pin			–3	mA
			Total			–20	mA

NOTE

These specifications are not tested on sorting and are specified based on the device characterization.

(4) 48-Pin Version

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJP}	PgE	Per pin			2	mA
			Total			50	mA
		PgE’	Per pin			3	mA
			Total			20	mA
		PgA0	Per pin			3	mA
			Total			20	mA
Negative overload current VIN < VSS	I_{INJN}	PgE	Per pin			–2	mA
			Total			–50	mA
		PgE’	Per pin			–3	mA
			Total			–20	mA
		PgA0	Per pin			–3	mA
			Total			–20	mA

NOTE

These specifications are not tested on sorting and are specified based on the device characterization.

3C.4.5 Power Management Characteristics

3C.4.5.1 Regulator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	REGVCC		VPOC*1		5.5	V
Output voltage	AWOVCL	AWOVCL pin	1.15	1.25	1.35	V
	ISOVCL	ISOVCL pin	1.15	1.25	1.35	V
Capacitance	CAWOVCL	AWOVCL pin	0.07	0.10	0.13	µF
	CISOVCL	ISOVCL pin	0.07	0.10	0.13	µF
Equivalent series resistance for load capacitance	RVRAWO	for CAWOVCL			40*2	mΩ
	RVRISO	for CISOVCL			40*2	mΩ
Inrush current during power-on					120	mA

Note 1. “VPOC” means POC (power-on clear) detection voltage (typ. 2.85 V). For detail, see **Section 3C.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.

Note 2. This is reference value.

3C.4.5.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Detection voltage (REGVCC)	VPOC	POC			2.7	2.85	3.0	V
	VLVI0	LVI	Rise		3.87	4.0	4.13	V
			Fall		3.9	4.0	4.1	V
	VLVI1		Rise		3.57	3.7	3.83	V
			Fall		3.6	3.7	3.8	V
	VLVI2		Rise		3.37	3.5	3.63	V
			Fall		3.4	3.5	3.6	V
	VVLVI	VLVI			1.8	1.9	2.0	V
Detection voltage (ISOVCL)	VCVMH	CVM	High voltage[Caution]		1.35	1.39	1.43	V
	VCVML*8		Low voltage[Caution]		1.10	1.15	1.20	V
Response time	t_{D_POC1}*6	POC	At power-on (Rise)	*1			2	ms
				*2			6.3	ms
			After power-on (Rise)	*3			2	ms
				*4			5	ms
	t_{D_POC2}*7		After power-on (Fall)	*5			5	µs
	t_{D_LVI}	LVI					2	ms
	t_{D_VLVI}	VLVI		*3			2	ms
				*4			5	ms
	t_{D_CVM}	CVM			0.2		10	µs
Setup time	t_{S_LVI}	LVI	LVICNT0,1 bits are set to 1 (except 00_B), then LVI is ready to operate				80	µs
REGVCC minimum width	t_{W_POC}	POC			0.2			ms
	t_{W_LVI}	LVI			0.2			ms
	t_{W_VLVI}	VLVI			0.2			ms

Note 1. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms

Note 2. Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms

Note 3. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 20 V/ms

Note 4. Voltage slope (t_{VS}): 20 V/ms < t_{VS} ≤ 500 V/ms

Note 5. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 500 V/ms

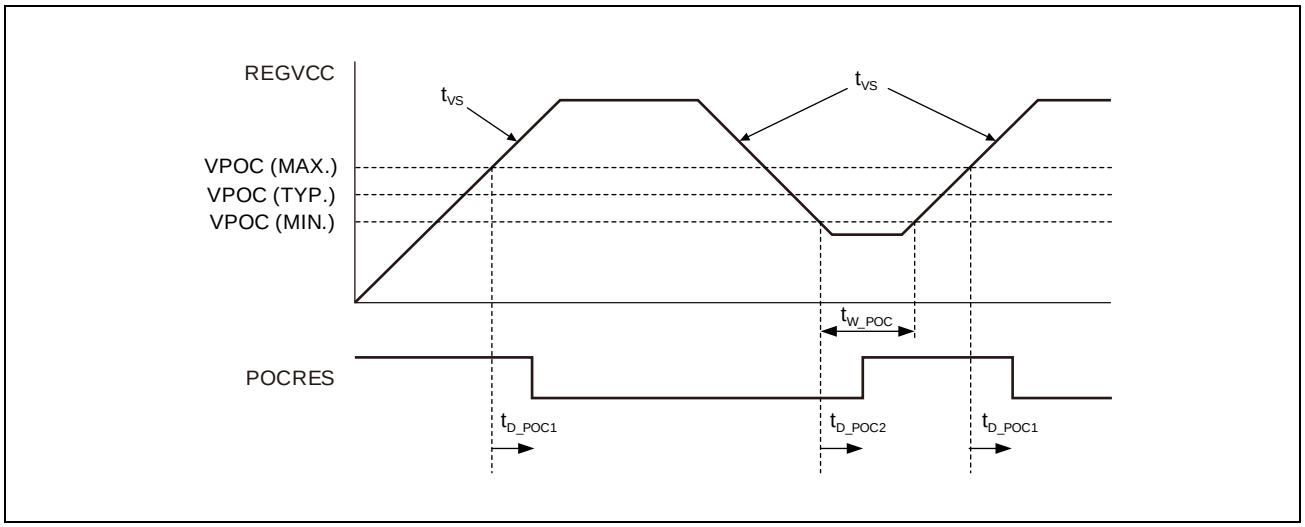
Note 6. t_{D_POC1} is the time from detection voltage to release of reset signal.

Note 7. t_{D_POC2} is the time from detection voltage to occurrence of reset signal.

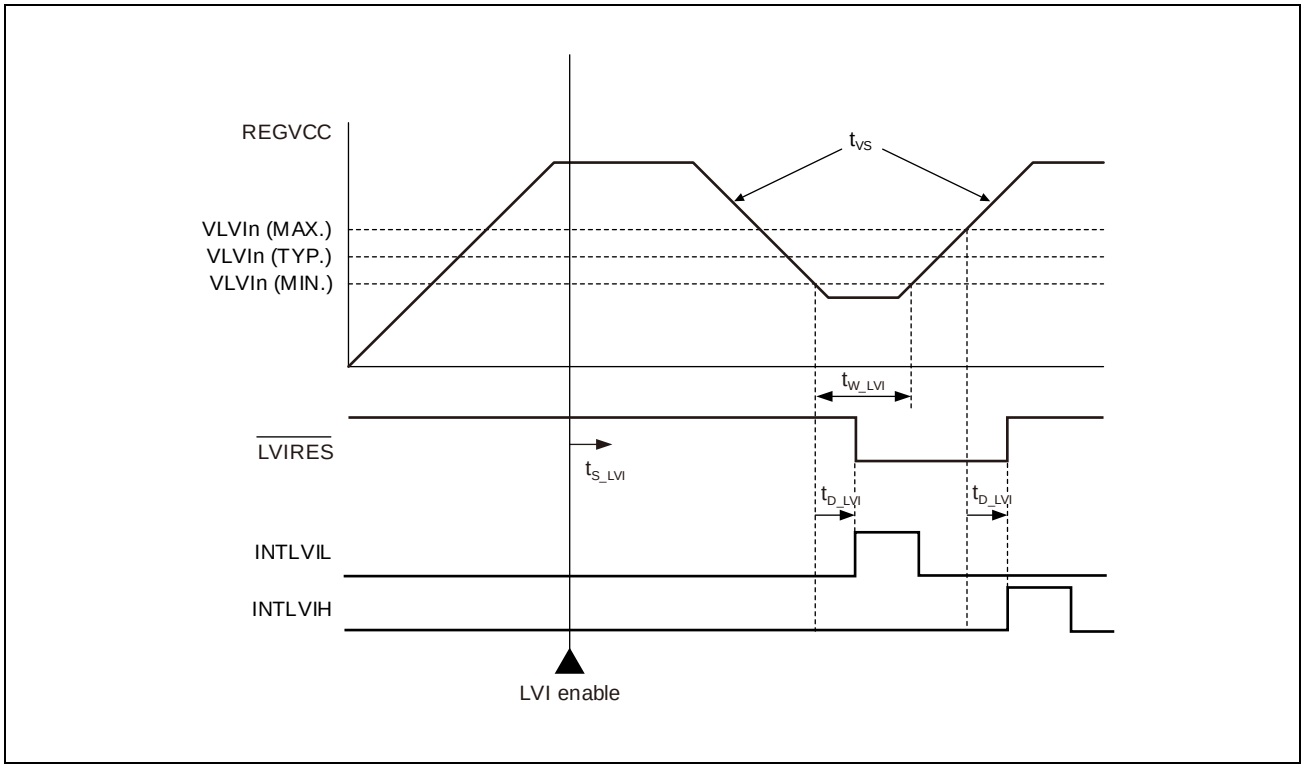
Note 8. The CVM monitors the internal voltage regulator output to ensure that ISOVCL is upper than specified minimum level.

Caution: A detection of the voltage ISOVCL outside the specified level of VCVMH and VCVML is not ensured by CVM.

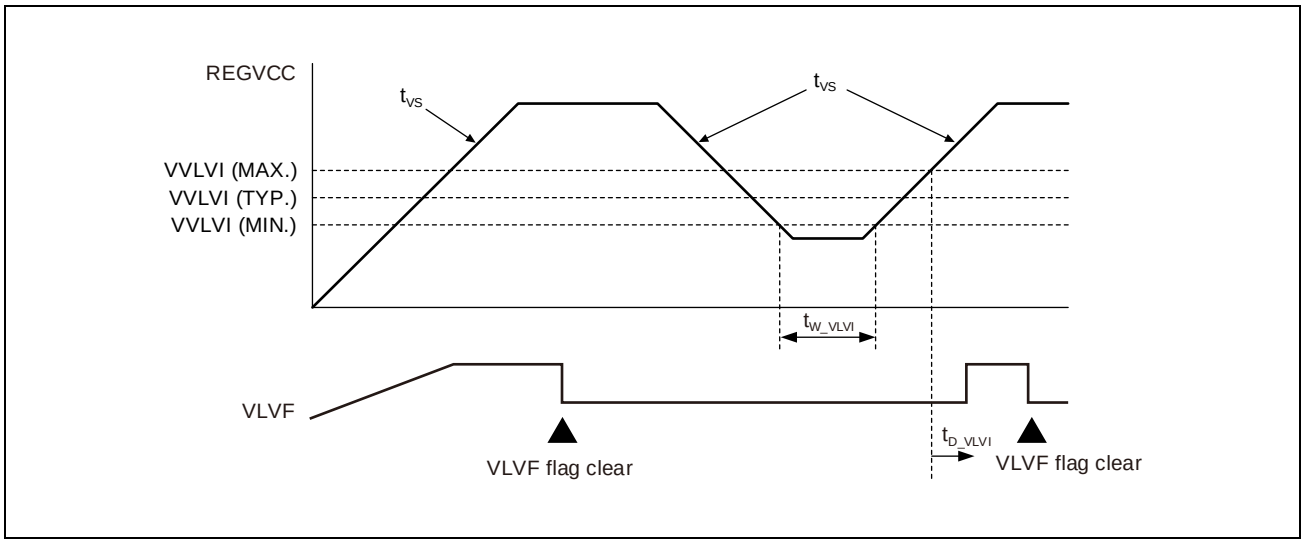
POC


REGVCC
VPOC (MAX.)
VPOC (TYP.)
VPOC (MIN.)
POCRES
tVS
tVS
tW_POC
tD_POC1
tD_POC2
tD_POC1

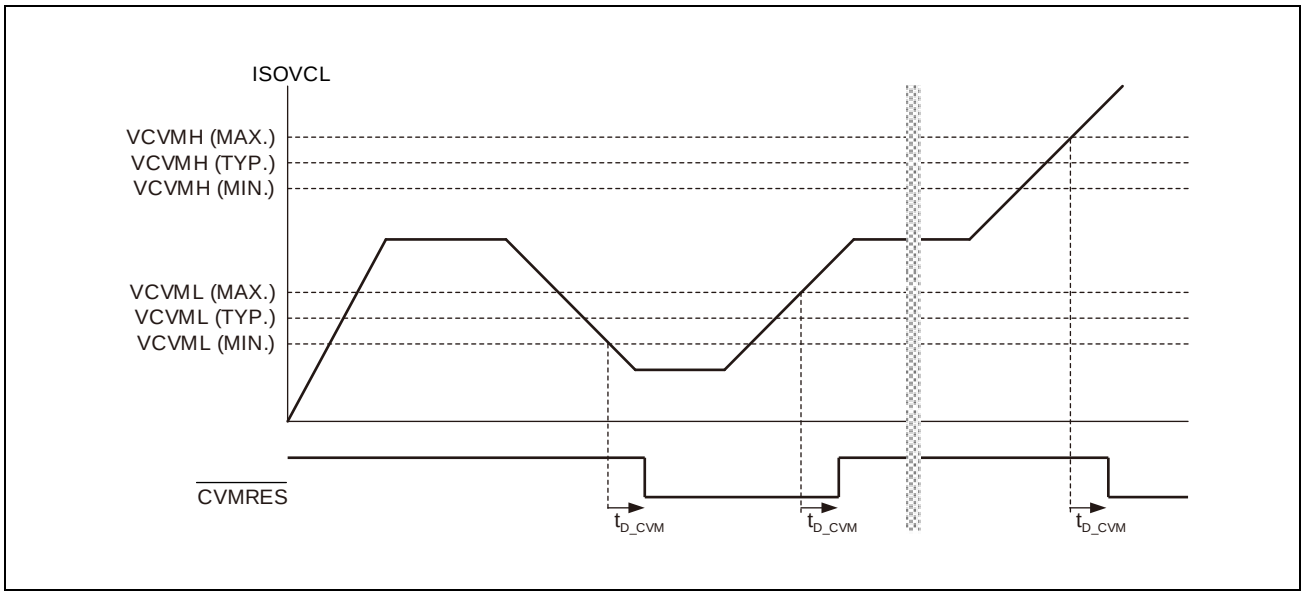
LVI


REGVCC
VLVIn (MAX.)
VLVIn (TYP.)
VLVIn (MIN.)
LVIRES
INTLVIL
INTLVIH
tVS
tW_LVI
tS_LVI
tD_LVI
tD_LVI
LVI enable

VLVI


REGVCC
t_{VS}
t_{VS}
VVLVI (MAX.)
VVLVI (TYP.)
VVLVI (MIN.)
t_{W_VLVI}
VLVF
VLVF flag clear
t_{D_VLVI}
VLVF flag clear

CVM


ISOVCL
VCVMH (MAX.)
VCVMH (TYP.)
VCVMH (MIN.)
VCVML (MAX.)
VCVML (TYP.)
VCVML (MIN.)
$\overline{CVMRES}$
t_{D_CVM}
t_{D_CVM}
t_{D_CVM}

3C.4.5.3 Power Up/Down Timing

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3C.5 In Case the $\overline{\text{RESET}}$ Pin is Used (for Normal Operating Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 hold time (vs $\overline{\text{RESET}}$ ↑)	t_{HMDR}		1			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↓)	t_{SMDF}		0			µs
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms

Note 1. IOVCC means EVCC, A0VREF.

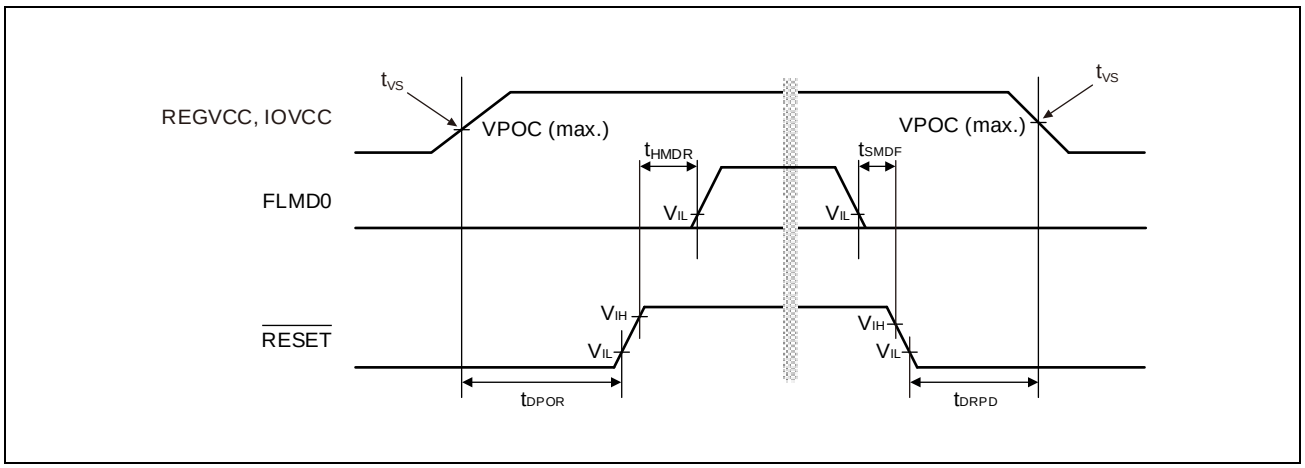


Table 3C.6 In Case the $\overline{\text{RESET}}$ Pin is Used (for Serial Programming Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms

Note 1. IOVCC means EVCC, A0VREF.

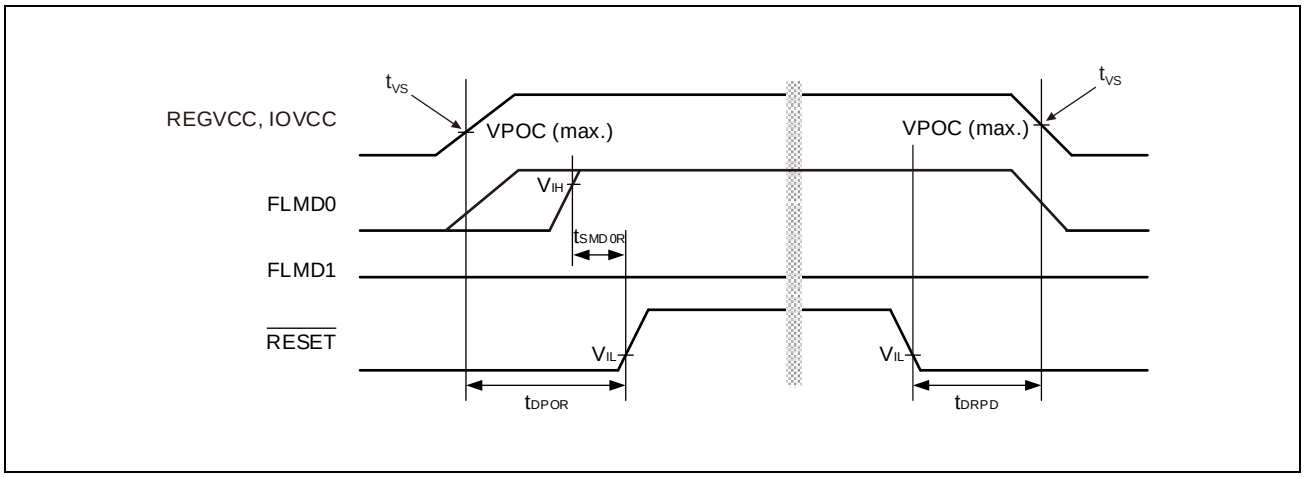


Table 3C.7 In Case the $\overline{\text{RESET}}$ Pin is Used (for Boundary Scan Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
FLMD1, MODE0, MODE1 setup time (vs FLMD0 ↑)	t_{SMD1R}		1			µs
FLMD0 hold time (vs $\overline{\text{RESET}}$ ↓)	t_{HMD0F}		1			µs
FLMD1, MODE0, MODE1 MODE2 hold time (vs FLMD0 ↓)	t_{HMD1F}		1			µs
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms
$\overline{\text{DCUTRST}}$ input delay time (vs $\overline{\text{RESET}}$ ↑)	t_{DRTRST}		1			ms
$\overline{\text{RESET}}$ hold time (vs $\overline{\text{DCUTRST}}$ ↓)	t_{HRTRST}		0			ms

Note 1. IOVCC means EVCC, and A0VREF.

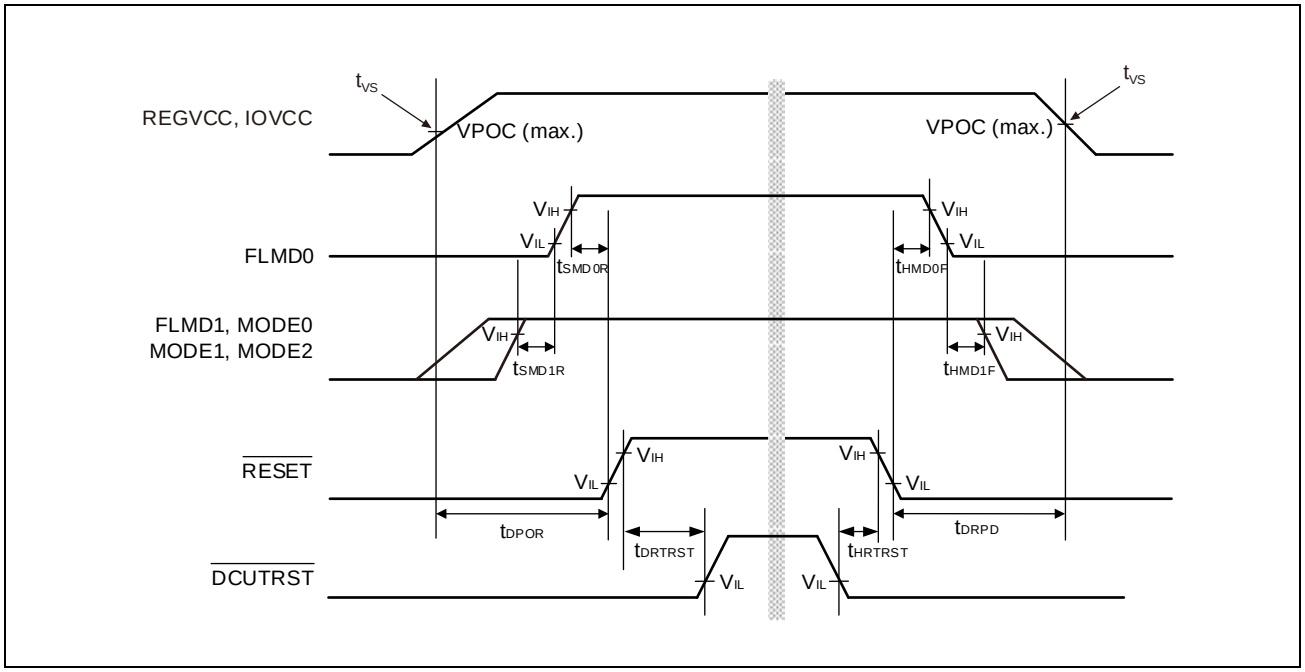


Table 3C.8 In Case the $\overline{\text{RESET}}$ Pin is Used (for User Boot Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500V/ms	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
FLMD1, MODE0, MODE1,MODE2 setup time (vs FLMD0 ↑)	t_{SMD1R}		1			µs
FLMD0 hold time (vs $\overline{\text{RESET}}$ ↓)	t_{HMD0F}		1			µs
FLMD1, MODE0, MODE1, MODE2 hold time (vs FLMD0 ↓)	t_{HMD1F}		1			µs
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC ↓ delay time	t_{DRPD}		0			ms

Note 1. IOVCC means EVCC, A0VREF.

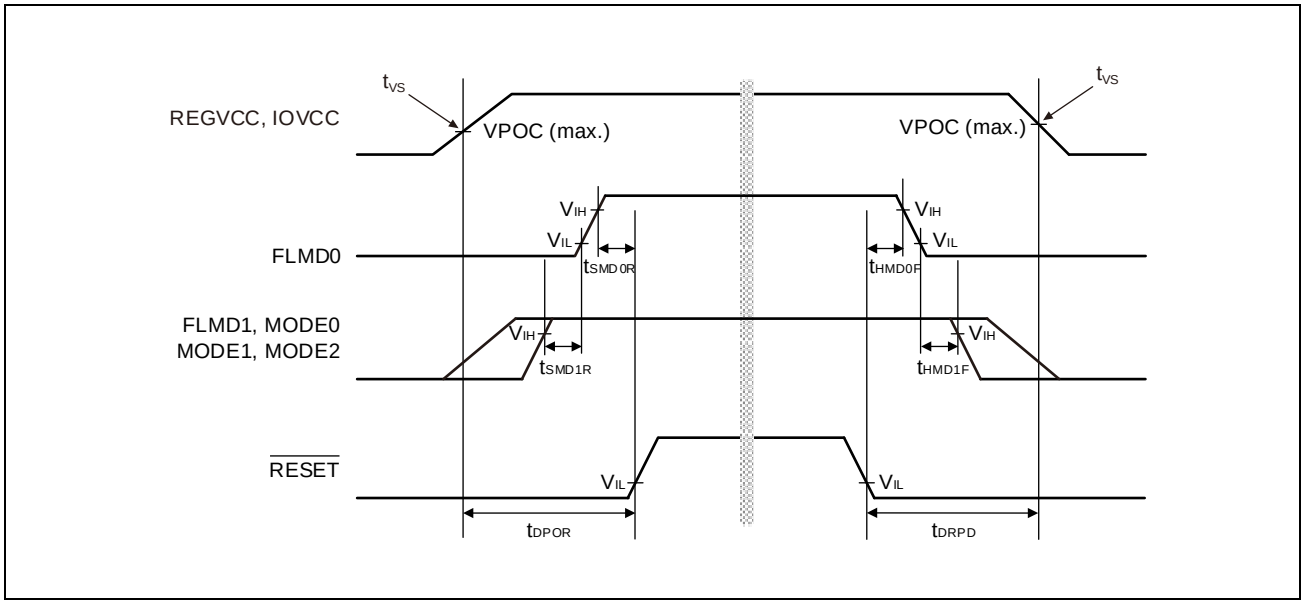
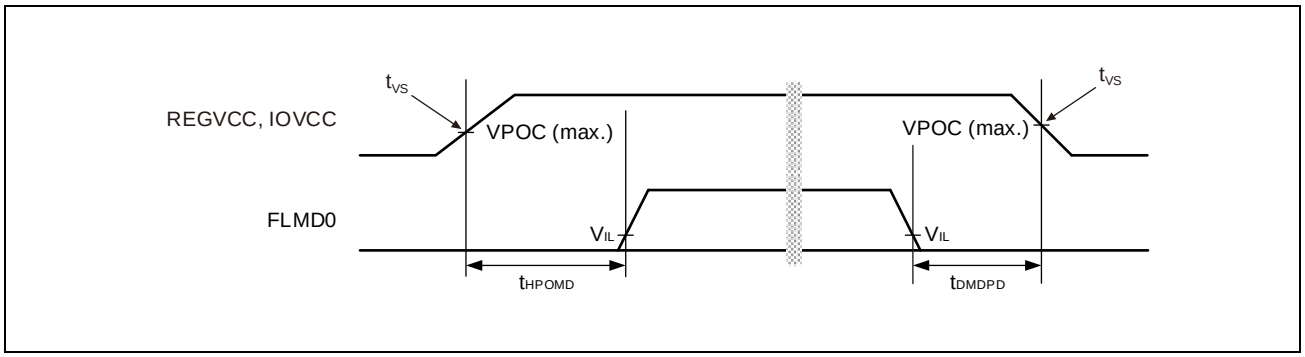


Table 3C.9 In Case the $\overline{\text{RESET}}$ Pin is Not Used and Fixed to High Level by Pull-up*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*2)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*2 ↑ to FLMD0 hold time	t_{HPOMD}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 ↓ to REGVCC ↓ and IOVCC*2 ↓ delay time	t_{DMDPD}		1			µs

Note 1. This operating condition is available only in normal operation mode (include self-programming mode). When the device is used in except normal operation mode, please use the $\overline{\text{RESET}}$ pin.

Note 2. IOVCC means EVCC, and A0VREF.



3C.4.5.4 CPU Reset Release Timing

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3C.10 In Case the $\overline{\text{RESET}}$ Pin is Not Used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REGVCC ↑ to CPU reset release*1	t_{DPCRR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms			2.58	ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms			8.3	ms

Note 1. This is reference value.

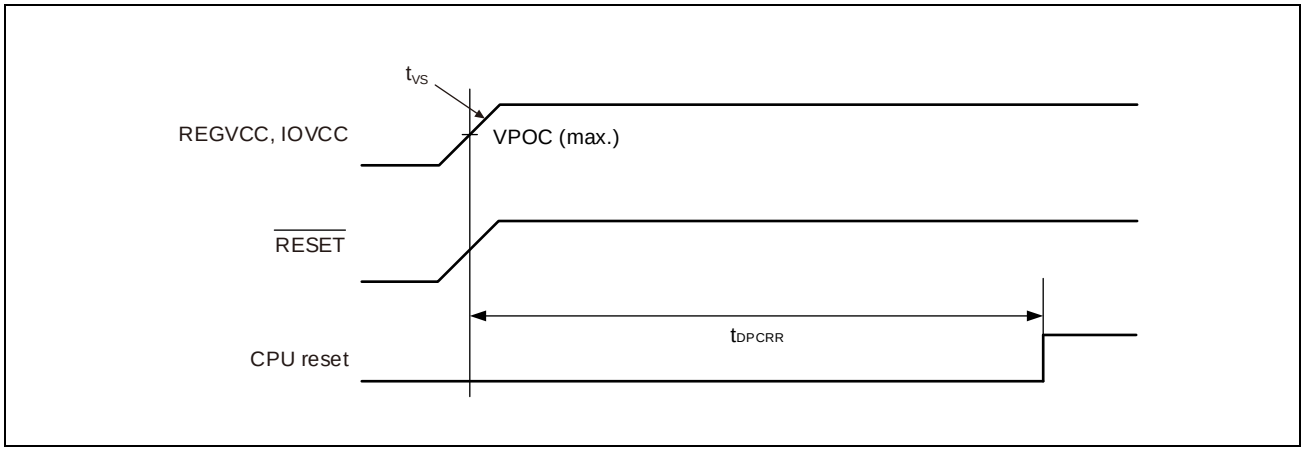
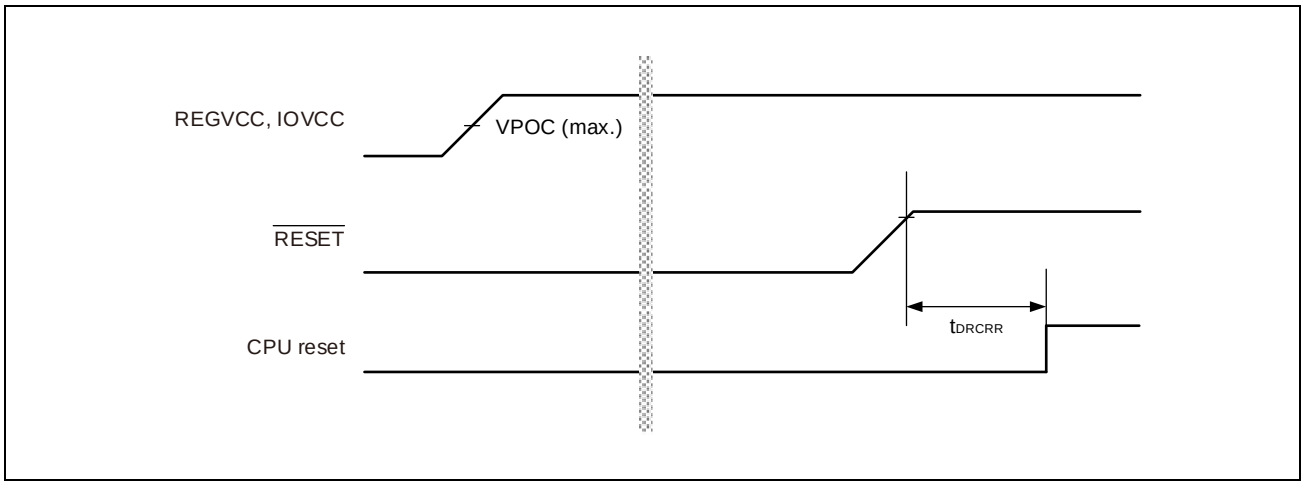


Table 3C.11 In Case the $\overline{\text{RESET}}$ Pin is Used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ ↑ to CPU reset release*1	t_{DRCRR}				16*2	µs

Note 1. This is reference value.

Note 2. In case the time until releasing the $\overline{\text{RESET}}$ pin is longer than t_{DPCRR}.



3C.5 AC Characteristics

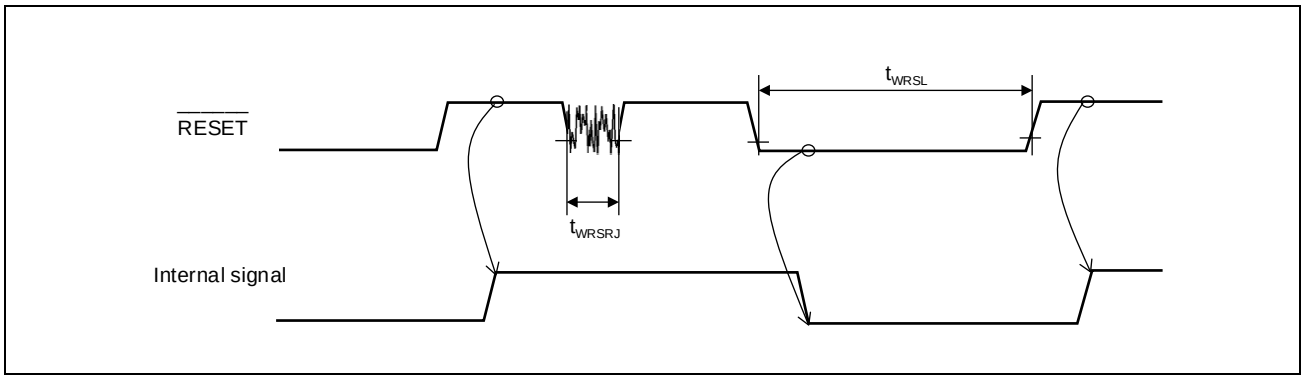
3C.5.1 $\overline{\text{RESET}}$ Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width*1	t_{WRSL}	Except power on	600			ns
$\overline{\text{RESET}}$ pulse rejection*2	t_{WRSRJ}		100			ns

Note 1. $\overline{\text{RESET}}$ input width is needed to ensure that the internal reset signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



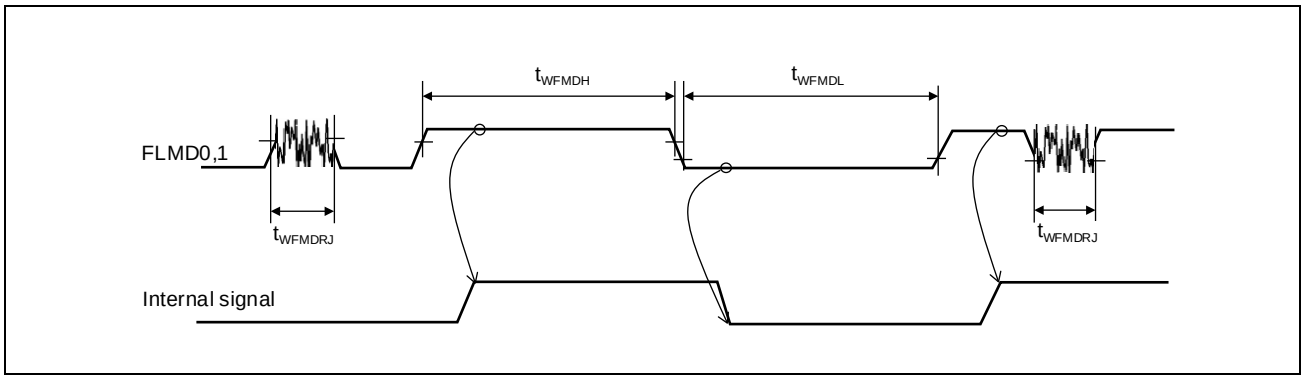
3C.5.2 Mode Timing

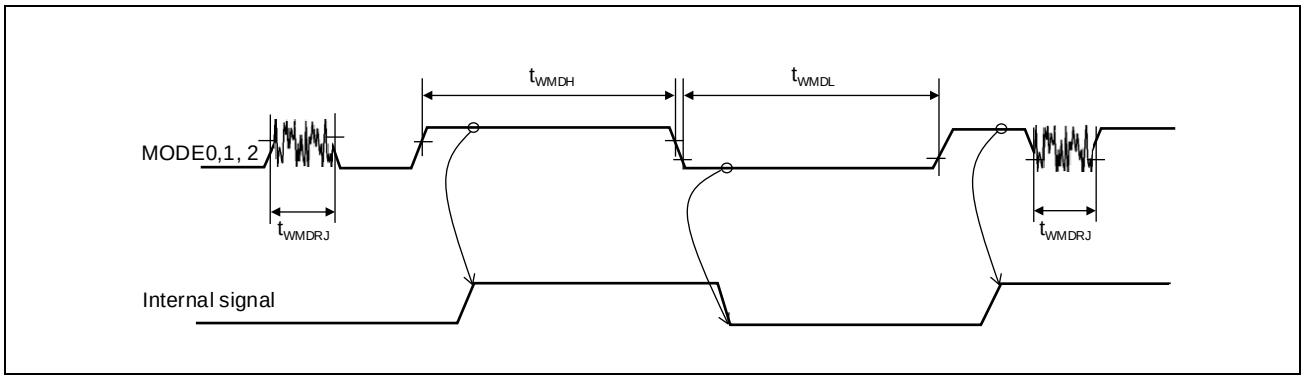
Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0, 1 input high/low level width*1	t_{WFMDH}/ t_{WFMDL}		600			ns
FLMD0, 1 pulse rejection*2	t_{WFMDRJ}		100			ns
MODE0, 1, 2 input high/low level width*1	t_{WMDH}/ t_{WMDL}		600			ns
MODE0, 1, 2 pulse rejection*2	t_{WMDRJ}		100			ns

Note 1. FLMD0,1 and MODE0, 1, 2 input width is needed to ensure that the internal mode signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.





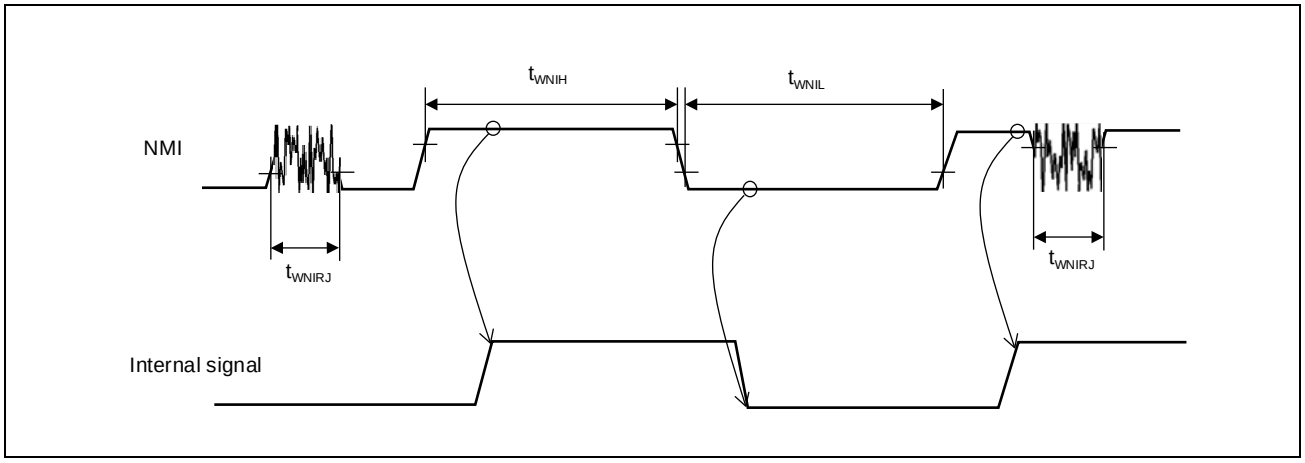
3C.5.3 Interrupt Timing

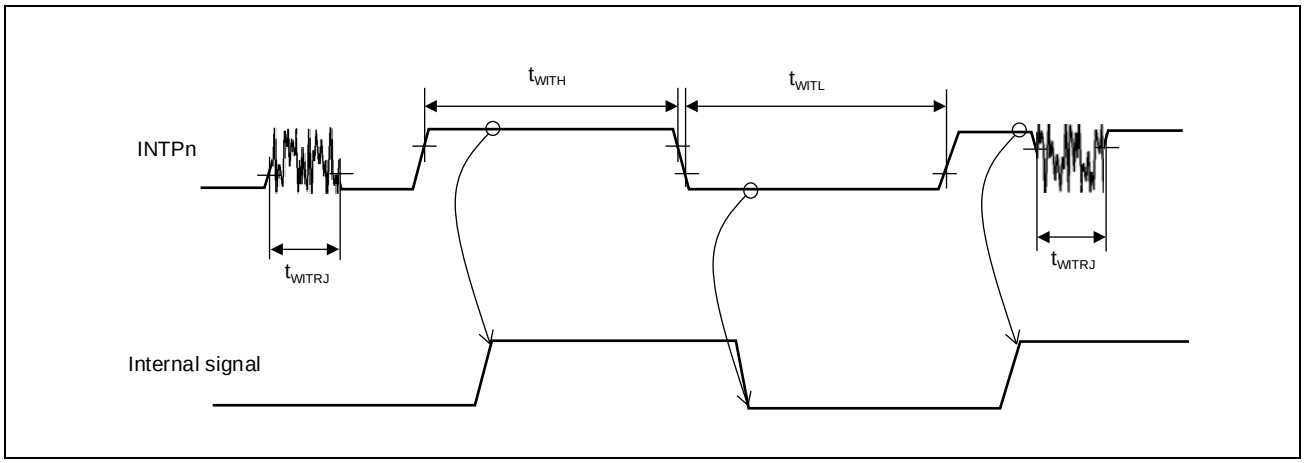
Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high/low level width*1	t_{WNIH}/ t_{WNIL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	24			µs
NMI pulse rejection*2	t_{WNIRJ}		100			ns
INTPn input high/low level width*1	t_{WITH}/ t_{WITL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	24			µs
INTPn pulse rejection*2	t_{WITRJ}		100			ns

Note 1. NMI and INTPn input width is needed to ensure that the internal interrupt signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



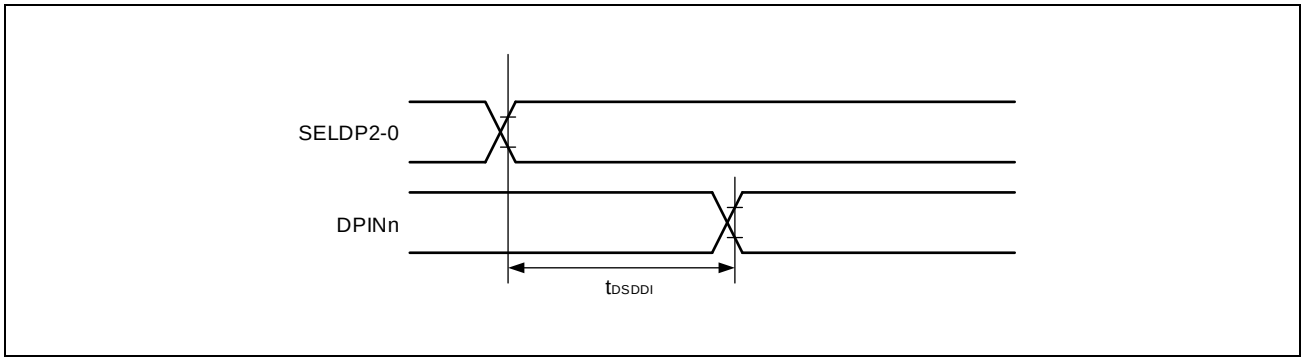


3C.5.4 Low Power Sampler (DPIN input) Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DPINn input delay time (vs SELDP2-0)	t_{DSDDI}				150	ns

Note: n = 7 to 0



3C.5.5 CSCXFOUT Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

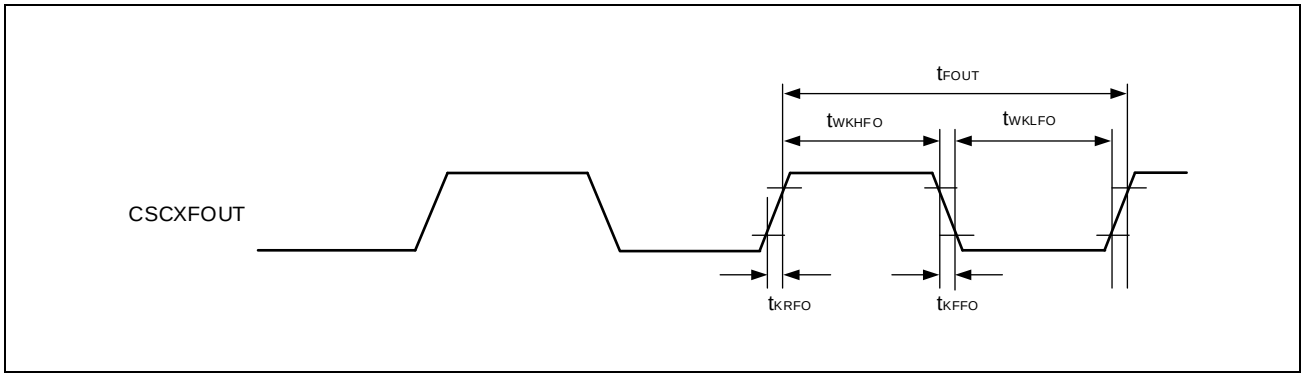
CSCXFOUT: Slow or fast mode (refer to the condition in the following table)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
CSCXFOUT output cycle	t_{FOUT}	Slow mode		100 (max. 10 MHz)			ns
		Fast mode		41.6 (max. 24 MHz)			ns
CSCXFOUT high level width	t_{WKHFO}	Slow mode	N: 1*1 or even value*2	t_{FOUT} / 2 – 37			ns
			N: Odd value (N ≥ 5)*2, *3	t_{FOUT} × (N+1) / 2N – 37			ns
		Fast mode	N: 1*1 or even value*2	t_{FOUT} / 2 – 10			ns
			N: Odd value (N ≥ 3)*2	t_{FOUT} × (N+1) / 2N – 10			ns
CSCXFOUT low level width	t_{WKLFO}	Slow mode	N: 1*1 or even value*2	t_{FOUT} / 2 – 37			ns
			N: Odd value (N ≥ 5)*2, *3	t_{FOUT} × (N–1) / 2N – 37			ns
		Fast mode	N: 1*1 or even value*2	t_{FOUT} / 2 – 10			ns
			N: Odd value (N ≥ 3)*2	t_{FOUT} × (N–1) / 2N – 10			ns
CSCXFOUT rise/ fall time	t_{KRFO}/ t_{KFFO}	Slow mode				37	ns
		Fast mode				10	ns

Note 1. When MainOSC, HS IntOSC, or LS IntOSC is selected as source clock with the condition of N = 1, the characteristics of output signal depends on the selected source clock. It is recommended to use output signal after evaluation on an actual environment.

Note 2. “N” is the value of “Clock divisor N” defined by FOUTDIV register.

Note 3. The selection of N = 3 is prohibited when slow mode is used.



3C.5.6 **Reserved**

3C.5.7 **Reserved**

3C.5.8 **Reserved**

3C.5.9 **Reserved**

3C.5.10 CSI Timing

3C.5.10.1 CSIG Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3C.12 CSIG Timing (Master Mode)

<Output driver strength>

CSIGnSO, CSIGnSC (output): Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYMGn}		100			ns
CSIGnSC high level width	t_{KWHMGn}		0.5 × t_{KCYMGn} – 10			ns
CSIGnSC low level width	t_{KWLMGn}		0.5 × t_{KCYMGn} – 10			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSIMGn}		30			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSIMGn}		0			ns
CSIGnSO output delay (vs. CSIGnSC)	t_{DSOMGn}				7	ns
CSIGnRYI setup time (vs. CSIGnSC)	t_{SRYIGn}	CSIGnCTL1.CSIGnSIT = x CSIGnCTL1.CSIGnHSE = 1	2 × t_{KCYGn} + 25			ns
CSIGnRYI high level width	t_{WRYIGn}	CSIGnCTL1.CSIGnHSE = 1	t_{KCYGn} + 5			ns

Note: n = 0

Table 3C.13 CSIG Timing (Slave Mode)

<Output driver strength>

CSIGnSO: Fast mode

CSIGnRYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYSGn}		200			ns
CSIGnSC high level width	t_{KWHSGn}		0.5 × t_{KCYSGn} – 10			ns
CSIGnSC low level width	t_{KWLSGn}		0.5 × t_{KCYSGn} – 10			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSISGn}		20			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSISGn}		t_{KCYGn} + 5			ns
CSIGnSO output delay (vs. CSIGnSC)	t_{DSOSGn}				30	ns
CSIGnRYO output delay	t_{SRYOGn}				38	ns
$\overline{\text{CSIGnSSI}}$ setup time (vs. CSIGnSC)	$t_{SSSISGn}$		0.5 × t_{KCYSGn} – 5			ns
$\overline{\text{CSIGnSSI}}$ hold time (vs. CSIGnSC)	$t_{HSSISGn}$		t_{KCYGn} + 5			ns

Note: n = 0

3C.5.10.2 CSIH Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3C.14 CSIH Timing (Master Mode: 10 Mbps)

<Output driver strength>
CSIHnSO, CSIHnSC (output): Fast mode (CL = 100pF@n=0 / 50pF@n=1-3)
CSIHnCSSx: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYMHn}		100			ns
CSIHnSC high level width	t_{KWHMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSC low level width	t_{KWLMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSIMHn}	SI positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	19			ns
		SI negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	14			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSIMHn}	SI positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	0			ns
		SI negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	t_{KCYHn}/2			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOMHn}				7	ns
CSIHnRYI setup time (vs. CSIHnSC)	t_{SRYIHn}	CSIHnCTL1.CSIHnSIT = x CSIHnCTL1.CSIHnHSE = 1	2 × t_{KCYHn} + 25			ns
CSIHnRYI high level width	t_{WRYIHn}	CSIHnCTL1.CSIHnHSE = 1	t_{KCYHn} + 5			ns
CSIHnCSS0-7 inactive width	$t_{WSCSBHn}$		CSIDLE × t_{KCYMHn} – 15			ns
CSIHnCSS0-7 setup time (vs. CSIHnSC)	$t_{SSCSBHn0}$	CSIHnCFGx.CSIHnDAP = 0	CSSETUP × t_{KCYMHn} – 23			ns
	$t_{SSCSBHn1}$	CSIHnCFGx.CSIHnDAP = 1	(CSSETUP + 0.5) × t_{KCYMHn} – 23			ns
CSIHnCSS0-7 hold time (vs. CSIHnSC)	$t_{HSCSBHn0}$	CSIHnCTL1.CSIHnSIT = 0	CSSHOLD × t_{KCYMHn} – 5			ns
	$t_{HSCSBHn1}$	CSIHnCTL1.CSIHnSIT = 1	(CSSHOLD + 0.5) × t_{KCYMHn} – 5			ns

Note: n = 0 to 3

NOTE

CSIDLE: Setting value of CSIHnCFGx.CSIHnIDx[2:0]
CSSETUP: Setting value of CSIHnCFGx.CSIHnSPx[3:0]
CSSHOLD: Setting value of CSIHnCFGx.CSIHnHDx[3:0]
x: Depends on number of the chip select signals.

CAUTION

When the serial clock level is changed during the communication (CSIHnCFGx.CSIHnCKPx) and the IDLE has a setting of 0.5 transmission clock cycles, an inactive width time $t_{WSCSBHn}$ of "0.5 × t_{KCYMHn}" is added.

Table 3C.15 CSIH Timing (Slave Mode: 5 Mbps)

<Output driver strength>
CSIHnSO: Fast mode
CSIHnRYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYSHn}		200			ns
CSIHnSC high level width	t_{KWHSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSC low level width	t_{KWLSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSISHn}		20			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSISHn}		$t_{KCYHn} + 5$			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOSHn}				30	ns
CSIHnRYO output delay	t_{SRYOHn}	$t_{KCYSHn} \geq 8 \times t_{KCYHn}$			38	ns
		$t_{KCYSHn} < 8 \times t_{KCYHn}$			$38 + t_{KCYHn}$	ns
$\overline{\text{CSIHnSSI}}$ setup time (vs. CSIHnSC)	$t_{SSSISHn}$		$0.5 \times t_{KCYSHn} - 5$			ns
$\overline{\text{CSIHnSSI}}$ hold time (vs. CSIHnSC)	$t_{HSSISHn}$		$t_{KCYHn} + 5$			ns

Note: n = 0 to 3

Table 3C.16 CSIH Timing (Slave Mode: 8 Mbps)

<Output driver strength>
CSIHnSO: Fast mode
CSIHnRYO: Slow mode

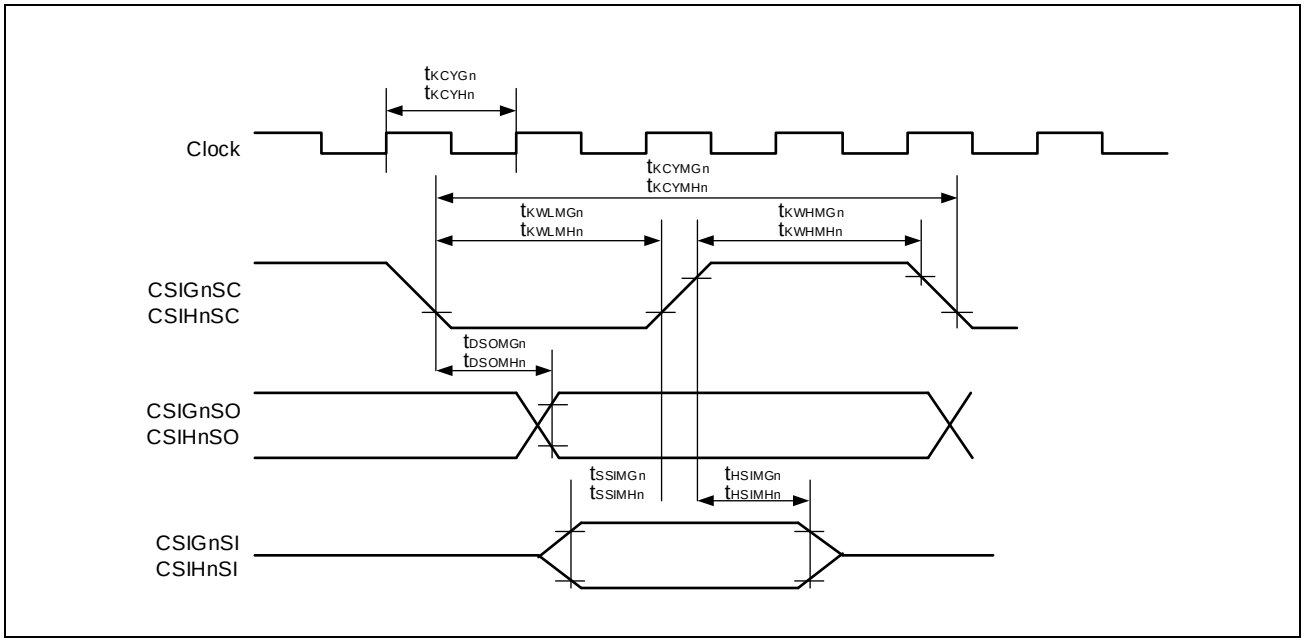
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYSHn}		125			ns
CSIHnSC high level width	t_{KWHSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSC low level width	t_{KWLSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSISHn}		12.5			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSISHn}		$t_{KCYHn} + 5$			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOSHn}				25	ns
CSIHnRYO output delay	t_{SRYOHn}	$t_{KCYSHn} \geq 8 \times t_{KCYHn}$			27	ns
		$t_{KCYSHn} < 8 \times t_{KCYHn}$			$27 + t_{KCYHn}$	ns
$\overline{\text{CSIHnSSI}}$ setup time (vs. CSIHnSC)	$t_{SSSISHn}$		$0.5 \times t_{KCYSHn} - 5$			ns
$\overline{\text{CSIHnSSI}}$ hold time (vs. CSIHnSC)	$t_{HSSISHn}$		$t_{KCYHn} + 5$			ns

Note: n = 2 (80/100-pin versions), n = 0 (48/64-pin versions)

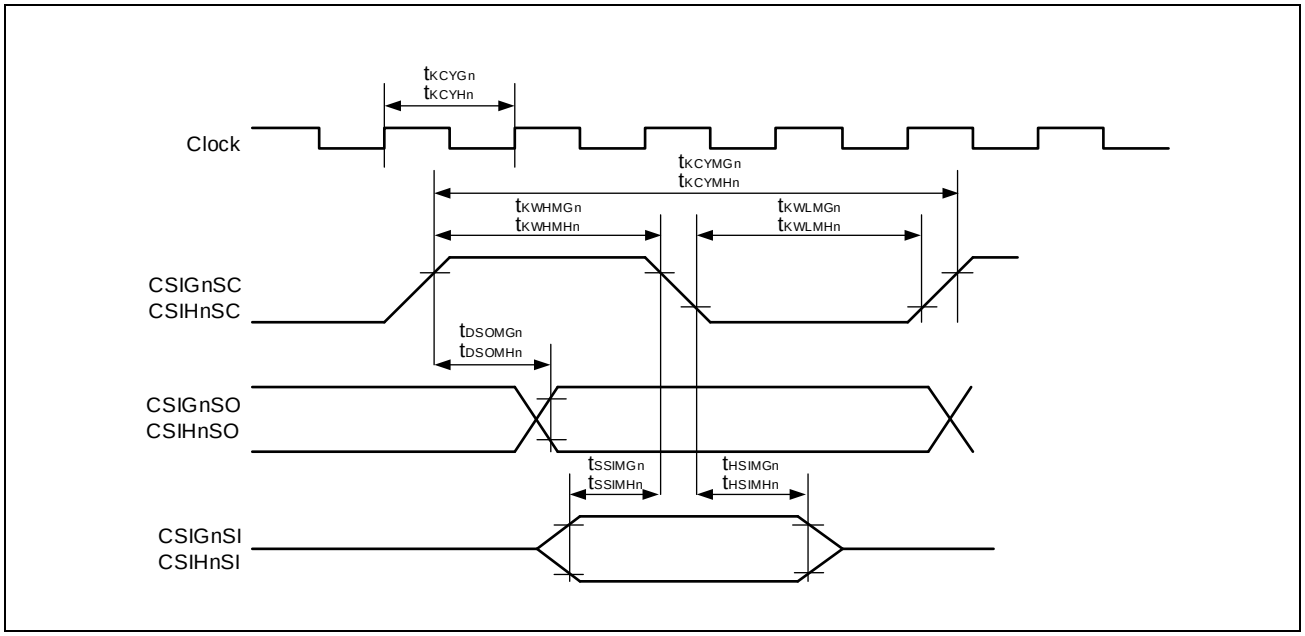
(1) SC/SI/SO

Master mode:

- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0 or 1/1)



- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0 or 0/1)



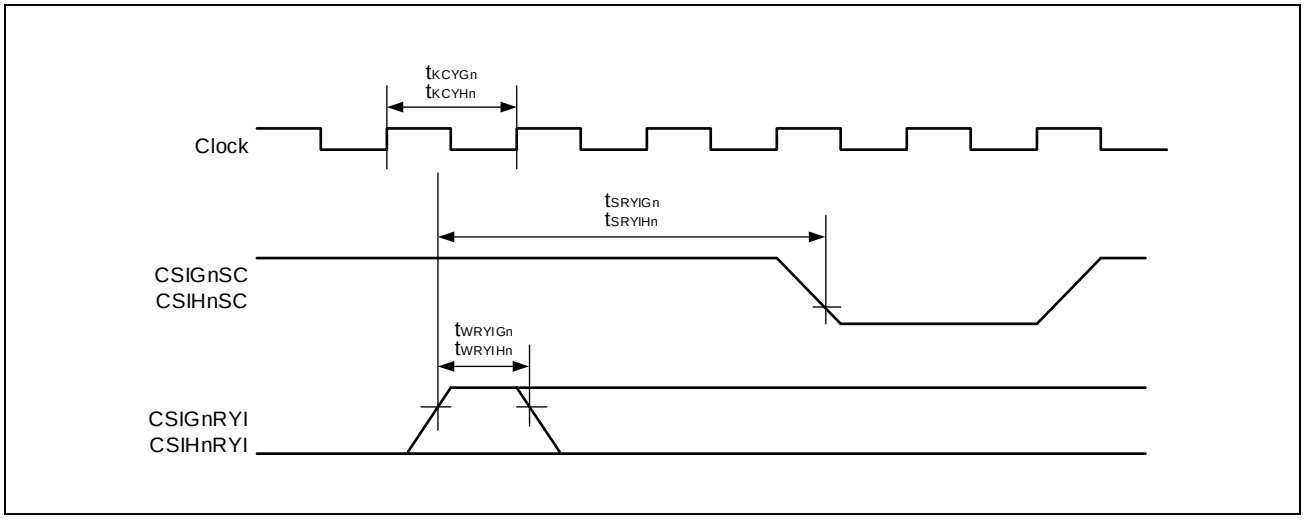
(2) RYI

Master mode:

- CSIG: Only master mode (CSIGnCTL1: CSIGnHSE = 1, CSIGnCTL1: CSIGnSIT = 0)
- CSIH: Only master mode (CSIHnCTL1: CSIHnHSE = 1, CSIHnCTL1: CSIHnSIT = 0)

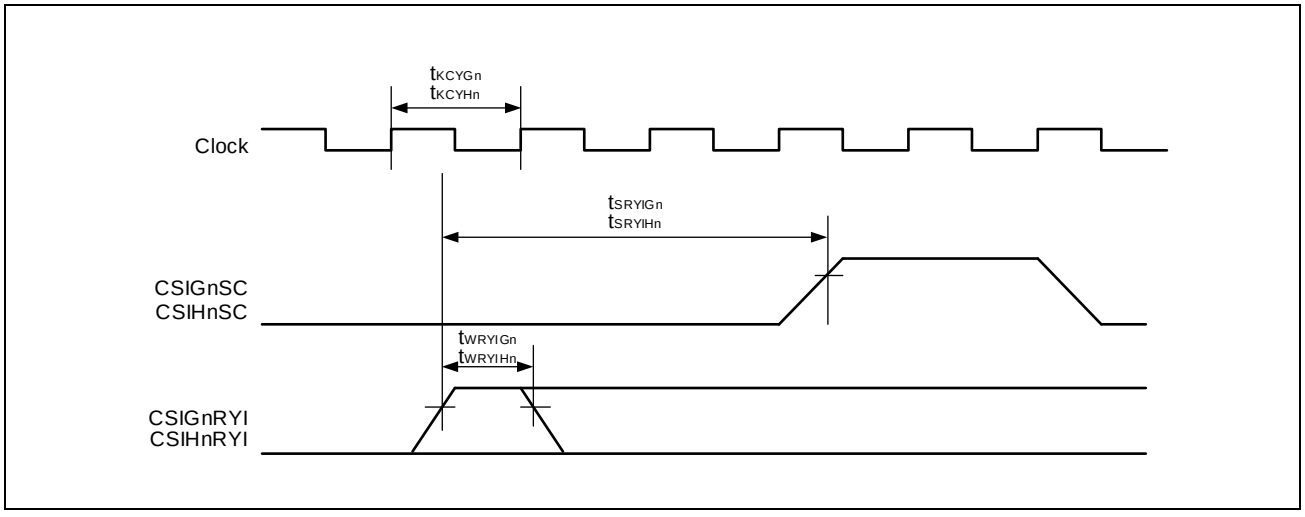
– CSIG (CSIGnCTL1: CSIGnCKR = 0)

– CSIH (CSIHnCFGx: CSIHnCKPx = 0)



– CSIG (CSIGnCTL1: CSIGnCKR = 1)

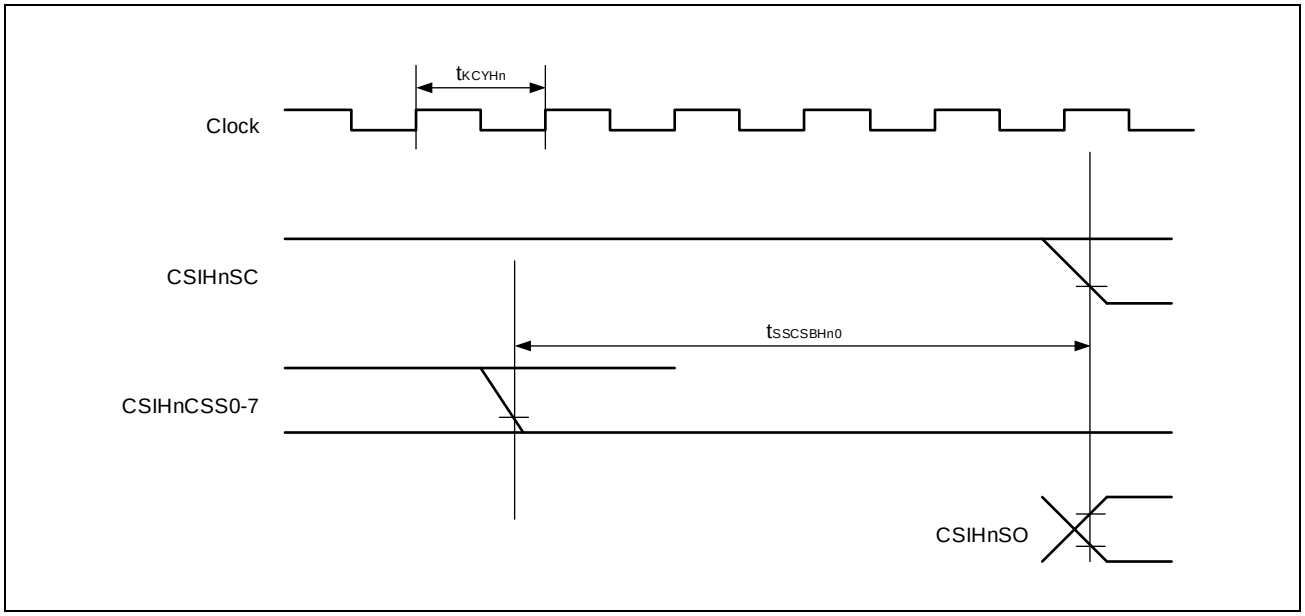
– CSIH (CSIHnCFGx: CSIHnCKPx = 1)



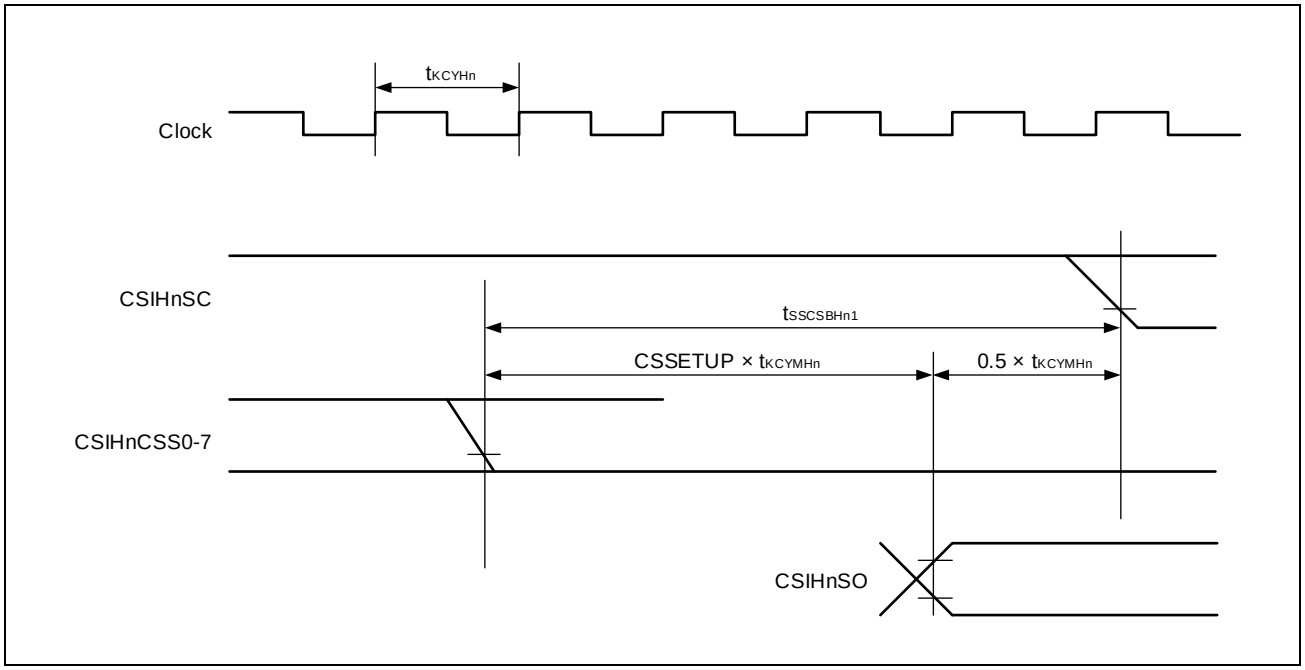
(3) CSSx

Only master mode (setup time):

- CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0

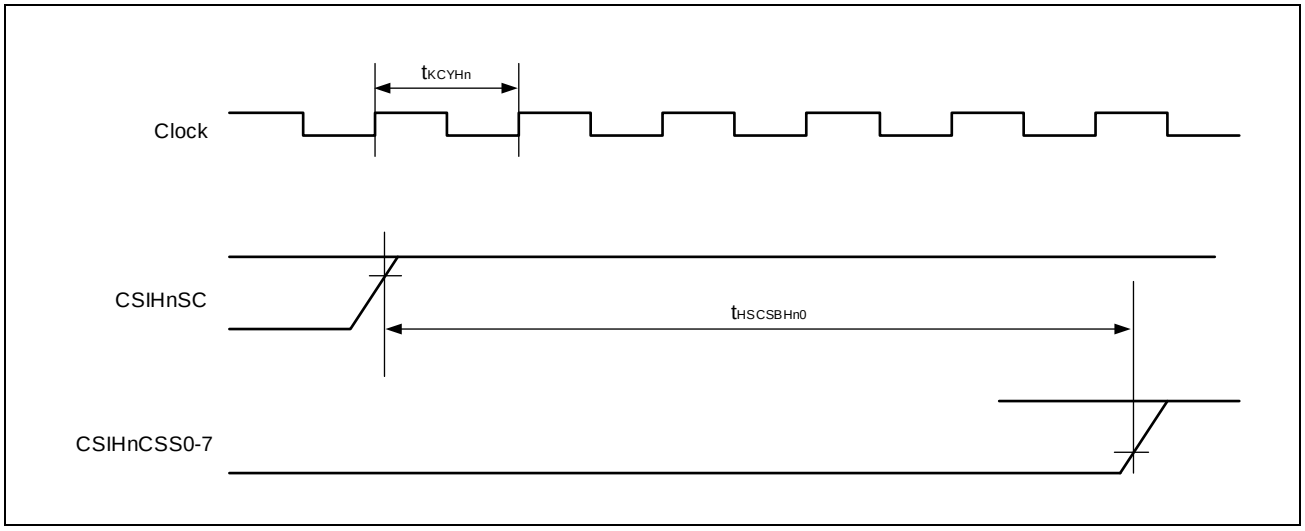


- CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 1

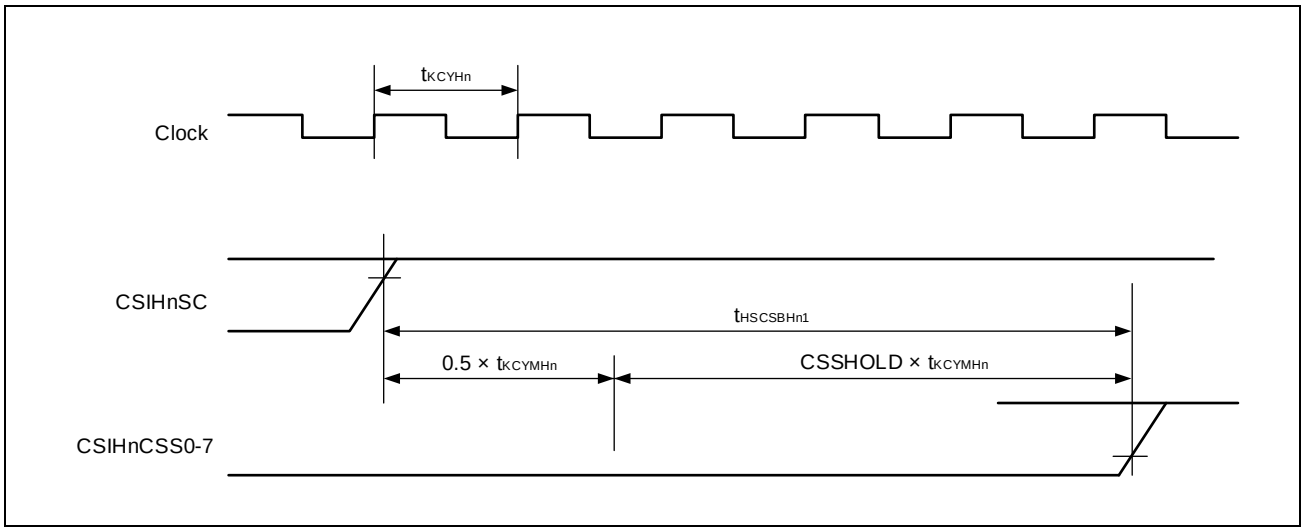


Only master mode (hold time):

- CSIHnCTL1: CSIHnSIT = 0, CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0



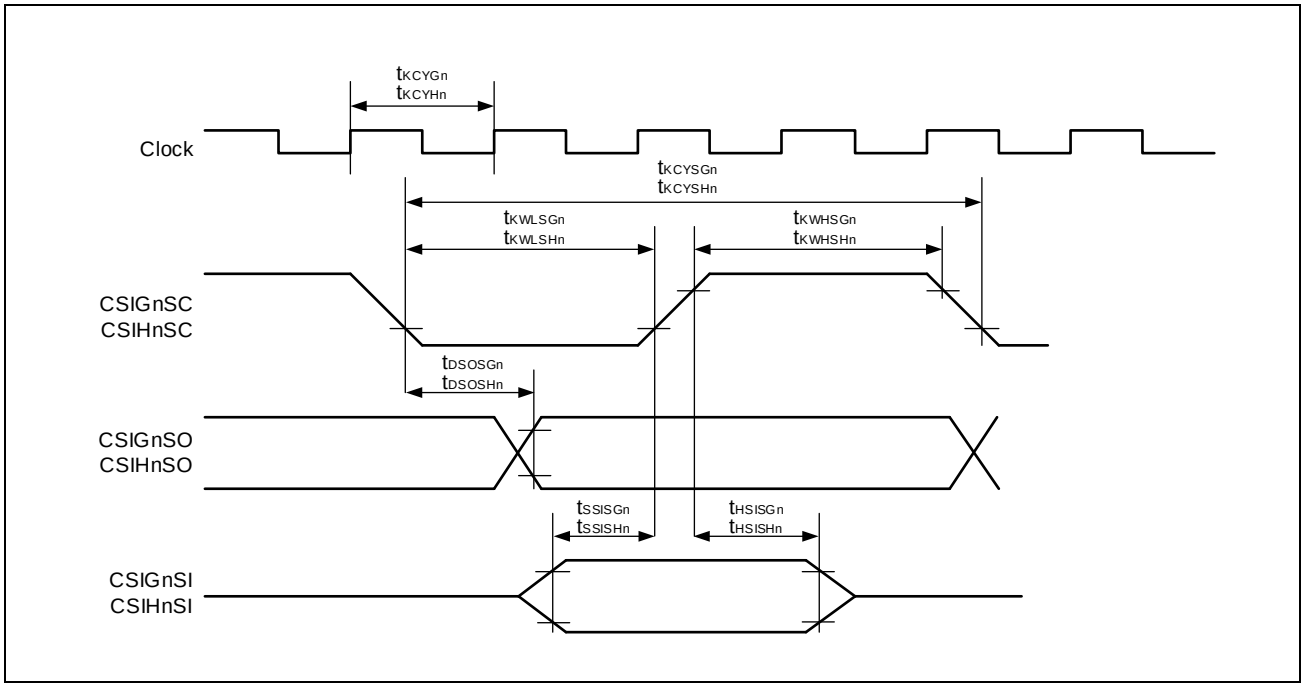
- CSIHnCTL1: CSIHnSIT = 1, CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0



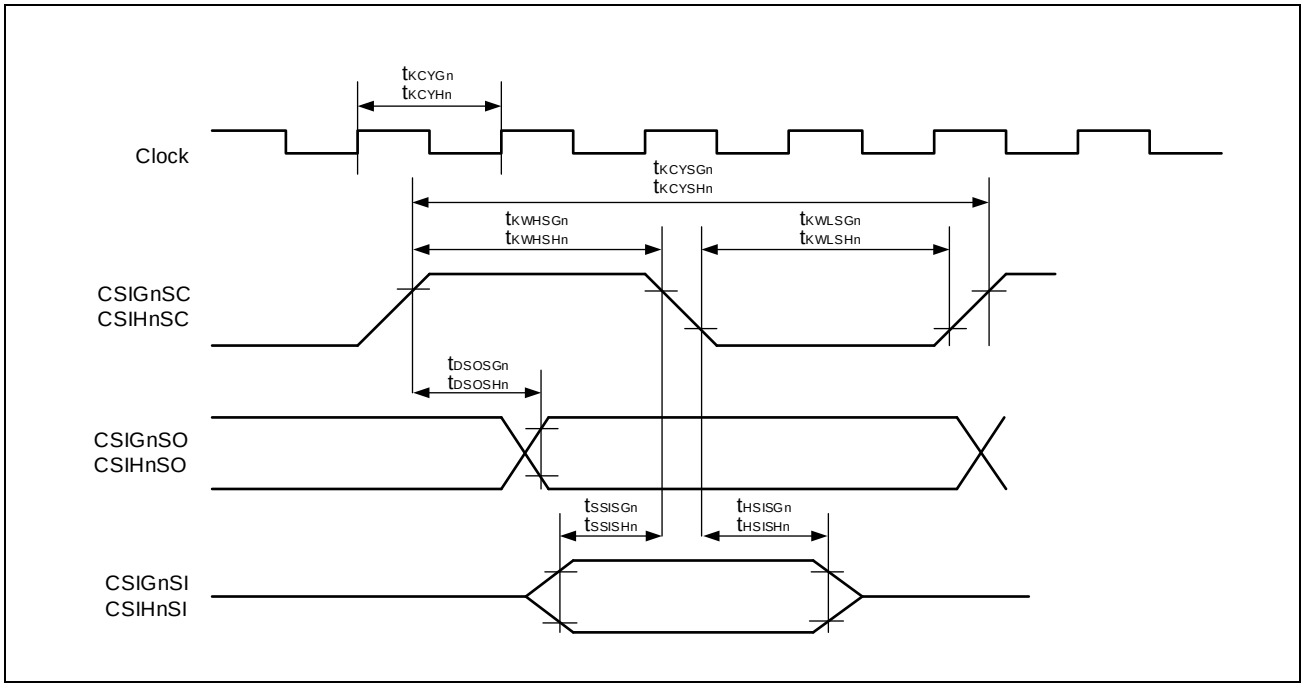
(4) SC/SI/SO

Slave mode:

- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0 or 1/1)

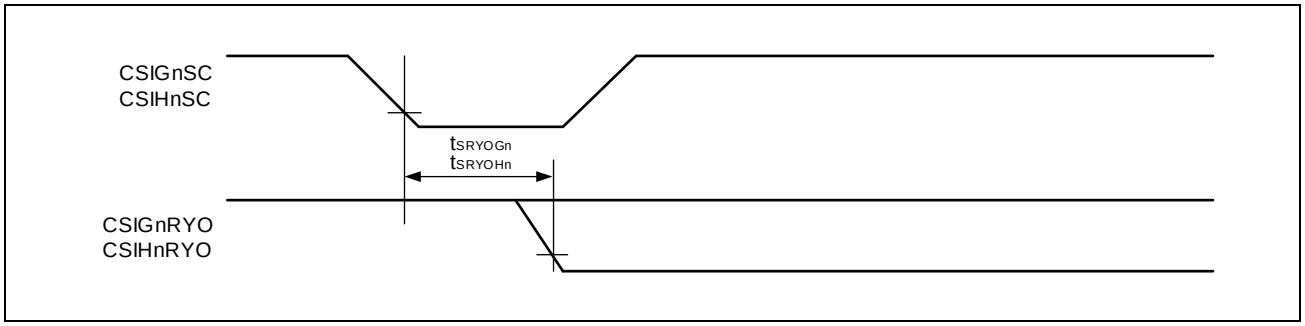


- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0 or 0/1)

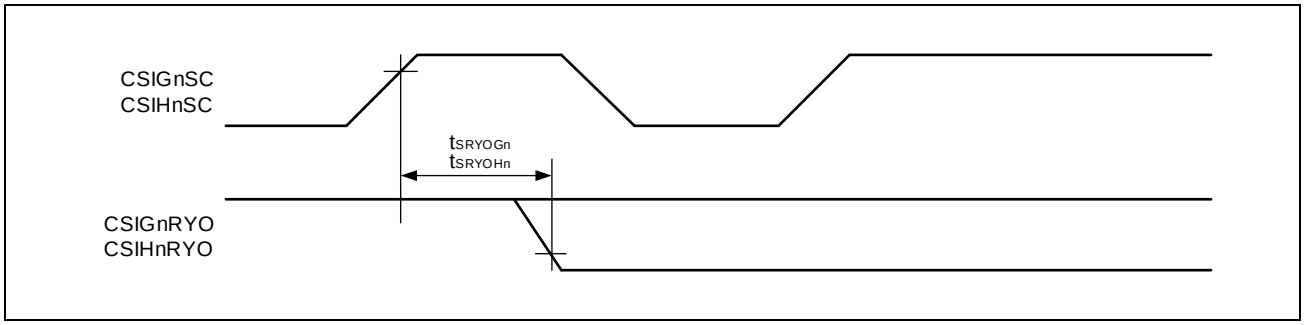


(5) RYO

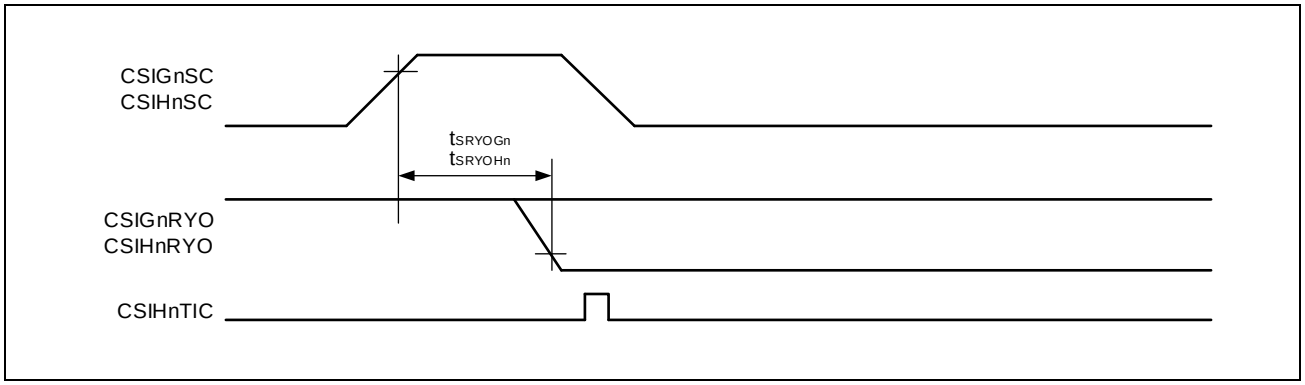
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0)



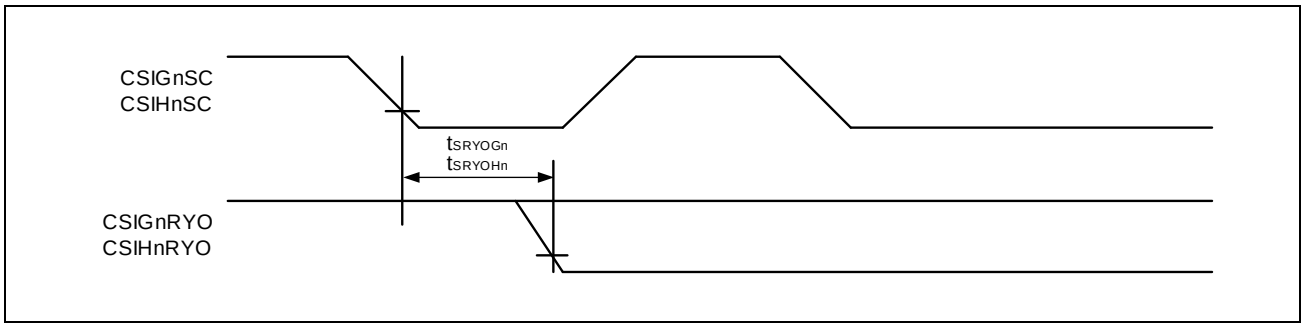
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/1)



- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0)



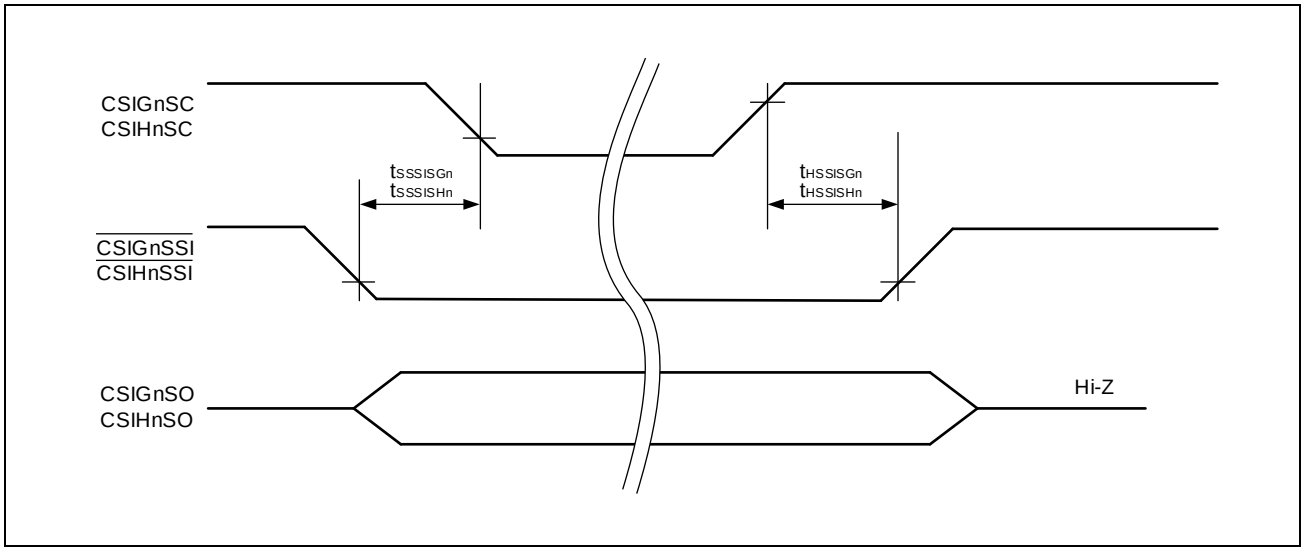
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/1)



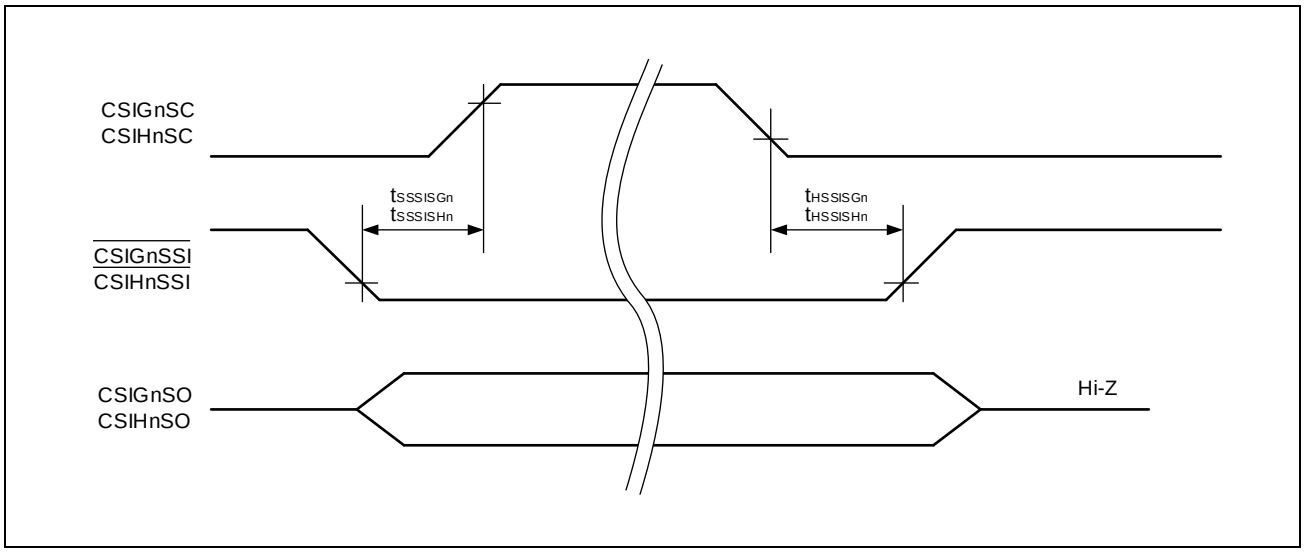
(6) SSI

Slave mode:

- CSIG (CSIGnCTL1: CSIGnSSE=1, CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0 or 1/1)



- CSIG (CSIGnCTL1: CSIGnSSE=1, CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0 or 0/1)



3C.5.11 RLIN2/RLIN3 Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate		LIN specification	1		20	kbps
		LIN extended baud rate	1		115.2*1	kbps
		UART function			1.5	Mbps
RLIN2 transfer rate		LIN specification	1		20	kbps

Note 1. The LIN extended baud rate is not part of the LIN standard specification.

3C.5.12 RIIC Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C

Table 3C.17 RIIC Timing (Normal Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIICnSCL clock period	f_{CLK}				100	kHz
Bus free time (between stop/start condition)	t_{BUF}		4.7			µs
Hold time*1	t_{HD}: STA		4.0			µs
RIICnSCL clock low-level width	t_{LOW}		4.7			µs
RIICnSCL clock high-level time	t_{HIGH}		4.0			µs
Setup time for start/restart condition	t_{SU}: STA		4.7			µs
Data hold time	t_{HD}: DAT	CBUS compatible master	5.0			µs
		I^2C mode	0*2			µs
Data setup time	t_{SU}: DAT		250			ns
Stop condition setup time	t_{SU}: STO		4.0			µs
Capacitance load of each bus line	Cb				400	pF

Remark: n = 0, 1

Note: If the system does not extend the RIICnSCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIICnSDA signal (at VIH min. of RIICnSCL signal). In order to occupy the undefined area at the falling edge of RIICnSCL.

Table 3C.18 RIIC Timing (Fast Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIICnSCL clock period	f_{CLK}				400	kHz
Bus free time (between stop/start condition)	t_{BUF}		1.3			µs
Hold time*1	t_{HD}: STA		0.6			µs
RIICnSCL clock low-level width	t_{LOW}		1.3			µs
RIICnSCL clock high-level time	t_{HIGH}		0.6			µs
Setup time for start/restart condition	t_{SU}: STA		0.6			µs
Data hold time	t_{HD}: DAT	I^2C mode	0*2			µs
Data setup time	t_{SU}: DAT		100*3			ns
Stop condition setup time	t_{SU}: STO		0.6			µs
Pulse width with spike suppressed by input filter	t_{SP}		0		50	ns
Capacitance load of each bus line	Cb				400	pF

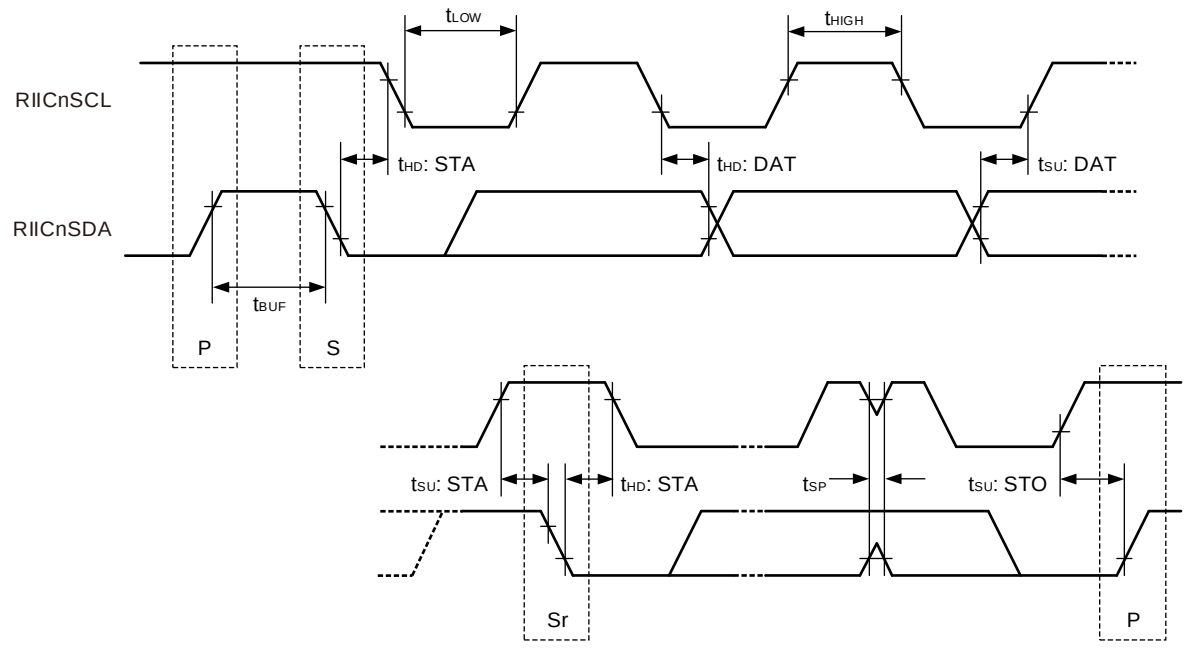
Remark: n = 0, 1

Note: If the system does not extend the RIICnSCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIICnSDA signal (at VIH min. of RIICnSCL signal). In order to occupy the undefined area at the falling edge of RIICnSCL

Note 3. The fast mode I^2C bus can be used in normal mode I^2C bus system. In this case, set the fast mode I^2C bus so that it meets the following conditions.
- If the system does not extend the RIICnSCL signal's low state hold time: t_{SU}: DAT ≥ 250 ns
- If the system extends the RIICnSCL signal's low state hold time:
  Transmit the following data bit to the RIICnSDA line prior to releasing the RIICnSCL line
  (1250 ns: Normal mode I^2C bus specification).



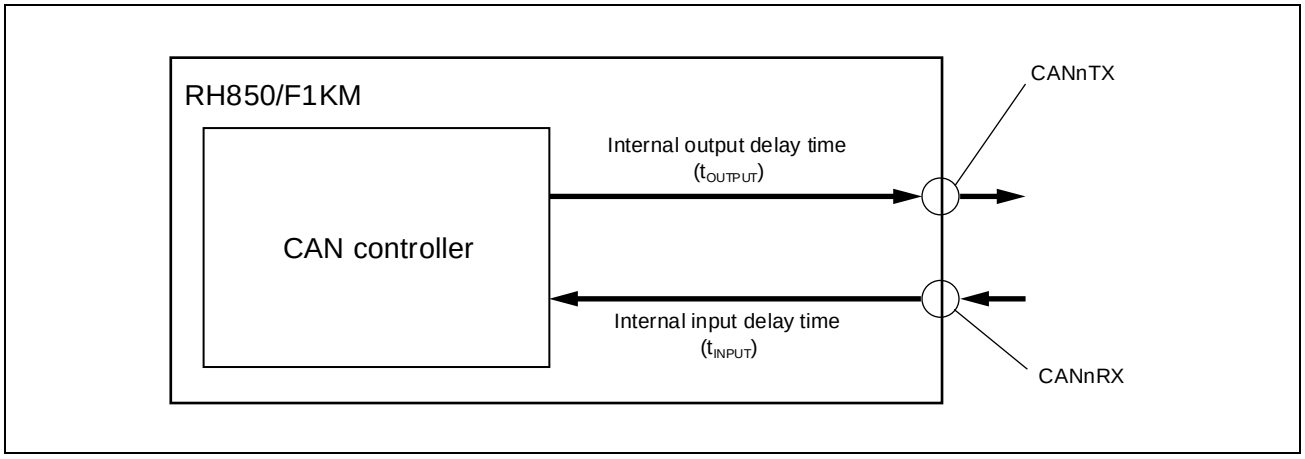
Note: P: Stop condition S: Start condition Sr: Restart condition

3C.5.13 RS-CANFD Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate		Classical CAN mode			1	Mbps
Data bit rate (CAN FD mode)		Nominal bit rate ≤ 500 kbps			5	Mbps
		Nominal bit rate > 500 kbps			2	Mbps
Internal delay time*1	t_{NODE}				50	ns

Note 1. t_{NODE} = Internal input delay time (t_{INPUT}) + Internal output delay time (t_{OUTPUT})



3C.5.14 Reserved

3C.5.15 Reserved

3C.5.16 RSENT Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF ±30%, CISOVCL: 0.1µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Tick Time			1		90	µs

3C.5.17 Timer Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

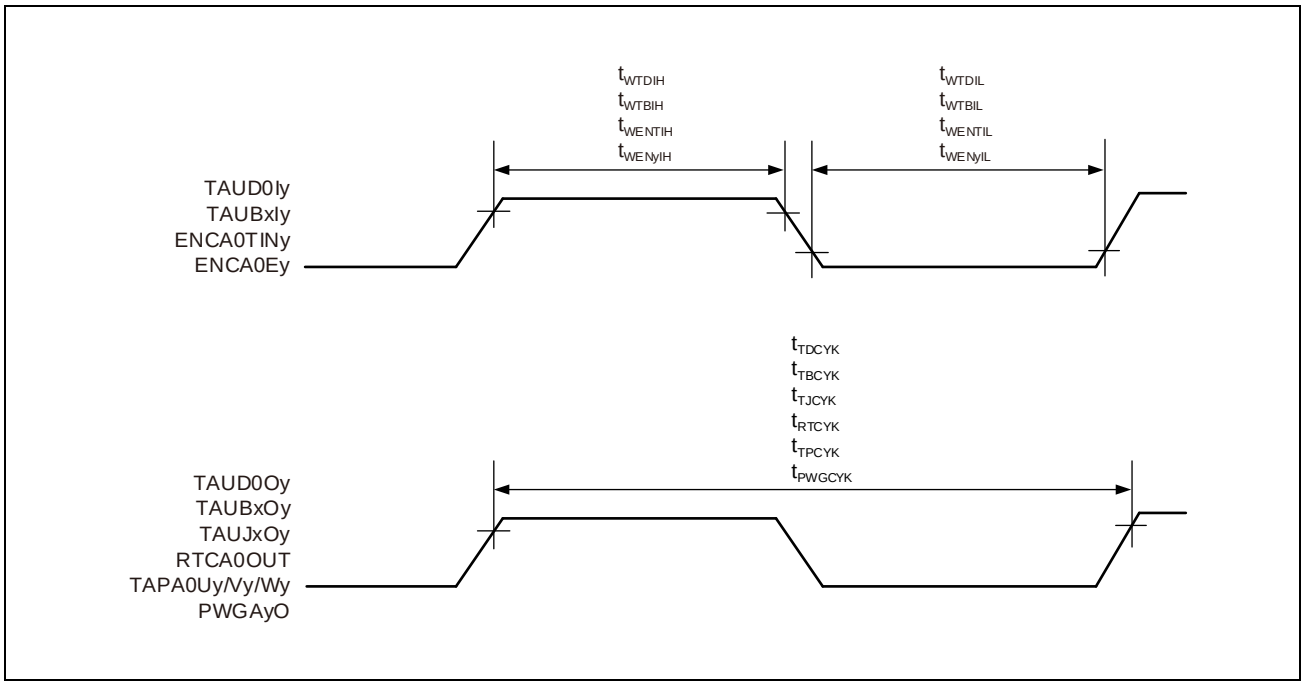
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUD0Iy input high/low level width (y = 0 to 15)	t_{WTDIH}/ t_{WTDIL}		n × Tsamp + 20*1, *2			ns
TAUD0Oy output cycle (y = 0 to 15)	t_{TDCYK}	Slow mode			10	MHz
TAUBxIy input high/low level width (x = 0, y = 0 to 15)	t_{WTBIH}/ t_{WTBIL}		n × Tsamp + 20*1, *2			ns
TAUBxOy output cycle (x = 0, y = 0 to 15)	t_{TBCYK}	Slow mode			10	MHz
TAUJxIy input high/low level width*3 (x = 0 to 3, y = 0 to 3)	t_{WTJIH}/ t_{WTJIL}		600			ns
TAUJxIy pulse rejection*4	t_{WTIJRJ}		100			ns
TAUJxOy output cycle (x = 0 to 3, y = 0 to 3)	t_{TJCYK}	Slow mode			10	MHz
RTCA0OUT output cycle	t_{RTCYK}			1		Hz
TAPA0ESO input high/low level width*3	t_{WESIH}/ t_{WESIL}		600			ns
TAPA0ESO pulse rejection*4	t_{WESIRJ}		100			ns
TAPA0Uy/Vy/Wy output cycle (y = P, N)	t_{TPCYK}	Slow mode			10	MHz
ENCA0TINy input high/low level width (y = 0, 1)	t_{WENTIH}/ t_{WENTIL}		n × Tsamp + 20*1			ns
ENCA0Ey input high/low level width (y = 0,1,C)	t_{WENyIH}/ t_{WENyIL}		n × Tsamp + 20*1			ns
PWGAyO output cycle (y = 0 to 47)	t_{PWGCYK}	Slow mode			10	MHz

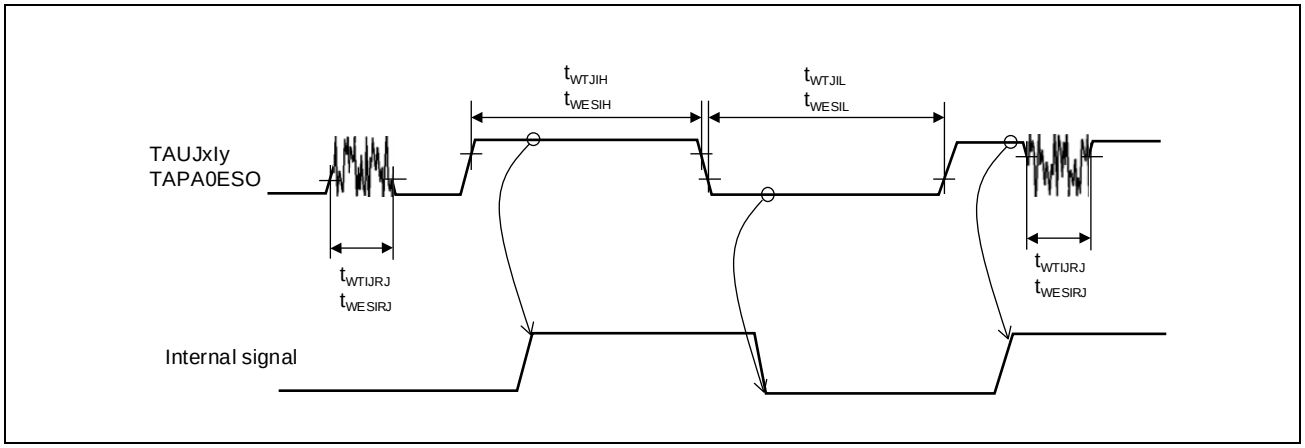
Note 1. n: Sampling number of the digital noise filter for each input. Tsamp: Sampling time of the digital noise filter for each input.

Note 2. Input more than 1 count clock width of each timer counter channel.

Note 3. TAUJxIy and TAPA0ESO input width is needed to ensure that the internal timer input signal is activated.

Note 4. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.


t_{WTDIH}
t_{WTBIH}
t_{WENTIH}
t_{WENyIH}
t_{WTDIL}
t_{WTBIL}
t_{WENTIL}
t_{WENyIL}
TAUD0Iy
TAUBxIy
ENCA0TINy
ENCA0Ey
t_{TDCYK}
t_{TBCYK}
t_{TJCYK}
t_{RTCYK}
t_{TPCYK}
t_{PWGCYK}
TAUD0Oy
TAUBxOy
TAUJxOy
RTCA0OUT
TAPA0Uy/Vy/Wy
PWGAyO

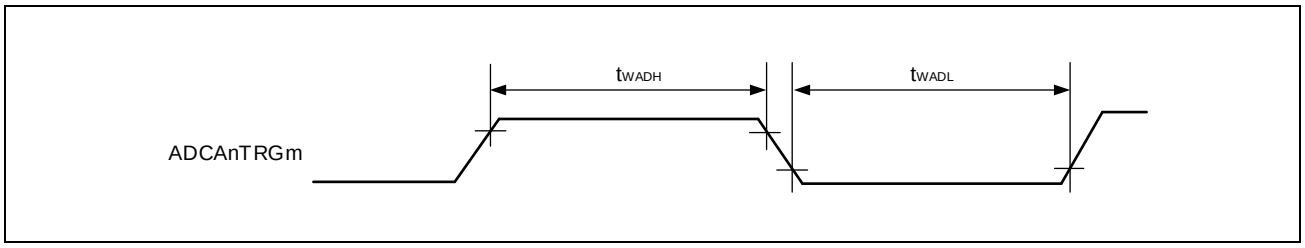

t_{WTJIH}
t_{WESIH}
t_{WTJIL}
t_{WESIL}
TAUJxIy
TAPA0ESO
t_{WTIJRJ}
t_{WESIRJ}
t_{WTIJRJ}
t_{WESIRJ}
Internal signal

3C.5.18 ADTRG Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCAnTRGm input high/ low level width	t_{WADH}/t_{WADL}		k × Tsamp + 20*1			ns

Note 1. k: Sampling number of the digital noise filter for each input.
Tsamp: Sampling time of the digital noise filter for each input.



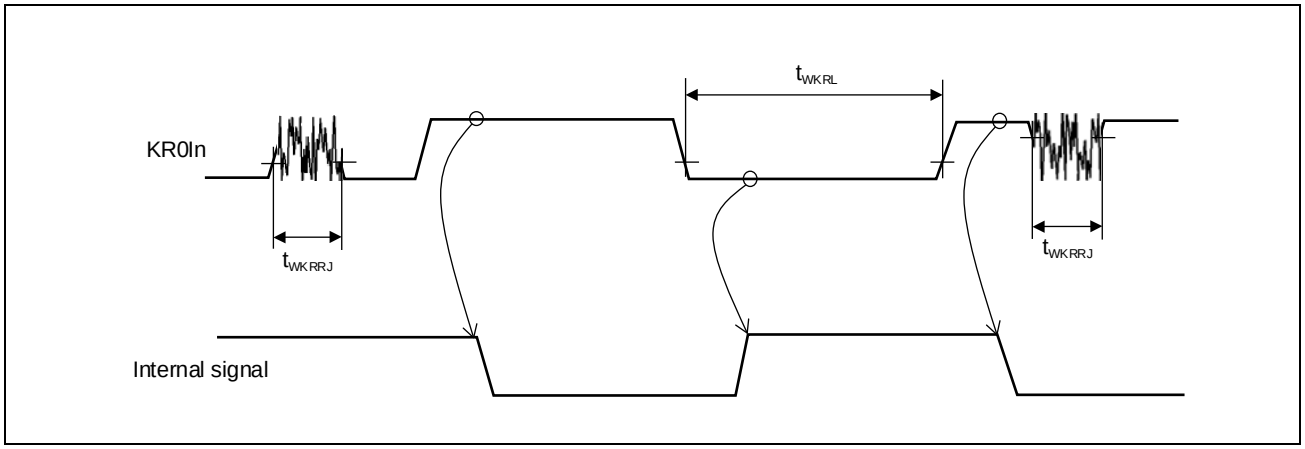
3C.5.19 Key Return Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
KR0In input low level width*1	t_{WKRL}		600			ns
KR0In pulse rejection*2	t_{WKRRJ}		100			ns

Note 1. KR0In input width is needed to ensure that the internal key input signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value.
Noise such as the figure can be filtered.



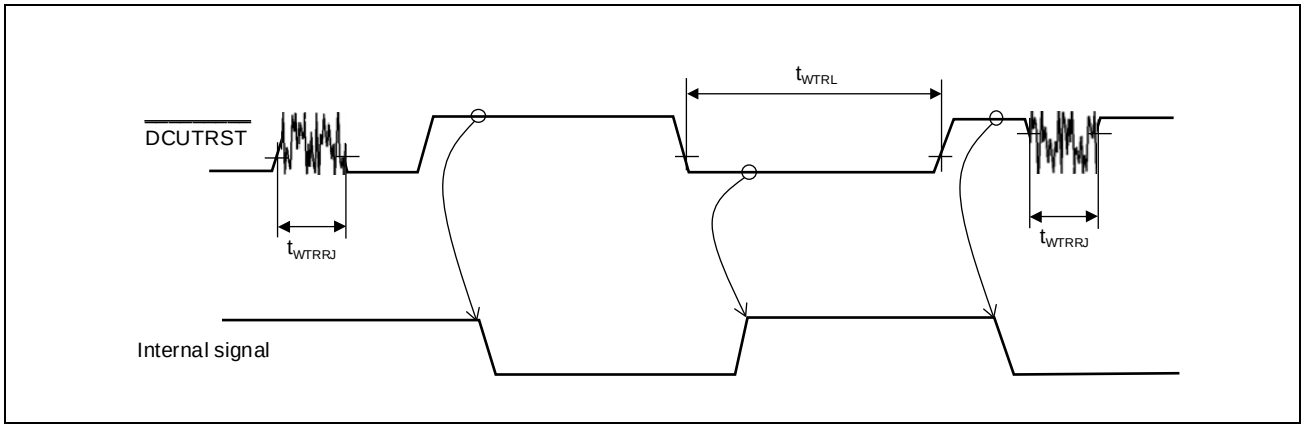
3C.5.20 $\overline{\text{DCUTRST}}$ Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{DCUTRST}}$ input low level width*1	t_{WTRL}		600			ns
$\overline{\text{DCUTRST}}$ pulse rejection*2	t_{WTRRJ}		100			ns

Note 1. $\overline{\text{DCUTRST}}$ input width is needed to ensure that the internal DCU reset input signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value.
Noise such as the figure can be filtered.



3C.5.21 Debug Interface Characteristics

3C.5.21.1 Nexus Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

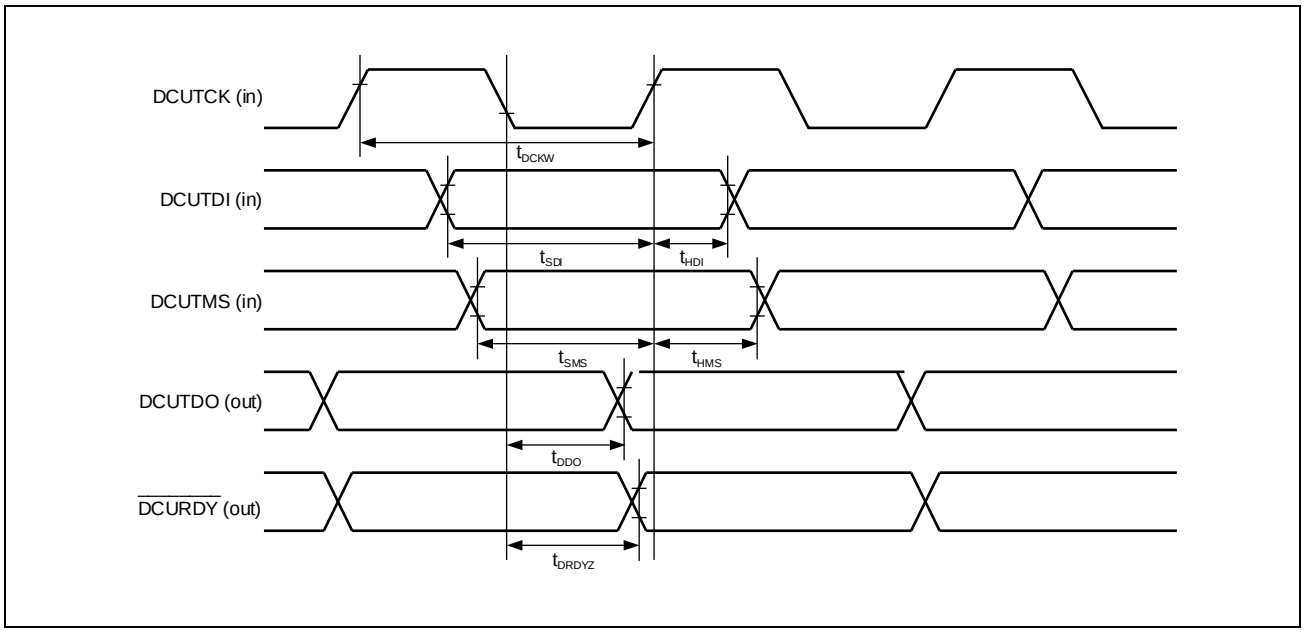
<Input buffer>

DCUTDI, DCUTCK, DCUTMS, $\overline{\text{DCUTRST}}$: TTL

<Output driver strength>

DCUTDO, $\overline{\text{DCURDY}}$: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DCUTCK cycle width	t_{DCKW}		50			ns
DCUTDI setup time (vs DCUTCK ↑)	t_{SDI}		12			ns
DCUTDI hold time (vs DCUTCK ↑)	t_{HDI}		3			ns
DCUTMS setup time (vs DCUTCK ↑)	t_{SMS}		12			ns
DCUTMS hold time (vs DCUTCK ↑)	t_{HMS}		3			ns
DCUTDO delay time (↓ DCUTCK)	t_{DDO}		0		20	ns
$\overline{\text{DCURDY}}$ delay time (↓ DCUTCK)	t_{RDYZ}		0		20	ns



3C.5.21.2 LPD (4 Pins) Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF ±30%, CISOVCL: 0.1µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 100 pF

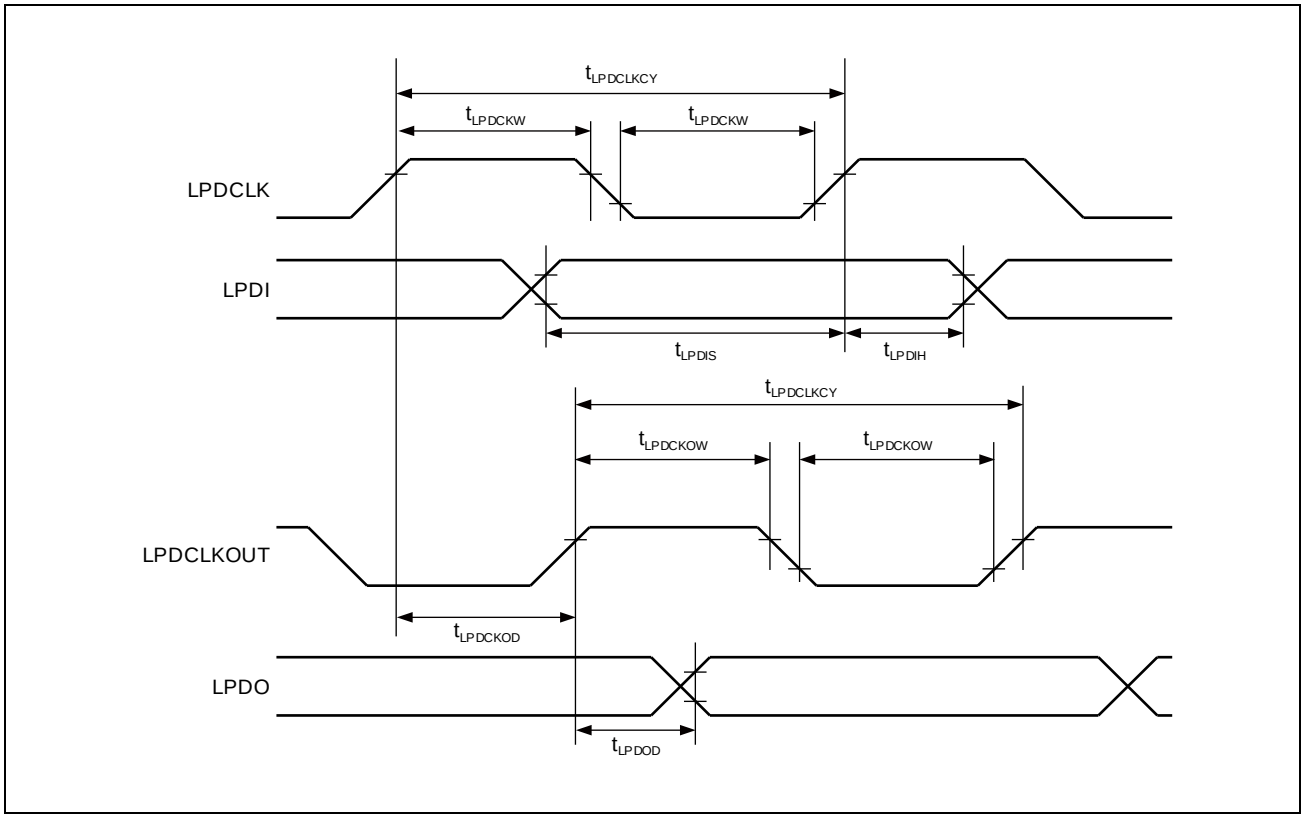
<Input buffer>

LPDCLK, LPDI: TTL

<Output driver strength>

LPDCLKOUT, LPDO: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPDCLK cycle time/ LPDCLKOUT cycle time	$t_{LPDCLKCY}$		83.3 (max.12 MHz)			ns
LPDCLK High-level width/ LPDCLK Low-level width	t_{LPDCKW}		0.5 × $t_{LPDCLKCY}$ – 10			ns
LPDCLKOUT High-level width/ LPDCLKOUT low-level width	$t_{LPDCKOW}$		t_{LPDCKW} – 10			ns
LPDI setup time (LPDCLK ↑)	t_{LPDIS}		41			ns
LPDI hold time (LPDCLK ↑)	t_{LPDIH}		3			ns
LPDCLK to LPDCLKOUT delay time	$t_{LPDCKOD}$				44	ns
LPDO delay time (LPDCLKOUT ↑)	t_{LPDOD}		0		15	ns



3C.5.21.3 LPD (1 Pin) Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF ±30%, CISOVCL: 0.1µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 50 pF

<Input buffer>
LPDIO: TTL

<Output driver strength>
LPDIO: Fast mode

<External pull-up resistor>
LPDIO: 1 kΩ to 10 kΩ

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPD (1 pin) baud rate					2.0	Mbps

3C.6 A/D Converter Characteristics

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF ±30%, CISOVCL: 0.1µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

(1/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Conversion clock	ADCLKn				8*3		40	MHz
Resolution	RESn	12-bit mode			12	12	12	bit
		10-bit mode			10	10	10	bit
Conversion time	t_{CONn}	ADCAnSMPCR.SMPT[7:0] = 12 H(40 cycle) (8M Hz*3 ≤ ADCLKn ≤ 32 MHz), External MPX is not used			1.25		5	µs
		ADCAnSMPCR.SMPT[7:0] = 18 H (46 cycle) (8 MHz*3 ≤ ADCLKn ≤ 40 MHz), External MPX is not used			1.15		5.75	µs
		ADCAnSMPCR.SMPT[7:0] = 12 H (80 cycle) (8 MHz*3 ≤ ADCLKn ≤ 32 MHz), External MPX is used			2.5*4		10	µs
		ADCAnSMPCR.SMPT[7:0] = 18 H (92 cycle) (8 MHz*3 ≤ ADCLKn ≤ 40 MHz), External MPX is used			2.3*4		11.5	µs
Sampling time	t_{SMP}	ADCAnSMPCR.SMPT[7:0] = 12 H (18 cycle) (8 MHz*3 ≤ ADCLKn ≤ 32 MHz)			0.56		2.25	µs
		ADCAnSMPCR.SMPT[7:0] = 18 H (24cycle) (8 MHz*3 ≤ ADCLKn ≤ 40 MHz)			0.6		3	µs
Overall error*1	TOEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±4.0	LSB
				ADCA0I0-5 (T&H used)			±6.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±6.0	LSB
				ADCA0I0-5 (T&H used)			±8.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB
Analog input voltage	VAIN0SN	ADCAnIm	T&H not used		AnVSS		AnVREF	V
		ADCA0I0-5	T&H used		0.2		A0VREF – 0.2	V
		ADCA0ImS	A0VREF ≥ EVCC		A0VSS		EVCC	V
			A0VREF < EVCC		A0VSS		A0VREF	V
Operation current	IA0VREF	T&H not used				1.1	3.0	mA
		T&H used (max. 6 pins)					*2	mA
STOP, DeepSTOP, Cyclic STOP current (@LPS is stopped)	IA0VREFS					1	10	µA
T&H current	ITH					0.5	1.3	mA/ch
T&H sampling time	t_{THSMP}				450			ns
T&H hold time	t_{THHOLD}						10	µs
Set up time of self diagnosis voltage circuit	t_{BOOT}				500			ns
Set up time of self diagnosis voltage level	t_{OUT}				500			ns
Pull-down resistor for diagnosis of open pins		ADCnIm pins	VI = AnVREF		350	500	650	kΩ
		ADCnImS pins	A0VREF ≥ EVCC: VI = EVCC A0VREF < EVCC: VI = A0VREF		100	215	800	kΩ
Accuracy of self-diagnosis function (except diagnosis of open pins)	TESH0SN	12-bit mode	Self-diagnosis voltage level = AnVREF		4015-|TOEn|		4095	—
			Self-diagnosis voltage level = 2/3AnVREF		2651-|TOEn|	2731	2811+|TOEn|	—
			Self-diagnosis voltage level = 1/2AnVREF		1968-|TOEn|	2048	2128+|TOEn|	—
			Self-diagnosis voltage level = 1/3AnVREF		1285-|TOEn|	1365	1445+|TOEn|	—
			Self-diagnosis voltage level = AnVSS		0		80+|TOEn|	—
		10-bit mode	Self-diagnosis voltage level = AnVREF		1003-|TOEn|		1023	—
			Self-diagnosis voltage level = 2/3AnVREF		663-|TOEn|	683	703+|TOEn|	—
			Self-diagnosis voltage level = 1/2AnVREF		492-|TOEn|	512	532+|TOEn|	—
			Self-diagnosis voltage level = 1/3AnVREF		321-|TOEn|	341	361+|TOEn|	—
			Self-diagnosis voltage level = AnVSS		0		20+|TOEn|	—

(2/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Integral nonlinearity error*1	ILEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±2.0	LSB
				ADCA0I0-5 (T&H used)			±3.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±3.0	LSB
				ADCA0I0-5 (T&H used)			±4.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB
Differential nonlinearity error*1	DLEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±1.0	LSB
				ADCA0I0-5 (T&H used)			±2.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±3.0	LSB
				ADCA0I0-5 (T&H used)			±4.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.0V to 4.5V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
Zero scale error (offset error)*1	ZSEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±3.5	LSB
				ADCA0I0-5 (T&H used)			±5.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±5.5	LSB
				ADCA0I0-5 (T&H used)			±7.5	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±0.5	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
Full scale error*1	FSEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (T&H not used)			±3.5	LSB
				ADCA0I0-5 (T&H used)			±5.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm (T&H not used)			±5.5	LSB
				ADCA0I0-5 (T&H used)			±7.5	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±0.5	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB

Note: Conversion accuracy when ADCA0ImS terminal is converted in 12-bit mode: Conversion accuracy can be applied if lower 2-bit is ignored from conversion result.

Note 1. This does not include quantization error.

Note 2. 3.0 + 1.3 × (the number of used T&H)

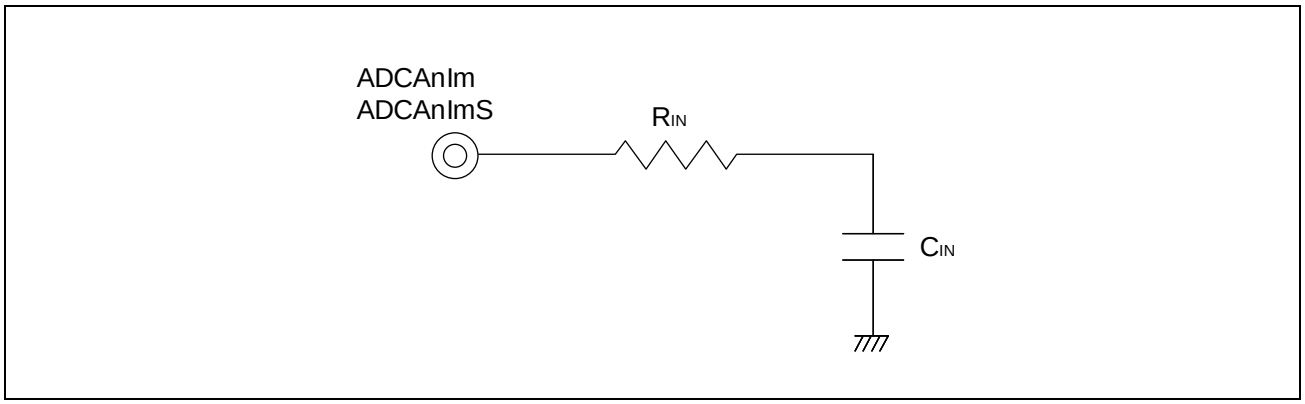
Note 3. Include the oscillation accuracy of HS IntOSC.

Note 4. When the external multiplexer is used, the detailed time of A/D conversion is MPX setup time, sampling time and successive approximation time. MPX setup time is same as “sampling time + successive approximation time”.

CAUTION

When an external digital pulse is applied to AP0, P8, and P9 pins during an A/D conversion this may lead to an A/D conversion result with a larger conversion error as expected due to the coupling noise of the external digital pulse. The same behavior may apply when the digital buffer is used as an output pin. For the output port the potential degradation increases with the driven total output current of the port. In addition the conversion resolution may drop if the output current fluctuates at adjacent pins due to the coupling effect of the external circuit connected to these port pins.

3C.6.1 Equivalent Circuit of the Analog Input Block



Terminals	Condition	RIN (kΩ)	CIN (pF)
ADCA0I0 to 5	When T&H is used	14.2	2.1
	When T&H is not used	4.2	2.1
ADCA0I6 to 15	—	4.2	2.1
ADCA0I0S to 3S, 5S to 16S	—	5.6	9.5
ADCA0I4S, 17S to 19S	—	6.2	9.5

CAUTION

This specification is not tested during outgoing inspection. Therefore RIN and CIN are reference values only and not guaranteed. In addition these values are specified as maximum values.

3C.7 Flash Programming Characteristics

3C.7.1 Code Flash

The code flash memory is shipped in the erased state. If the code flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3C.19 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3		4*4		30	MHz
Number of rewrites*1	CWRT	Data retention of 20 years*2	1000			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 1000), the device can be erased “n” times for each block. For example, when a block of 32 KB is erased after 256 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Note 3. f_{PCLK} = 1/4 f_{CPUCLK_M}: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 3C.20 Programming Characteristic

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz CWRT < 100 times	256 B		0.4*1	6*1	ms
			8 KB		20	90	ms
			32 KB		80	360	ms
			256 KB		0.6	2.7	s
			384 KB		0.9	4.1	s
			512 KB		1.2	5.4	s
			768 KB		1.7	8.1	s
			1 MB		2.3	10.8	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	256 B		0.5*1	7.2*1	ms
			8 KB		24	108	ms
			32 KB		96	432	ms
			256 KB		0.7	3.3	s
			384 KB		1.1	4.9	s
			512 KB		1.4	6.5	s
			768 KB		2.1	9.8	s
			1 MB		2.7	13	s
Erase time		f_{PCLK} ≥ 20 MHz CWRT < 100 times	8 KB		39	120	ms
			32 KB		141	480	ms
			256 KB		1.2	3.5	s
			384 KB		1.7	5.3	s
			512 KB		2.3	7	s
			768 KB		3.4	10.5	s
			1 MB		4.5	14	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	8 KB		47	144	ms
			32 KB		169	576	ms
			256 KB		1.4	4.2	s
			384 KB		2.1	6.3	s
			512 KB		2.7	8.4	s
			768 KB		4.1	12.6	s
			1 MB		5.4	16.8	s

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

3C.7.2 Data Flash

The data flash memory is shipped in the erased state. If the data flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Table 3C.21 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3		4*4		30	MHz
Number of rewrites*1	CWRT	Data retention 20 years*2	125 k			times
		Data retention 3 years*2	250 k			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 125000), the device can be erased “n” times for each block. For example, when a block of 64 bytes is erased after 4 bytes of writing have been performed for different addresses 16 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the data flash memory.

Note 3. f_{PCLK} = 1/4 f_{CPUCLK_M}: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 3C.22 Programming Characteristics

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz	4 B		0.16*1	1.7*1	ms
			32 KB		1.4	6.8	s
			64 KB		2.79	13.44	s
Erase time		f_{PCLK} ≥ 20 MHz	64 B		1.7*1	10*1	ms
			32 KB		0.9	5.2	s
			64 KB		1.74	10.24	s
Blank check time		f_{PCLK} ≥ 20 MHz	4 B			30*1	µs
			64 B			100*1	µs
			32 KB			35.2	ms
			64 KB			70.4	ms

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

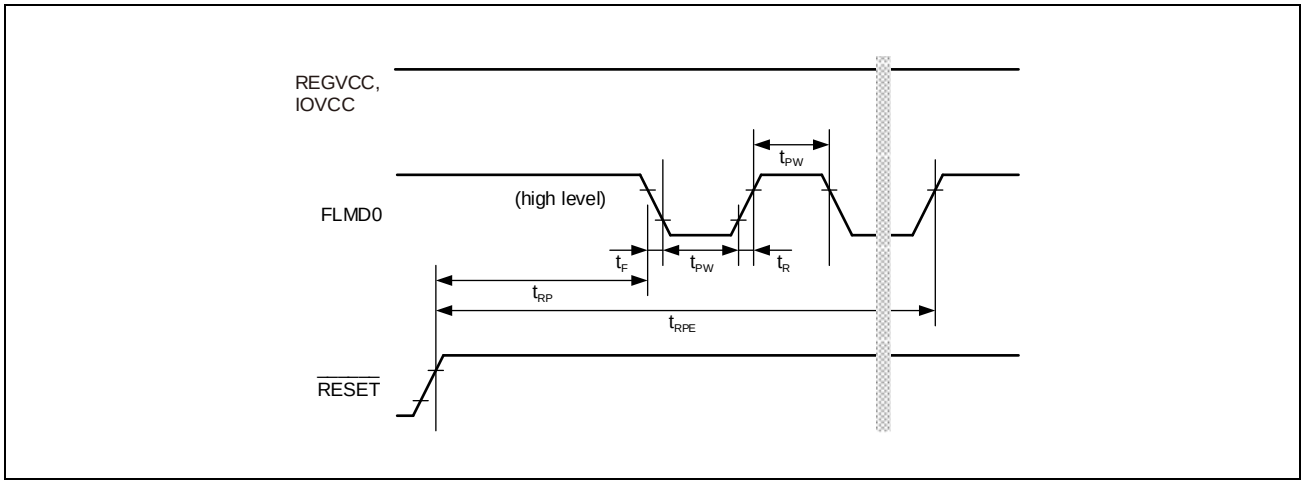
3C.7.3 Serial Programming Interface

3C.7.3.1 Serial Programmer Setup Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0 pulse input start time	t_{RP}		1.5			ms
FLMD0 pulse input end time	t_{RPE}				101.5	ms
FLMD0 low/high level width	t_{PW}		1.6			µs
FLMD0 rise time	t_R				20	ns
FLMD0 fall time	t_F				20	ns

Note: IOVCC: EVCC = A0VREF



3C.7.3.2 Flash Programming Interface

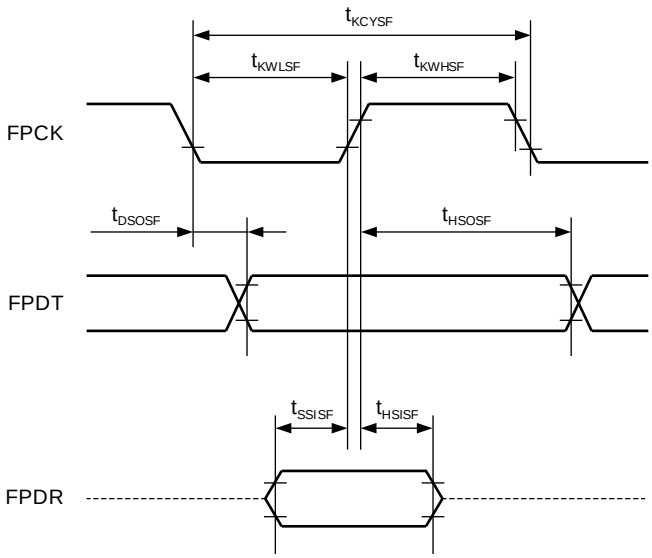
Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%,
Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Flash Programming transfer rate		1-wired UART mode			1	Mbps
		2-wired UART mode			1.5	Mbps
FPCK cycle time	t_{KCYSF}	3-wired clock sync mode	200*1			ns
FPCK high level width	t_{KWHSF}	3-wired clock sync mode	t_{KCYSF} / 2 – 15			ns
FPCK low level width	t_{KWLSF}	3-wired clock sync mode	t_{KCYSF} / 2 – 15			ns
FPDR setup time (vs. FPCK)	t_{SSISF}	3-wired clock sync mode	t_{Pcyc} × 2			ns
FPDR hold time (vs. FPCK)	t_{HSISF}	3-wired clock sync mode	t_{Pcyc} × 2			ns
FPDT output delay (vs. FPCK)	t_{DSOSF}	3-wired clock sync mode Not continuous transfer (data: 1st bit)			0	ns
		3-wired clock sync mode Not continuous transfer (data: except 1st bit)			$–t_{KWHSF}$ + 3 × t_{Pcyc} + 36	ns
FPDT hold time (vs. FPCK)	t_{HSOSF}	3-wired clock sync mode	t_{Pcyc} × 2			ns

Note 1. Input an external clock that is more than 6 clocks of PCLK.

NOTE

t_{Pcyc} is period of PCLK.



3C.8 Thermal Characteristics

3C.8.1 Parameters

Package	Item	Symbol	Estimate	Unit	Note
100-pin LQFP	Thermal Resistance	Θja	44.3	°C/W	Conforming to JESD51-7
	Thermal Characterization Parameter	ψjb	34.7		(4 layers)
80-pin LQFP	Thermal Resistance	Θja	44.5	°C/W	Conforming to JESD51-7
	Thermal Characterization Parameter	ψjb	34.0		(4 layers)
64-pin LQFP	Thermal Resistance	Θja	45.3	°C/W	Conforming to JESD51-7
	Thermal Characterization Parameter	ψjb	33.8		(4 layers)
48-pin LQFP	Thermal Resistance	Θja	47.0	°C/W	Conforming to JESD51-7
	Thermal Characterization Parameter	ψjb	33.8		(4 layers)

NOTE

The thermal resistance and characterization parameters depend on the usage environment.

3C.8.2 Board

Conforming to JESD51-7 (4 layers)

	Board Size (mm)		
	X	Y	Area (mm^2)
Board	76.2	114.3	8709.66
Remaining copper rates	Thickness of conductors		
50-95-95-50%	70-35-35-70 µm		

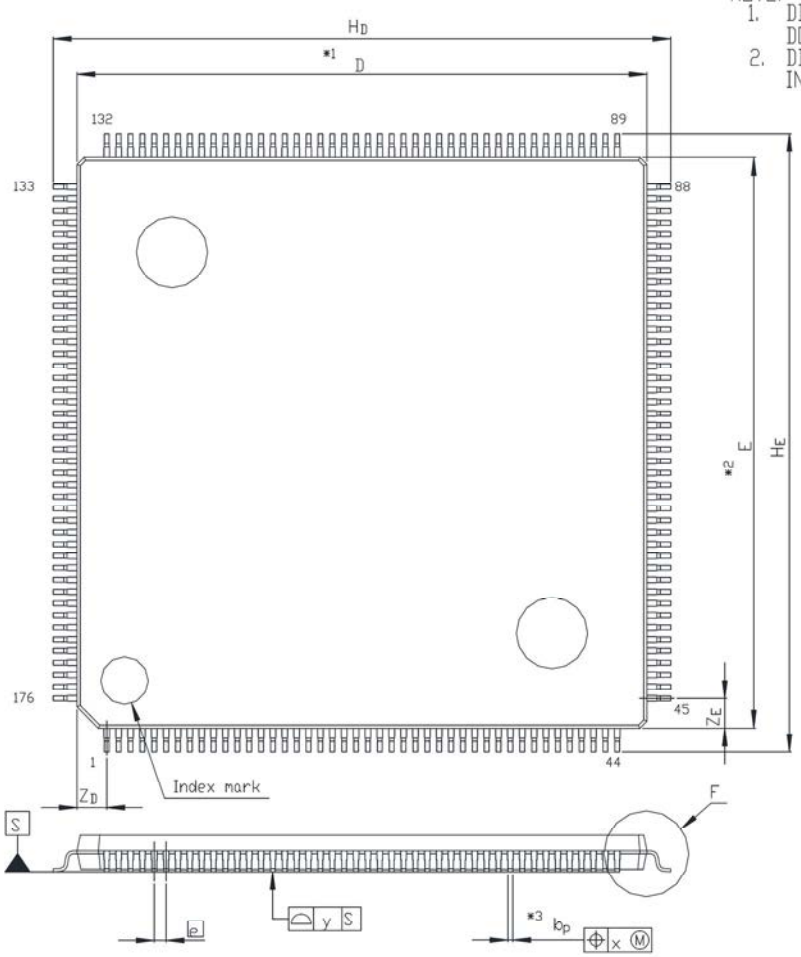
Appendix A Package

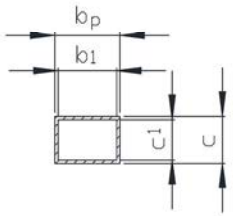
A.1 Package Dimensions of RH850/F1KH-D8

A.1.1 176 Pins

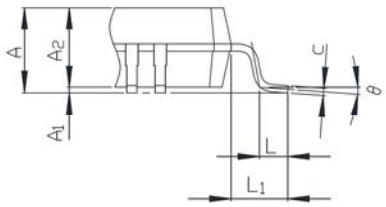
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A / FP-176E / FP-176EV	1.8

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.





Terminal cross section



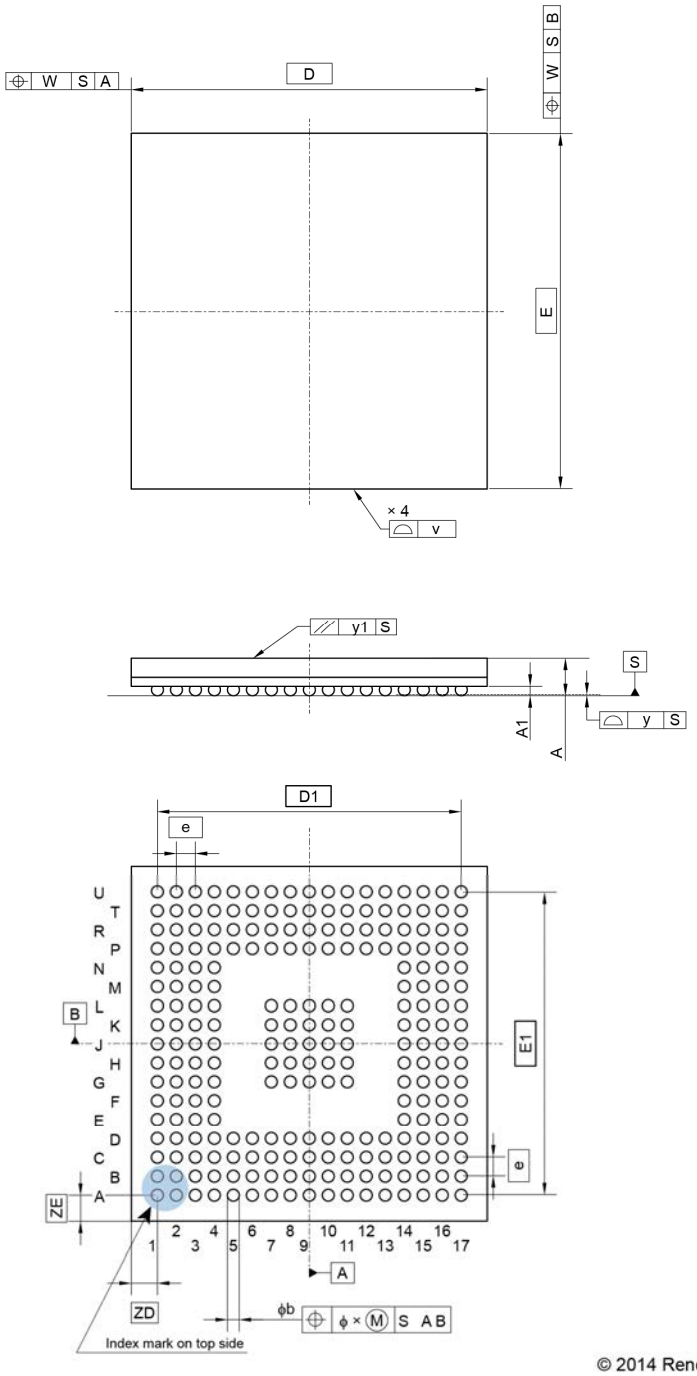
Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

A.1.2 233 Pins

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-FBGA233-15x15-0.80	PRBG0233GA-A	—	0.75

Unit: mm



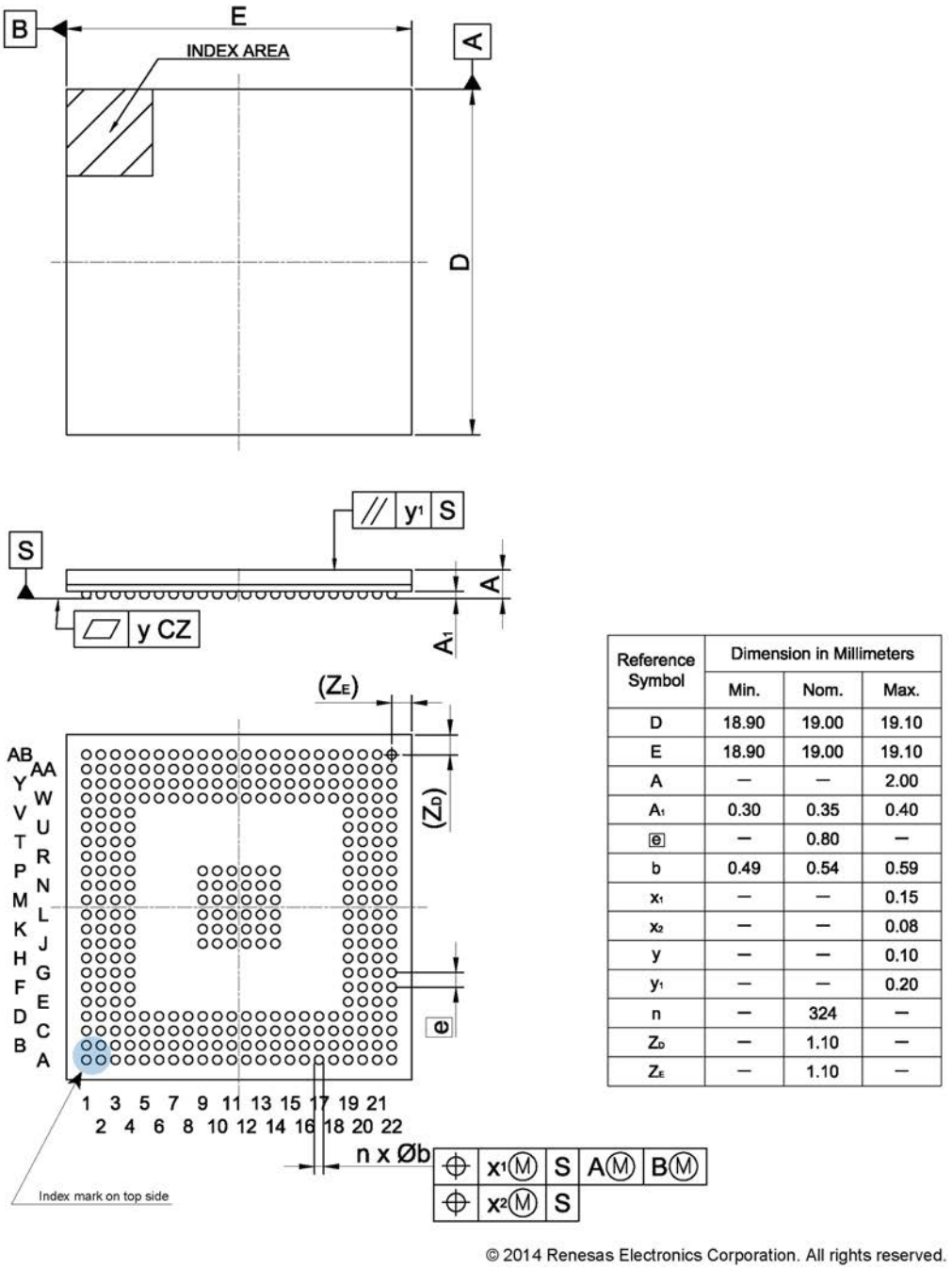
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	—	15.00	—
D1	—	12.80	—
E	—	15.00	—
E1	—	12.80	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.58	1.90
A1	0.30	0.35	0.40
b	0.49	0.54	0.59
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
ZD	—	1.10	—
ZE	—	1.10	—

Note: The index mark on the top side can be displayed by different characters (e.g. triangle, square).

A.1.3 Reserved

A.1.4 324 Pins

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-FBGA324-19x19-0.80	PRBG0324GB-A	1.10



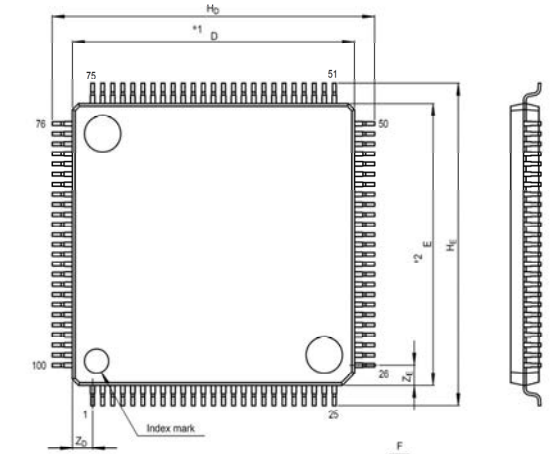
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	18.90	19.00	19.10
E	18.90	19.00	19.10
A	—	—	2.00
A_1	0.30	0.35	0.40
e	—	0.80	—
b	0.49	0.54	0.59
x_1	—	—	0.15
x_2	—	—	0.08
y	—	—	0.10
y_1	—	—	0.20
n	—	324	—
Z_D	—	1.10	—
Z_E	—	1.10	—

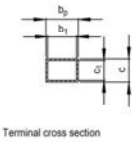
Note: The index mark on the top side can be displayed by different characters (e.g. triangle, square).

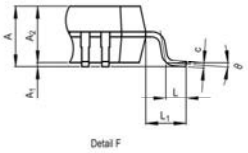
A.2 Package Dimensions of RH850/F1KM-S4 and RH850/F1KM-S2

A.2.1 100 Pins in RH850/F1KM-S4 and RH850/F1KM-S2

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g





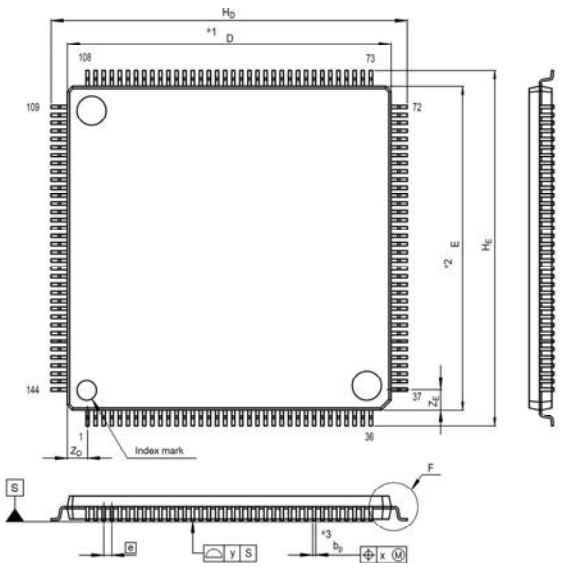


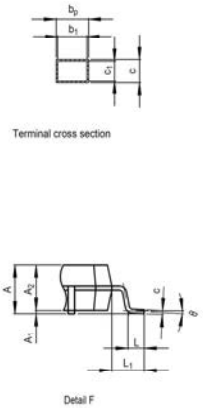
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

A.2.2 144 Pins in RH850/F1KM-S4 and RH850/F1KM-S2

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





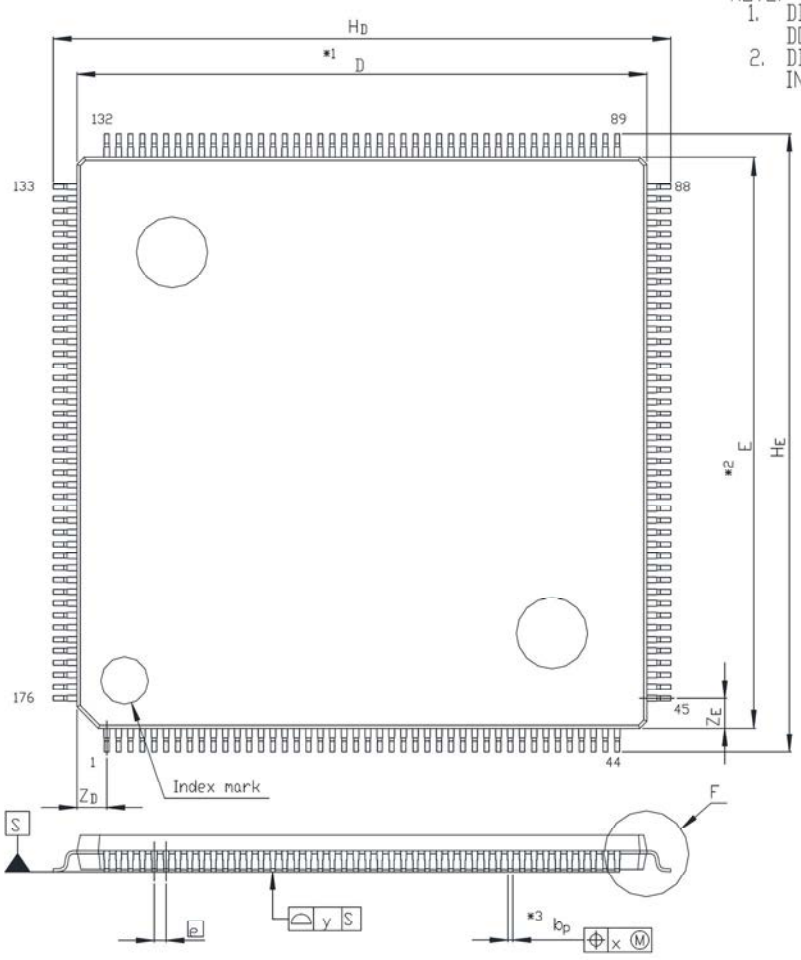
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

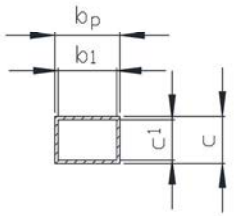
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

A.2.3 176 Pins in RH850/F1KM-S4 and RH850/F1KM-S2

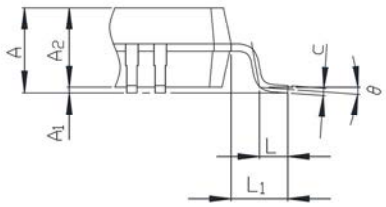
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A / FP-176E / FP-176EV	1.8

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.





Terminal cross section



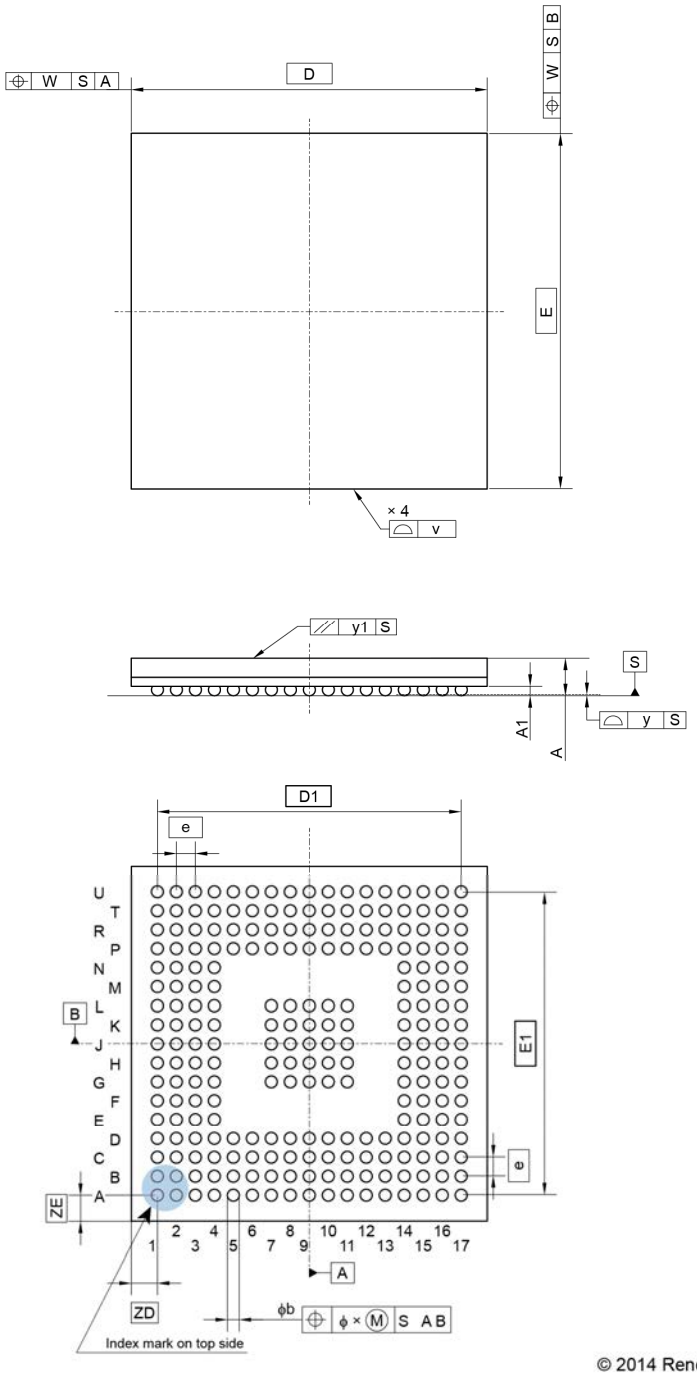
Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

A.2.4 233 Pins in RH850/F1KM-S4

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-FBGA233-15x15-0.80	PRBG0233GA-A	—	0.75

Unit: mm



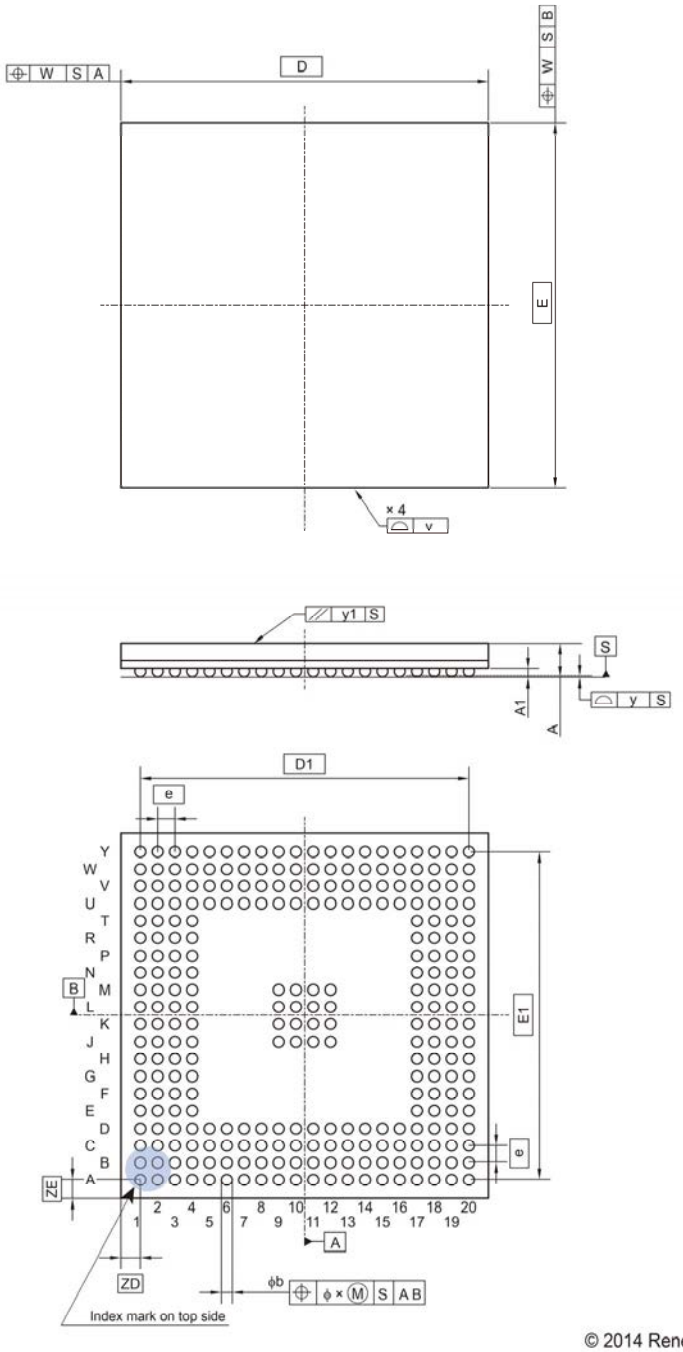
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	—	15.00	—
D1	—	12.80	—
E	—	15.00	—
E1	—	12.80	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.58	1.90
A1	0.30	0.35	0.40
b	0.49	0.54	0.59
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
ZD	—	1.10	—
ZE	—	1.10	—

Note: The index mark on the top side can be displayed by different characters (e.g. triangle, square).

A.2.5 272 Pins in RH850/F1KM-S4

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-FBGA272-17x17-0.80	PRBG0272GB-A	—	0.90

Unit: mm



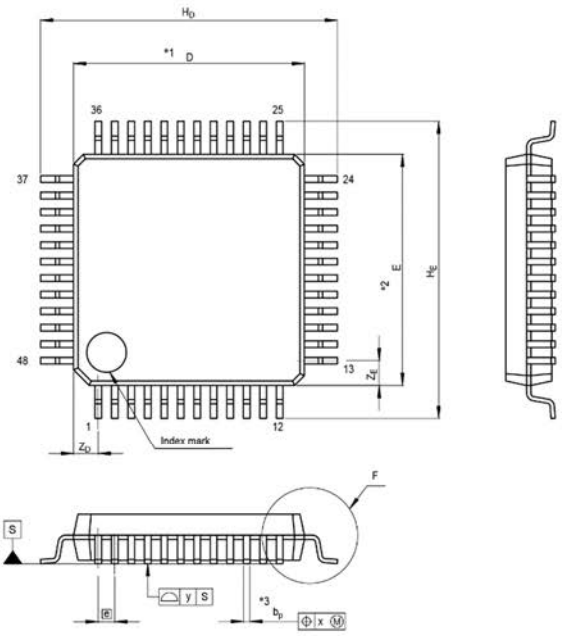
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	—	17.00	—
D1	—	15.20	—
E	—	17.00	—
E1	—	15.20	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.58	2.00
A1	0.30	0.35	0.40
b	0.49	0.54	0.59
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
ZD	—	0.90	—
ZE	—	0.90	—

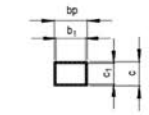
Note: The index mark on the top side can be displayed by different characters (e.g. triangle, square).

A.3 Package Dimensions of RH850/F1KM-S1

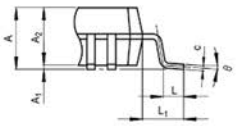
A.3.1 48 Pins

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g





Terminal cross section



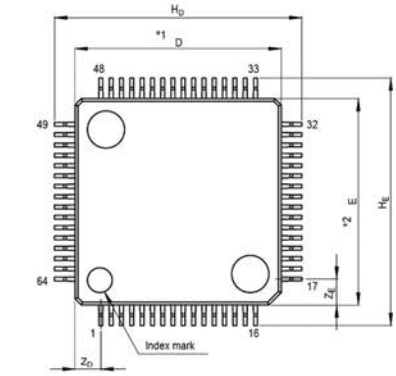
Detail F

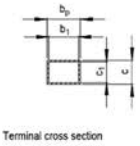
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

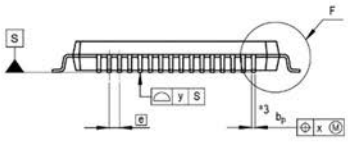
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

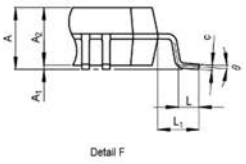
A.3.2 64 Pins

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g









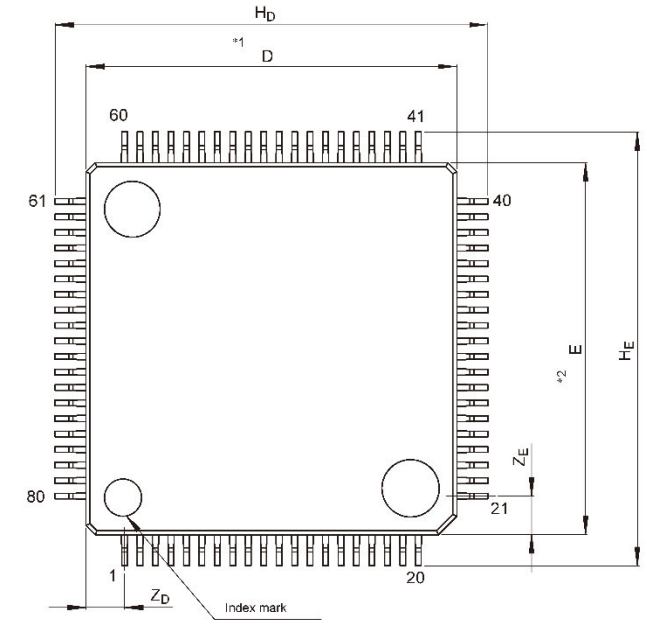
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

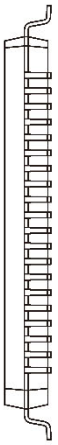
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

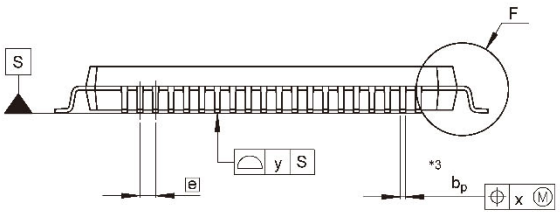
A.3.3 80 Pins

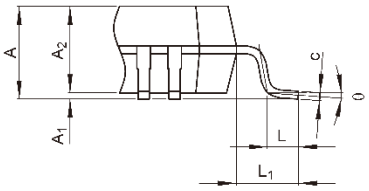
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KG-A	—	0.50

Unit: mm

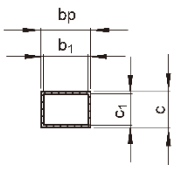








Detail F



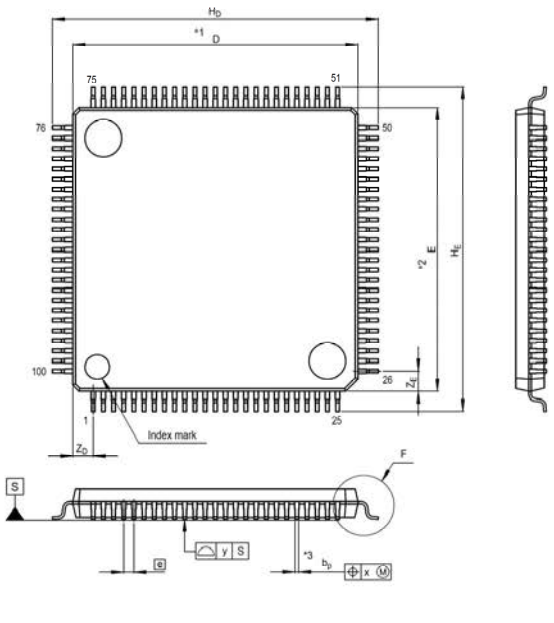
Terminal cross section

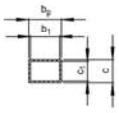
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0.05	0.10	0.15
bp	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

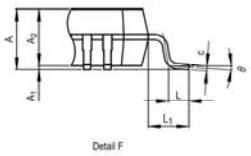
A.3.4 100 Pins

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Revision History	RH850/F1KH, RH850/F1KM Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Sep 15, 2023	—	First Edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
5. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
6. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
7. Power ON/OFF sequence
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.