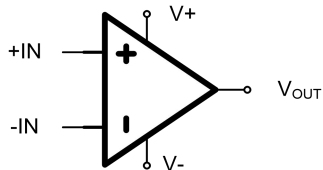


GT8501 GT8502 GT8504

High Precision, Low-Offset, Rail-to-Rail I/O CMOS Op Amps

1 Features	2 Application
<ul style="list-style-type: none"> - Low offset voltage: $\pm 20 \mu\text{V}$ - Low offset drift: $\pm 0.1 \mu\text{V}/^\circ\text{C}$ - Low-input bias current: 50 pA - Low noise: 13 μV p-p (0.01Hz ~ 10Hz) - Rail-to-rail input and output - High gain, CMRR, PSRR: 105 dB - High slew rate: 60 V/ms - Gain bandwidth: 45 KHz - Quiescent current: 7 μA per amplifier - Single supply: 2.5 V to 5.5 V 	<ul style="list-style-type: none"> - Temperature sensors - Medical/industrial instrumentation - Pressure sensors - Battery-powered instrumentation - Active filtering - Weight scale sensor - Strain gage amplifiers - Power converter/inverter

3 Description	Circuit Diagram
<p>The GT850X, GT8501, GT8502 and GT8504, family of precision amplifiers offers state-of-the-art performance. With zero-drift technology, the GT850X offset voltage and offset drift provide unparalleled long-term stability. With a mere 7 μA of quiescent current, the GT850X are able to achieve a 45-KHz bandwidth. These small-size, high-precision operational amplifiers have high input impedance and rail-to-rail input and rail-to-rail output swing. The GT850X feature flat bias current over temperature. Therefore, no calibration is needed in high input impedance applications over temperature.</p> <p>All versions are specified over the temperature range of -40°C to $+125^\circ\text{C}$.</p>	

4 Revision History

Revision	Date	Note
Rev. A1.0	2023. 10. 23	Original Version
Rev.A1.1	2023. 10. 23	1.Updated Package Qty 2.Added Tape and Reel Information 3. Added Application Note
Rev.A1.2	2023. 12. 26	1. Added Marking 2. Added MSL
Rev.A1.3	2024. 01. 26	Updated Part Name

The latest datasheet version should be checked on the GTIC official website, as the company does not actively inform customers about updates to the datasheet.

5 Device Summary, Pin and Packages

Table 5-1. Device Summary⁽¹⁾

Serial Name	Part Name	Package	Body Size (Nom)	Marking ⁽²⁾	MSL ⁽³⁾	Package Qty
GT8501	GT8501C5	SC70-5	2.10mm×1.25mm×1.00mm	GT8501 XXXXX	3	Tape and Reel,3000
	GT8501S5	SOT23-5	2.90mm×1.60mm×1.10mm	GT8501 XXXXX	3	Tape and Reel,3000
	GT8501M8	MSOP-8	3.00mm×3.00mm×1.10mm	GT8501 XXXXXXXX	3	Tape and Reel,4000
	GT8501P8	SOP-8(SOIC-8)	6.00mm×3.90mm×1.75mm	GT8501 XXXXXXXX	3	Tape and Reel,4000
GT8502	GT8502M8	MSOP-8	3.00mm×3.00mm×1.10mm	GT8502 XXXXXXXX	3	Tape and Reel,4000
	GT8502P8	SOP-8(SOIC-8)	6.00mm×3.90mm×1.75mm	GT8502 XXXXXXXX	3	Tape and Reel,4000
GT8504	GT8504TD	TSSOP-14	5.00mm×4.40mm×1.20mm	GT8504 XXXXXXXX	3	Tape and Reel,4000
	GT8504PD	SOP-14(SOIC-14)	8.65mm×3.90mm×1.75mm	GT8504 XXXXXXXX	3	Tape and Reel,4000

(1) For all available packages, please contact product sales

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

(4) "XXXXX" in Marking will be appeared as the batch code.

FAE: 13148878879

5 Device Summary, Pin and Packages(continued)

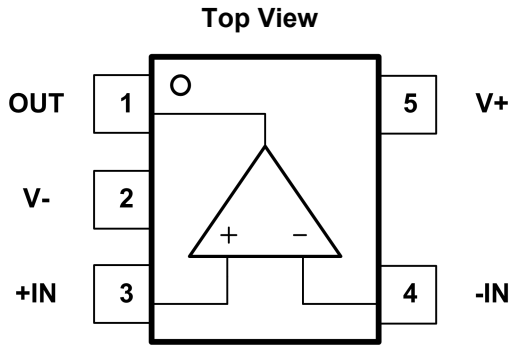


Fig. 5-1. GT8501: S5(SOT23-5) Package
GT8501: C5(SC70-5) Package

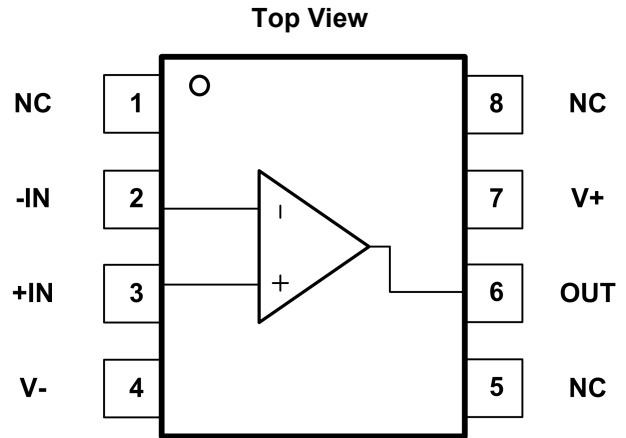
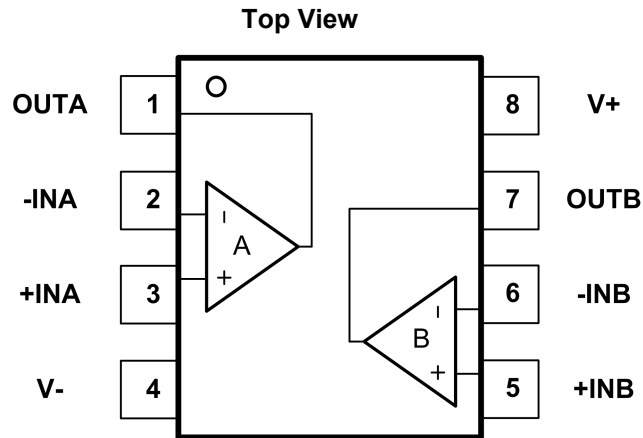


Fig.5-2. GT8501: P8(SOP8/ SOIC-8) Package
GT8501: M8(MSOP8) Package

Table 5-2 Pin Definition

Name	Pin		I/O	Description
	S5 C5	P8 M8		
-IN	4	2	I	Negative (inverting) input
+IN	3	3	I	Positive(noninverting) input
NC	-	1,5,8	-	No internal connection (can be left floating)
OUT	1	6	O	Output
V-	2	4	-	Negative (lowest) power supply
V+	5	7	-	Positive (highest) power supply

* It is suggested to leave the unconnected pins floating.

5 Device Summary, Pin and Packages(continued)

Fig.5-3. GT8502: P8(SOP8/ SOIC-8) Package
GT8502: M8(MSOP8) Package
Table 5-3 Pin Definition

Name	Pin		I/O	Description
	P8	M8		
-INA	2		I	Inverting input, channel A
+INA	3		I	Noninverting input, channel A
-INB		6	I	Inverting input, channel B
+INB		5	I	Noninverting input, channel B
OUTA	1		O	Output, channel A
OUTB		7	O	Output, channel B
V-	4		-	Negative (lowest) power supply
V+		8	-	Positive (highest) power supply

* It is suggested to leave the unconnected pins floating.

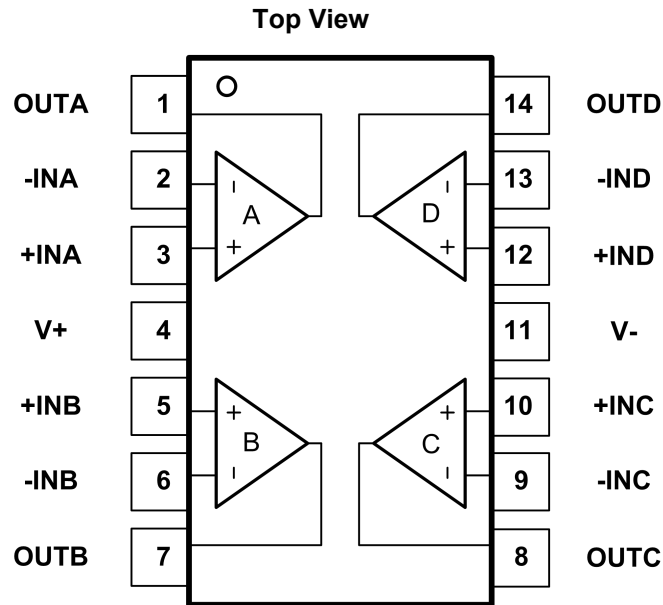
5 Device Summary, Pin and Packages(continued)


Fig.5-4. GT8504: PD(SOIC-14/SOP14) Package
GT8504: TD(TSSOP14) Package

Table 5-4 Pin Definition

Name	Pin	I/O	Description
	PD TD		
-INA	2	I	Inverting input, channel A
+INA	3	I	Noninverting input, channel A
-INB	6	I	Inverting input, channel B
+INB	5	I	Noninverting input, channel B
-INC	9	I	Inverting input, channel C
+INC	10	I	Noninverting input, channel C
-IND	13	I	Inverting input, channel D
+IND	12	I	Noninverting input, channel D
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
OUTC	8	O	Output, channel C
OUTD	14	O	Output, channel D
V-	11	-	Negative (lowest) power supply
V+	4	-	Positive (highest) power supply

* It is suggested to leave the unconnected pins floating.

6 Voltage, Temperature, ESD and Thermal ratings

6.1 Absolute Maximum Ratings

Parameters	Min	Max	Unit
Supply Voltage ,Vs=(V+)-(V-)		6.5	V
Select Input Voltage	(V-)-0.5	(V+)+0.5	V
Maximum Junction Temperature	-55	150	°C
Storage Temperature Range	-55	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current- limited to 10mA or less.

6.2 ESD Ratings

ESD		Value	Unit
V(ESD)	Electrostatic discharge	Human-body model (HBM)	7 K
		Charged-Device Model (CDM)	2 K

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Min	Max	Unit
VCC	Single-supply ,Vs=(V+)-(V-)	2.5	5.5	V
VCC	Dual-supply ,Vs=(V+)-(V-)	±1.25	±2.75	V
TA	Operating temperature	-40	125	°C

6.4 Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SC70-5	400	150	°C/W
SOT23-5	250	81	°C/W
MSOP-8	210	45	°C/W
SOP-8(SOIC-8)	158	43	°C/W
TSSOP-14	180	35	°C/W
SOP-14(SOIC-14)	120	36	°C/W

7 Electrical Specifications

V_{CC}=5.0V, V_{CM}=V_{CC}/2, and R_L=10kΩ, FULL=-40°C to +125°C, Typical values are at TA=+25°C. (unless otherwise noted)

Parameter	Symbol	Condition	GT8501 GT8502 GT8504			
			Min	Typ	Max	Unit
OFFSET VOLTAGE						
Input Offset Voltage	VOS	V _{CM} =V _S /2	-40	±20	40	μV
Input Offset Voltage Average Drift	VOS TC			±0.1	±0.2	μV/°C
Power-Supply Rejection Ratio	PSRR	V _S =+2.5V to +5.5V, V _{CM} =0	95	105		dB
Channel Separation, dc				0.1		μV/V
INPUT BIAS CURRENT						
Input Bias Current	IB	V _{CM} =V _S /2		±50		pA
Input Offset Current	IOS			±10		pA
NOISE PERFORMANCE						
Input Voltage Noise	enp-p	f=0.01Hz to 10Hz		13		μVpp
Input Voltage Noise	enp-p	f=0.01Hz to 1Hz		NA		μVpp
Input Voltage Noise Density	en	f=1KHz		300		nV/√Hz
Input Current Noise Density	in	f=10Hz		NA		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V _{CM}		(V ₋)-0.1		(V ₊)+0.1	V
Common-Mode Rejection Ratio	CMRR	(V ₋)-0.1V<V _{CM} <(V ₊)+0.1V	95	105		dB
INPUT CAPACITANCE						
Differential				1		pF
Common-Mode				5		pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	AOL	R _L =10KΩ, V _O =0.3V to 4.7V, T _A =-40°C to 125°C	95	105		dB
DYNAMIC PERFORMANCE						
Slew Rate	SR	G=+1		60		V/ms
Gain-Bandwidth Product	GBW			45		KHz
Overload Recovery Time				50		μs
OUTPUT CHARACTERISTICS						
Output Voltage High	VOH	R _L =100 KΩ to GND	4.99	4.997		V
		R _L =10 KΩ to GND	4.95	4.98		V
Output Voltage Low	VOL	R _L =100 KΩ to V ₊		1	20	mV
		R _L =10 KΩ to V ₊		10	40	mV
Short-Circuit Current	ISC			10		mA
POWER SUPPLY						
Operating Voltage Range	V _S		2.5		5.5	V
Quiescent Current/ Amplifier	I _Q			7	10	μA

8 Typical Characteristics

V_{cc}=5.0V, V_{cm}=V_{cc}/2, and R_L=10kΩ, T_A=+25°C. (unless otherwise noted)

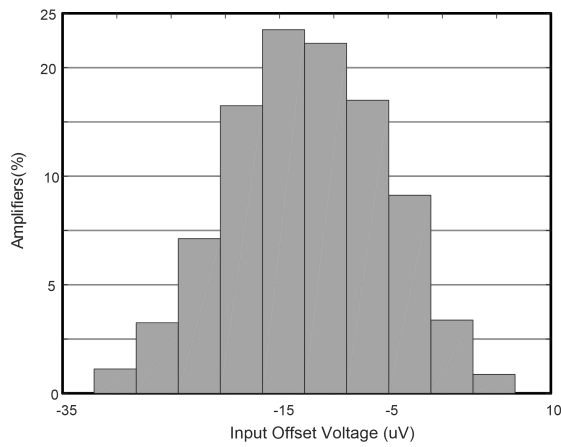


Fig.8-1. Offset Voltage Distribution

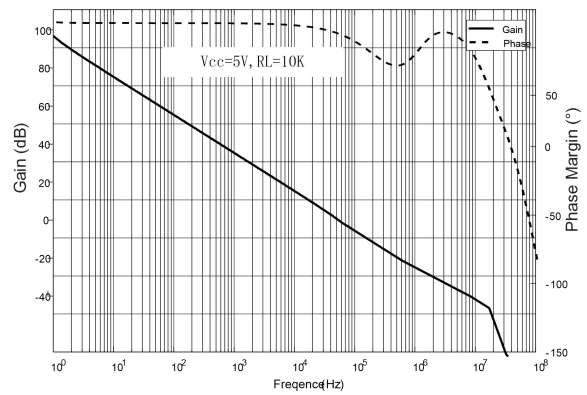


Fig.8-2. Open-Loop Gain and Phase vs Frequency

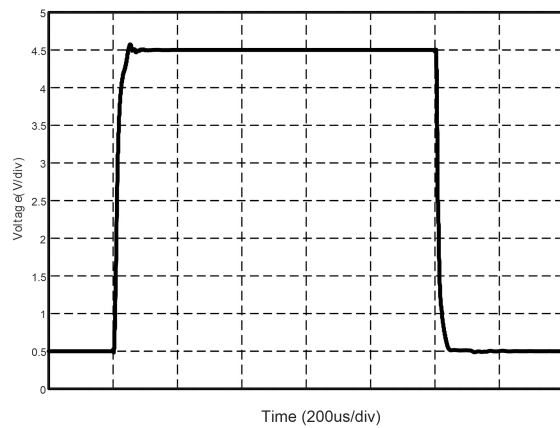


Fig.8-3. Large-Signal Step Response

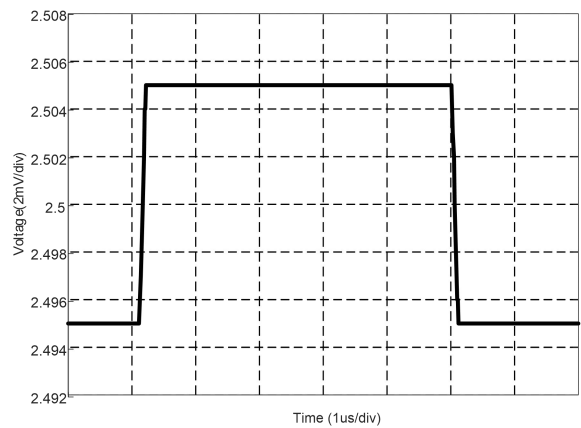


Fig.8-4. Small-Signal Step Response

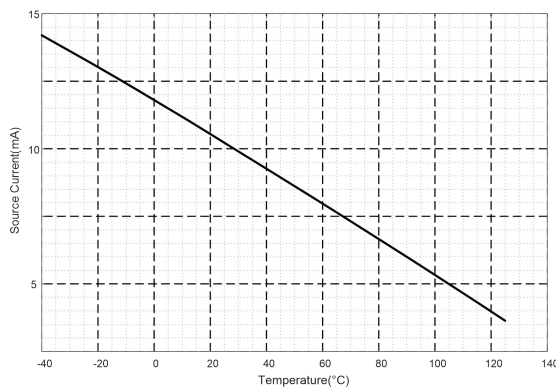


Fig.8-5. Source Current vs Temperature

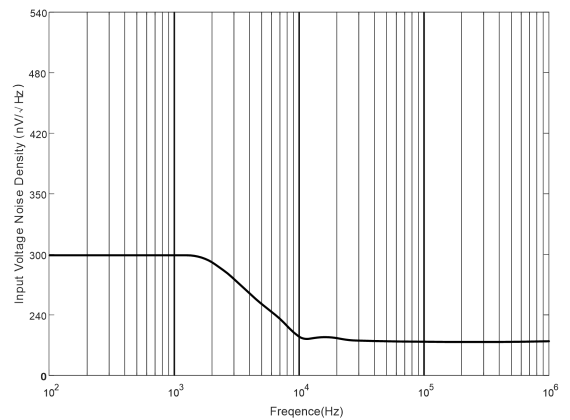


Fig.8-6. Input Voltage Noise Density vs Frequency

9 Detailed Description

9.1 Overview

The GT850X family of zero-drift amplifiers is engineered with state-of-the-art, proprietary, precision zero-drift technology. These amplifiers offer ultra-low input offset voltage and drift, and achieve excellent input and output dynamic linearity. The GT850X operate from 2.5 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose and precision applications.

9.2 Feature Description

The GT8501, GT8502, GT8504 series op amplifiers operate over a power-supply range of +2.5 V to +5.5V ($\pm 1.25V$ to $\pm 2.75V$). Supply voltages higher than 6.5 V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

10 Application Note

The GT8501, GT8502, GT8504 series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature. Good layout practice mandates use of a 0.1 μ F capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

During normal operation, the typical input bias current of the GT850X is 50 pA. The device exhibits low drift over the full temperature range of $-40^{\circ}C$ to $+125^{\circ}C$. There are no antiparallel diodes between the input pins (+IN and -IN); therefore, the differential input maximum voltage is limited only by diodes connected to the supply voltage pins. The equivalent input circuit of GT850X is shown in Figure 10-1.

However, designer should then avoid the input voltage difference exceeding the device's recommended operating range. If the input voltage difference is too large, it may take a long time (please refer to the indicators Overload Recovery Time) for the auto-zero circuit inside the op amp to return to VOS accuracy when the input voltage difference returns to the normal range.

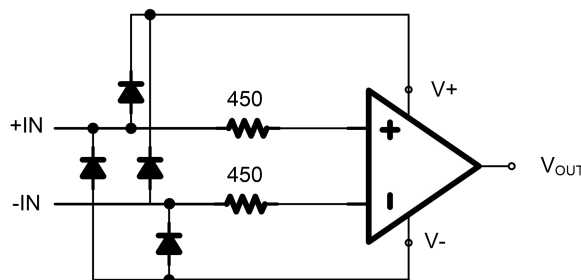
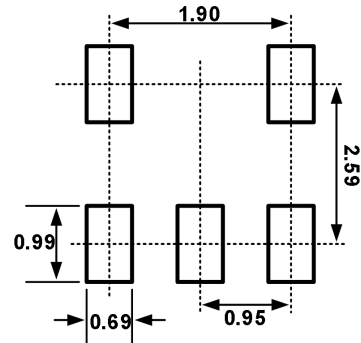
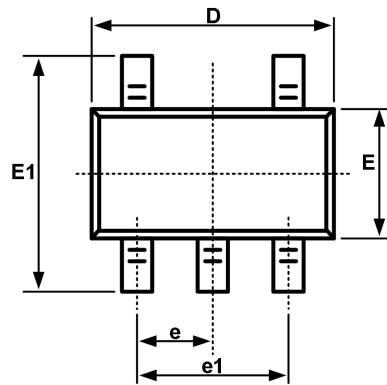


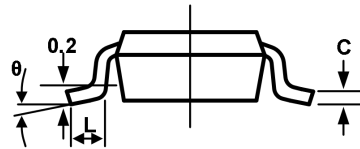
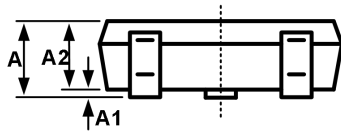
Fig.10-1. Equivalent Input Circuit

11 Package Outline Dimension

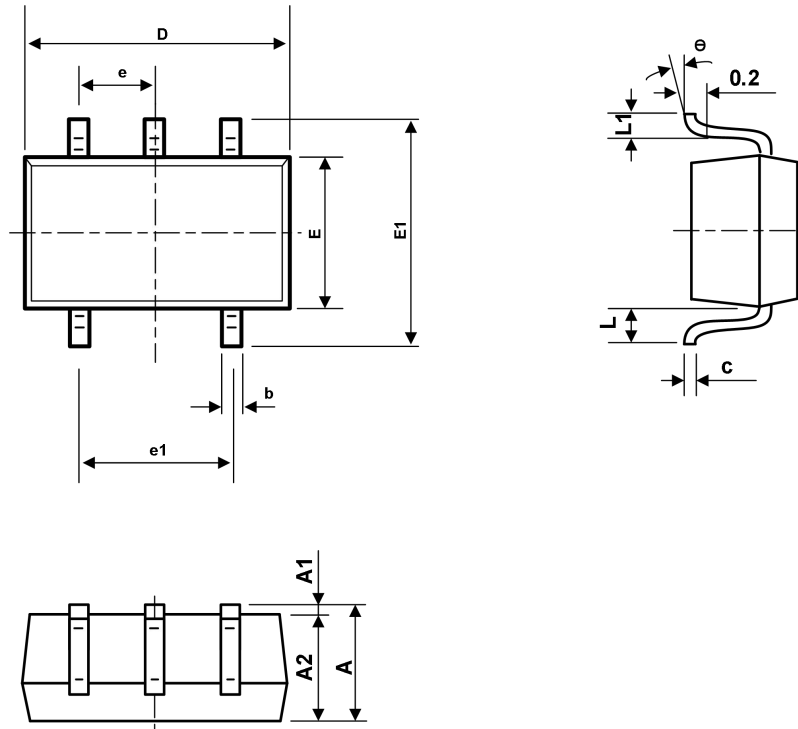
SOT23-5



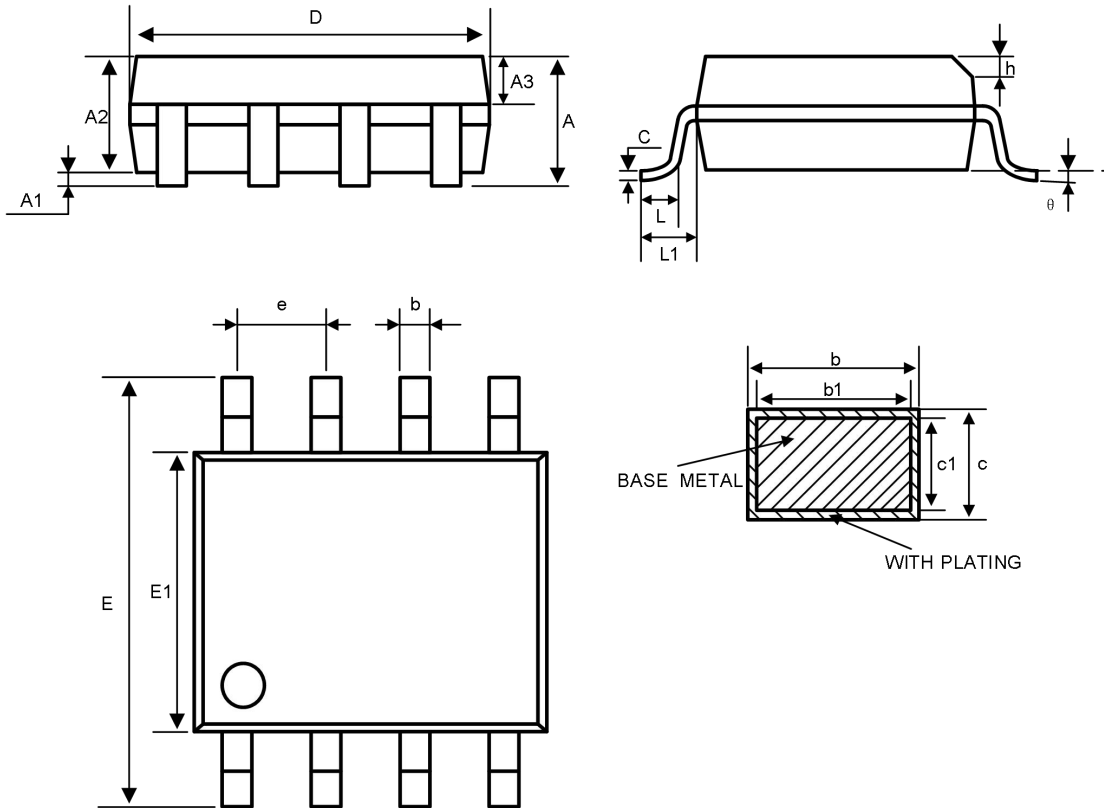
Recommended Land Pattern (Unit: mm)



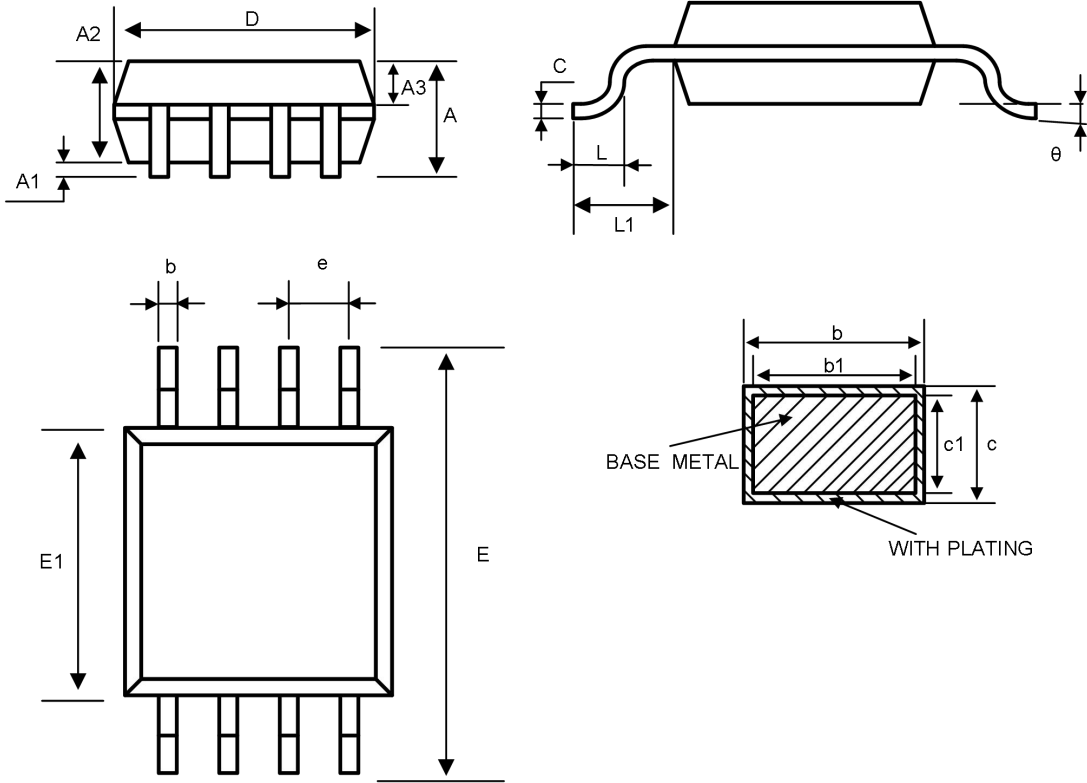
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF		0.024REF	
θ	0°	8°	0°	8°

11 Package Outline Dimension(continued)
SC70-5


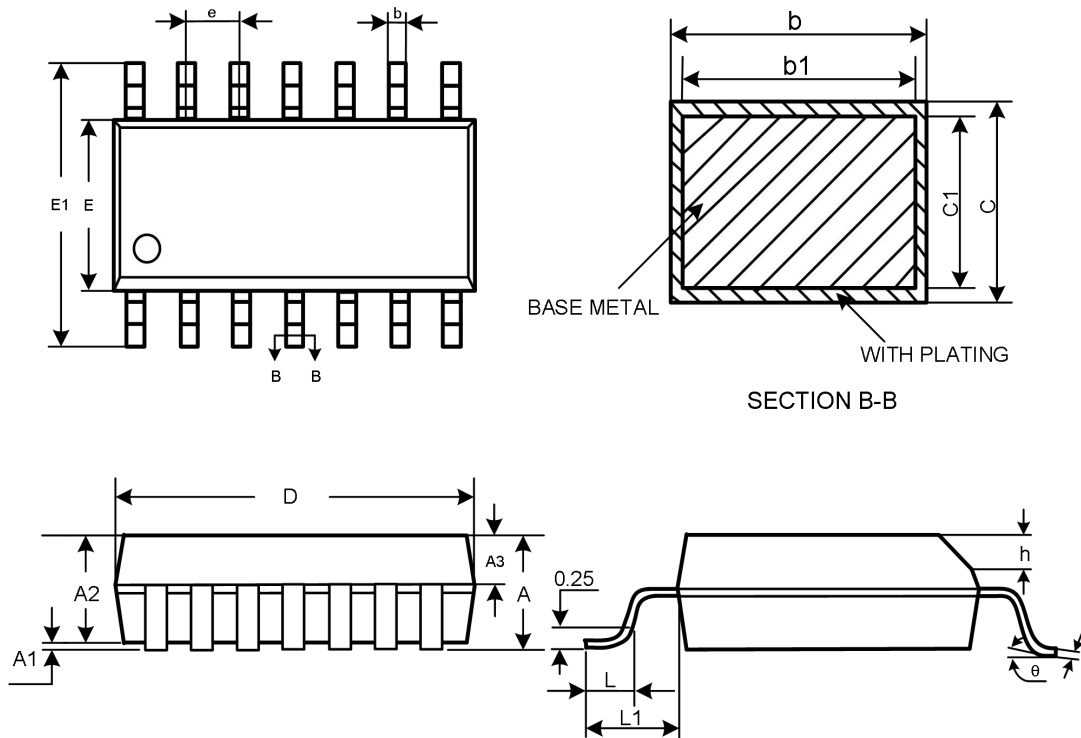
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L	0.525REF		0.021REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

11 Package Outline Dimension(continued)
SOP8


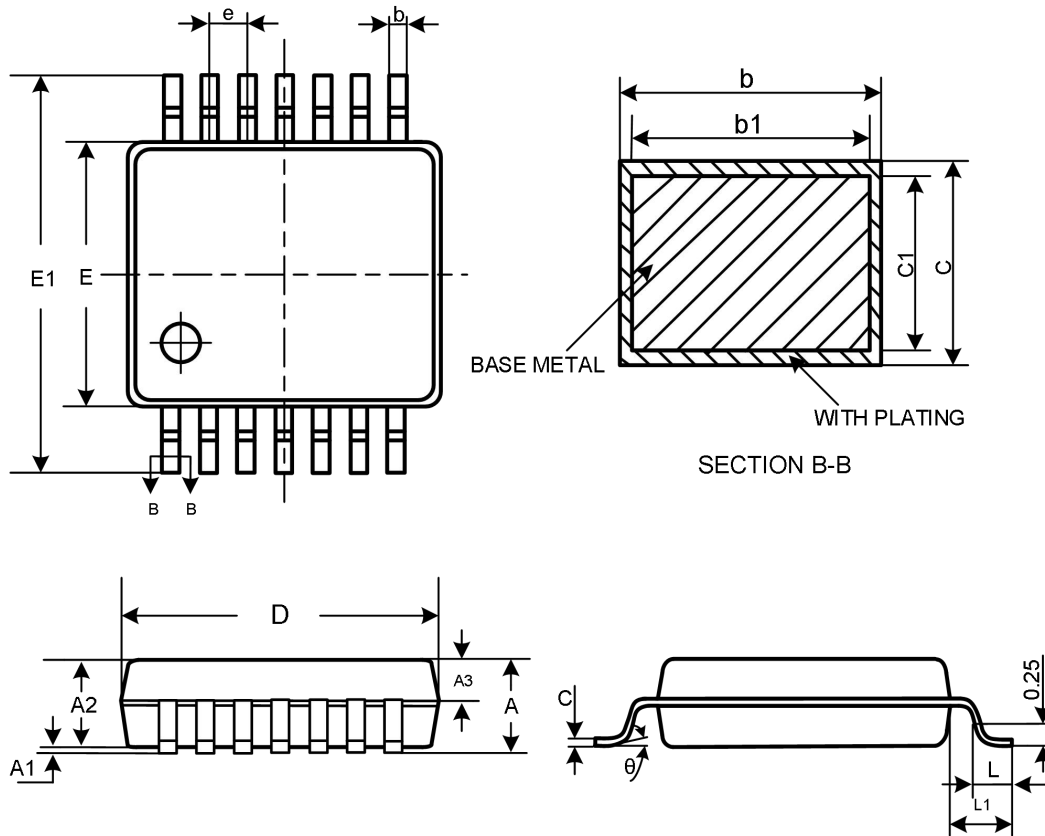
Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.75			0.069
A1	0.10	—	0.225	0.004		0.009
A2	1.30	1.40	1.50	0.051	0.055	0.059
A3	0.60	0.65	0.70	0.024	0.026	0.028
b	0.39	—	0.47	0.015		0.019
b1	0.38	0.41	0.44	0.015	0.016	0.017
c	0.20	—	0.21	0.008		0.008
c1	4.80	4.90	5.00	0.189	0.193	0.197
D	5.80	6.00	6.20	0.228	0.236	0.244
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27BSC			0.05BSC		
h	0.25	—	0.50	0.010		0.020
L	0.50	—	0.80	0.020		0.031
L1	1.05REF			0.041REF		
θ	0	—	8°	0	—	8°

11 Package Outline Dimension(continued)
MSOP8


Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.10	—	—	0.043
A1	0.05	—	0.15	0.002	—	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
A3	0.30	0.35	0.40	0.012	0.014	0.016
b	0.28	—	0.36	0.011	—	0.014
b1	0.27	0.30	0.33	0.011	0.012	0.013
c	0.15	—	0.19	0.006	—	0.007
c1	0.14	0.15	0.16	0.006	0.006	0.006
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.70	4.90	5.10	0.185	0.193	0.201
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65BSC			0.026BSC		
L	0.40	—	0.70	0.016	—	0.028
L1	0.95REF			0.037REF		
θ	0	—	8°	0	—	8°

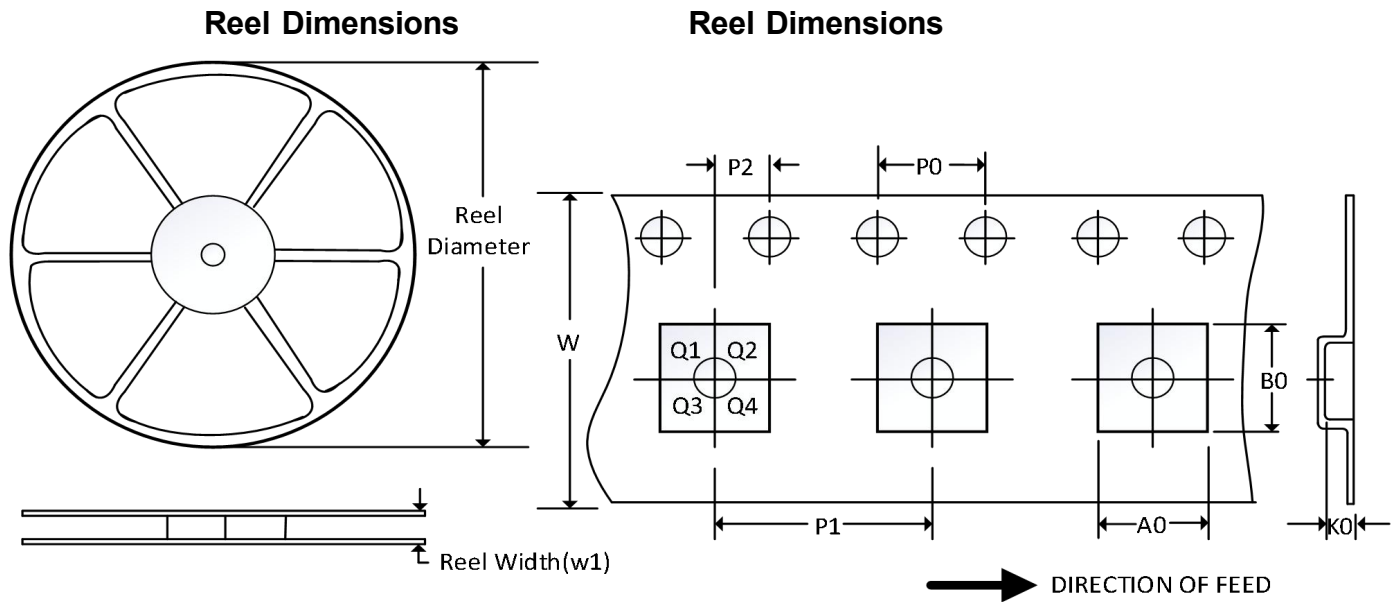
11 Package Outline Dimension(continued)
SOP14


Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.75	—	—	0.069
A1	0.10	—	0.225	0.004	—	0.009
A2	1.30	1.40	1.50	0.051	0.055	0.059
A3	0.60	0.65	0.70	0.024	0.026	0.028
b	0.39	—	0.47	0.015	—	0.019
b1	0.38	0.41	0.44	0.015	0.016	0.017
c	0.20	—	0.24	0.008	—	0.009
c1	0.19	0.20	0.21	0.007	0.008	0.008
D	8.55	8.65	8.75	0.337	0.341	0.344
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27BSC			0.05BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.50	—	0.80	0.020	—	0.031
L1	1.05REF			0.041REF		
θ	0	—	8°	0	—	8°

11 Package Outline Dimension(continued)
TSSOP14


Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.90	1.00	1.05	0.035	0.039	0.041
A3	0.39	0.44	0.49	0.015	0.017	0.019
b	0.20	—	0.28	0.008	—	0.011
b1	0.19	0.22	0.25	0.007	0.009	0.010
c	0.13	—	0.17	0.005	—	0.007
c1	0.12	0.13	0.14	0.005	0.005	0.006
D	4.90	5.00	5.10	0.193	0.197	0.201
E1	4.30	4.40	4.50	0.169	0.173	0.177
E	6.20	6.40	6.60	0.244	0.252	0.260
e	0.65BSC			0.026BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00BSC			0.039BSC		
θ	0	—	8°	0	—	8°

12 Tape and Reel Information



NOTE: The picture is only for reference. Please make the object as the standard.

Key Parameter List of Tape and Reel

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SC70-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
MSOP-8	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
TSSOP-14	13"	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1
SOIC-8 (SOP8)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
SOIC-14 (SOP14)	13"	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.