GT74LVC2G08
Dual 2-Input Positive-AND Gate

1 Features

- **Supports 5V V_{CC} operation**
- **Inputs accept voltages to 5.5 V**
- **Provides down translation to V_{CC}**
- **Low power consumption, 10-μA Max I_{CC}**
- **±24-mA output drive at 3.3 V**
- **I_{off} supports live insertion, partial-power-down mode, and back drive protection**

2 Application

- **IP phones: wired and wireless**
- **Point-to-point microwave backhaul**
- **Optical networking: EPON and video over fiber**
- **Power:telecom DC/DC module: analog and digital**
- **Private branch exchanges (PBX)**
- **Telecom shelters: power distribution units (PDU)**
- **Vector signal analyzers and generators**
- **Wireless communications testers and**
- **Wireless repeaters**

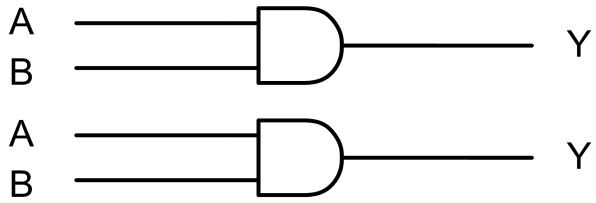
3 Description

This dual 2-input positive-AND gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The GT74LVC2G08 performs the Boolean function $Y=A\cdot B$ or $Y=\overline{\overline{A}+\overline{B}}$ in positive logic. The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Circuit Diagram



4 Revision History

Revision	Date	Note
Rev. A1.0	2023. 10. 23	Original Version
Rev.A1.1	2023. 10. 23	1.Updated Package Qty 2.Added Tape and Reel Information 3. Added Application Note
Rev.A1.2	2023. 12. 26	1. Added Marking 2. Added MSL
Rev.A1.3	2024. 01. 26	Updated Part Name

The latest datasheet version should be checked on the GTIC official website, as the company does not actively inform customers about updates to the datasheet.

5 Device Summary, Pin and Packages

Table 5-1. Device Summary(1)

Serial Name	Part Name	Package	Body Size (Nom)	Marking(2)(4)	MSL(3)	Package Qty
GT74LVC2G08	GT74LVC2G08P8	SOP8	6.00mm×3.90mm×1.75mm	2G08 XXXXXXX	3	Tape and Reel,4000
GT74LVC2G08	GT74LVC2G08V8	VSSOP8	2.00mm×2.30mm×0.75mm	2G08 XXXX	3	Tape and Reel,3000

(1) For all available packages, please contact product sales

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

(4) "XXXXX" in Marking will be appeared as the batch code.

FAE: 13148878879

5 Device Summary, Pin and Packages(continued)

Top View

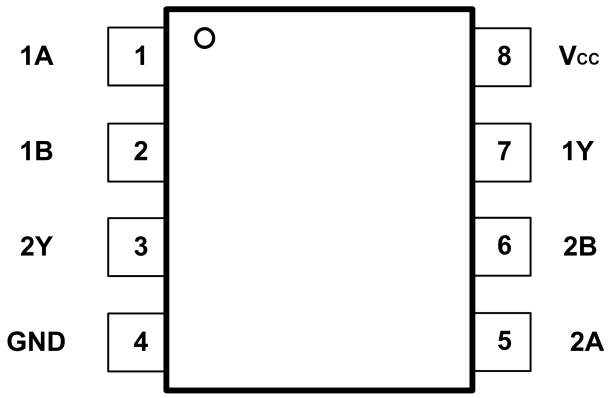


Fig.5-1. GT74LVC2G08: P8 (SOP8/SOIC-8) Package

GT74LVC2G08: V8 (VSSOP8) Package

Table 5-1 Pin Definition

Pin		Type	Description
Name	P8 V8		
1A	1	I	A input for gate 1
1B	2	I	B input for gate 1
2Y	3	O	Output for gate 2
GND	4	-	Ground
2A	5	I	A input for gate 2
2B	6	I	B input for gate 2
1Y	7	O	Output for gate 1
V_{CC}	8	-	Power input

6 Voltage, Temperature, ESD and Thermal Ratings

6.1 Absolute Maximum Ratings(1)

Parameters			Min	Max	Unit
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range		-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2)		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature under bias			150	°C
T_{stg}	Storage temperature range		-55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability..

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

ESD			Value	Unit
V(ESD)	Electrostatic Discharge	Human-Body Model (HBM)(1)	8 K	V
		Charged-Device Model (CDM)(2)	2 K	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6 Voltage, Temperature, ESD and Thermal Ratings(continued)

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		1.65	5.5	V
V_{IH}	High-Level Input Voltage	VCC=1.65V to1.95V	0.65×VCC		V
		VCC=2.3V to 2.7V	1.7		
		VCC=3V to 3.6V	2		
		VCC=4.5V to 5.5V	0.7×VCC		
V_{IL}	Low-Level Input Voltage	VCC=1.65V to1.95V		0.35×VCC	V
		VCC=2.3V to 2.7V		0.7	
		VCC=3V to 3.6V		0.8	
		VCC=4.5V to 5.5V		0.3×VCC	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	VCC	V
I_{OH}	High-Level Output Current	VCC=1.65V		-4	mA
		VCC=2.3V		-8	
		VCC=3V		-16	
				-24	
		VCC=4.5V		-32	
I_{OL}	Low-Level Output Current	VCC=1.65V		4	mA
		VCC=2.3V		8	
		VCC=3V		16	
				24	
		VCC=4.5V		32	
Δt/Δv	Input Transition Rise or Fall Rate	VCC=1.8V±0.15V,2.5V±0.2V		20	ns/V
		VCC=3.3V±0.3V		10	
		VCC=5V±0.5V		5	
TA	Operating Free-Air Temperature		-40	125	°C

6.4 Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
VSSOP-8	227	84	°C/W
SOP-8(SOIC-8)	158	43	°C/W

7 Electrical Specifications(1)

Over recommended operating free-air temperature range (unless otherwise noted)

Parameter	Test Conditions	V_{CC}	–40°C to 85°C			–40°C to 125°C			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	I_{OH} = – 100 µA	1.65 V to 5.5 V	V_{CC}-0.1			V_{CC}-0.1			V
	I_{OH} = –4 mA	1.65 V	1.2			1.2			
	I_{OH} = –8 mA	2.3 V	1.9			1.9			
	I_{OH} = – 16 mA	3 V	2.4			2.4			
	I_{OH} = –24 mA		2.3			2.3			
	I_{OH} = –32 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 100 µA	1.65 V to 5.5 V			0.1			0.1	V
	I_{OL} = 4 mA	1.65 V			0.45			0.45	
	I_{OL} = 8 mA	2.3 V			0.3			0.3	
	I_{OL} = 16 mA	3 V			0.4			0.4	
	I_{OL} = 24 mA				0.55			0.55	
	I_{OL} = 32 mA	4.5 V			0.55			0.55	
I_I A or B Inputs	V_I = 5.5 V or GND	0 to 5.5 V			±5			±5	µA
I_{off}	V_I or V_O = 5.5 V	0			± 10			± 10	µA
I_{CC}	V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10			10	µA
ΔI_{CC}	One Input at V_{CC} – 0.6 V, Other Inputs at V_{CC} or GND	3 V to 5.5 V			10			10	µA
C_i	V_I = V_{CC} or GND	3.3 V		5			5		pF

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation

7 Electrical Specifications (continued)

Switching Characteristics, CL = 15 pF

Over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
tpd	A or B	Y	1.5	7.2	0.7	4.4	0.8	3.6	0.8	3.4	ns

Over recommended operating free-air temperature range, CL = 30 pF or 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
tpd	A or B	Y	2.4	8	1.1	5.5	1	4.5	1	4	ns

Over recommended operating free-air temperature range, CL = 30 pF or 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 125°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
tpd	A or B	Y	2.4	10	1.1	7	1	6	1	5	ns

Operating Characteristics

T_A=25°C

	PARAMETER	TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			Typ	Typ	Typ	Typ	
Cpd	Power Dissipation Capacitance	f = 10 MHz	18	21	22	25	pF

8 Typical Characteristics

Over recommended operating free-air temperature range, CL=30 pF or 50 pF (unless otherwise noted)

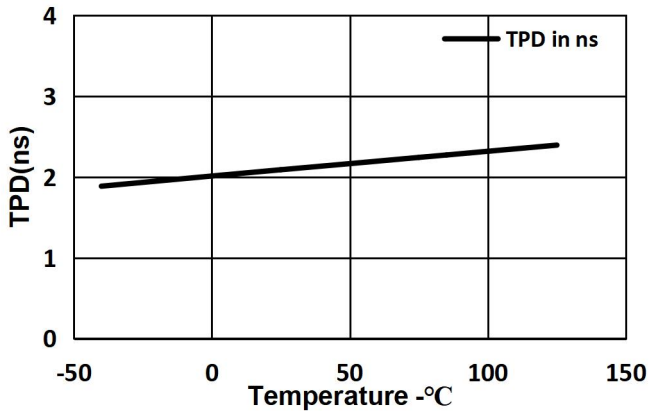


Fig.8-1. T_{PD} Across Temperature at 3.3 V V_{CC}

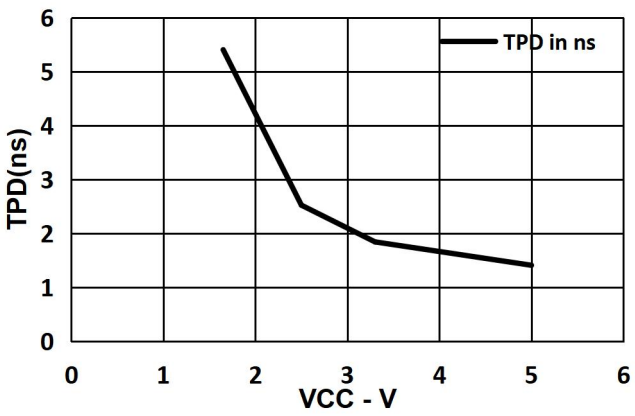
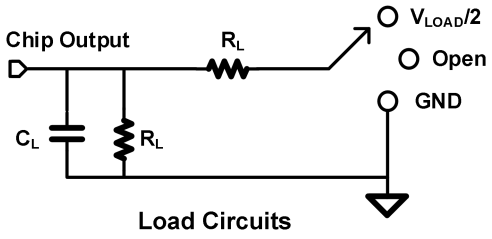


Fig.8-2. T_{PD} Across V_{CC} at 25℃

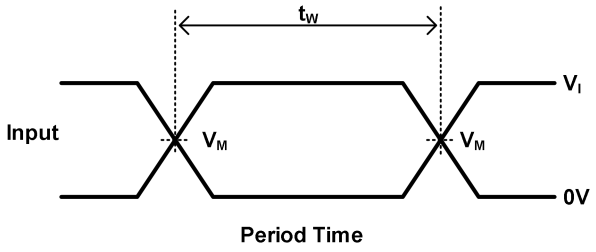
9 Parameter Measurement Information



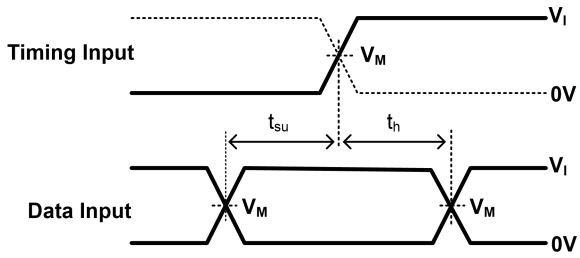
Load Circuits

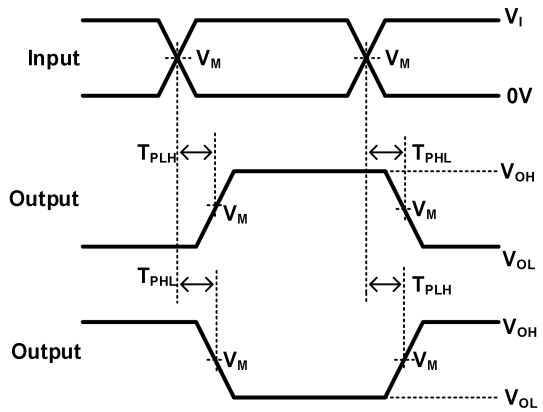
TEST	S1
T_{PHL}/T_{PLH}	OPEN
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	T_r/T_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	15pF	1MΩ	0.15V
2.5V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	15pF	1MΩ	0.15V
3.3V±0.15V	3V	≤2.5ns	1.5V	6V	15pF	1MΩ	0.3V
5V±0.15V	V_{CC}	≤2.5ns	$V_{CC}/2$	$2\times V_{CC}$	15pF	1MΩ	0.3V

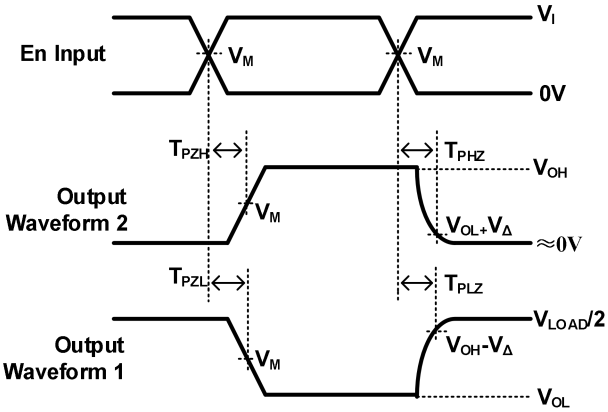


Period Time





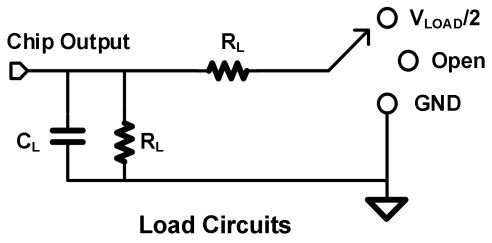
Propagation Delay
for Output and Inverted Output



Enable and Disable Times
Low-And High-Level Enabling

Notes: A. C includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z = 50.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all device.

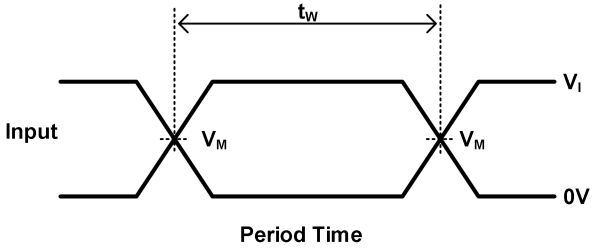
9 Parameter Measurement Information (Continued)



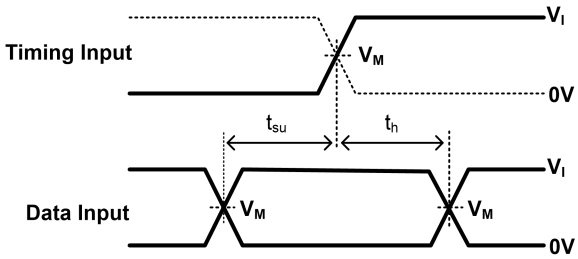
Load Circuits

TEST	S1
T_{PHL}/T_{PLH}	OPEN
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

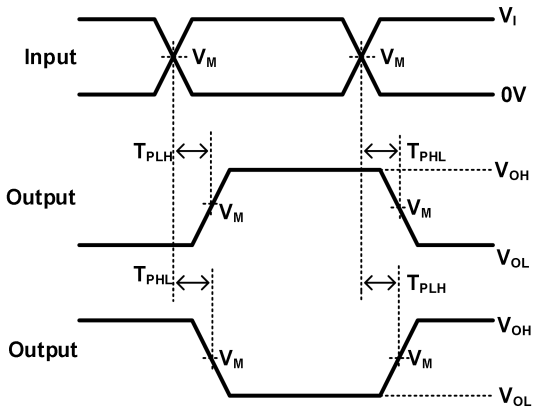
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	T_r/T_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	1kΩ	0.15V
2.5V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	500Ω	0.15V
3.3V±0.15V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.15V	V_{CC}	≤2.5ns	$V_{CC}/2$	$2\times V_{CC}$	50pF	500Ω	0.3V



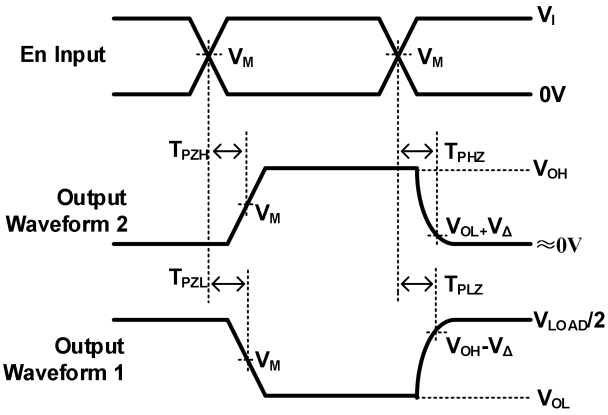
Period Time



Setup and Hold Times



Propagation Delay
for Output and Inverted Output



Enable and Disable Times
Low-And High-Level Enabling

Notes: A. C includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z=50.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all device.

10 Detailed Description

10.1 Overview

The GT74LVC2G08 device contains two 2 -input positive AND gate devices and perform the Boolean function $Y=A\cdot B$ or $Y=\overline{\overline{A}+\overline{B}}$. This device is fully specified for partial-power-down applications using I_{off}.The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

10.2 Functional Block Diagram

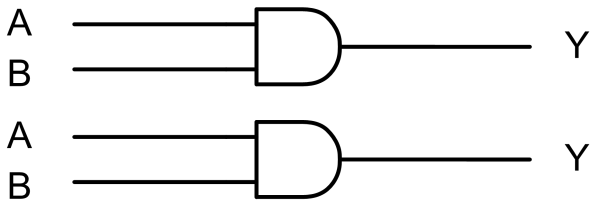


Fig.10-1.Functional Block Diagram

10.3 Feature Description

- Wide operating voltage range.
- Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

10.4 Device Functional Modes

Input A		Output Y
A	**B**	**Y**
H	H	H
L	X	L
X	L	L

11 Application Note

11.1 Application Information

The GT74LVC2G08 is a high drive CMOS device that can be used for implementing AND logic with high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5V tolerant allowing it to translate down to V_{CC}.

11.2 Typical Application

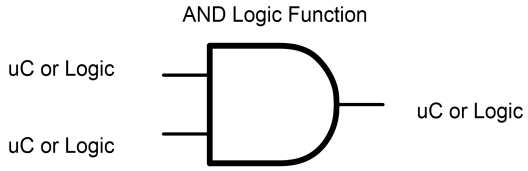


Fig.11-1.Typical Application

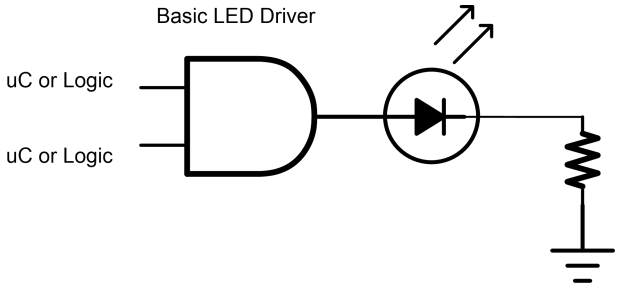
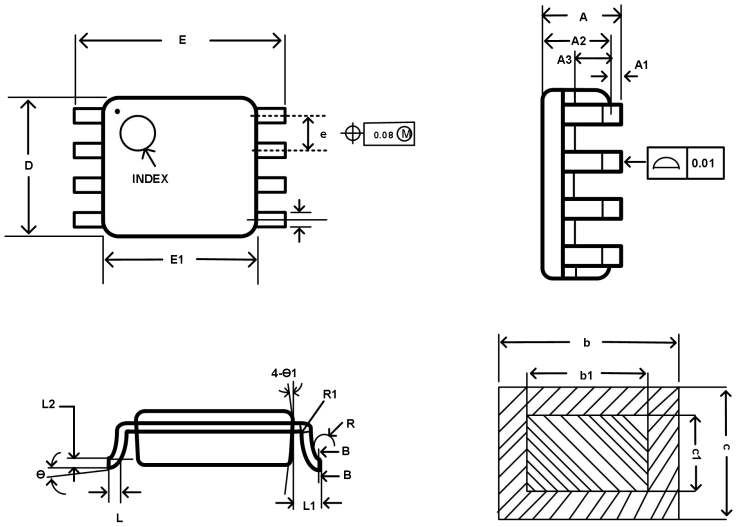


Fig.11-2.Typical Application

12 Package Outline Dimension

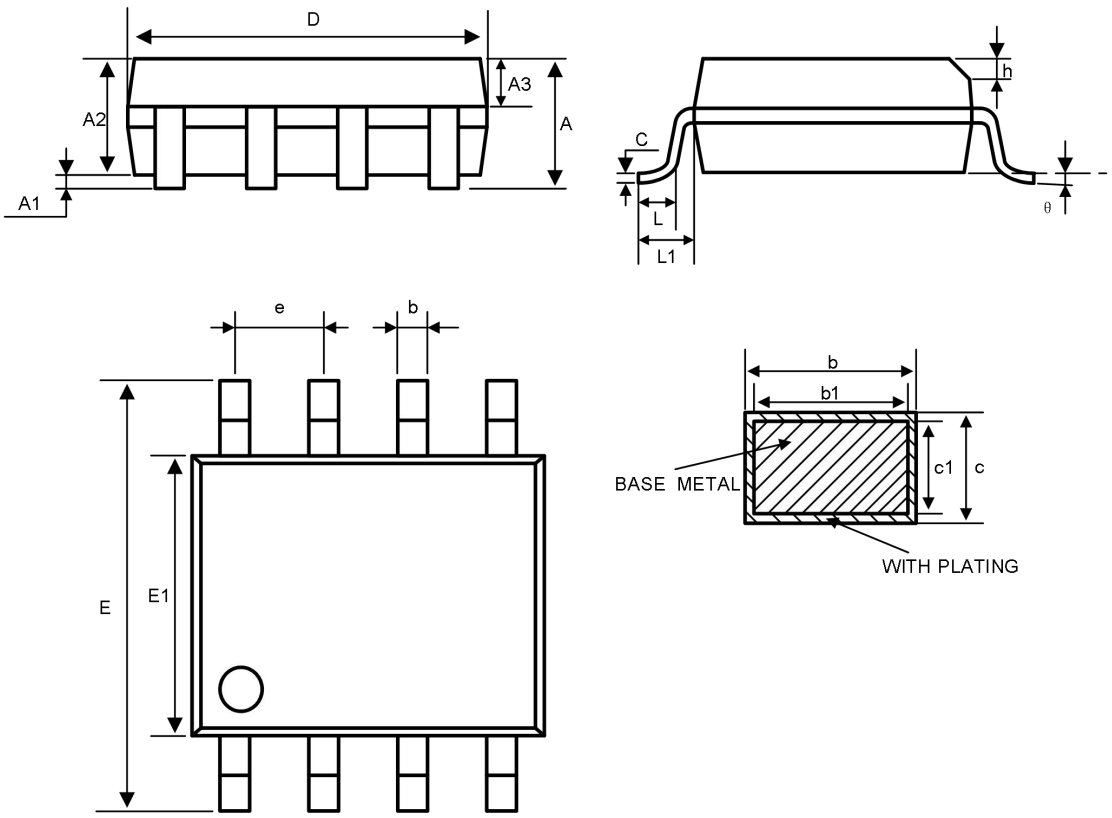
VSSOP8



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.90	-	-	0.035
A1	0	0.05	0.10	0.000	0.002	0.004
A2	0.65	0.75	0.80	0.026	0.030	0.031
A3	0.32	0.37	0.42	0.013	0.015	0.017
b	0.17	-	0.27	0.007	-	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.10	-	0.18	0.004	-	0.007
c1	0.10	0.13	0.14	0.004	0.005	0.006
E	3.00	3.10	3.20	0.118	0.122	0.126
D	1.90	2.00	2.10	0.075	0.079	0.083
E	3.00	3.10	3.20	0.118	0.122	0.126
E1	2.20	2.30	2.40	0.087	0.091	0.094
e	0.40	0.50	0.60	0.016	0.020	0.024
L	0.20	0.26	0.35	0.008	0.010	0.014
L1	0.40REF			0.016REF		
L2	0.12BSC			0.005BSC		
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
θ	0°	-	6°	0°	-	6°
θ1	9°	12°	15°	9°	12°	15°

12 Package Outline Dimension(continued)

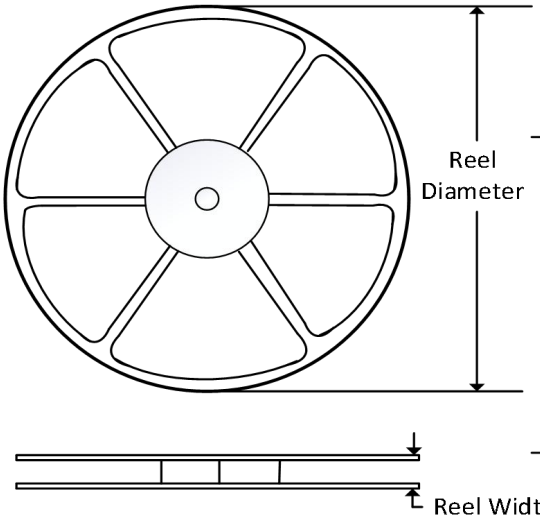
SOP8



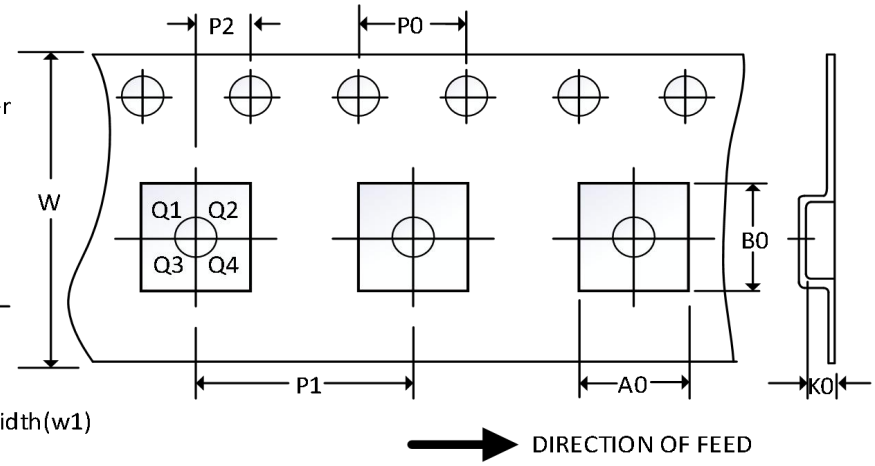
Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.75			0.069
A1	0.10	—	0.225	0.004		0.009
A2	1.30	1.40	1.50	0.051	0.055	0.059
A3	0.60	0.65	0.70	0.024	0.026	0.028
b	0.39	—	0.47	0.015		0.019
b1	0.38	0.41	0.44	0.015	0.016	0.017
c	0.20	—	0.21	0.008		0.008
c1	4.80	4.90	5.00	0.189	0.193	0.197
D	5.80	6.00	6.20	0.228	0.236	0.244
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27BSC			0.05BSC		
h	0.25	—	0.50	0.010		0.020
L	0.50	—	0.80	0.020		0.031
L1	1.05REF			0.041REF		
θ	0°	—	8°	0°	—	8°

13 Tape and Reel Information

Reel Dimensions



Reel Dimensions



NOTE: The picture is only for reference. Please make the object as the standard.

Key Parameter List of Tape and Reel

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOP8	13''	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
VSSOP-8	7''	9.5	2.25	3.35	1.40	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.