

ESDUL5V0BDB

Description

ESDUL5V0BDB is an ultra-low capacitance TVS designed to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-stress caused by ESD.

ESDUL5V0BDB may be used to provide ESD protection up to $\pm 15\text{kV}$ (contact discharge) according to IEC61000-4-2, and withstand peak pulse current up to 4A (8/20 μs) according to IEC61000-4-5.

ESDUL5V0BDB is available in DFN1006-2L package. Standard products are Pb-free and Halogen-free.

Features

- ◆ Stand-off voltage: 5V Max.
- ◆ Transient protection for each line according to IEC61000-4-2(ESD): $\pm 15\text{kV}$ (contact)
IEC61000-4-5(surge): 4A (8/20 μs)
- ◆ Ultra-low capacitance: $C_J = 0.35\text{pF}$ typ.
- ◆ Ultra-low leakage current: $I_R < 1\text{nA}$ typ.
- ◆ Low clamping voltage: $V_{CL} = 14.0\text{V}$ typ. @ $I_{PP} = 16\text{A}$ (TLP)
- ◆ Solid-state silicon technology

Applications

- ◆ USB 2.0 and USB 3.0
- ◆ HDMI 1.3, HDMI 1.4 and HDMI 2.0
- ◆ SATA and eSATA interface
- ◆ DVI
- ◆ IEEE 1394
- ◆ Portable Electronics and Notebooks

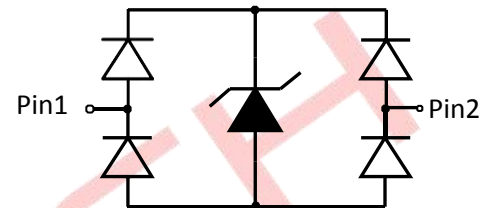
Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Peak pulse power ($t_p = 8/20\mu\text{s}$)	P_{PK}	44	W
Peak pulse current ($t_p = 8/20\mu\text{s}$)	I_{PP}	4	A
IEC61000-4-2 (Contact)	V_{ESD}	± 15	kV
IEC61000-4-2 (Air)	V_{ESD}	± 15	kV
Lead Temperature	T_L	260	$^{\circ}\text{C}$
Operating temperature	T_{OP}	-40 to 85	$^{\circ}\text{C}$
Junction Temperature	T_J	125	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55 to 150	$^{\circ}\text{C}$

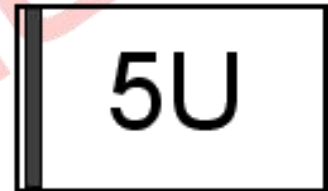
DFN1006-2L



Pin configuration



Marking



Order information

Device	Package	Shipping
ESDUL5V0BDB	DFN1006-2L	10000/Tape&Reel

ESDUL5V0BDB

Electrical Characteristics (T =25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-off voltage	V_{RWM}				5	V
Reverse Breakdown voltage	V_{BR}	$I_t = 1\text{ mA}$	6.0	8.0		V
Reverse Leakage Current	I_R	$V_{RWM} = 5\text{ V}$			50	nA
Clamping voltage ¹⁾	V_{CL}	$I_{PP} = 16\text{ A}$, $t_p = 100\text{ ns}$		14		V
Dynamic resistance ¹⁾	R_{DYN}			0.55		Ω
Clamping voltage ²⁾	V_{CL}	$V_{ESD} = 8\text{ kV}$		14.0		V
Clamping voltage ³⁾	V_{CL}	$I_{PP} = 1\text{ A}$, $t_p = 8/20\text{ us}$		8.3		V
		$I_{PP} = 4\text{ A}$, $t_p = 8/20\text{ us}$		10		V
Junction Capacitance	C_J	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$		0.35	0.5	pF

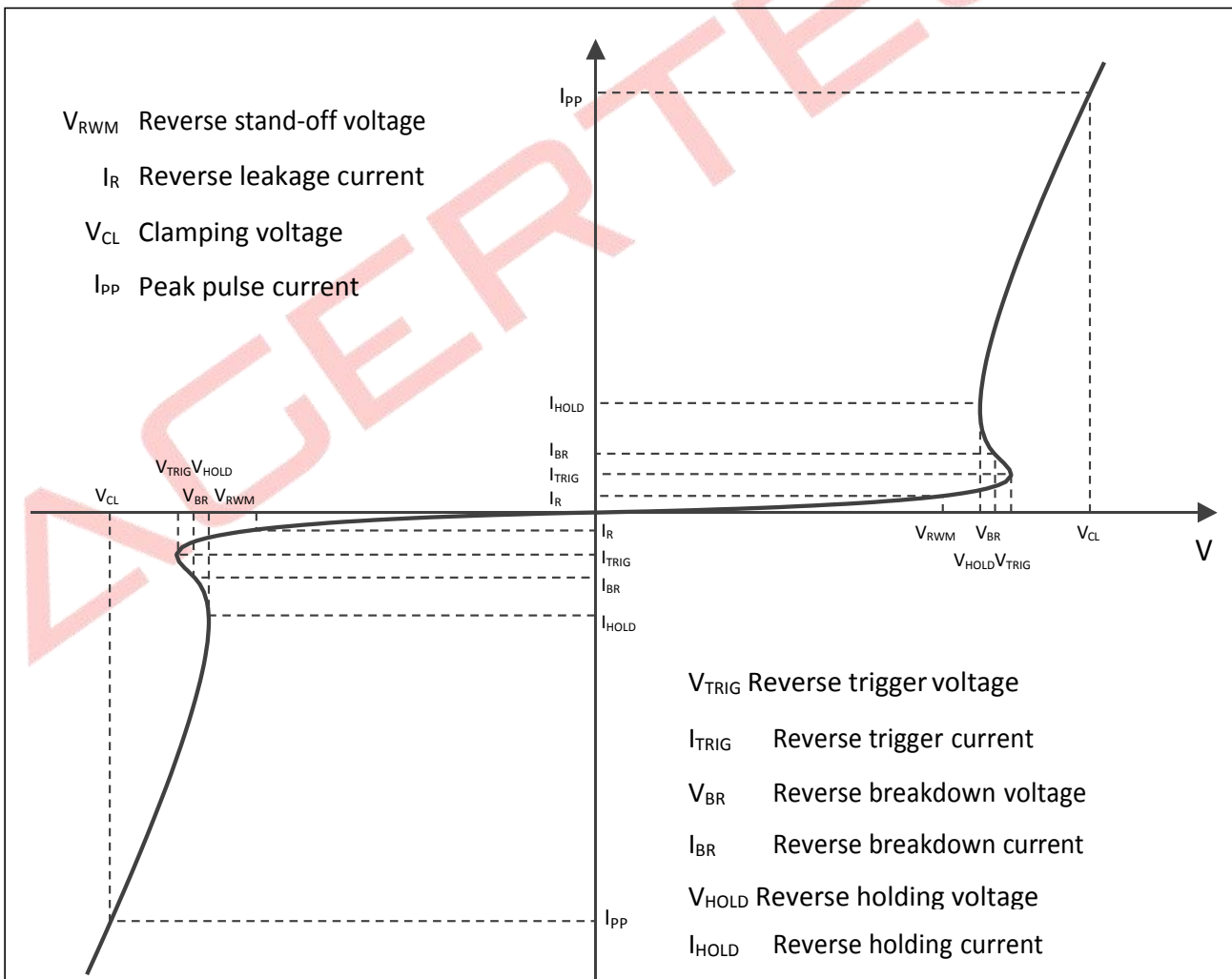
Notes:

1) TLP parameter: $Z_0 = 50\Omega$, $t_p = 100\text{ ns}$, $t_r = 2\text{ ns}$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.

2) Contact discharge mode, according to IEC61000-4-2.

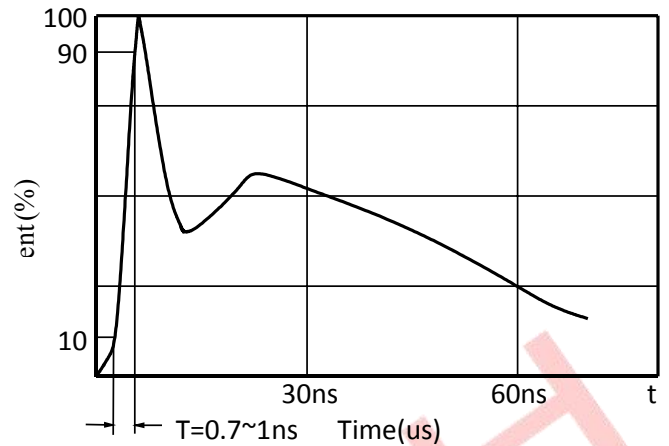
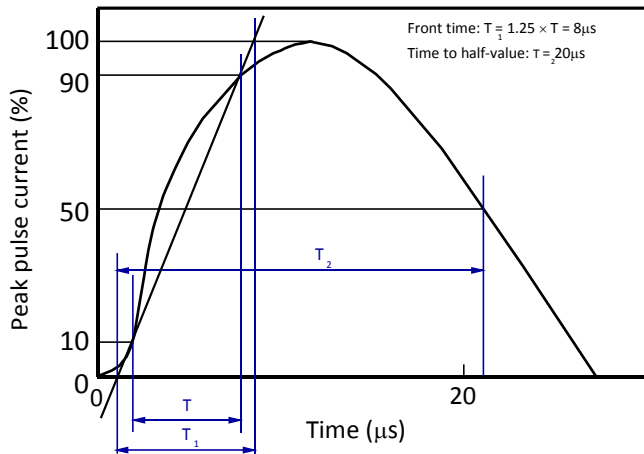
3) Non-repetitive current pulse, according to IEC61000-4-5.

Electrical Characteristics



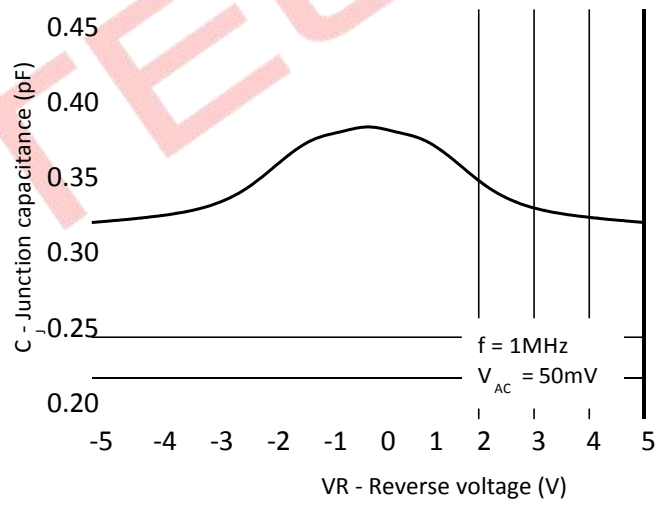
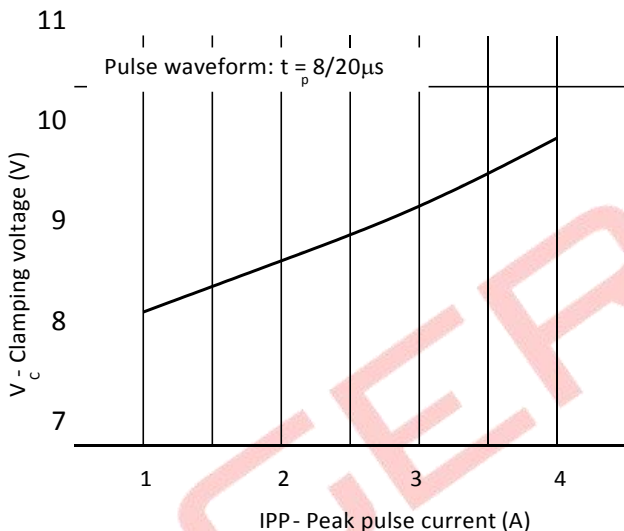
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Typical characteristics(TA=25°C,unless otherwise noted)



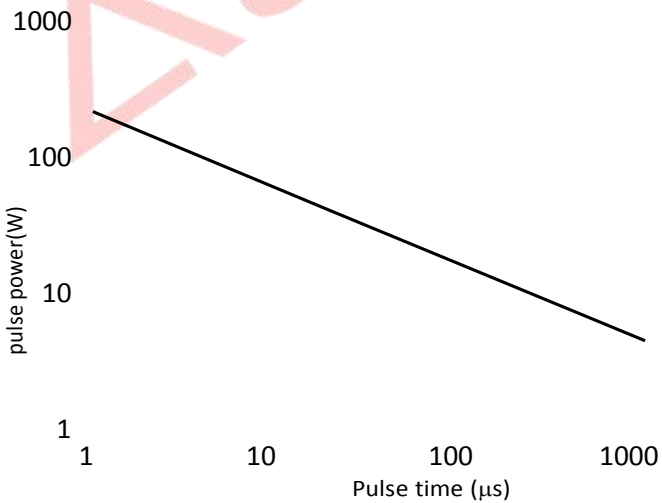
8/20μs waveform per IEC61000-4-5
 Capacitance vs. Reverse voltage

Contact discharge current waveform per IEC61000-4-2

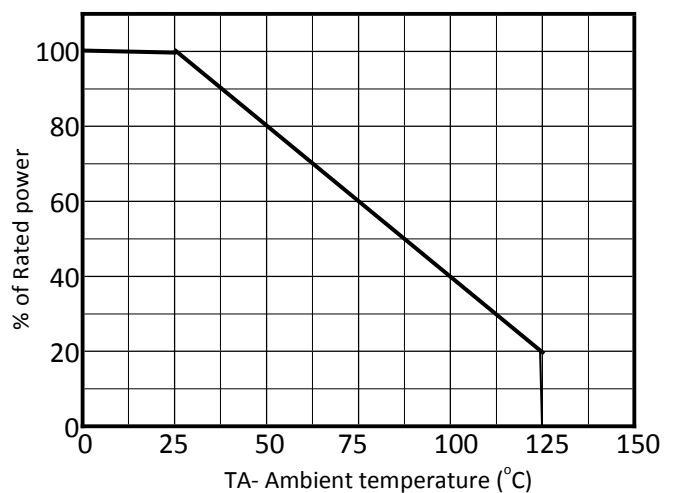


Clamping voltage vs. Peak pulse current

Capacitance vs. Reverse voltage

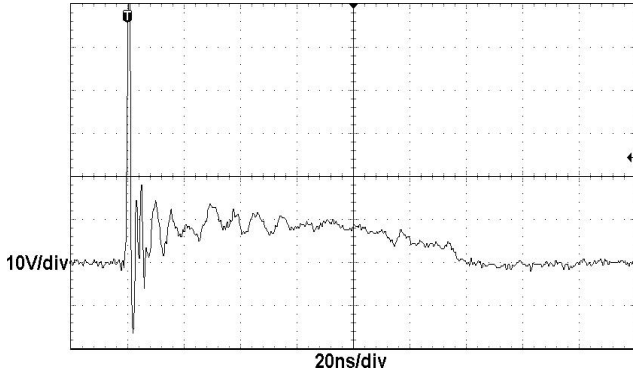


Non-repetitive peak pulse power vs. Pulse time

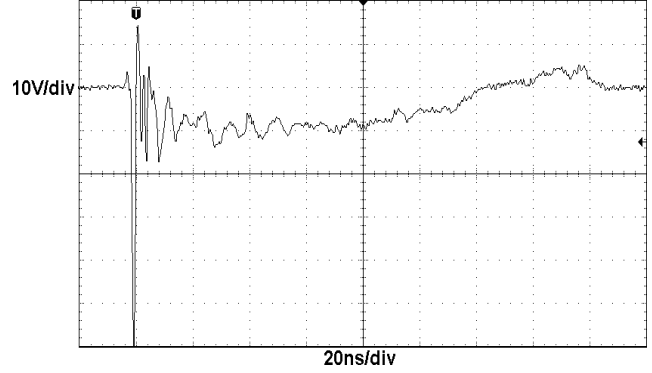


Power derating vs. Ambient temperature

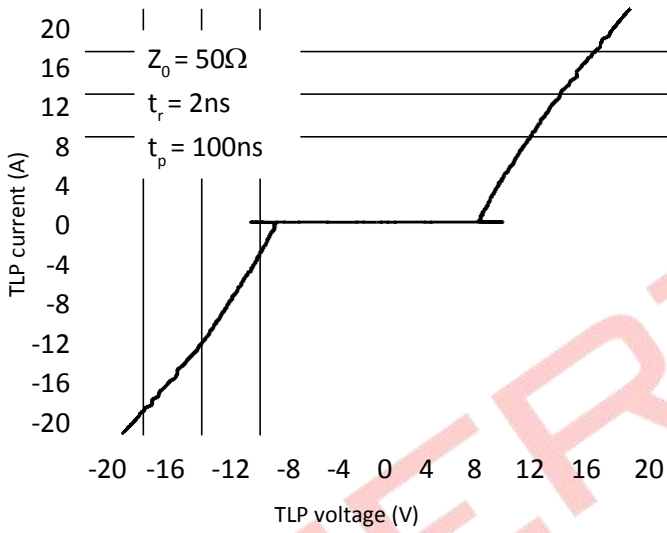
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ESD clamping
(+8kV contact discharge per IEC61000-4-2)



ESD clamping
(-8kV contact discharge per IEC61000-4-2)

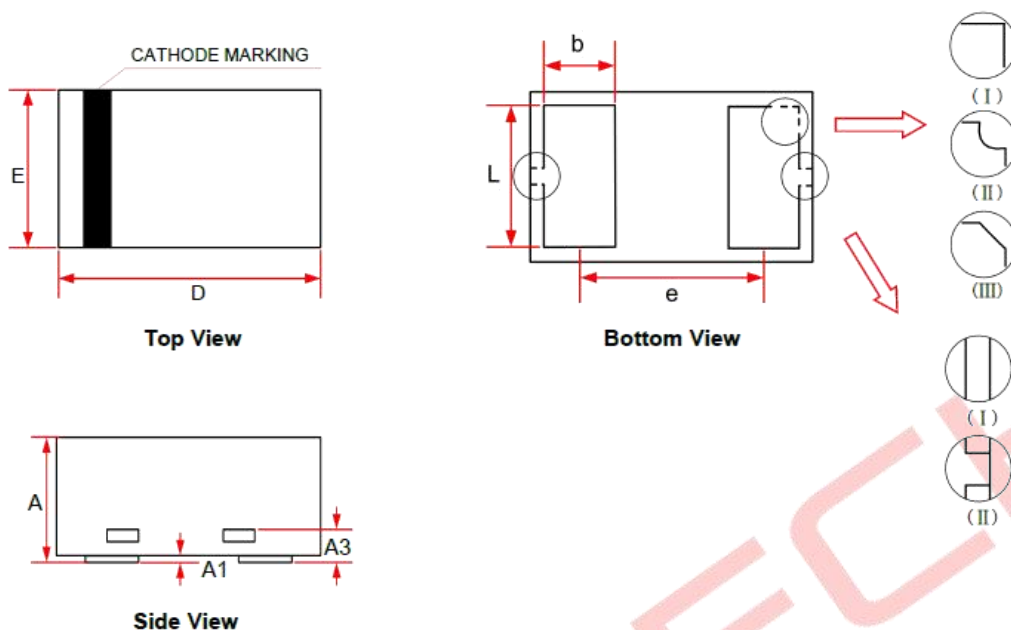


TLP Measurement

ESDUL5V0BDB

Package Outline

DFN1006-2L



Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.340	0.450	0.530
A1	0.000	0.020	0.050
A3	0.125 Ref.		
D	0.950	1.000	1.075
E	0.550	0.600	0.675
b	0.200	0.250	0.300
L	0.450	0.500	0.550
e	0.650 BSC		

Recommended PCB Layout

