

Description

The ST2303SRG uses advanced trench technology to provide excellent R_{DS(ON)}, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

 $V_{DS} = -30V, I_D = -4.1A$ $R_{DS(ON)} < 56m\Omega @ V_{GS} = 10V$

Application

High power and current handing capability Lead free product is acquired Surface mount package PWM applications Load switch Power management

Package Marking and Ordering Information

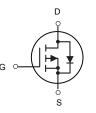
Product ID	Pack	Brand	Qty(PCS)
ST2303SRG	SOT-23	HXY MOSFET	3000

Absolute Maximum Ratings (T_A=25[°]C unless otherwise noted)

Symbol	Parameter	Limit	Unit	
Vds	Drain-Source Voltage	-30	V	
Vgs	Gate-Source Voltage	±20	V	
l _D	Drain Current-Continuous	-4.1	A	
DM	Drain Current-Pulsed (Note 1)	-13	A	
PD	Maximum Power Dissipation	1.32	W	
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	°C	
Reja	Thermal Resistance, Junction-to-Ambient (Note 2)	125	°C /W	







P-Channel MOSFET



Electrical Characteristics (T _J =25 °C, u	unless otherwise noted)
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Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =-250uA	-30			V	
∆BV _{DSS} /∆T _J	BVDSS Temperature Coefficient	Reference to 25° C , I _D =-1mA		-0.02		V/°C	
Rds(on)	Static Drain-Source On-Resistance ²	V _{GS} =-10V , I _D =-3A		48	56	mΩ	
	Static Drain-Source On-Resistance-	V _{GS} =-4.5V , I _D =-1.5A		78	90		
V _{GS(th)}	Gate Threshold Voltage		-1.2	-1.5	-2.5	V	
$ riangle V_{GS(th)}$	V _{GS(th)} Temperature Coefficient	VGS=VDS , ID =-2300A		4.32		mV/°C	
	Drain-Source Leakage Current	V _{DS} =-24V , V _{GS} =0V , T _J =25°C			-1		
I _{DSS}		V _{DS} =-24V , V _{GS} =0V , T _J =55°C			-5	uA	
Igss	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$			±100	nA	
gfs	Forward Transconductance	V _{DS} =-5V , I _D =-3A		4.8		S	
Rg	Gate Resistance	V _{DS} =0V , V _{GS} =0V , f=1MHz		24	48	Ω	
Qg	Total Gate Charge (-4.5V)			5.22	7.3		
Qgs	Gate-Source Charge	V _{DS} =-20V , V _{GS} =-4.5V , I _D =-3A		1.25	1.8	nC	
Q _{gd}	Gate-Drain Charge			2.3	3.2		
T _{d(on)}	Turn-On Delay Time			18.4	37		
Tr	Rise Time	V_{DD} =-15V , V_{GS} =-10V , R_{G} =3.3 Ω		11.4	21		
T _{d(off)}	Turn-Off Delay Time	I _D =-1A		39.4	79	ns	
T _f	Fall Time			5.2	10.4		
Ciss	Input Capacitance			463	650		
Coss	Output Capacitance	V _{DS} =-15V , V _{GS} =0V , f=1MHz		82	115	pF	
Crss	Reverse Transfer Capacitance			68	95		
ls	Continuous Source Current ^{1,4}				-3.2	А	
lsм	Pulsed Source Current ^{2,4}	−−−V _G =V _D =0V , Force Current			-13	А	
Vsd	Diode Forward Voltage ²	V _{GS} =0V , I _S =-1A , T _J =25°C			-1	V	

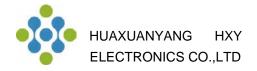
Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width $\,\leq\,$ 300us , duty cycle $\,\leq\,$ 2%

3. The power dissipation is limited by 150°C junction temperature

4. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.



Typical Characteristics

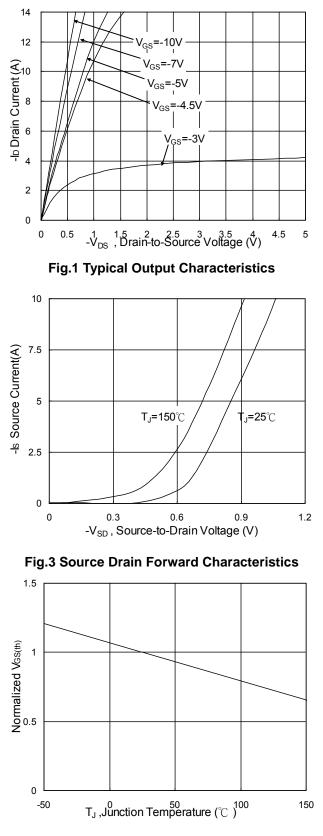


Fig.5 Normalized V_{GS(th)} vs. T_J

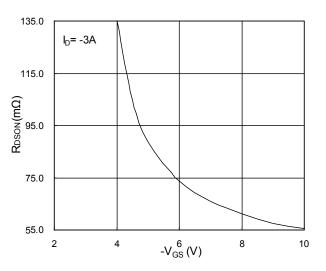


Fig.2 On-Resistance vs. G-S Voltage

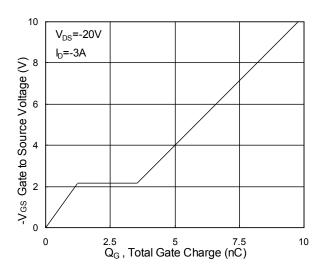


Fig.4 Gate-Charge Characteristics

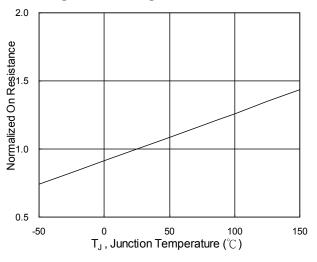
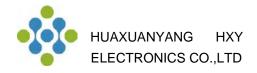


Fig.6 Normalized RDSON vs. TJ



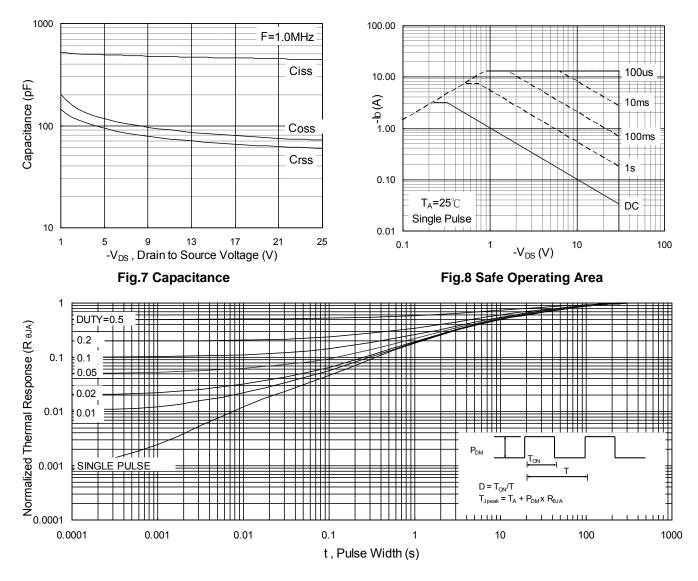


Fig.9 Normalized Maximum Transient Thermal Impedance

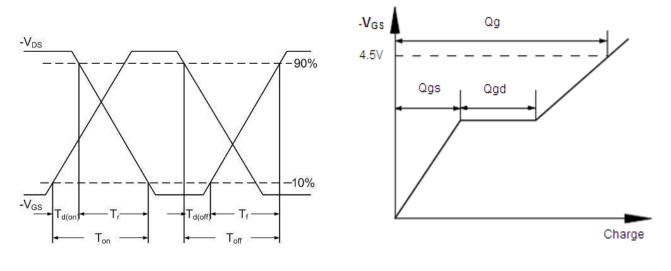
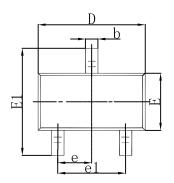


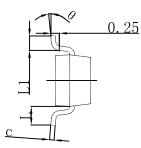
Fig.10 Switching Time Waveform

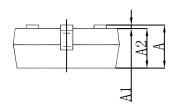
Fig.11 Gate Charge Waveform



SOT-23 Package Outline Dimensions

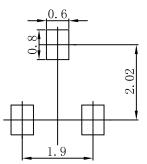






Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
Α	0.900	1.150	0.035	0.045	
A1	0.000	0.100	0.000	0.004	
A2	0.900	1.050	0.035	0.041	
b	0.300	0.500	0.012	0.020	
С	0.080	0.150	0.003	0.006	
D	2.800	3.000	0.110	0.118	
E	1.200	1.400	0.047	0.055	
E1	2.250	2.550	0.089	0.100	
е	0.950 TYP		0.037 TYP		
e1	1.800	2.000	0.071	0.079	
L	0.550 REF		0.022 REF		
L1	0.300	0.500	0.012	0.020	
θ	0°	8°	0°	8°	

SOT-23 Suggested Pad Layout



Note: 1.Controlling dimension:in millimeters.

2.General tolerance:± 0.05mm.
 3.The pad layout is for reference purposes only.



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