

## Description

The IRF7328PbF uses advanced trench technology and design to provide excellent R<sub>DS(ON)</sub> with low gat e charge. It can be used in a wide variety of applications.

#### **General Features**

 $V_{DS} = -30V, I_{D} = -11A$ 

 $R_{DS(ON)}$  < 18m @ V  $_{GS}$ =-10V

 $R_{DS(ON)}$  < 27m @ V GS=-4.5V

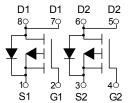
## **Application**

PWM application

Load switch



SOP-8



#### **Dual P-Channel MOSFET**

## **Package Marking and Ordering Information**

Product ID	Pack	Brand	Qty(PCS)
IRF7328PbF	SOP-8	HXY MOSFET	3000

## Absolute Maximum Ratings (T<sub>A</sub>=25<sup>°</sup>C unless otherwise noted)

Symbol	Parameter	Limit	Unit
V <sub>DS</sub>	Drain-Source Voltage	-30	V
V <sub>G</sub> s	Gate-Source Voltage	±20	V
l <sub>D</sub>	Drain Current-Continuous	-11	Α
Ірм	Drain Current-Pulsed (Note 1)	-40	Α
Po	Maximum Power Dissipation	3.7	W
T <sub>J</sub> ,T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 To 150	$^{\circ}$
Reja	Thermal Resistance,Junction-to-Ambient (Note 2)	33.8	°C/W



# Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> = -250μA	-30	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -30V, V <sub>GS</sub> =0V,	-	-	-1	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=-250\mu A$	-1.0	-1.6	-2.5	V
П	Static Drain-Source on-Resistance	V <sub>GS</sub> = -10V, I <sub>D</sub> = -10A	-	14	18	m0
$R_{DS(on)}$	Note3	$V_{GS}$ = -4.5V, $I_{D}$ = -5A	-	20	27	mΩ
C <sub>iss</sub>	Input Capacitance	\/ - 45\/ \/ -0\/	-	1330	-	pF
Coss	Output Capacitance	V <sub>GS</sub> =0V, I <sub>D</sub> = -250μA  V <sub>DS</sub> = -30V, V <sub>GS</sub> =0V,  V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V  V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = -250μA  V <sub>GS</sub> = -10V, I <sub>D</sub> = -10A  V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -5A  V <sub>DS</sub> = -15V, V <sub>GS</sub> =0V,  f=1.0MHz  V <sub>DS</sub> = -15V, I <sub>D</sub> = -5A,  V <sub>DS</sub> = -10V  Ce Diode Forward	-	183	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1-1.0IVII 12	-	156	-	pF
Qg	Total Gate Charge	\/ - 45\/ I - 5A	-	22	-	nC
Q <sub>gs</sub>	Gate-Source Charge	, - , , ,	-	1.0	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge	V GS = -10 V	-	1.8	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time		-	9	-	ns
t <sub>r</sub>	Turn-on Rise Time	V <sub>DD</sub> = -15V, I <sub>D</sub> = -10A,	-	13	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	$V_{GS}$ =-10V, $R_{GEN}$ =2.5 $\Omega$	-	48	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	20	-	ns
Is	Maximum Continuous Drain to Source Current	ırce Diode Forward		-	-11	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Dioc	de Forward Current		-	-40	Α
$V_{\text{SD}}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> = -15A	-	-0.8	-1.2	V
trr	Reverse Recovery Time	TJ=25℃,	-	64	-	ns
Qrr	Reverse Recovery Charge	$V_{DD}$ = -24V,I <sub>F</sub> =-2.8A, dI/dt=-100A/µs	-	25	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

- 2. EAS condition:  $T_J = 25\,^{\circ}\!\!\mathrm{C}$  ,  $V_{GS} = 10V$  ,  $R_G = 25\Omega$  , L=0.5mH,  $I_{AS} = -12.7A$
- 3. Pulse Test: Pulse Width≤300µs, Duty Cycle≤0.5%



# **Typical Performance Characteristics**

Figure1: Output Characteristics

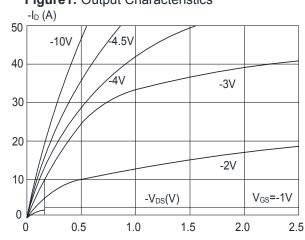


Figure 2: Typical Transfer Characteristics

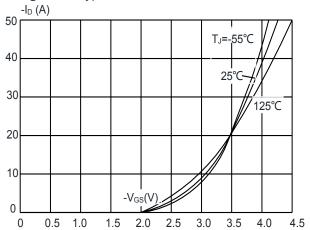


Figure 3:On-resistance vs. Drain Current

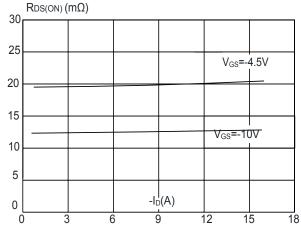


Figure 4: Body Diode Characteristics

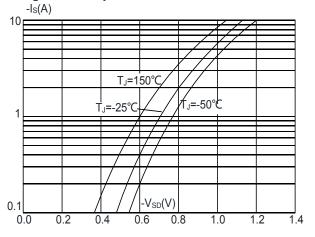


Figure 5: Gate Charge Characteristics

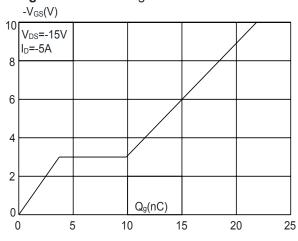
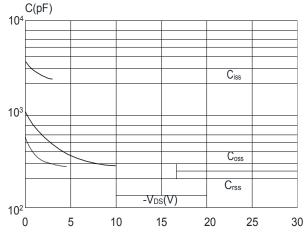


Figure 6: Capacitance Characteristics





**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature

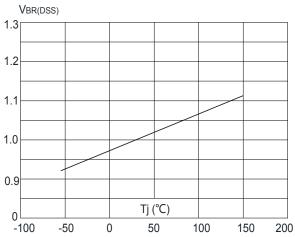
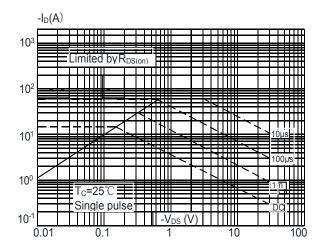
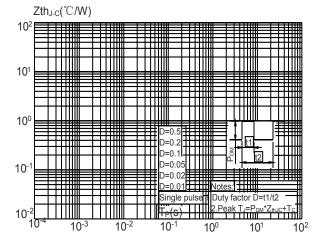


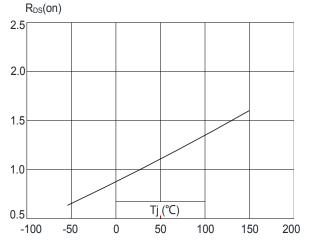
Figure 9: Maximum Safe Operating Area



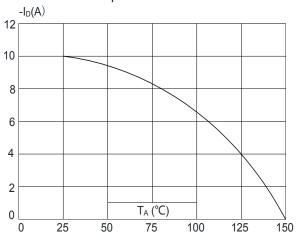
**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Figure 8:** Normalized on Resistance vs. Junction Temperature

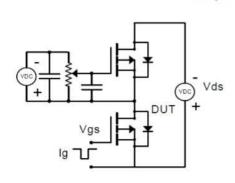


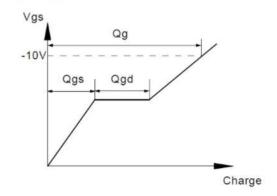
**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature



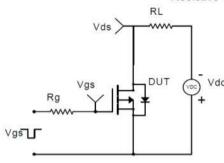
## **Test Circuit**

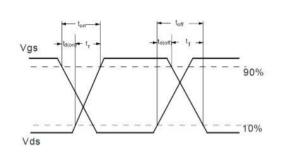
## Gate Charge Test Circuit & Waveform



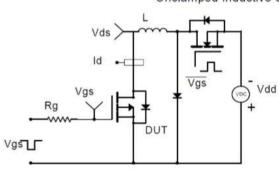


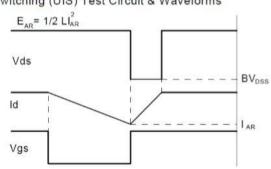
Resistive Switching Test Circuit & Waveforms



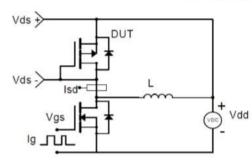


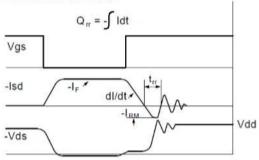
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



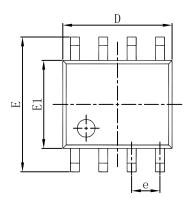


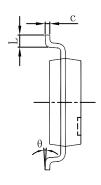
Diode Recovery Test Circuit & Waveforms

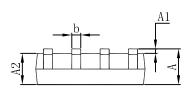




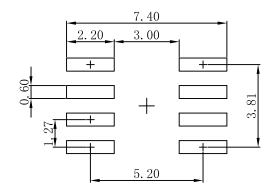
# **SOP-8 Package Outline Dimensions**







Symbol	Dimensions In Millimeters		Dimensions In Inches		
Symbol	Min	Max	Min	Max	
A	1.350	1.750	0.053	0.069	
A1	0.100	0. 250	0.004	0.010	
A2	1. 350	1.550	0.053	0.061	
b	0.330	0.510	0.013	0.020	
c	0.170	0. 250	0.007	0.010	
D	4.800	5.000	0. 189	0. 197	
e	1. 270 (	(BSC)	0.050 (BSC)		
E	5. 800	6. 200	0. 228	0. 244	
E1	3.800	4.000	0. 150	0. 157	
L	0.400	1. 270	0.016	0.050	
θ	0°	8°	0°	8°	



- Note: 1.Controlling dimension: in millimeters.
- 2.General tolerance:± 0.05mm.
  3.The pad layout is for reference purposes only.

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