UMW®

ADA4051

1.8 V, Micropower, Zero-Drift, Rail-to-Rail Input/Output Op Amps

GENERAL DESCRIPTION

The ADA4051-1 are CMOS, micropower, zero-drift operational amplifiers utilizing an innovative chopping technique. These amplifiers feature rail-to-rail input/output swing and extremely low offset voltage while operating from a 1.8 V to 5.5 V power supply. In addition, these amplifiers offer high power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) while operating with a typical supply current of 13 μA per amplifier. This combination of features makes the ADA4051-1 / ADA4051-2 amplifiers ideal choices for battery-powered applications where high precision and low power consumption are important.

APPLICATIONS

- Pressure and position sensors
- Temperature measurements
- Electronic scales
- Medical instrumentation
- Battery-powered equipment
- Handheld test equipment

FEATURES

- Very low supply current: 13 μA typical
- Low offset voltage: 15 μV maximum
- Offset voltage drift: 20 nV/°C
- Single-supply operation: 1.8 V to 5.5 V
- High PSRR: 110 dB minimum
- High CMRR: 110 dB minimum
- Rail-to-rail input/output
- Unity-gain stable
- Extended industrial temperature range

PIN CONFIGURATIONS

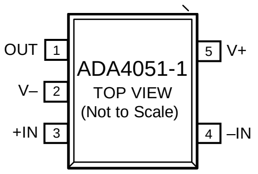


Figure 1. SOT-23-5

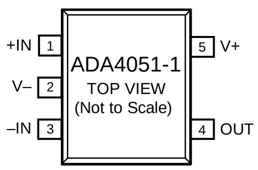


Figure 2. SC-70-5

ELECTRICAL CHARACTERISTICS—1.8 V OPERATION

V_{SY} = 1.8 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, R_L = 100 kΩ to GND, unless otherwise noted.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Offset Voltage	V_{OS}					
ADA4051-2		0 V ≤ V_{CM} ≤ 1.8 V		2	15	μV
ADA4051-1		0 V ≤ V_{CM} ≤ 1.8 V		2	17	μV
		−40°C ≤ T_A ≤ +125°C			27	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.02	0.1	μV/°C
Input Bias Current	I_B			5	50	pA
		−40°C ≤ T_A ≤ +125°C			200	pA
Input Offset Current	I_{OS}			10	100	pA
		−40°C ≤ T_A ≤ +125°C			150	pA
Input Voltage Range		−40°C ≤ T_A ≤ +125°C	0		1.8	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 1.8 V	105	125		dB
		−40°C ≤ T_A ≤ +125°C	100			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 10 kΩ to V_{CM},	106	130		dB
		0.1 V ≤ V_{OUT} ≤ V_{SY} − 0.1 V				
		−40°C ≤ T_A ≤ +125°C	100			dB
Differential Mode	R_{INDM}			8		MΩ
Common Mode	R_{INCM}			250		GΩ
Input Capacitance, Differential Mode	C_{INDM}			2		pF
Input Capacitance, Common Mode	C_{INCM}			5		pF
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}	1.796	1.799		V
		−40°C ≤ T_A ≤ +125°C	1.79			V
		R_L = 10 kΩ to V_{CM}	1.76	1.796		V
		−40°C ≤ T_A ≤ +125°C	1.7			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}		1	3	mV
		−40°C ≤ T_A ≤ +125°C			9	mV
		R_L = 10 kΩ to V_{CM}		3	20	mV
		−40°C ≤ T_A ≤ +125°C			40	mV
Short-Circuit Current	I_{SC}	V_{OUT} = V_{SY} or GND		13		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, G = 10		1		Ω
Power Supply Rejection Ratio	PSRR	1.8 V ≤ V_{SY} ≤ 5.5 V	110	135		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
Supply Current per Amplifier	I_{SY}					
ADA4051-2		V_{OUT} = V_{SY}/2		13	17	μA
ADA4051-1		V_{OUT} = V_{SY}/2		15	18	μA
		−40°C ≤ T_A ≤ +125°C			20	μA
Slew Rate	SR+	R_L = 10 kΩ, C_L = 100 pF, G = 1		0.04		V/μs
	SR−	R_L = 10 kΩ, C_L = 100 pF, G = 1		0.03		V/μs
Settling Time	t_S	To 0.1%, V_{IN} = 1 V p-p,		120		μs
		R_L = 10 kΩ, C_L = 100 pF				
Gain Bandwidth Product	GBP	C_L = 100 pF, G = 1		115		kHz
Phase Margin	Φ_M	C_L = 100 pF, G = 1		40		Degrees
Channel Separation	CS	V_{IN} = 1.7 V, f = 100 Hz		140		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		1.96		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		95		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		100		fA/√Hz

ELECTRICAL CHARACTERISTICS—5 V OPERATION

V_{SY} = 5.0 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, R_L = 100 kΩ to GND, unless otherwise noted.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Offset Voltage	V_{OS}					
ADA4051-2		0 V ≤ V_{CM} ≤ 5 V		2	15	µV
ADA4051-1		0 V ≤ V_{CM} ≤ 5 V		2	17	µV
		−40°C ≤ T_A ≤ +125°C			27	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.02	0.1	µV/°C
Input Bias Current	I_B			20	70	pA
		−40°C ≤ T_A ≤ +125°C			200	pA
Input Offset Current	I_{OS}			40	100	pA
		−40°C ≤ T_A ≤ +125°C			150	pA
Input Voltage Range		−40°C ≤ T_A ≤ +125°C	0		5	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 5 V	110	135		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 10 kΩ to V_{CM},	115	135		dB
		0.1 V ≤ V_{OUT} ≤ V_{SY} − 0.1 V				
		−40°C ≤ T_A ≤ +125°C	106			dB
Differential Mode	R_{INDM}			8		MΩ
Common Mode	R_{INCM}			250		GΩ
Input Capacitance, Differential Mode	C_{INDM}			2		pF
Input Capacitance, Common Mode	C_{INCM}			5		pF
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}	4.996	4.998		V
		−40°C ≤ T_A ≤ +125°C	4.985			V
		R_L = 10 kΩ to V_{CM}	4.96	4.99		V
		−40°C ≤ T_A ≤ +125°C	4.9			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}		1	4	mV
		−40°C ≤ T_A ≤ +125°C			13	mV
		R_L = 10 kΩ to V_{CM}		9	30	mV
		−40°C ≤ T_A ≤ +125°C			90	mV
Short-Circuit Current	I_{SC}	V_{OUT} = V_{SY} or GND		15		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, G = 10		1		Ω
Power Supply Rejection Ratio	PSRR	1.8 V ≤ V_{SY} ≤ 5.5 V	110	135		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
Supply Current per Amplifier	I_{SY}					
ADA4051-2		V_{OUT} = V_{SY}/2		13	17	µA
ADA4051-1		V_{OUT} = V_{SY}/2		15	18	µA
		−40°C ≤ T_A ≤ +125°C			20	µA
Slew Rate	SR+	R_L = 10 kΩ, C_L = 100 pF, G = 1		0.06		V/µs
	SR−	R_L = 10 kΩ, C_L = 100 pF, G = 1		0.04		V/µs
Settling Time	t_S	To 0.1%, V_{IN} = 1 V p-p,		110		µs
		R_L = 10 kΩ, C_L = 100 pF				
Gain Bandwidth Product	GBP	C_L = 100 pF, G = 1		125		kHz
Phase Margin	Φ_M	C_L = 100 pF, G = 1		40		Degrees
Channel Separation	CS	V_{IN} = 4.99 V, f = 100 Hz		140		dB

Param eter	Symbol	Test Conditions /Comments	Min	Typ	Max	Unit
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		1.96		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		95		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		100		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Supply Voltage	6 V
Input Voltage	$\pm V_{SY} \pm 0.3$ V
Input Current[1]	±10 mA
Differential Input Voltage[2]	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

[2] Inputs are protected against high differential voltages by internal series 1.33 kΩ resistors and back-to-back diode-connected N-MOSFETs(with a typical V_T of 0.7 V for V_{CM} of 0 V)

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

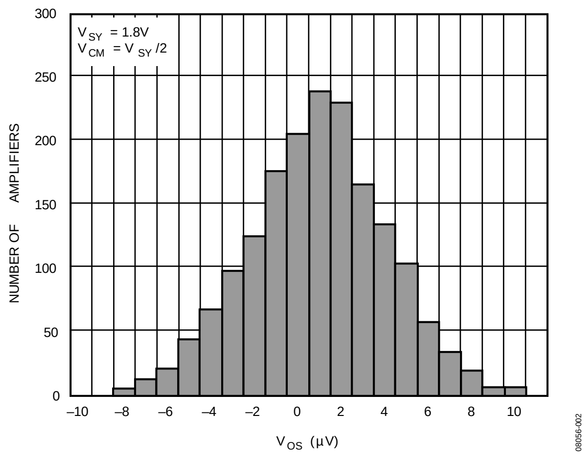


Figure 5. Input Offset Voltage Distribution

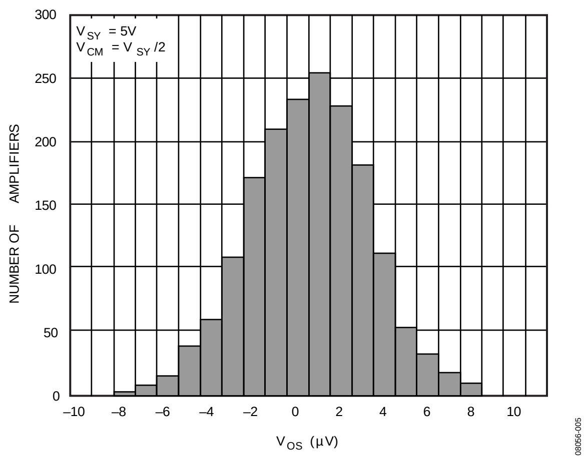


Figure 8. Input Offset Voltage Distribution

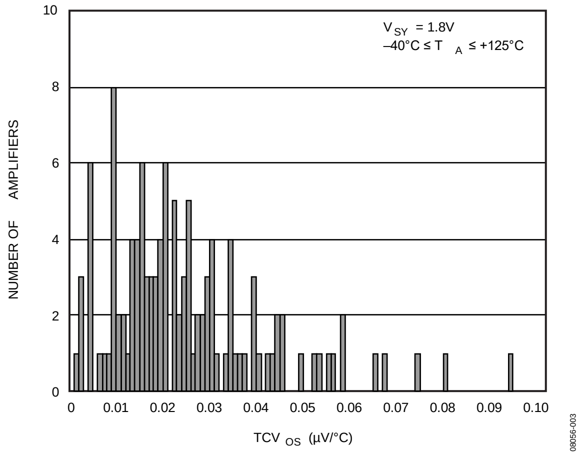


Figure 6. Input Offset Voltage Drift Distribution with Temperature

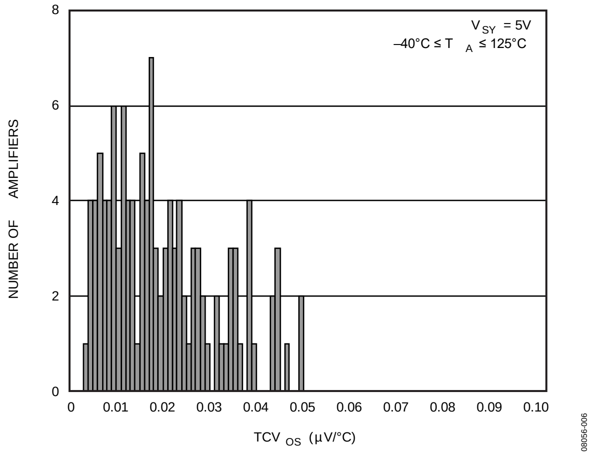


Figure 9. Input Offset Voltage Drift Distribution with Temperature

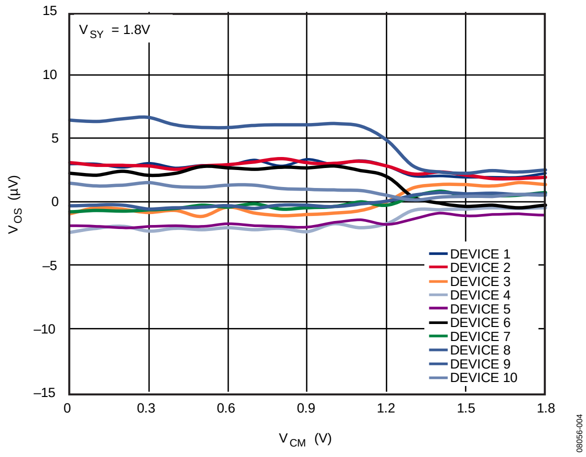


Figure 7. Input Offset Voltage vs. Input Common -Mode Voltage

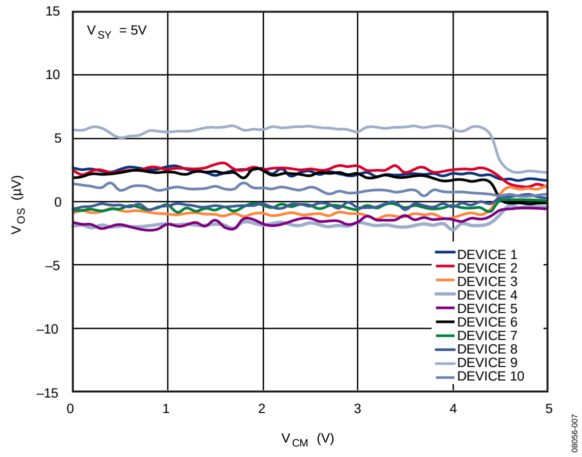


Figure 10. Input Offset Voltage vs. Input Common -Mode Voltage

T_A = 25°C, unless otherwise noted.

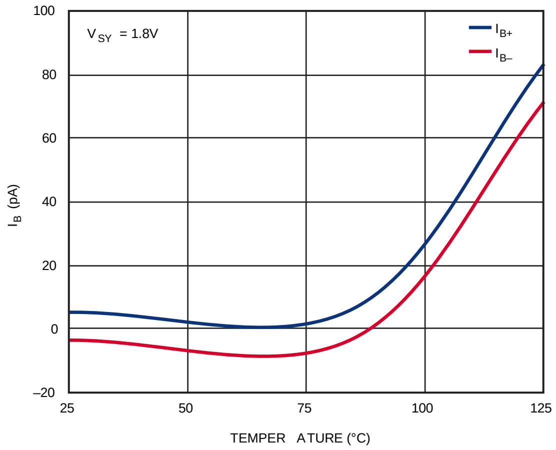


Figure 11. Input Bias Current vs. Temperature

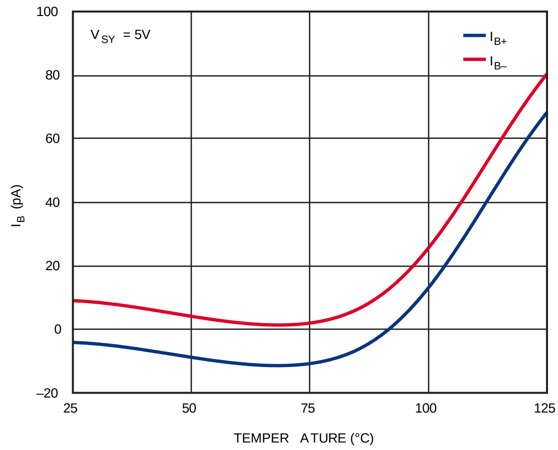


Figure 14. Input Bias Current vs. Temperature

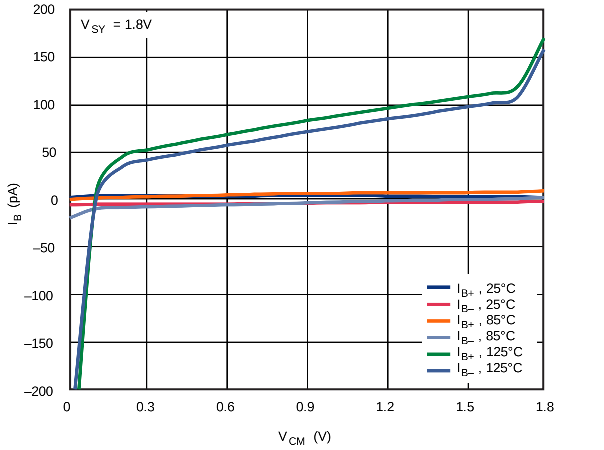


Figure 12. Input Bias Current vs. Common-Mode Voltage and Temperature

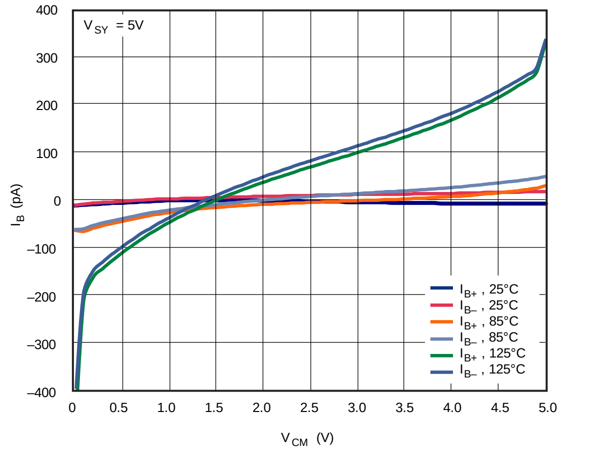


Figure 15. Input Bias Current vs. Common-Mode Voltage and Temperature

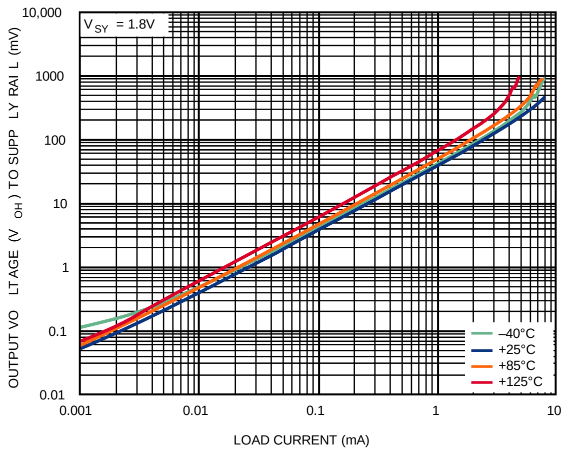


Figure 13. Output Voltage (V_{OH}) to Supply Rail vs. Load Current and Temperature

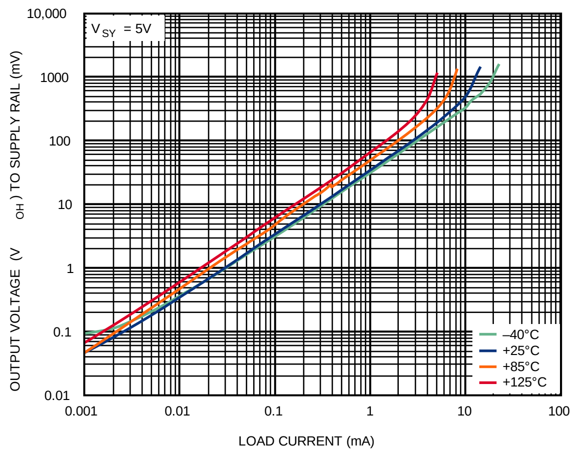


Figure 16. Output Voltage (V_{OH}) to Supply Rail vs. Load Current and Temperature

T_A = 25°C, unless otherwise noted.

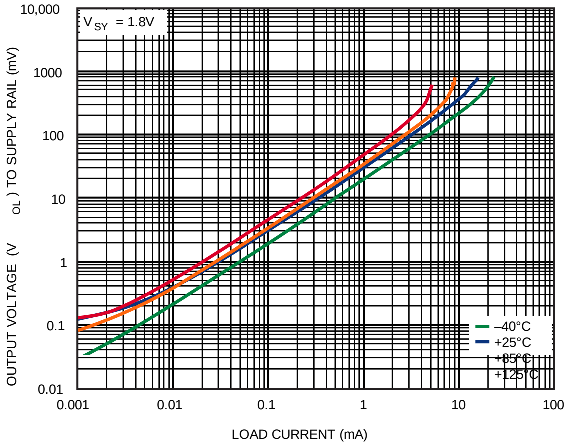


Figure 17. Output Voltage (V_{OL}) to Supply Rail vs. Load Current and Temperature

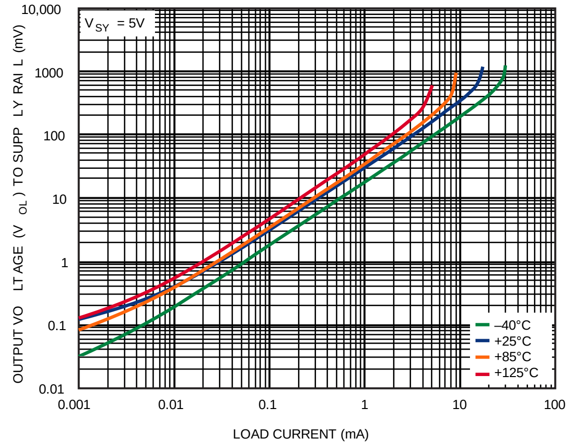


Figure 20. Output Voltage (V_{OL}) to Supply Rail vs. Load Current and Temperature

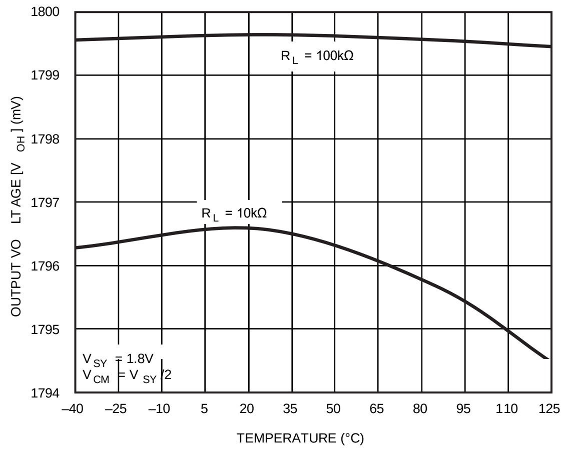


Figure 18. Output Voltage (V_{OH}) vs. Temperature

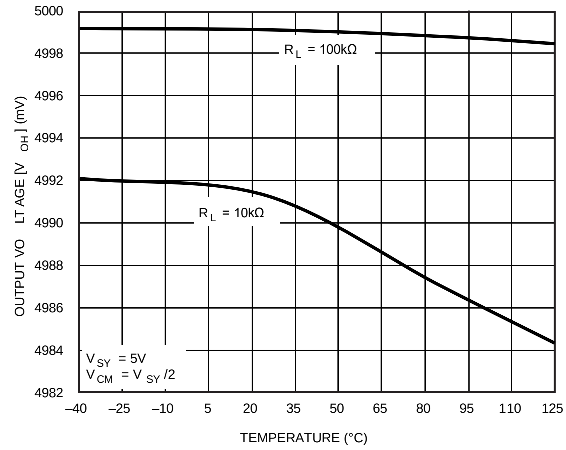


Figure 21. Output Voltage (V_{OH}) vs. Temperature

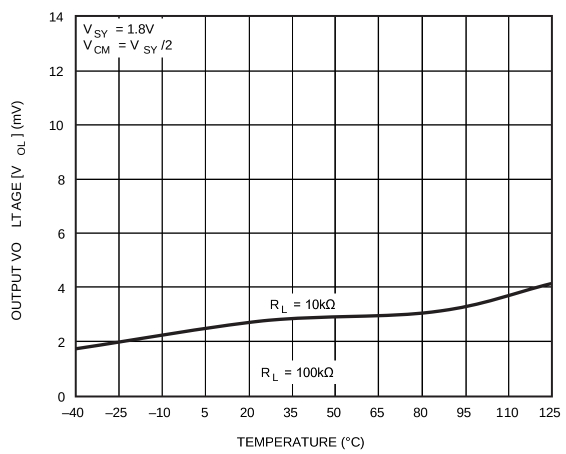


Figure 19. Output Voltage (V_{OL}) vs. Temperature

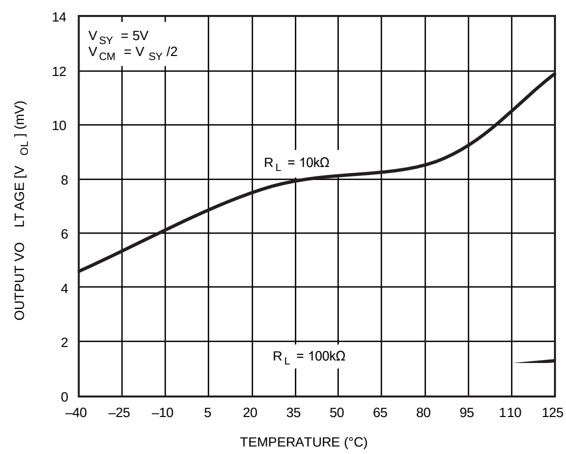


Figure 22. Output Voltage (V_{OL}) vs. Temperature

T_A = 25°C, unless otherwise noted.

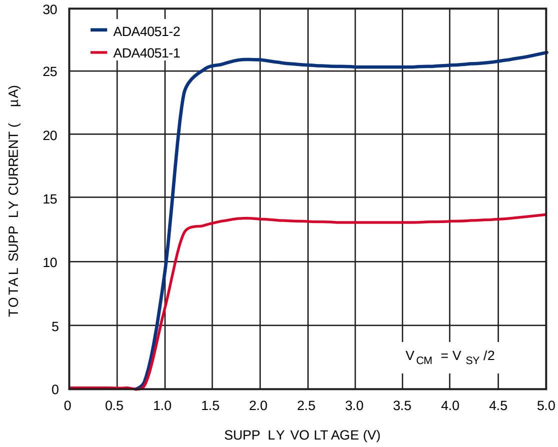


Figure 23. Total Supply Current vs. Supply Voltage

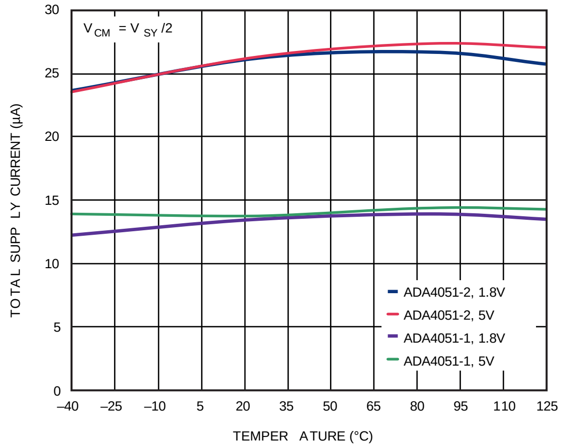


Figure 26. Total Supply Current vs. Temperature

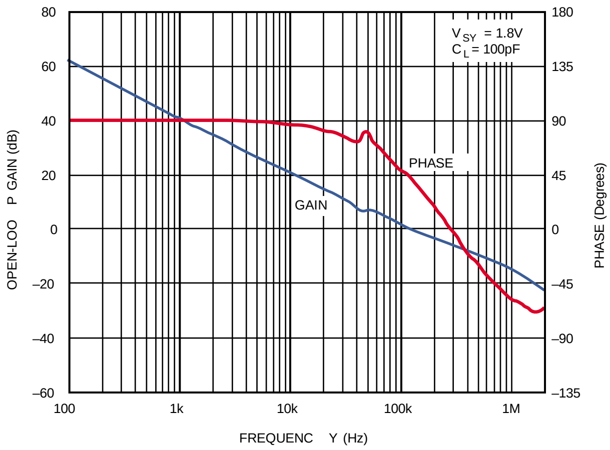


Figure 24. Open-Loop Gain and Phase vs. Frequency

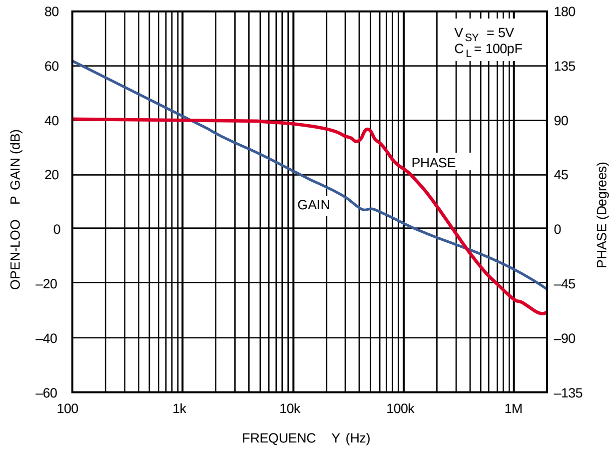


Figure 27. Open-Loop Gain and Phase vs. Frequency

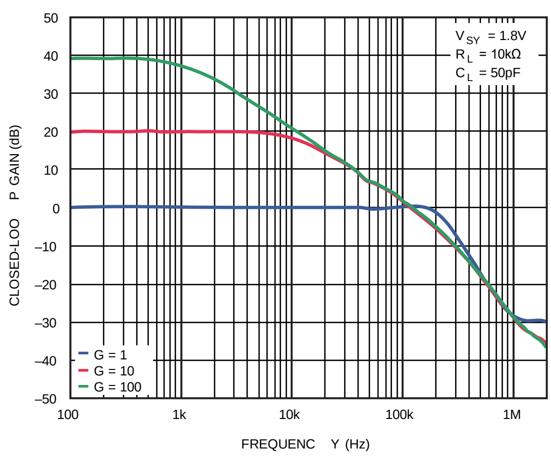


Figure 25. Closed-Loop Gain vs. Frequency

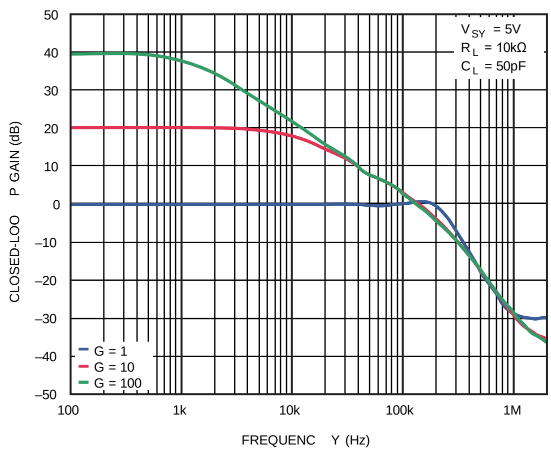


Figure 28. Closed-Loop Gain vs. Frequency

T_A = 25°C, unless otherwise noted.

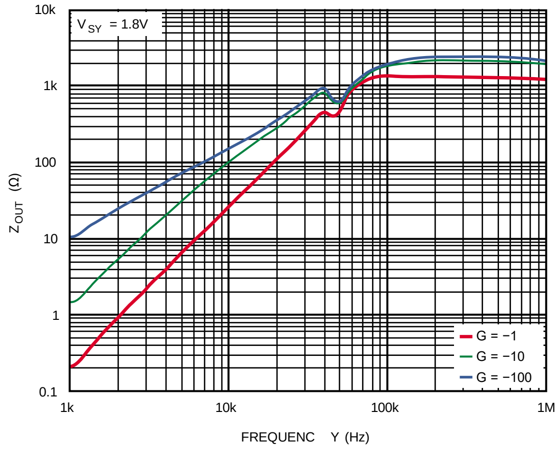


Figure 29. Output Impedance vs. Frequency

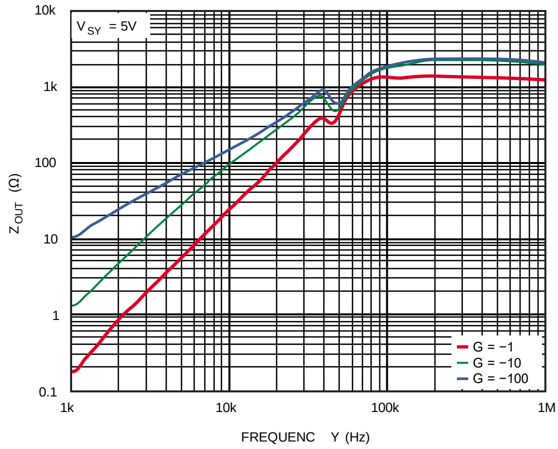


Figure 32. Output Impedance vs. Frequency

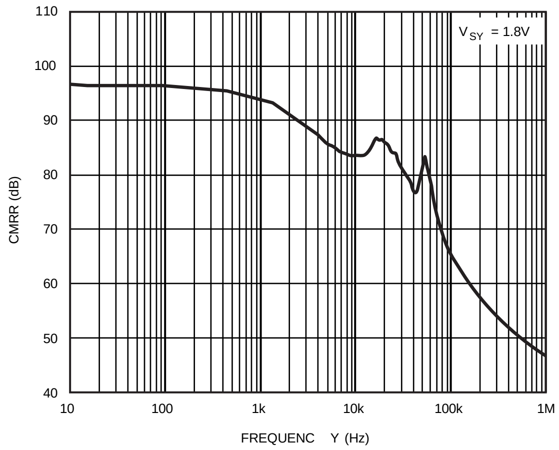


Figure 30. CMRR vs. Frequency

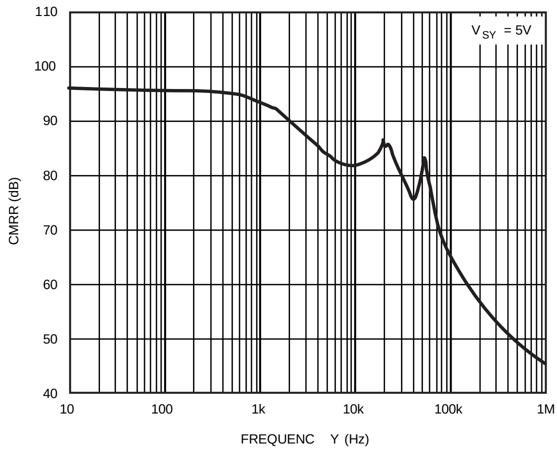


Figure 33. CMRR vs. Frequency

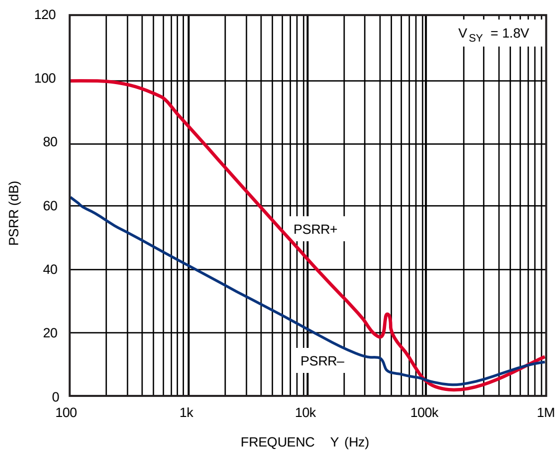


Figure 31. PSRR vs. Frequency

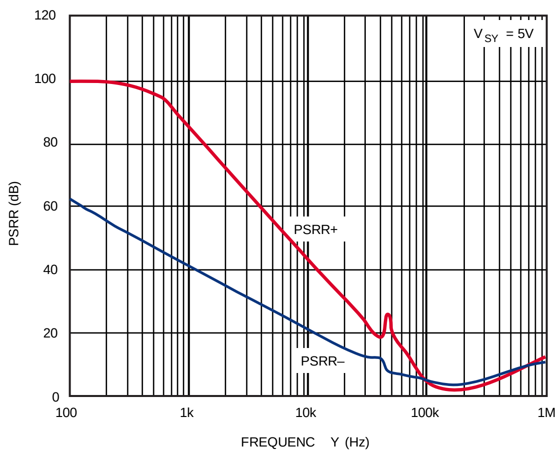


Figure 34. PSRR vs. Frequency

T_A = 25°C, unless otherwise noted.

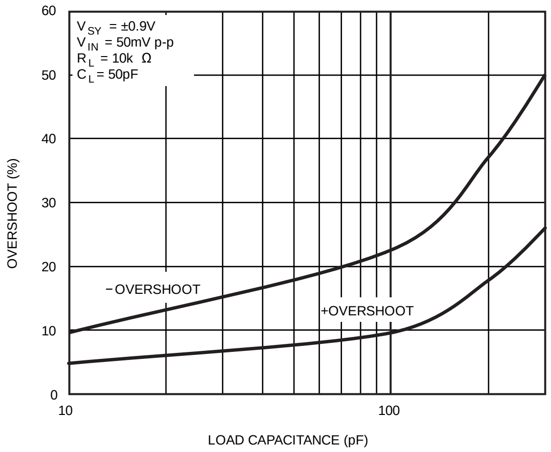


Figure 35. Small-Signal Overshoot vs. Load Capacitance

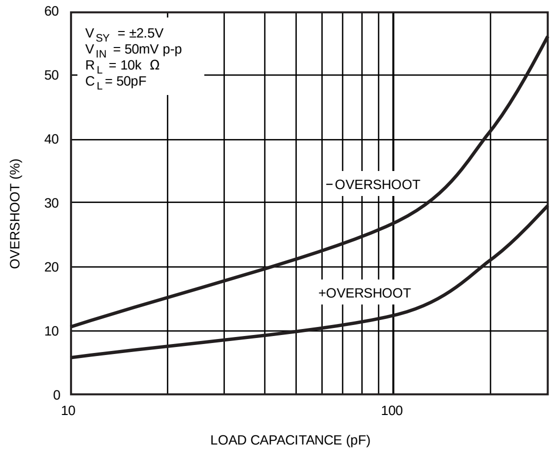


Figure 38. Small-Signal Overshoot vs. Load Capacitance

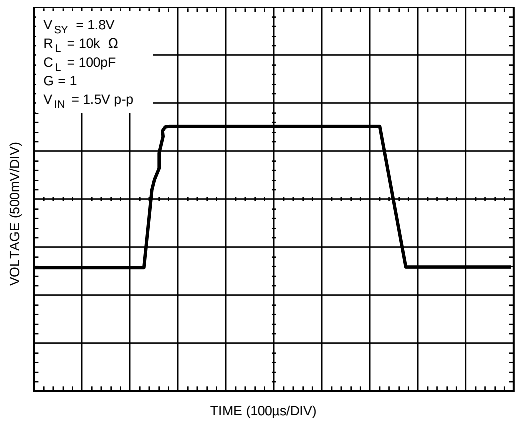


Figure 36. Large-Signal Transient Response

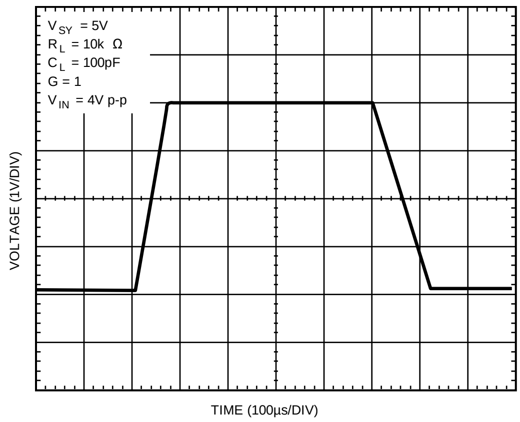


Figure 39. Large-Signal Transient Response

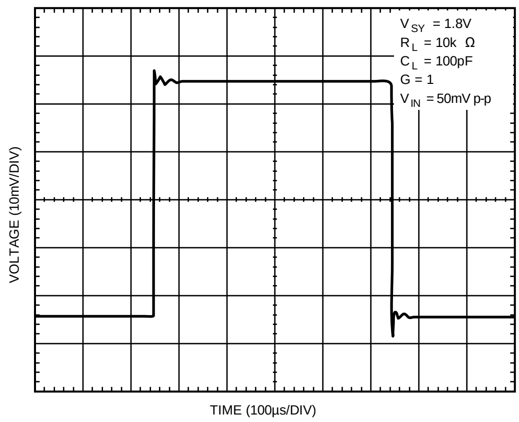


Figure 37. Small-Signal Transient Response

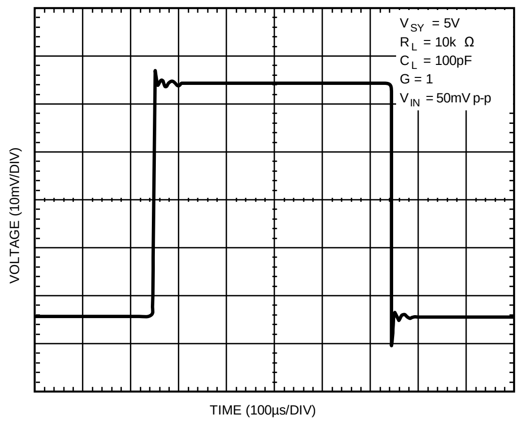


Figure 40. Small-Signal Transient Response

T_A = 25°C, unless otherwise noted.

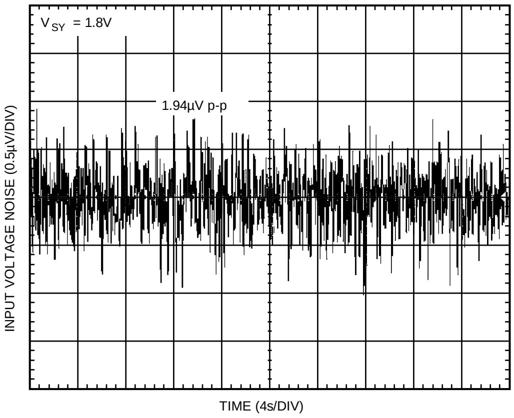


Figure 41. Input Voltage Noise, 0.1 Hz to 10 Hz

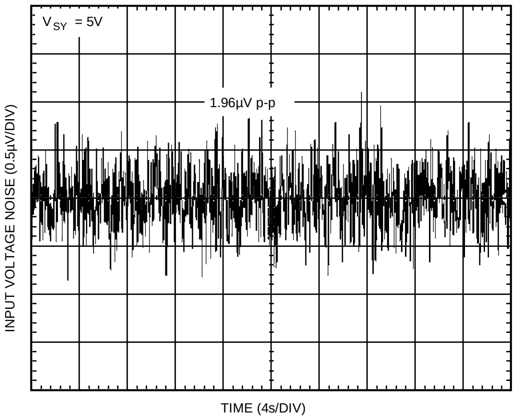


Figure 44. Input Voltage Noise, 0.1 Hz to 10 Hz

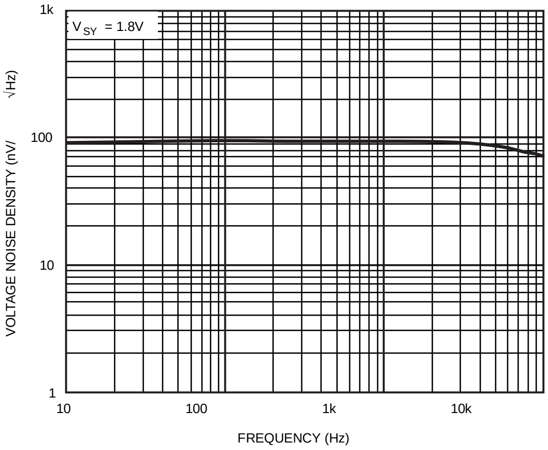


Figure 42. Voltage Noise Density vs. Frequency

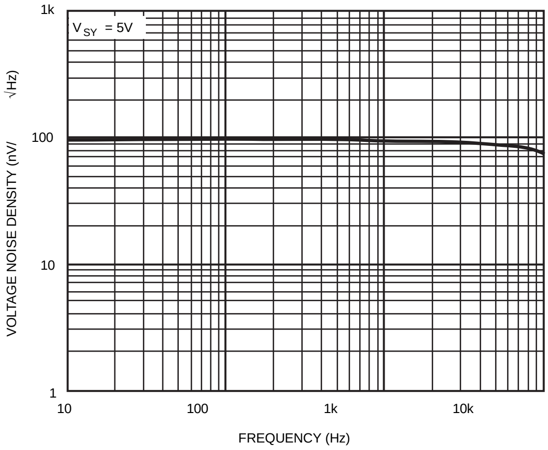


Figure 45. Voltage Noise Density vs. Frequency

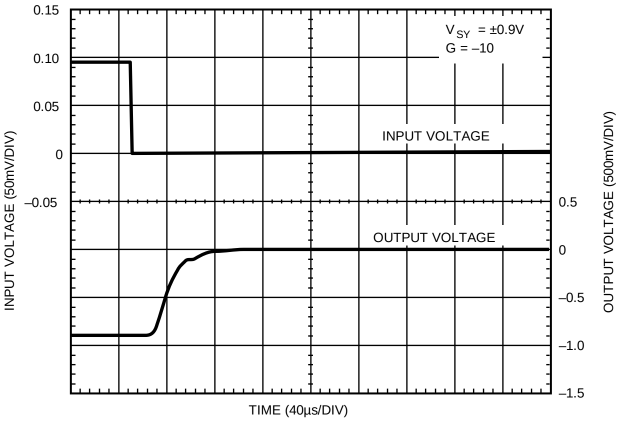


Figure 43. Positive Overload Recovery

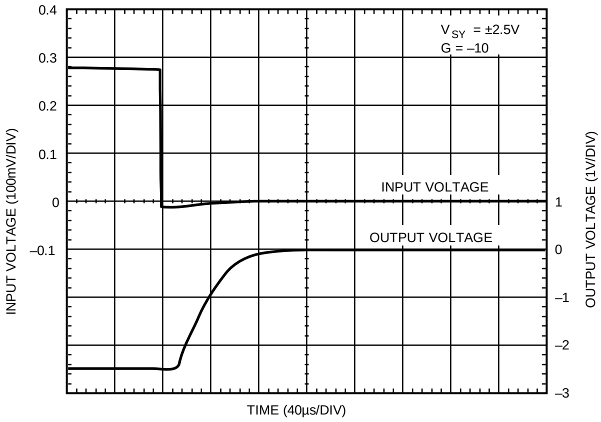


Figure 46. Positive Overload Recovery

T_A = 25°C, unless otherwise noted.

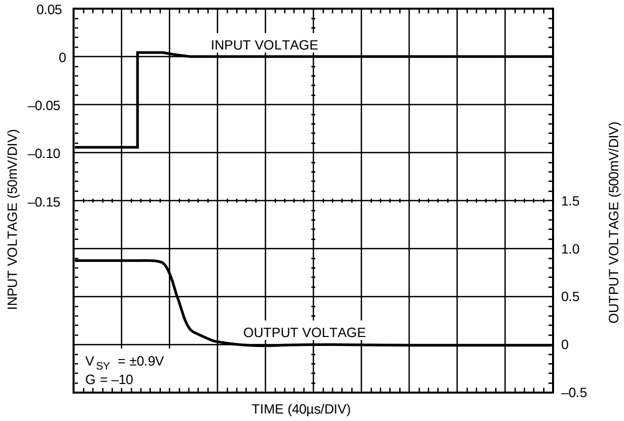


Figure 47. Negative Overload Recovery

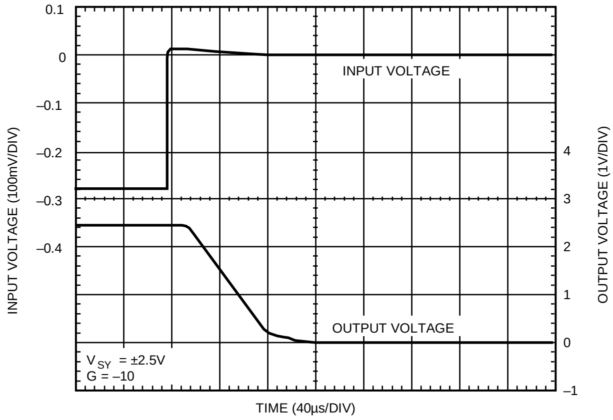


Figure 50. Negative Overload Recovery

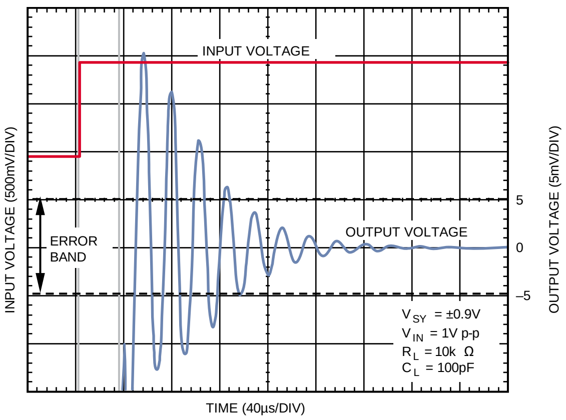


Figure 48. Positive Settling Time to 0.1%

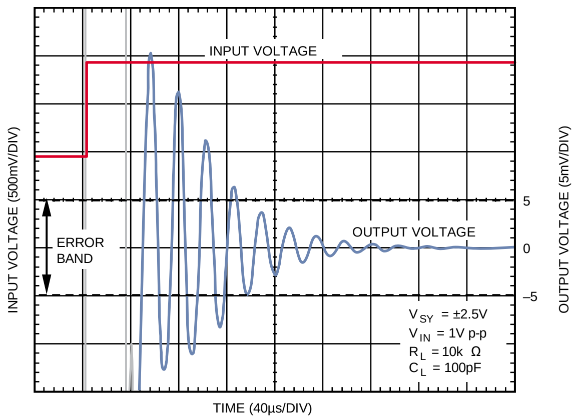


Figure 51. Positive Settling Time to 0.1%

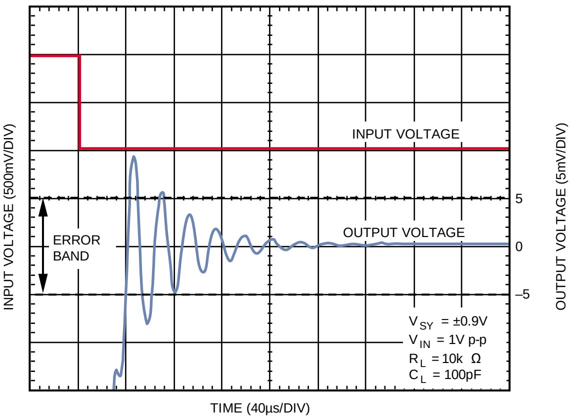


Figure 49. Negative Settling Time to 0.1%

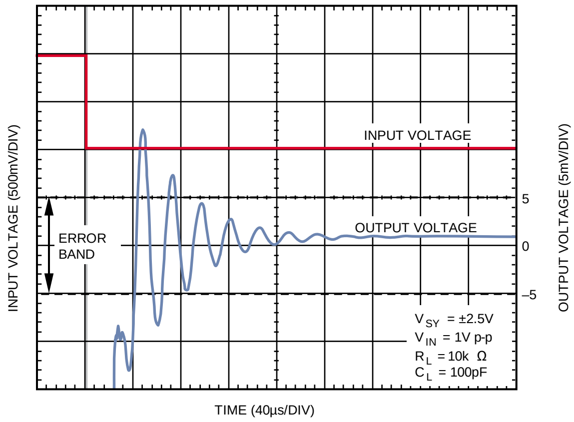


Figure 52. Negative Settling Time to 0.1%

T_A = 25°C, unless otherwise noted.

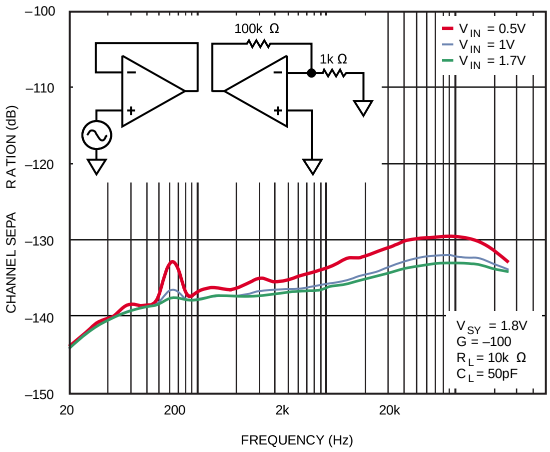


Figure 53. Channel Separation vs. Frequency

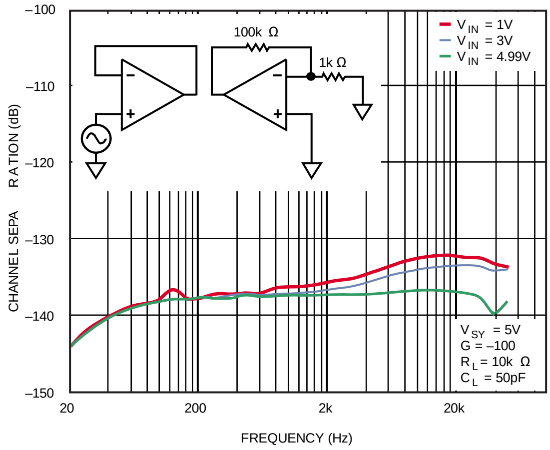


Figure 56. Channel Separation vs. Frequency

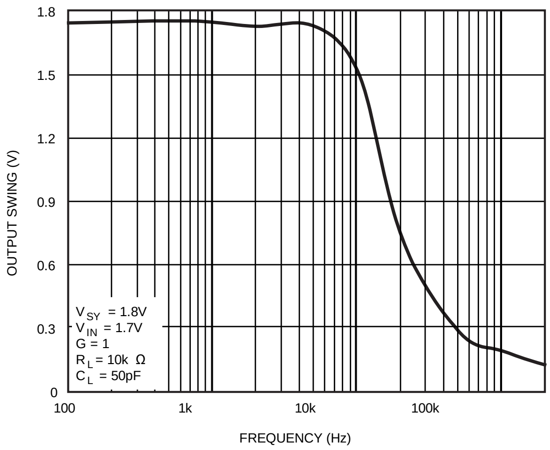


Figure 54. Output Swing vs. Frequency

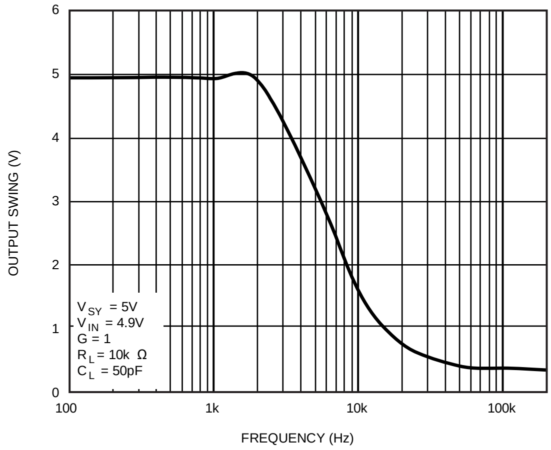


Figure 57. Output Swing vs. Frequency

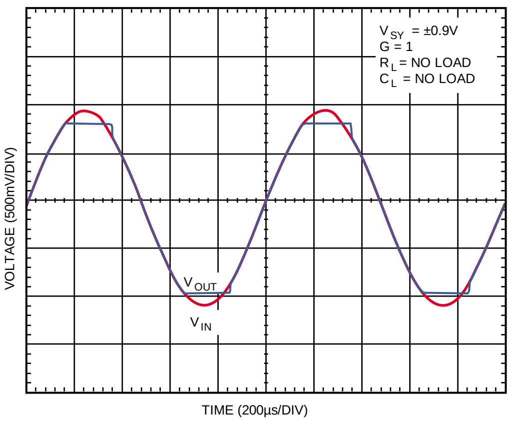


Figure 55. No Phase Reversal

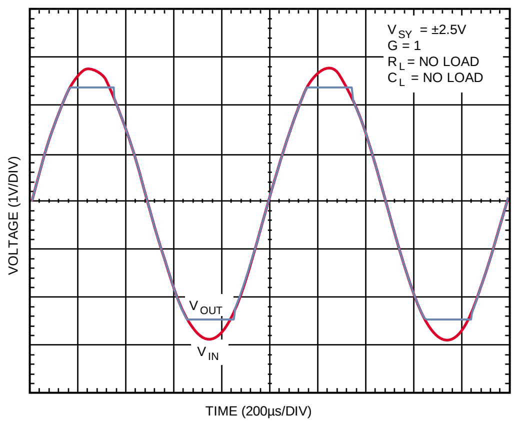
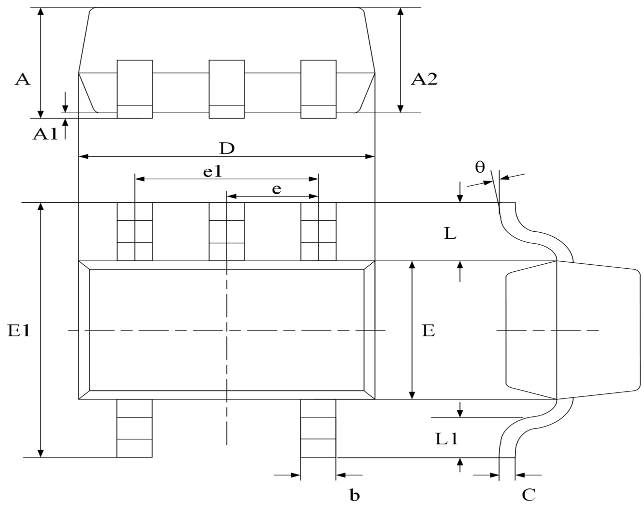


Figure 58. No Phase Reversal

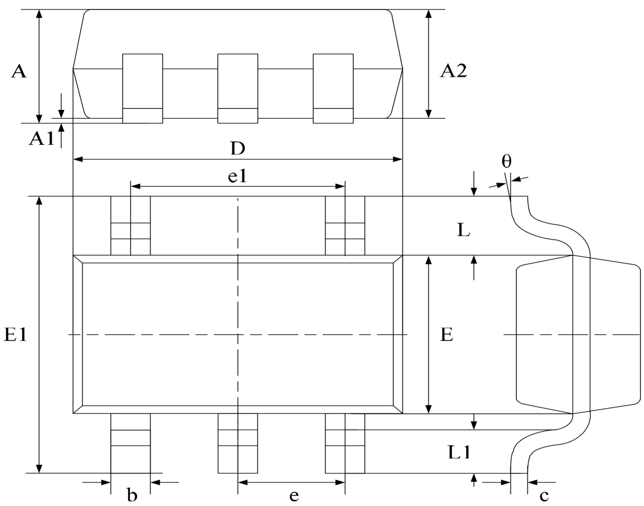
Package Dimension

SC70-5（SOT353）



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	0.900	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	1.8500	2.150	0.079	0.087
E	1.100	1.400	0.045	0.053
E1	1.950	2.200	0.085	0.096
e	0.850 typ.		0.026 typ.	
e1	1.200	1.400	0.047	0.055
L	0.42 ref.		0.021 ref.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.040	1.350	0.042	0.055
A1	0.040	0.150	0.002	0.006
A2	1.000	1.200	0.041	0.049
b	0.380	0.480	0.015	0.020
c	0.110	0.210	0.004	0.009
D	2.720	3.120	0.111	0.127
E	1.400	1.800	0.057	0.073
E1	2.600	3.000	0.106	0.122
e	0.950 typ.		0.037 typ.	
e1	1.900 typ.		0.078 typ.	
L	0.700 ref.		0.028 ref.	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Ordering information

Order code	Package	Baseqty	Deliverymode	Marking
UMW ADA4051-1ARJZ	SOT23-5	3000	Tape and reel	A0U
UMW ADA4051-1AKSZ	SC70-5	3000	Tape and reel	A0U