

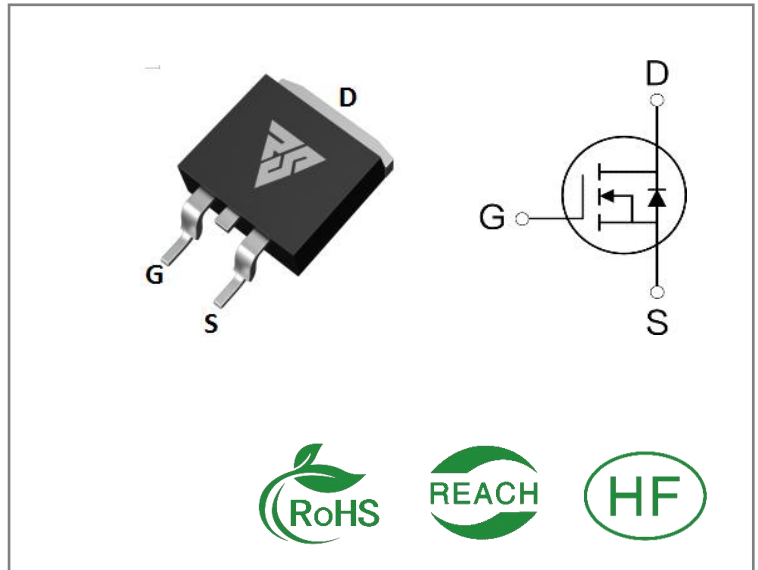
ID	R <sub>DS(ON)</sub> (Typ)	VDSS
20A	0.21Ω	500V

**Applications:**

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

**Features:**

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability


**Ordering Information**

Part Number	Package	Marking	Packing	Qty.
RS20N50S	T0-263	RS20N50S	Tape&reel	800 PCS

**Absolute Maximum Ratings** Tc= 25°C unless otherwise specified

Symbol	Parameter	RS20N50S	Units
VDSS	Drain-to-Source Voltage	500	V
ID	Continuous Drain Current TC=25°C	20	A
IDM	Pulsed Drain Current (Note*1)	80	
PD	Power Dissipation	173	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Energy L = 10mH,,VDD = 50V, RG = 25Ω	650	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

\* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

**Thermal Resistance**

Symbol	Parameter	RS20N50S	Units	Test Conditions
R $\theta$ JC	Junction-to-Case	0.72	$^{\circ}\text{C} / \text{W}$	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}\text{C}$
R $\theta$ JA	Junction-to-Ambient	62.5		1 cubic foot chamber, free air.

**OFF Characteristics**  $T_J = 25^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	500	--	--	V	VGS=0V, ID=250 $\mu$ A
IDSS	Drain- to- Source Leakage Current	--	--	1	$\mu$ A	VDS=500V, VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V , VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V , VDS=0V

**ON Characteristics**  $T_J = 25^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	0.21	0.27	$\Omega$	VGS=10V, ID=10A
VGS(TH)	Gate Threshold Voltage	3	--	4	V	VGS=VDS, ID=250 $\mu$ A

**Resistive Switching Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	55	--	nS	VDS=250V ID=20A RG=25 $\Omega$
trise	Rise Time	--	32	--		
td(OFF)	Turn- OFF Delay Time	--	226	--		
tfall	Fall Time	--	58	--		

**Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	2707	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	292	--		
Crss	Reverse Transfer Capacitance	--	10.5	--		
Qg	Total Gate Charge	--	49	--	nC	VDS=400V ID=20A VGS=10V
Qgs	Gate- to- Source Charge	--	13.3	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	17.9	--		

**Source- Drain Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	20	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	80	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=10A,VGS=0V
trr	Reverse Recovery Time	--	318	--	nS	VGS=0V IS=20A,di/dt=100 A/μs
Qrr	Reverse Recovery Charge	--	4.5	--	μC	

**Notes:**

- \* 1. Repetitive rating, pulse width limited by maximum junction temperature.
- \* 2. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 1\%$

Typical Feature Curve

Figure 1. Output Characteristics ( $T_J = 25^\circ\text{C}$ )

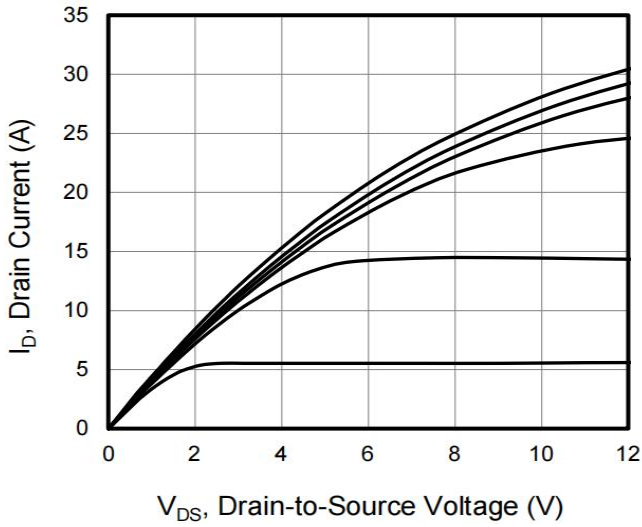


Figure 2. Body Diode Forward Voltage

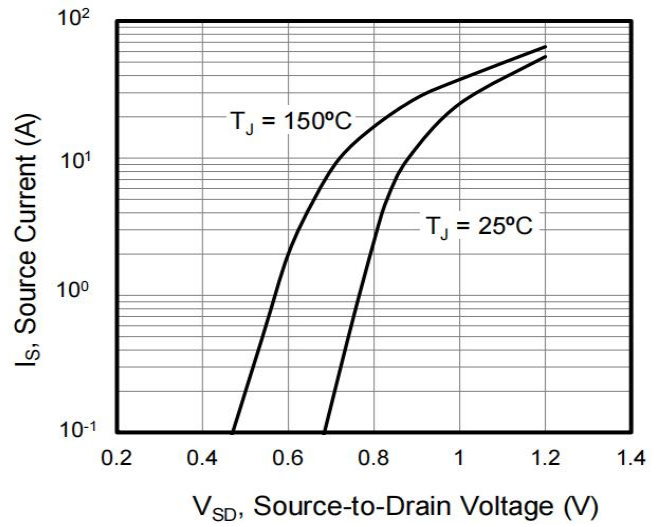


Figure 3. Drain Current vs. Temperature

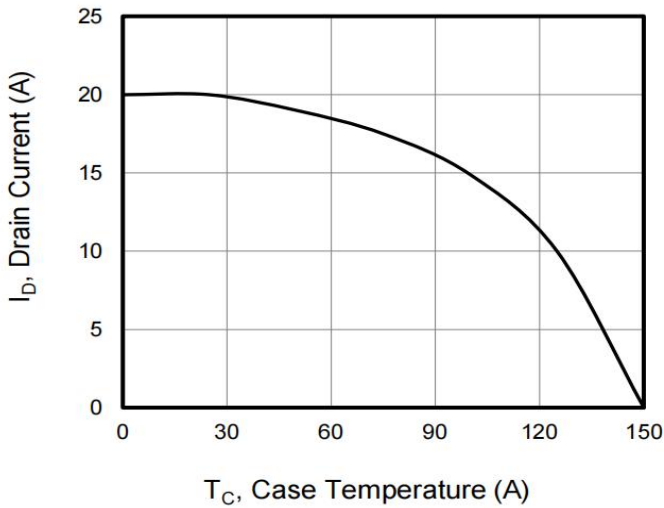


Figure 4.  $BV_{DSS}$  Variation vs. Temperature

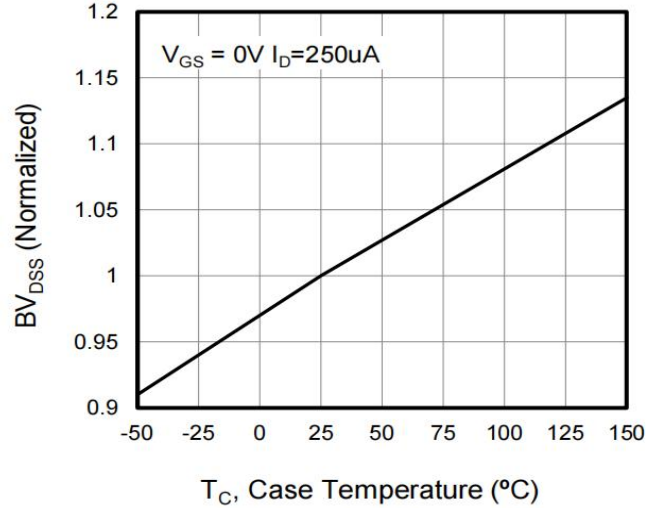


Figure 5. Transfer Characteristics

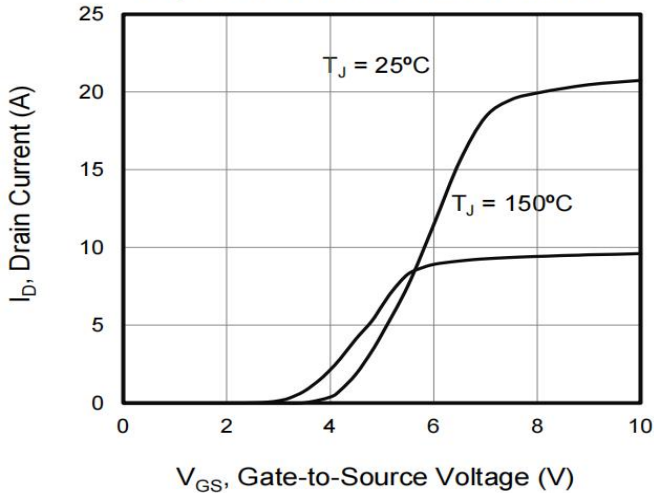


Figure 6. On-Resistance vs. Temperature

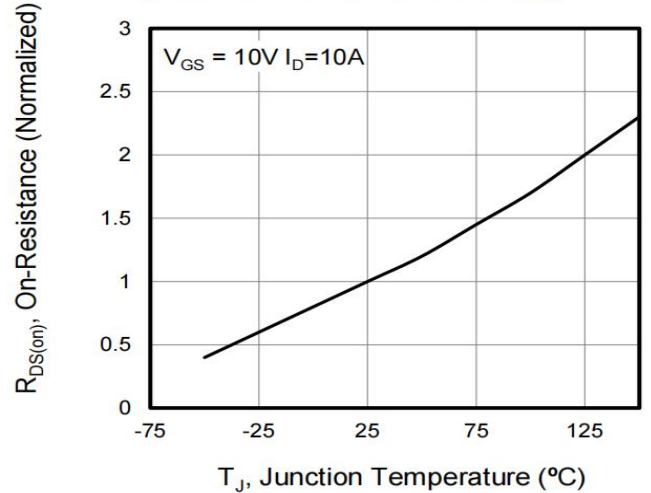


Figure 7. Capacitance

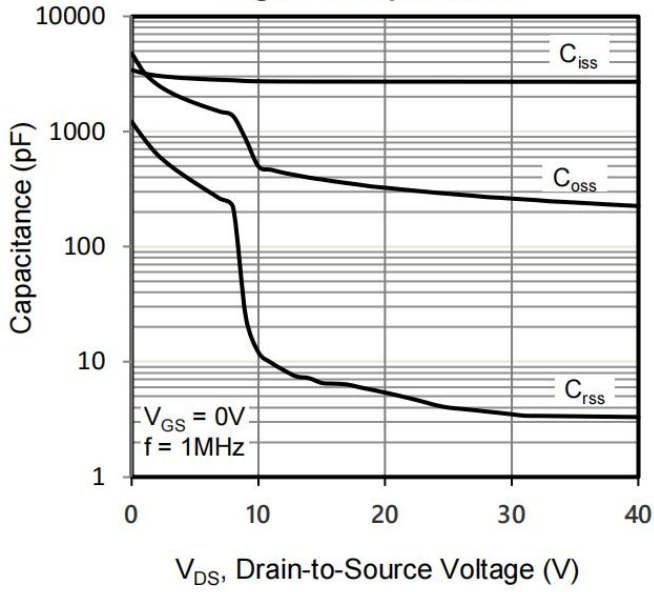


Figure 8. Gate Charge

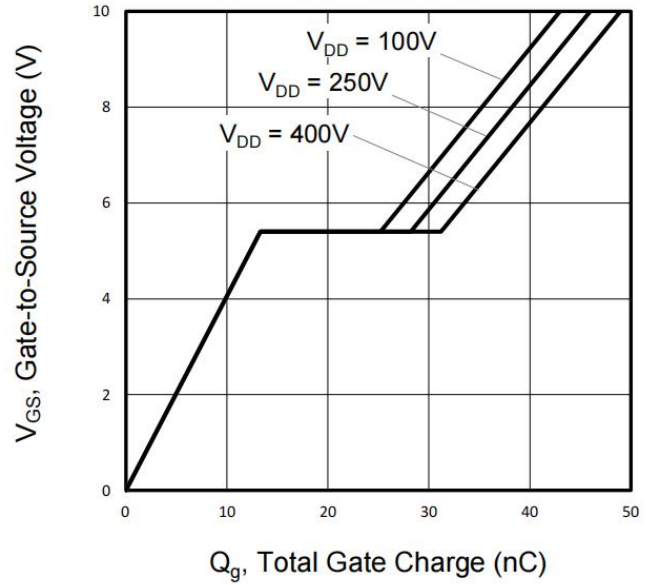
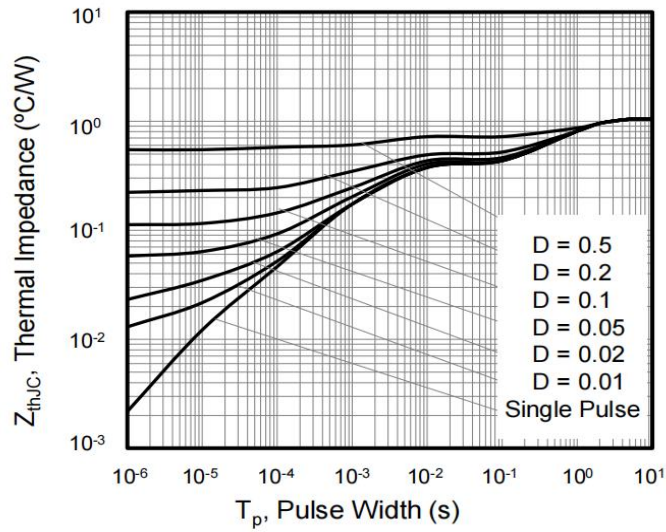
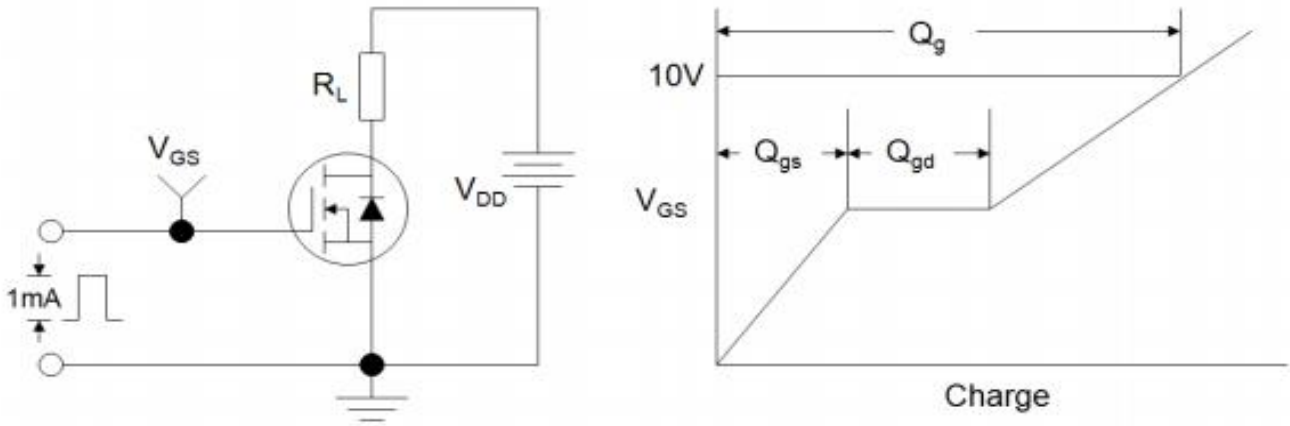


Figure 9. Transient Thermal Impedance

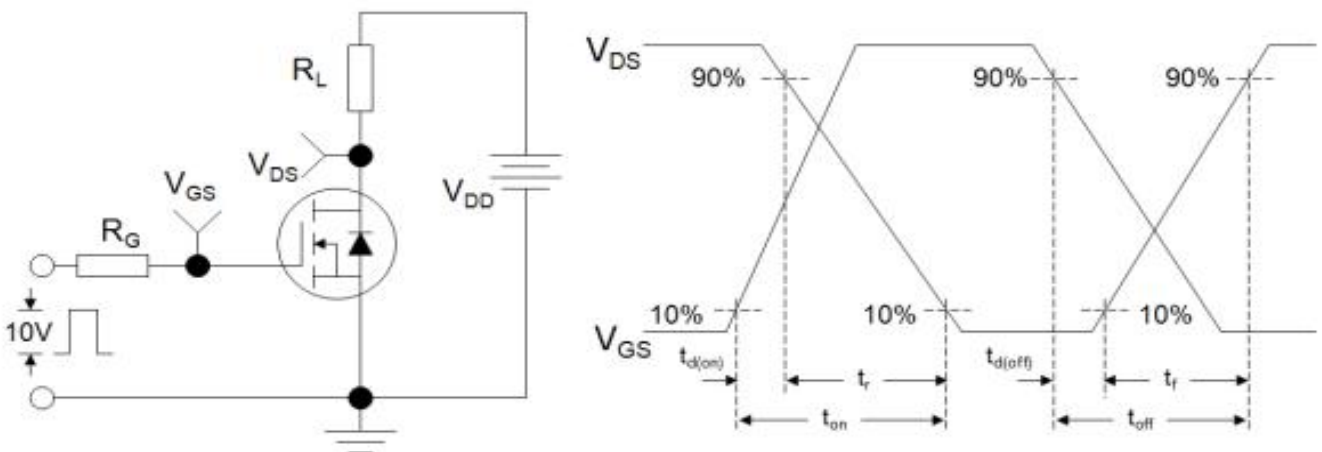


**Test Circuits and Waveforms**

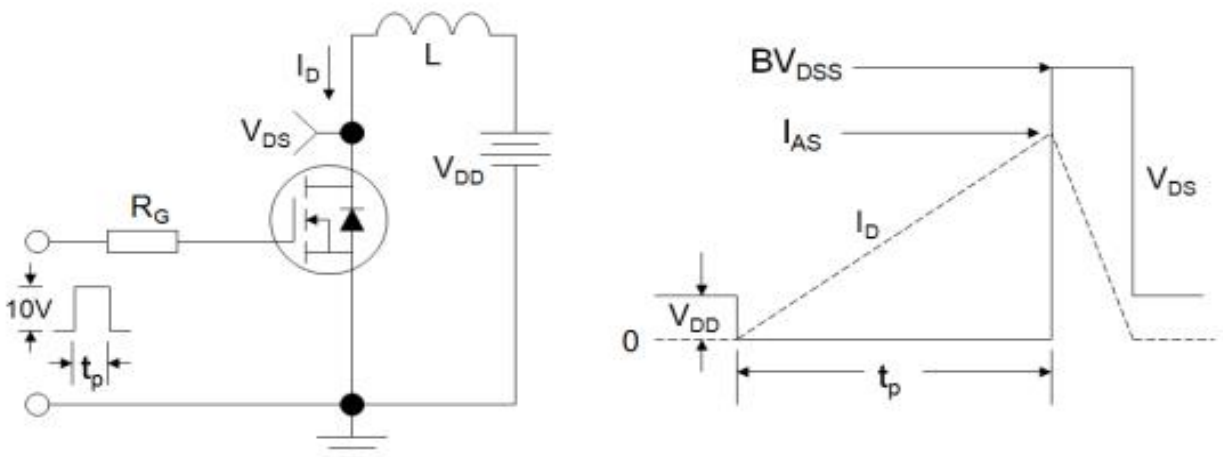
**Figure A: Gate Charge Test Circuit and Waveform**



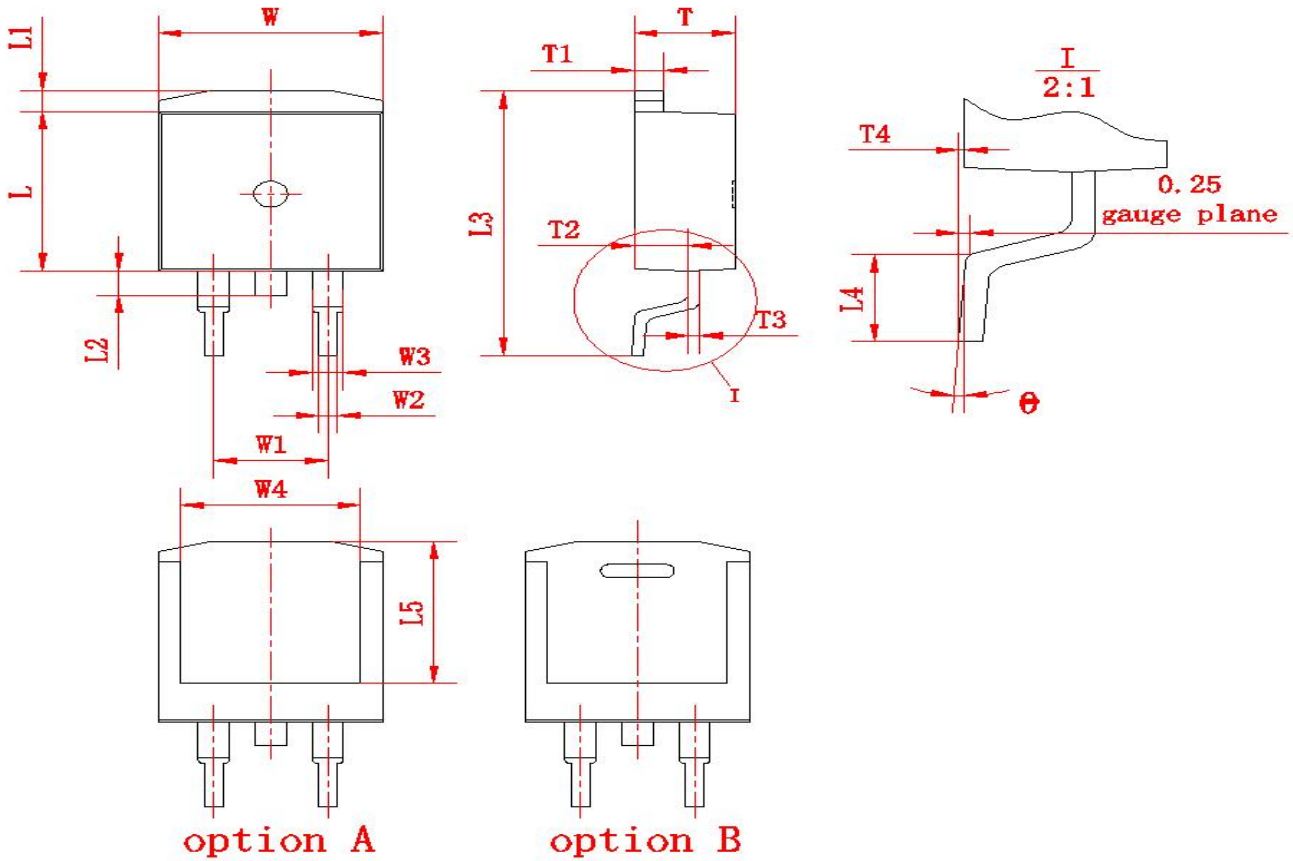
**Figure B: Resistive Switching Test Circuit and Waveform**



**Figure C: Unclamped Inductive Switching Test Circuit and Waveform**



Package outline drawing(TO-263 Unit: mm)



(单位: mm)

符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	9.80	10.20	L1	1.00	1.40	T1	1.20	1.40
W1	(5.08)		L2	1.20	1.60	T2	2.20	2.60
W2	0.70	0.95	L3	15.00	15.60	T3	0.45	0.65
W3	1.17	1.62	L4	2.20	2.80	T4	0	0.25
W4	(8.0)		L5	(8.2)		$\theta$	0°	8°
L	9.00	9.40	T	4.30	4.70			

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