HARRIS SEMICONDUCTOR

HI5714

January 1998

8-Bit, 40/60/75/80 MSPS A/D Converter

Features

- Sampling Rate . . . . . 40/60/75/80 MSPS
- Low Power 325mW
- 7.65 ENOB at 4.43MHz
- Overflow/Underflow Three-State TTL Output
- Operates with Low Level AC Clock
- Very Low Analog Input Capacitance
- No Buffer Amplifier Required
- No Sample and Hold Required
- TTL Compatible I/O
- Pin-Compatible to Philips TDA8714

Applications

- Video Digitizing
- QAM Demodulator
- Digital Cable Setup Box
- Tape Drive/Mass Storage
- Medical Ultrasound Imaging
- Communication Systems

Description

The HI5714 is a high precision, monolithic, 8-bit, Analog-to-Digital Converter fabricated in Harris' advanced HBC10 BiCMOS process.

The HI5714 is optimized for a wide range of applications such as ultrasound imaging, mass storage, instrumentation, and video digitizing, where accuracy and low power consumption are essential. The HI5714 is offered in 40 MSPS, 60 MSPS, and 75 MSPS sample rates.

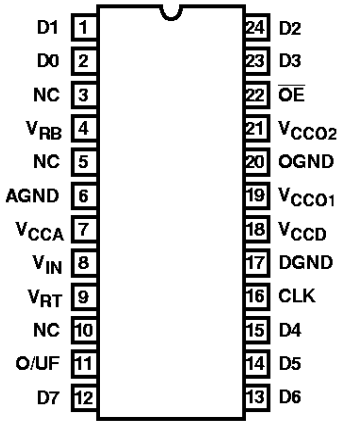
The HI5714 delivers ±0.4 LSB differential nonlinearity while consuming only 325mW power (Typical) at 75 MSPS. The digital inputs and outputs are TTL compatible, as well as allowing for a low-level sine wave clock input.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	SAMPLING FREQUENCY (MHz)	PKG. NO.
HI5714/4CB	0 to 70	24 Ld SOIC	40	M24.3
HI5714/6CB	0 to 70	24 Ld SOIC	60	M24.3
HI5714/7CB	0 to 70	24 Ld SOIC	75	M24.3
HI5714/8CB	0 to 70	24 Ld SOIC	80	M24.3
HI5714EVAL	25	Evaluation Board		

Pinout

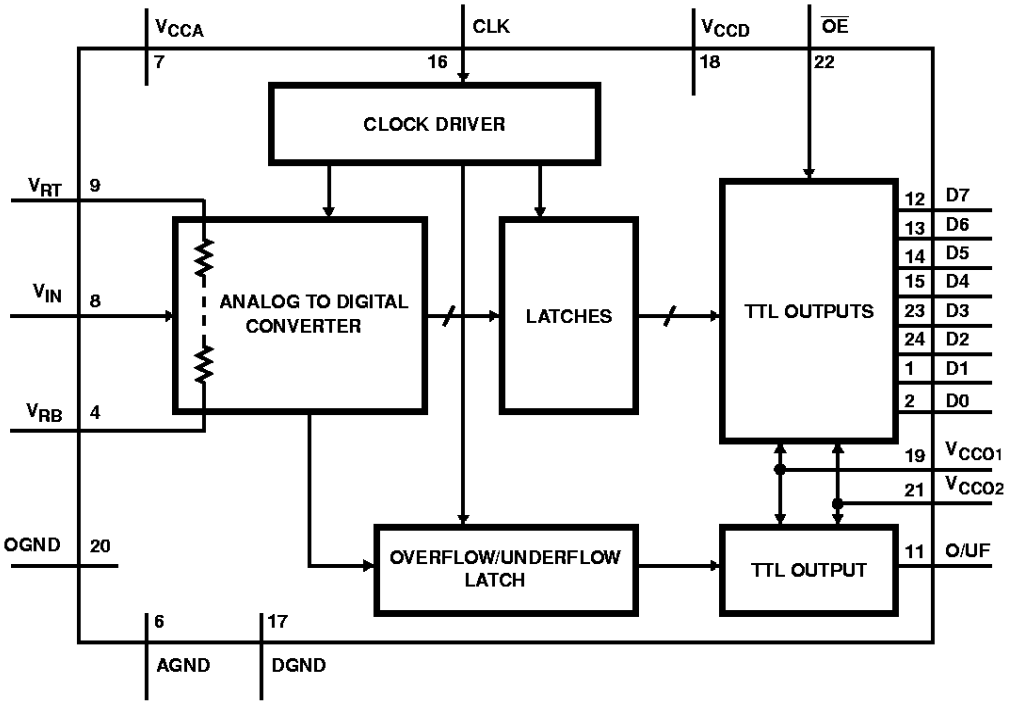
HI5714
(SOIC)
TOP VIEW



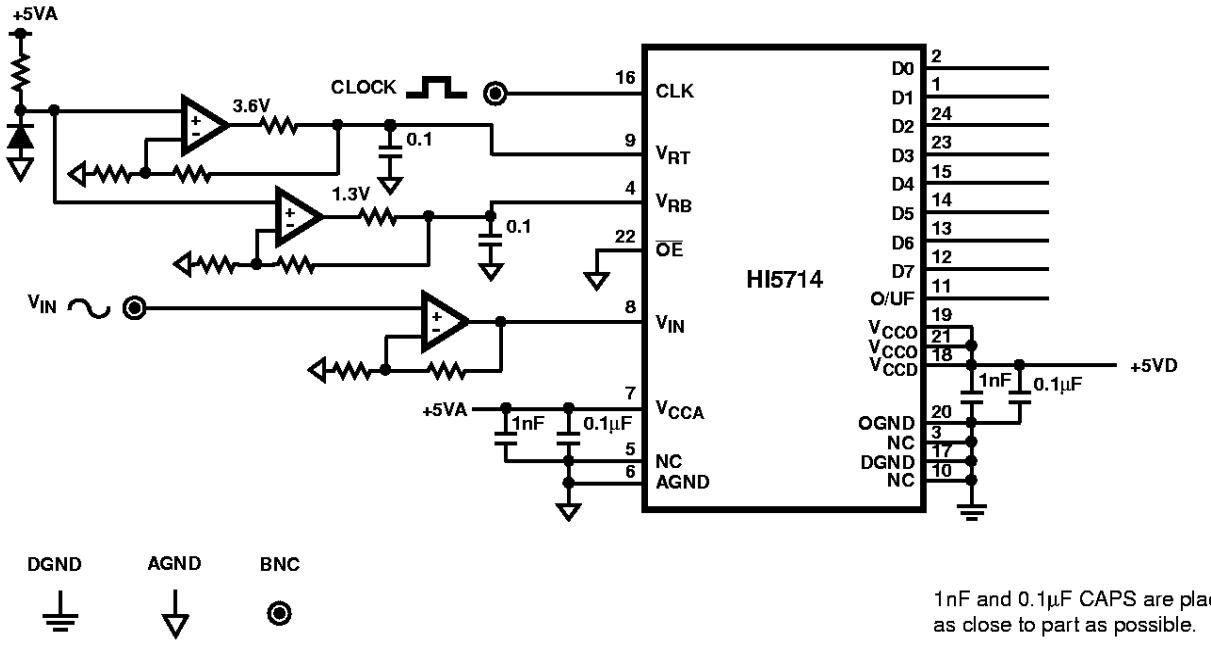
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3973.4

Functional Block Diagram



Typical Application Schematic



1nF and 0.1µF CAPS are placed as close to part as possible.

NOTES:

1. Pin 5 should be connected to AGND and pins 3 and 10 to DGND to reduce noise coupling into the device.
2. Analog and Digital supplies should be separated and decoupled to reduce digital noise coupling into the analog supply.

Absolute Maximum Ratings $T_A = 25^oC$

V_{CCA}, V_{CCD}, V_{CCO} . . . . . -0.3V to +6.0V
V_{CCA} - V_{CCD} 0.3V
V_{CCO} - V_{CCD} 0.3V
V_{CCA} - V_{CCO} 0.3V
V_{IN}, V_{CLK}, V_{RT}, V_{RB}, $\overline{OE}$ . . . . . -0.3V to +6.0V
I_{OUT}, Digital Pins 10mA
Input Current, All Pins. 1mA
Digital I/O Pins . . . . . OGND to V_{CCO}

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SOIC Package 75
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range
HI5714CB . . . . . 0^oC to 70^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{CCA} = V_{CCD} = V_{CCO} = +5V$; $V_{RB} = 1.3V$; $V_{RT} = 3.6V$; $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
CLOCK (Referenced to DGND) (Note 1)					
Logic Input Voltage Low, V_{IL}		0	-	0.8	V
Logic Input Voltage High, V_{IH}		2.0	-	V_{CCD}	V
Logic Input Current Low, I_{IL}	$V_{CLK} = 0.4V$	-400	-	-	µA
Logic Input Current High, I_{IH}	$V_{CLK} = 2.7V$	-	-	300	µA
Input Impedance, Z_{IN}	$f_{CLK} = 75MHz$ (Note 8)	-	2	-	kΩ
Input Capacitance, C_{IN}	$f_{CLK} = 75MHz$ (Note 8)	-	4.5	-	pF
$\overline{OE}$ (Referenced to DGND)					
Logic Input Voltage Low, V_{IL}		0	-	0.8	V
Logic Input Voltage High, V_{IH}		2.0	-	V_{CCD}	V
Logic Input Current Low, I_{IL}	$V_{IL} = 0.4V$	-400	-	-	µA
Logic Input Current High, I_{IH}	$V_{IH} = 2.7V$	-	-	20	µA
V_{IN} (Referenced to AGND)					
Input Current Low, I_{IL}	$V_{IN} = 1.2V$	-	0	-	µA
Input Current High, I_{IH}	$V_{IN} = 3.5V$	-	100	180	µA
Input Impedance, Z_{IN}	$f_{IN} = 4.43MHz$	-	10	-	kΩ
Input Capacitance, C_{IN}	$f_{IN} = 4.43MHz$	-	14	-	pF
REFERENCE INPUT					
Bottom Reference Range, V_{RB}		1.2	1.3	1.6	V
Top Reference Range, V_{RT}		3.5	3.6	3.9	V
Reference Range, V_{REF} (V_{RT} - V_{RB})		1.9	2.3	2.7	V
Reference Current, I_{REF}		-	10	-	mA
Reference Ladder Resistance, R_{LAD}		-	240	-	Ω
R_{LADTC}		-	0.24	-	$Ω/^oC$
Bottom Offset Voltage, V_{OB}	(Note 4)	-	255	-	mV

Electrical Specifications $V_{CCA} = V_{CCD} = V_{CCO} = +5V$; $V_{RB} = 1.3V$; $V_{RT} = 3.6V$; $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
V_{OBTC}	(Note 4)	-	136	-	$\mu V/^oC$
Top Offset Voltage, V_{OT}	(Note 4)	-	-300	-	mV
V_{OTTC}	(Note 4)	-	480	-	$\mu V/^oC$
DIGITAL OUTPUTS (D0 to D7 and O/UF Referenced to OGND)					
Logic Output Voltage Low, V_{OL}	$I_O = 1mA$	0	-	0.4	V
Logic Output Voltage High, V_{OH}	$I_O = -0.4mA$	2.7	-	V_{CCO}	V
Output Leakage Current, I_D	$0.4V < V_{OUT} < V_{CCO}$	-20	-	+20	μA
SWITCHING CHARACTERISTICS (Notes 3, 4) See Figure 9					
Sample Rate, f_{CLK}					
HI5714/8		80	-	-	MHz
HI5714/7		75	-	-	MHz
HI5714/6		60	-	-	MHz
HI5714/4		40	-	-	MHz
Clock Pulse Width High, t_{CPH}		6	-	-	ns
Clock Pulse Width Low, t_{CPL}		6	-	-	ns
ANALOG SIGNAL PROCESSING ($f_{CLK} = 40MHz$)					
Differential Gain, DG	(Notes 5, 8)	-	1.0	-	%
Differential Phase, DP	(Notes 5, 8)	-	0.05	-	degree
HARMONICS ($f_{CLK} = 75MHz$)					
Second Harmonic, H2	$f_{IN} = 4.43MHz$	-	-63	-	dB
Third Harmonic, H3	$f_{IN} = 4.43MHz$	-	-65	-	dB
Total Harmonic Distortion, THD	$f_{IN} = 4.43MHz$	-	-59	-	dB
Spurious Free Dynamic Range, SFDR	$f_{IN} = 4.43MHz$	-	62	-	dB
Analog Input Bandwidth (-3dB)		-	18	-	MHz
TRANSFER FUNCTION					
Differential Linearity Error, DNL	(Note 6)	-	± 0.4	-	LSB
Integral Linearity Error, INL	(Note 6)	-	± 0.75	-	LSB
EFFECTIVE NUMBER OF BITS					
ENOB					
HI5714/4 ($f_{CLK} = 40MHz$)	$f_{IN} = 4.43MHz$	-	7.65	-	Bits
	$f_{IN} = 7.5MHz$	-	7.5	-	Bits
HI5714/6 ($f_{CLK} = 60MHz$)	$f_{IN} = 4.43MHz$	-	7.65	-	Bits
	$f_{IN} = 7.5MHz$	-	7.5	-	Bits
HI5714/7 ($f_{CLK} = 75MHz$)	$f_{IN} = 4.43MHz$	-	7.4	-	Bits
	$f_{IN} = 7.5MHz$	-	7.15	-	Bits
	$f_{IN} = 10MHz$	-	6.8	-	Bits

Electrical Specifications $V_{CCA} = V_{CCD} = V_{CCO} = +5V$; $V_{RB} = 1.3V$; $V_{RT} = 3.6V$; $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
HI5714/8 (f_{CLK} = 80MHz)	f_{IN} = 4.43MHz	-	7.3	-	Bits
	f_{IN} = 7.5MHz	-	7.0	-	Bits
	f_{IN} = 10MHz	-	6.64	-	Bits
Bit Error Rate, BER	(Note 7)	-	10^{-11}	-	Times/ Sample
TIMING (f_{CLK} = 75MHz) See Figures 1, 2					
Sampling Delay, t_{SD}		-	-	2	ns
Output Hold Time, t_{HD}		5	-	-	ns
Output Delay Time, t_D	HI5714/4/6/7	-	10	13	ns
Output Delay Time, t_D	HI5714/8	-	10	12.25	ns
Output Enable Delay, t_{PZH}	Enable to High	-	14.6	-	ns
Output Enable Delay, t_{PZL}	Enable to Low	-	17.8	-	ns
Output Disable Delay, t_{PHZ}	Disable from High	-	5.3	-	ns
Output Disable Delay, t_{PLZ}	Disable from Low	-	6.7	-	ns
Aperture Jitter, t_{AJ}		-	50	-	ps
POWER SUPPLY CHARACTERISTICS					
Analog Power Supply Range, V_{CCA}		4.75	5.0	5.25	V
Digital Power Supply Range, V_{CCD}		4.75	5.0	5.25	V
Output Power Supply Range, V_{CCO}		4.75	5.0	5.25	V
Total Supply Current		-	65	75	mA
Supply Current, I_{CCA}		-	30	-	mA
Supply Current, I_{CCD}		-	26	-	mA
Supply Current, I_{CCO}		-	9	-	mA
Power Dissipation		-	325	375	mW

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. The supply voltages V_{CCA} and V_{CCD} may have any value between -0.3V and +6V as long as the difference V_{CCA} - V_{CCD} lies between -0.3V and +0.3V.
3. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock not be less than 1ns.
4. Analog input voltages producing code 00 up to and including FF.

   V_{OB} (Bottom Offset Voltage) is the difference between the analog input which produces data equal to 00 and the Bottom Reference Voltage (V_{RB}).

   V_{OBTC} (Bottom Offset Voltage Temperature Coefficient) is the variation of V_{OB} with temperature.

   V_{OT} (Top Offset Voltage) is the difference between the Top Reference Voltage (V_{RT}) and the analog input which produces data output equal to FF.

   V_{OTTC} (Top Offset Voltage Temperature Coefficient) is the variation of V_{OT} with temperature.
5. Input is standard 5 step video test signal. A 12-bit R reconstruct DAC and VM700 are used for measurement.
6. Full scale sinewave, f_{IN} = 4.43MHz.
7. f_{CLK} = 75MHz, f_{IN} = 4.43MHz, V_{IN} = $\pm$8 LSB at code 128, 50% Clock duty cycle.
8. Parameter is guaranteed by design, not production tested.