HARRIS SEMICONDUCTOR

CA3252

March 1998

Quad Gated Non-Inverting Power Driver

Features

- Four 600mA Non-Inverting Power Output Drivers
- 50V and 1A Maximum Rated Power Output Drivers
- $V_{CE(SUS)}$ Capability 35V
- Inputs Compatible With TTL or 5V CMOS Logic
- Suitable For Resistive, Lamp or Inductive Loads
- Inductive Clamps on Each Output
- High Dissipation Power-Frame Package
- Operating Temperature Ranges . . . . . -40°C to 105°C

Applications

- Solenoids
- Relays
- Lamps
- Steppers
- Small Motors
- Displays

System Applications

- Automotive
- Appliances
- Industrial Controls
- Robotics

Description

The CA3252 is used to interface low-level logic to high current loads. Each Power Driver has four inverting switches consisting of an inverting logic input stage and an inverting low-side driver output stage. All inputs are 5V TTL/CMOS logic compatible and have a common Enable input. On-chip steering diodes are connected from each output (in pairs) to the CLAMP pins (in pairs) which may be used in conjunction with external zener diodes to protect the IC against over-voltage transients that result from inductive load switching. The CA3252 may be used in a variety of automotive and industrial control applications to drive relays, solenoids, lamps and small motors.

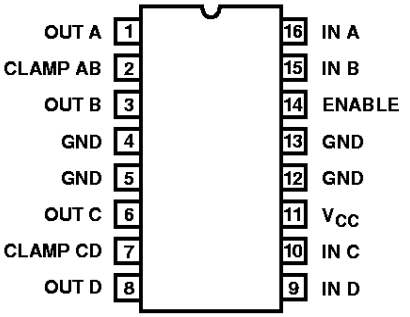
To allow for maximum heat transfer from the chip, all ground pins on the DIP and SOIC packages are directly connected to the mounting pad of the chip. Integral heat spreading lead frames directly connect the bond pad and ground leads for good heat dissipation. In a typical application, the package is mounted on a copper PC Board. By increasing copper ground area on the PC Board, more heat is conducted away from the ground leads. The junction-to-ambient thermal resistances may be reduced to less than 40°C/W with approximately two square inches of copper area.

Ordering Information

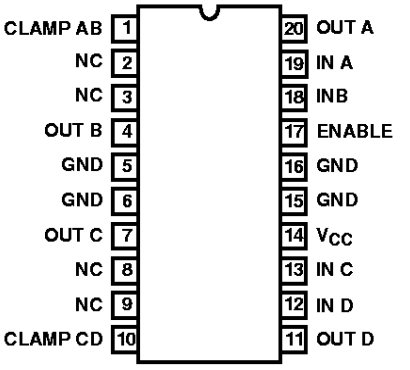
PART NUMBER	TEMP. (°C)	PACKAGE	PKG. NO.
CA3252E	-40 to 105	16 Ld PDIP	E16.3
CA3252M	-40 to 105	20 Ld SOIC	M20.3

Pinouts

CA3252E
(PDIP)
TOP VIEW



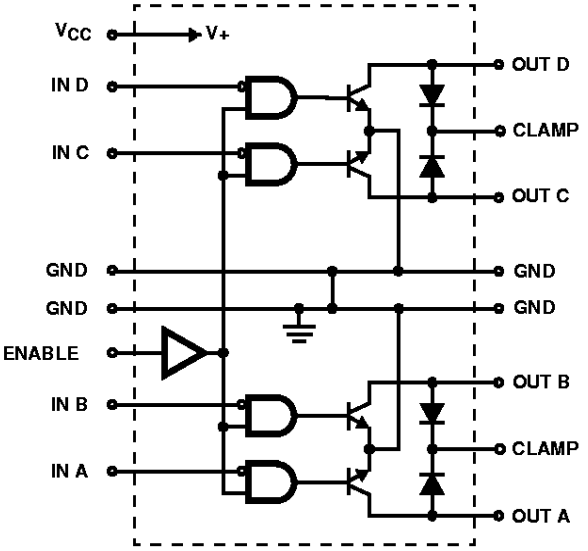
CA3252M
(SOIC)
TOP VIEW

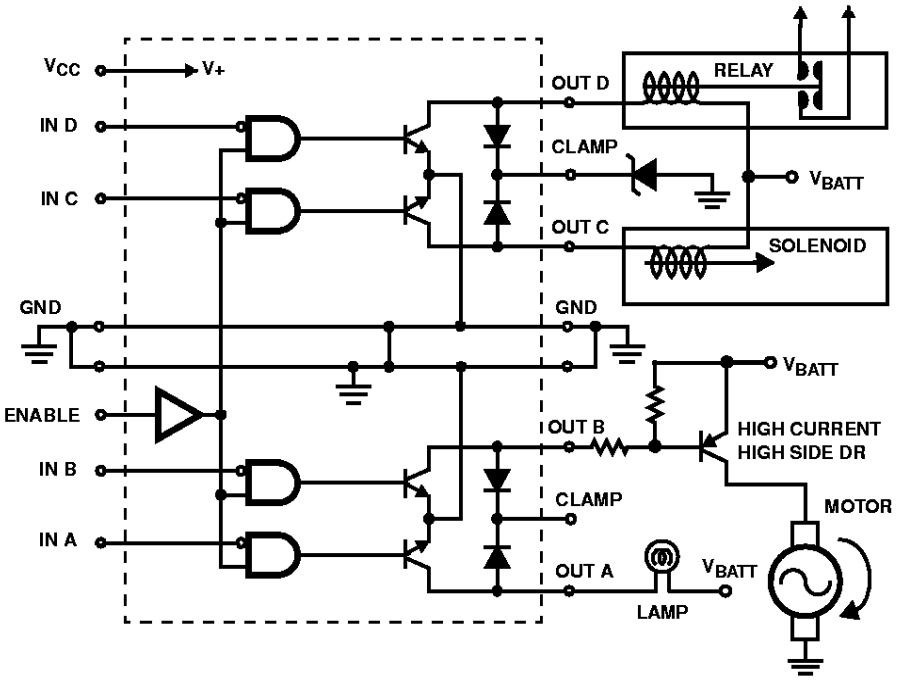


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1542.2**

Functional Block Diagram





TRUTH TABLE (Each Output)

ENABLE	IN	OUT
H	L	L
H	H	H
L	X	H

H = High, L = Low, X = Don't Care

FIGURE 1. CA3252 QUAD NON-INVERTING POWER DRIVER SHOWN WITH TYPICAL APPLICATION LOADS

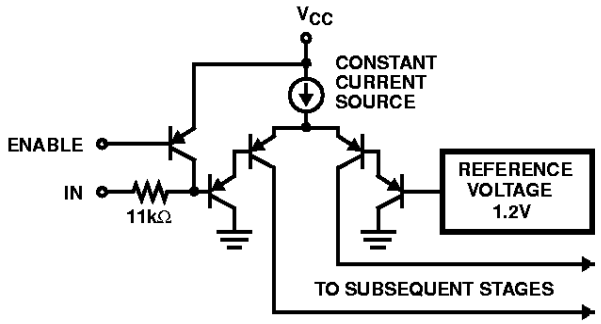


FIGURE 2. SCHEMATIC OF ONE INPUT SECTION

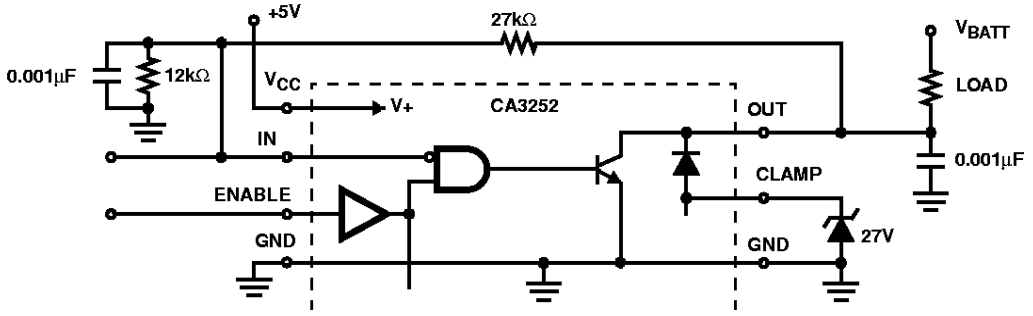


FIGURE 3. TYPICAL LATCHED ON CIRCUIT SWITCHING CONFIGURATION. WHEN V_{IN} IS SWITCHED LOW, THE OUTPUT IS TURNED ON (LOW).

Absolute Maximum Ratings

Output Voltage, V_{CEX} . . . . . -0.7 to 50V_{DC}
Logic Supply Voltage, V_{CC} 7V
Logic Input Voltage, V_{IN} . . . . . -0.7 to 15V
Output Sustaining Voltage, $V_{CE(SUS)}$ . . . . . 35V_{DC}
Output Current, I_O (Note 1) . . . . . 1A_{DC}

Operating Conditions

Temperature Range . . . . . -40°C to 105°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} °C/W
CA3252E	45
CA3252M	54

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature Soldering (10s Max) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The Maximum Ambient Temperature is limited for the sustained conditions of the $I_{CC(ON)}$ Supply Current test with all Outputs ON. The total DC current for the CA3252 with all 4 outputs ON should not exceed 0.7A at each output for a total of (4 X 0.7A + Max. I_{CC}) ~ 2.9A. This level of sustained current will significantly increase the on-chip temperature due to increased dissipation. Under any condition, the Absolute Maximum Junction Temperature must not exceed150°C. While any one loaded output may exceed 0.7A, the maximum rating limit is 1A.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = -40°C to 105°C, V_{CC} = V_{EN} = 5V; Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Output Sustaining Voltage	$V_{CE(SUS)}$	I_C = 100mA, V_{IN} = 2V, V_{EN} = 2V	35	-	V
Output Leakage Current	I_{CEX}	V_{CE} = 50V, V_{IN} = 2V, V_{EN} = 0.8V	-	100	µA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100mA, V_{IN} = 0.8V	-	0.3	V
		I_C = 300mA, V_{IN} = 0.8V	-	0.5	V
		I_C = 600mA, V_{IN} = 0.8V	-	0.8	V
Input Low Voltage	V_{IL}		-	0.8	V
Input Low Current	I_{IL}	V_{IN} = 0.4V	-15	10	µA
Input High Voltage	V_{IH}	I_C = 600mA	2	-	V
Input High Current	I_{IH}	I_C = 600mA, V_{IN} = 4.5V	-10	-10	µA
Logic Supply Current, All Outputs ON	$I_{CC(ON)}$	I_C = 600mA, All Outputs ON (Note 1)	-	90	mA
Logic Supply Current, All Outputs OFF	$I_{CC(OFF)}$	All Outputs OFF	-	10	mA
Clamp Diode Leakage Current	I_R	V_R = 50V (Diode Reverse Voltage)	-	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 0.6A	-	1.8	V
		I_F = 1.2A	-	2.0	V
Output Current	I_{OUT}	V_{IN} = 0.4V, V_{BATT} = +13V, Output Load = 10Ω	0.9	-	A
Turn-ON Propagation Delay Time	t_{PHL}	I_C = 600mA	-	10	µs
Turn-OFF Propagation Delay Time	t_{PLH}	I_C = 600mA	-	10	µs
Low Enable Voltage	V_{ENL}		-	0.8	V
Low Enable Current	I_{ENL}	V_{EN} = 0.4V	-15	10	µA
High Enable Voltage	V_{ENH}		2.0	-	V
High Enable Current	I_{ENH}	$V_{EN} \geq 2V$	-250	+250	µA