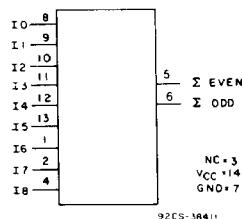


CD54AC280/3A
CD54ACT280/3A

9-Bit Odd/Even Parity Generator/Checker

The RCA CD54AC280/3A and CD54ACT280/3A are 9-bit odd/even parity generator/checkers that utilize the new RCA ADVANCED CMOS LOGIC technology. Both even and odd parity outputs are available for checking or generating parity for words up to nine bits long. Even parity is indicated (ΣE output is HIGH) when an even number of data inputs is HIGH. Odd parity is indicated (ΣO output is HIGH) when an odd number of data inputs is HIGH. Parity checking for words larger than nine bits can be accomplished by tying the ΣE output to any output of an additional AC/ACT280 parity checker.

The CD54AC280/3A and CD54ACT280/3A are supplied in 14-lead dual-in-line ceramic packages (F suffix).



Package Specifications

See Section 11, Fig. 10

FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

6

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

| CHARACTERISTICS | TEST CONDITIONS | | V_{CC} (V) | AMBIENT TEMPERATURE (T_A) - °C | | | | UNITS | |
|--------------------------------|-----------------|-----------------|--------------|------------------------------------|------|-------------|------|-------|---------|
| | | | | +25 | | -55 to +125 | | | |
| | | | | MIN. | MAX. | MIN. | MAX. | | |
| Quiescent Supply Current (MSI) | I_{CC} | V_{CC} or GND | 0 | 5.5 | — | 8• | — | 160• | μA |

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

| INPUT | UNIT LOAD* |
|-------|------------|
| All | 1.43 |

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

| Static | STATIC BURN-IN I | | | STATIC BURN-IN II | | |
|---------------|------------------|------------|-------------------|-------------------|------------|---------------|
| | OPEN | GROUND | V_{CC} (6V) | OPEN | GROUND | V_{CC} (6V) |
| CD54AC/ACT280 | 3,5,6 | 1,2,4,7-13 | 14 | 3,5,6 | 7 | 1,2,4,8-14 |
| Dynamic | OPEN | GROUND | $1/2 V_{CC}$ (3V) | V_{CC} (6V) | OSCILLATOR | |
| CD54AC/ACT280 | 3 | 7 | 5,6 | 14 | 50 kHz | 25 kHz |
| | | | | | 1,2,4,8-13 | — |

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54AC280/3A CD54ACT280/3A

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Limits with black dots (•) are tested 100%.)

| CHARACTERISTICS | SYMBOL | V_{CC} (V) | -55 to +125° C | | UNITS |
|--|------------|-----------------|----------------|------|-------|
| | | | MIN. | MAX. | |
| Propagation Delays: Any Input to ΣO | t_{PLH} | 1.5 | — | 263 | ns |
| | t_{PHL} | 3.3* | 8.7 | 29 | |
| | | 5† | 6.3 | 21• | |
| Any Input to ΣE | t_{PLH} | 1.5 | — | 250 | ns |
| | t_{PHL} | 3.3 | 8.4 | 28 | |
| | | 5 | 6 | 20• | |
| Power Dissipation Capacitance | $C_{PD}\S$ | — | 115 Typ. | | pF |
| Input Capacitance | C_I | — | — | 10 | pF |

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Limits with black dots (•) are tested 100%.)

| CHARACTERISTICS | SYMBOL | V_{CC} (V) | -55 to +125° C | | UNITS |
|--|------------|-----------------|----------------|-------|-------|
| | | | MIN. | MAX. | |
| Propagation Delays: Any Input to ΣO | t_{PLH} | 5† | 6.5 | 21.6• | ns |
| | t_{PHL} | | | | |
| Any Input to ΣE | t_{PLH} | 5 | 6.5 | 21.6• | ns |
| | t_{PHL} | | | | |
| Power Dissipation Capacitance | $C_{PD}\S$ | — | 115 Typ. | | pF |
| Input Capacitance | C_I | — | — | 10 | pF |

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§ C_{PD} is used to determine the dynamic power consumption per package.

For AC, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
 C_L = output load capacitance
 V_{CC} = supply voltage