# RTS5411T

## USB3.2 Gen1x1 Super-Speed USB HUB Controller DATASHEET

**Doc Rev. 0.99**
**13. Oct. 2021**

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## Revision History

| Revision | Description | Page | Date |
|---|---|---|---|
| 0.99 | First release | | 2021/10/13 |
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# 1. General Description

RTS5411T is an advanced USB3.2 Gen1x1 4-port HUB controller, which integrates USB3.2 Gen1x1 and USB2.0 Transceivers, MCU, SIE, regulator and charger circuits into a single chip. That could dramatically reduce the system BOM cost. With high compatibility, RTS5411T is fully backward compatible to USB2.0 and USB1.1 specification which can be operated in Super-Speed Usb, High-Speed, Full-Speed and Low-Speed.

RTS5411T provides the battery charging function for each downstream port. Besides complies with USB Battery Charging specification rev1.2, RTS5411T also provides charging function for various portable devices. Not only downstream ports can be used as charger, RTS5411T's upstream port also supports two special functions regarding the BC1.2 specification. The first one charger function of RTS5411T's upstream port is called "ACA-dock" mode. When a device which complies with ACA-dock of the BC1.2 specification is put into an ACA-Dock, it would act as a host to various USB peripherals, such as a hub, keyboard, mouse, printer, etc. However, while in ACA-dock, the device should also be able to charge at the same time. The second charger function of the RTS5411T's upstream port is called "charger detection" function. RTS5411T can recognize the BC1.2 charger mode which attached to the upstream port, including CDP, DCP and SDP. RTS5411T supports an auto detection-switch mechanism to charge portable device in suitable mode.

RTS5411T can update its firmware with an external SPI flash through flexible ISP channel. With the ISP function, it can configure lots of features and settings by the external SPI flash. The ISP function is easy to complete with just one USB cable and RTS5411T's download tool.

The features and settings of RTS5411T can also configure by the SMBUS interface.

RTS5411T has various interfaces to communicate with other components, such as GPIO, I2C, SMBUS. It's flexible for extending varieties of applications by using these interfaces.

Moreover, RTS5411T supports a special power saving function named delink mode.

It can save more power for the system when there is no device connected to the hub even though the upstream port of the RTS5411T is attached to the downstream port of the behind host or hub.

## 2. Features

■ Compliant with Universal Serial Bus 3.2 Specification Revision 1.0

- 4 downstream ports for Super-Speed Usb, high-speed, full-speed and low-speed traffic.

- Backward compatible with USB specification Revision 2.0, 1.1 and 1.0.

■ MTT(Multiple Transaction Translator)

- One TT for each downstream port.

- Better data throughput when multiple downstream ports act on FS concurrently.

■ Support SMBUS to customize configurations

- SMBUS address is configurable by external SPI Flash.

■ Support I2C to configure other chips on the same platform.

■ Compliant with USB Battery Charging Specification Revision 1.2 and other portable devices

- DCP Mode of BC 1.2.

- CDP Mode of BC 1.2.

- ACA-Dock functions of BC 1.2.

- Charger detection functions for upstream port's charger which complies with BC1.2.

- D+/D– Divider Modes 2.0V/2.7V, 2.7/2.0V and 2.7/2.7V.

- D+/D- 1.1V Mode.

■ The Up Stream Port of the RTS5411T can detect the DSP it is connected to is a SDP, CDP, or DCP. When the RTS5411T is connected to a charging port, it is allowed to draw more current from the DSP.

■ Support Gang mode and Individual mode for downstream port.

■ Support USB2.0 LPM-L1 function

■ Support USB3.2 Gen1x1 U1/U2/U3 power saving mode

■ Integrated Fast 8051 microprocessor

■ Support one HID device

■ Support one BillBoard device

■ Support Pending HP timer, PM timers, U1/U2/LFPS exit latency which are defined in the USB3.2 spec.

■ Support 12MHz Crystal clock

■ Integrated 3.3V output LDO inside, the input range supports from 4.5V to 5.5V

■ Integrated 1.1V output switching regulator, the input range supports from 3.1V to 5.5V.

■ Support LED control function of indicating Downstream Ports transfer activity and over-current

condition.

- 76-pin QFN (9 x9 mm) package

- Support the "Delink" function for extreme power saving

  - If there is no any device attached to the RTS5411T's downstream ports, the RTS5411T will disconnect itself from the downstream port of the host or another hub controller for further power saving.

  The connection of the upstream port will be established automatically once there is any device attached to its downstream ports.

# 3. Block Diagram

# 4. Pin Information

## 4.1 Pin Assignment

| Left pins | | Top pins | | Right pins | | Bottom pins | |
|---|---|---|---|---|---|---|---|

Top pins (57→39): USP_DM (57), USP_DP (56), V33_OUT (55), LDO_V5_IN (54), SWR_V5_IN (53), SWR_OUT (52), SWR_GND (51), DV11 (50), DV11 (49), DV33 (48), MOSI (47), MISO (46), SCS (45), SCK (44), DSP4_PWR (43), DSP3_PWR (42), DSP2_PWR (41), DSP1_PWR (40), GPIO7 (39)

Left pins:
- AV11 (58)
- USP_SSTX- (59)
- USP_SSTX+ (60)
- GND (61)
- USP_SSRX- (62)
- USP_SSRX+ (63)
- AV11 (64)
- DSP1_SSTX+ (65)
- DSP1_SSTX- (66)
- OCP1 (67)
- DSP1_SSRX+ (68)
- DSP1_SSRX- (69)
- AV11 (70)
- DSP1_DP (71)
- DSP1_DM (72)
- DV33 (73)
- XTLI (74)
- XTLO (75)
- SPWR_DET (76)

Center:
**REALTEK**
**RTS5411T**

**LLLLLL**
**GXXXVV**

The e-pad shall be connected to reference ground

Right pins:
- GPIO6 (38)
- GPIO5 (37)
- GPIO4 (36)
- GPIO3/SDA (35)
- GPIO2/SCL (34)
- GPIO1/SMBDA (33)
- GPIO0/SMBCL (32)
- AV11 (31)
- DSP4_SSRX- (30)
- DSP4_SSRX+ (29)
- OCP4 (28)
- DSP4_SSTX- (27)
- DSP4_SSTX+ (26)
- AV11 (25)
- DSP4_DM (24)
- DSP4_DP (23)
- DV33 (22)
- DSP3_DM (21)
- DSP3_DP (20)

Bottom pins (1→19): RREF (1), BPWR_DET (2), DV11 (3), DV33 (4), DSP2_DP (5), DSP2_DM (6), AV11 (7), DSP2_SSTX+ (8), DSP2_SSTX- (9), OCP2 (10), DSP2_SSRX+ (11), DSP2_SSRX- (12), AV11 (13), DSP3_SSTX+ (14), DSP3_SSTX- (15), OCP3 (16), DSP3_SSRX+ (17), DSP3_SSRX- (18), AV11 (19)

The version number is shown in the location marked 'VV' and G means Green Package

## 4.2 Pin Descriptions

| Pin Name | Pin No. | I/O Type | Description |
|---|---|---|---|
| **Power supply** | | | |
| DV33 | 4,22,48,73 | Power | 3.3V power supply for digital circuits |
| DV11 | 3,49,50 | Power | 1.1V power supply for digital circuits |
| AV11 | 7,13,19,25,31, 58,64,70 | Power | 1.1V power supply for analog circuits |
| LDO_V5_IN | 54 | Power | 5V to 3.3V LDO input. Short this pin to DV33, when on-chip LDO is not used. |
| V33_OUT | 55 | Power | 3.3V output (from internal 5V to 3.3V Low Dropout Regulator) Short this pin to DV33, when on-chip LDO is not used. |
| SWR_V5_IN | 53 | Power | 5V to 1.1V SWR input Connect this pin to LDO_V5_IN if internal switching regulator isn't used. |
| SWR_GND | 51 | GND | Reference GND for 1.1V SWR |
| SWR_OUT | 52 | Power | 5V to 1.1V SWR output Left this pin floating if internal switching regulator isn't used. |
| GND | 61 | GND | Reference ground |
| E-PAD | - | GND | The bottom of the package has a thermal pad. The pad shall be connected to the reference ground |
| **Analog Interface** | | | |
| RREF | 1 | I | Connect an external resistor (6.2K ±1%) to the Reference GND |
| **System Clock** | | | |
| XTLI | 74 | I | 12Mhz Crystal input. |
| XTLO | 75 | O | 12Mhz Crystal output. |
| **LED Control Pins** | | | |
| GPIO0/SMBCL, GPIO2/SCL, GPIO4,GPIO6 | 32,34,36,38 | I/O | General Purpose I/O. Now used for LED application to indicate Downstream Ports transmit and receive activity. The LEDs will on when there is a device connected to the corresponding port and not in suspend. These pins have weak internal pull up resistances. Left these pins floating when unused. The GPIO0 can be configured as a SMBus clock pin The GPIO2 can be configured as a I2C clock pin |
| GPIO1/SMBDA, GPIO3/SDA, GPIO5,GPIO7 | 33,35,37,39 | I/O | General Purpose I/O. Now used for LED application to indicate Downstream Ports over-current condition. The LEDs will on when over-current condition is detected. These pins have weak internal pull up resistances. Left these pins floating when unused. The GPIO1 can be configured as a SMBus data pin The GPIO3 can be configured as a I2C data pin |

## Pin Descriptions（continued）

| Pin Name | Pin No. | I/O Type | Description |
|---|---|---|---|
| **USB Port Control Pins** | | | |
| DSP1_PWR, DSP2_PWR, DSP3_PWR, DSP4_PWR | 40,41,42,43 | O | External power switch enable pin for corresponding downstream port. Active low[1]. Left these pins floating when unused. 0: Power supply for VBUS is on. 1: Power supply for VBUS is off. |
| OCP1,OCP2, OCP3,OCP4 | 67,10,16,28 | I | Over Current Protection flag for corresponding downstream port .Active low[1]. The external pull-up resistors shall be connected to these pins. 0: Over-current condition is detected. 1: Non over-current condition is detected. |
| BPWR_DET | 2 | I | Upstream VBUS power detection pin. Active High. 0: Upstream VBUS power is absent. 1: Upstream VBUS power exists. |
| SPWR_DET | 76 | I | Self Power Detection pin. Active High. 0: Bus-power setting 1: Self-power setting |
| **SPI Interface** | | | |
| SCK | 44 | I/O | This is I/O bi-direction. Now used as clock output for Serial Flash memory |
| SCS | 45 | I/O | This is I/O bi-direction. Now used as output chip select for Serial Flash memory Upon power on reset this pin is also used for pin strap option to perform code execution from internal ROM or external SPI ROM. 0:Execute codes from internal ROM . 1:Execute codes from Serial Flash. |
| MISO | 46 | I/O | This is I/O bi-direction. Now used as data input from Serial Flash memory |
| MOSI | 47 | I/O | This is I/O bi-direction. Now used as data output to Serial Flash memory |

(1) Active low by default. It can be configured to be active high by firmware through executing external codes.

## Pin Descriptions（continued）

| Pin Name | Pin No. | I/O Type | Description |
|---|---|---|---|
| **USB3.2 GEN1X1 Interface** | | | |
| USP_SSTX+ | 60 | O | USB3.2 Gen1x1 SuperSpeed TX+ of Upstream Port |
| DSP1_SSTX+, DSP2_SSTX+, DSP3_SSTX+, DSP4_SSTX+ | 65,8,14,26 | O | USB3.2 Gen1x1 SuperSpeed TX+ of Downstream Ports |
| USP_SSTX- | 59 | O | USB3.2 Gen1x1 SuperSpeed TX- of Upstream Port |
| DSP1_SSTX-, DSP2_SSTX-, DSP3_SSTX-, DSP4_SSTX- | 66,9,15,27 | O | USB3.2 Gen1x1 SuperSpeed TX- of Downstream Ports |
| USP_SSRX+ | 63 | I | USB3.2 Gen1x1 SuperSpeed RX+ of Upstream Port |
| DSP1_SSRX+, DSP2_SSRX+, DSP3_SSRX+, DSP4_SSRX+ | 68,11,17,29 | I | USB3.2 Gen1x1 SuperSpeed RX+ of Downstream Ports |
| USP_SSRX- | 62 | I | USB3.2 Gen1x1 SuperSpeed RX- of Upstream Port |
| DSP1_SSRX-, DSP2_SSRX-, DSP3_SSRX-, DSP4_SSRX- | 69,12,18,30 | I | USB3.2 Gen1x1 SuperSpeed RX- of Downstream Ports |
| **USB2.0 Interface** | | | |
| USP_DP | 56 | I/O | USB2.0 D+ signal of Upstream Port |
| DSP1_DP, DSP2_DP, DSP3_DP, DSP4_DP | 71,5,20,23 | I/O | USB2.0 D+ signal of Downstream Ports |
| USP_DM | 57 | I/O | USB2.0 D- signal of Upstream Port |
| DSP1_DM, DSP2_DM, DSP3_DM, DSP4_DM | 72,6,21,24 | I/O | USB2.0 D- signal of Downstream Ports |

## 4.3 Buffer list

**5V input buffer with internal 10K pull-up resistor**

OCP[4:1] [2]

**Open drain output buffer**

DSP_PWR [4:1] [1]

**3.3V bi-directional buffer**

SCK.SCS, MISO, MOSI

**3.3V bi-directional buffer with internal 200K pull-up resistor**

GPIO[7:0]

**5V input buffer**

BPWR_DET, SPWR_DET

**3.3V clock interface**

XTLI, XTLO

**USB2.0 interface**

DSP_DP [4:1], USP_DP, DSP_DM [4:1], USP_DM

**USB3.2 GEN1X1 interface**

DSP_SSTX+[4:1], DSP_SSTX- [4:1], DSP_SSRX+[4:1], DSP_SSRX-[4:1],

USP_SSTX+,USP_SSTX-,USP_SSRX+, USP_SSRX-

**LDO interface**

LDO_V5_IN, V33_OUT

**Switching Regulator interface**

SWR_V5_IN, SWR_OUT

(1)    Use open drain output buffer by default when configured as active low. If configured as active high by F/W, it will use the 3.3V output buffer instead.

(2)    The pull-up resistors are only valid when the 'power switch' mode is selected.

# 5. Electrical Characteristics

## 5.1 Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Units |
|---|---|---|---|---|
| Power supply voltage | $V_{5IN}$ | | 5.5 | V |
| | $V_{AV11}, V_{DV11}$ | | -0.2 to 1.3 | V |
| | $V_{DV33}$ | | -0.5 to 4.1 | V |
| Input voltage[1] | $V_I$ | 3V buffer | -0.5 to $V_{DV33}$+0.5 | V |
| | | 5V buffer Open drain buffer | -0.5 to +6 | V |
| Output voltage[2] | $V_O$ | | -0.5 to $V_{DV33}$+0.5 | V |
| Output current [3] | $I_O$ | 4mA Type [4] | 6 | mA |
| | | 8mA Type [4] | 12 | mA |
| Storage temperature | $T_{stg}$ | | -20 to +80 | °C |
| Latch up Current | | | $\pm$400 | mA |
| Electrostatic Discharge Voltage (HBM) | | | $\pm$5 | KV |
| Electrostatic Discharge Voltage (MM) | | | $\pm$200 | V |
| Electrostatic Discharge Voltage (CDM) | | | $\pm$500 | V |

(1)  This parameter indicates voltage exceeding which damage or reduced reliability will occur when power is applied to an input pin.

(2)  This Parameter indicates voltage exceeding which damage or reduced reliability will occur when power is applied to an output pin.

(3)  This parameter indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into output pin.

(4)  The output driving strength of all output is 4mA by default, which can be configured as 8mA by firmware through executing external codes.

## 5.2 Recommended Operating Ranges

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Power supply voltage | $V_{5IN}$ | | 4.45 | 5 | 5.25 | V |
| | $V_{AV11}, V_{DV11}$ | Active | | 1.1 | | V |
| | | Disconnect / Suspend | | 1.05 | | V |
| | $V_{DV33}$ | | 2.97 | 3.3 | 3.63 | V |
| Available current of 3.3V power supply for external circuits[1] | | $V_{5IN}$=5V | | | 150 | mA |
| Operating ambient temperature | $T_A$ | | 0 | | +70 | °C |
| Absolute maximum junction temperature | $T_J$ | | 0 | | +125 | °C |
| Surface Temperature of body | $T_C$ | PCB Layer:4L | 0 | | +118.2 | °C |
| | | PCB Layer:2L | 0 | | +120.7 | °C |

(1)   Load current of external circuits shouldn't exceed the max value when using on-chip LDO. It is

recommended that the external circuits are limited to SPI Flash and LEDs

## 5.3 DC Characteristics

### 5.3.1 DC Characteristics except USB differential signals

The following specifications apply when power supply voltages are within the recommended operating ranges in section 6.2.

| Parameter | Symbol | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| Input leakage current[1] | $I_I$ | 3V buffer, $V_I=V_{DV33}$ or GND | -0.5 | +0.5 | μA |
| | | 5V buffer, $V_I=V_{5IN}$ or GND | -30 | +30 | μA |
| Input High Voltage | $V_{IH}$ | 3V buffer, | 2 | | V |
| | | 5V buffer | 3.16 | | V |
| Input Low Voltage | $V_{IL}$ | 3V buffer | | 0.8 | V |
| | | 5V buffer | | 0.8 | V |
| Output High Voltage | $V_{OH}$ | | $0.9V_{DV33}$ | | V |
| Output Low Voltage | $V_{OL}$ | | | $0.1V_{DV33}$ | V |
| TRI-STATE Output Leakage Current[2] | $I_{OZ}$ | 3.3V buffer, Vo= $V_{DV33}$ or GND | -0.5 | +0.5 | μA |
| Input pin Capacitance | $C_{in}$ | | | 10 | pF |

(1)   This parameter indicates the current that flows through the input pin when power supply voltage is supplied to it.

(2)   This parameter indicates the current that flows through the output pin in tri-stated when the power supply voltage is applied to it.

### 5.3.2 USB 2.0 Interface DC Characteristics

RTS5411T conforms to DC characteristics of Universal Serial Bus 2.0 Specification. Refer to the specification for more information.

### 5.3.3 USB3.2 Gen1x1 Interface DC Characteristics

RTS5411T conforms to DC characteristics of Universal Serial Bus 3.2 Specification. Refer to the specification for more information.

## 5.4 AC Characteristics

### 5.4.1 System Clock

The following specifications apply when power supply voltages and operating temperature are within the recommended operating ranges in section 5.2.

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Clock frequency | $F_{CLK}$ | Crystal [1] | -100ppm | 12 | 100ppm | MHz |

(1)  Crystal used shall conform to the frequency ratings in the table over the temperature from 0°C to +70°C.

## 5.5 Power Consumption

The following consumption value applies upon the typical condition **without on-chip LDO and Switch Regulator operating**. The **VDD33** and **VDD11** are powered externally.

$T_A$= 25°C, VDD33($V_{DV33}$)= 3.3 V, VDD11($V_{AV11}$,$V_{DV11}$)= 1.1 V.

| Device Connection | Condition | Typical Supply Current(mA) | | Typical Power(mW) |
|---|---|---|---|---|
| | | VDD11 | VDD33 | |
| No Upstream connection | Hub is not connected to host controller. | TBD | TBD | TBD |
| Suspend | Hub is connected to host controller both with SuperSpeed and High-Speed. SuperSpeed hub goes into U3 state and USB2.0 hub goes into L2 state | TBD | TBD | TBD |
| 4 LS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Low-Speed data transfer on the four ports. | TBD | TBD | TBD |
| 4 HS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. High-Speed data transfer on the four ports. | TBD | TBD | TBD |
| 4 SS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Super-Speed Usb data transfer on the four ports.[3] | TBD | TBD | TBD |
| 2 SS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Super-Speed Usb data transfer on the two ports.[3] | TBD | TBD | TBD |
| 1 SS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Super-Speed Usb data transfer on one port.[3] | TBD | TBD | TBD |
| 4 SS/HS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Four SuperSpeed hubs are connected on all ports under SuperSpeed and High-Speed data transfer. [3] | TBD | TBD | TBD |
| 2 SS/HS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Two SuperSpeed hubs are connected on all ports under SuperSpeed and High-Speed data transfer. [3] | TBD | TBD | TBD |

(1)	Charging function is disabled, and all the GPIO pins are configured as input to avoid unexpected current consumption drawn by external circuits which connect to GPIOs.

(2)	When charging function is enabled. The VDD33 power consumption will also increase by 2mA in SS devices connection when charging function is enabled.

(3)	The SS devices under test support U1/U2 function. When the SS devices are Idle with little data transfer. The SuperSpeed hub will keep in U1/U2 power saving status most of the time.

(4)	The SS devices under test do not support U1/U2 function. So this is the worst case for SS power consumption

The following consumption value applies upon the typical condition **with on-chip LDO and Switch Regulator operating**. Only **VDD5** needs to be provided in this 5V mode.

**TA= 25°C, VDD5( V$_{5IN}$) = 5 V.**

| Device Connection | Condition | Typical Supply Current(mA) VDD5 | Typical Power(mW) |
|---|---|---|---|
| No Upstream connection | Hub is not connected to host controller. | TBD | TBD |
| Suspend | Hub is connected to host controller both with SuperSpeed and High-Speed. SuperSpeed hub goes into U3 state and USB2.0 hub goes into L2 state | TBD | TBD |
| 4 LS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Low-Speed data transfer on the four ports. | TBD | TBD |
| 4 HS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. High-Speed data transfer on the four ports. | TBD | TBD |
| 4 SS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Super-Speed Usb data transfer on the four ports.[1] | TBD | TBD |
| 2 SS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Super-Speed Usb data transfer on the two ports.[1] | TBD | TBD |
| 1 SS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Super-Speed Usb data transfer on one port.[1] | TBD | TBD |
| 4 SS/HS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Four SuperSpeed hubs are connected on all ports under SuperSpeed and High-Speed data transfer. [1] | TBD | TBD |
| 2 SS/HS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Two SuperSpeed hubs are connected on all ports under SuperSpeed and High-Speed data transfer. [3] | TBD | TBD |

(1) Charging function is disabled, and all the GPIO pins are configured as input to avoid unexpected current consumption drawn by external circuits which connect to GPIOs.

(2) When charging function is enabled. The VDD33 power consumption will also increase by 2mA in SS devices connection when charging function is enabled.

(3) The SS devices under test support U1/U2 function. When the SS devices are Idle with little data transfer. The SuperSpeed hub will keep in U1/U2 power saving status most of the time.

(4) The SS devices under test do not support U1/U2 function. So this is the worst case for SS power consumption

The following consumption value applies upon the typical condition **with on-chip Switch Regulator operating**. Only **VDD33** needs to be provided in this 3.3V mode.

**TA= 25°C, VDD33($V_{DV33}$) = 3.3 V.**

| Device Connection | Condition | Typical Supply Current(mA) VDD33 | Typical Power(mW) |
|---|---|---|---|
| No Upstream connection | Hub is not connected to host controller. | TBD | TBD |
| Suspend | Hub is connected to host controller both with SuperSpeed and High-Speed. SuperSpeed hub goes into U3 state and USB2.0 hub goes into L2 state | TBD | TBD |
| 4 LS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Low-Speed data transfer on the four ports. | TBD | TBD |
| 4 HS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. High-Speed data transfer on the four ports. | TBD | TBD |
| 4 SS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Super-Speed Usb data transfer on the four ports.[1] | TBD | TBD |
| 2 SS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Super-Speed Usb data transfer on the two ports.[1] | TBD | TBD |
| 1 SS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Super-Speed Usb data transfer on one port.[1] | TBD | TBD |
| 4 SS/HS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Four SuperSpeed hubs are connected on all ports under SuperSpeed and High-Speed data transfer. [1] | TBD | TBD |
| 2 SS/HS devices | Hub is connected to host controller both with SuperSpeed and High-Speed. Two SuperSpeed hubs are connected on all ports under SuperSpeed and High-Speed data transfer. [3] | TBD | TBD |

(1)  Charging function is disabled, and all the GPIO pins are configured as input to avoid unexpected current consumption drawn by external circuits which connect to GPIOs.

(2)  When charging function is enabled. The VDD33 power consumption will also increase by 2mA in SS devices connection when charging function is enabled.

(3)  The SS devices under test support U1/U2 function. When the SS devices are Idle with little data transfer. The SuperSpeed hub will keep in U1/U2 power saving status most of the time.

(4)  The SS devices under test do not support U1/U2 function. So this is the worst case for SS power consumption

## 5.6 Power On/Off Sequence

When the on-chip LDO and switch regulator are not used, both 1.1V and 3.3V power need to be provided externally. The power on/off sequence between 1.1V and 3.3V need to be noticed as in Figure 5-1. During power on, it is recommended that the point where both power supplies are stabilized should be no later than 50ms after the start of the 3.3V rising. During power off, the end of 1.1V falling should be no later than 350ms after the start of 3.3V falling. Meanwhile, the falling time ($0.9V_{DD}$ to $0.1V_{DD}$) of 3.3V power should be no less than 50us. During the whole process, the voltage of 3.3V power should be always above the 1.1V power.

When the 5V to 3.3V LDO is used and 1.1V power is provided externally. The power on/off sequence between 1.1V and 5V should be as the same as the sequence between 1.1V and 3.3V mentioned above.
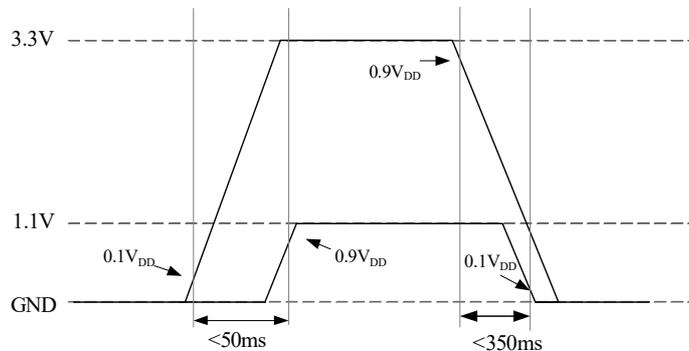


**Figure 5-1.  Power On/Off Sequence when 1.1V and 3.3V are provided externally**

When both 5V to 3.3V LDO and 5V to 1.1 switch regulator are used, only 5V power needs to be provided. During power on, the rising time of 5V should be less than 50ms. During power off, the falling time from $0.9V_{DD}$ to 2V should be less than 500ms as in Figure 5-2.

When switch regulator is operated in 3.3V to 1.1V mode, only 3.3V power needs to be provided. The rising and falling during power on/off should comply with the timing mentioned in adjacent section above.
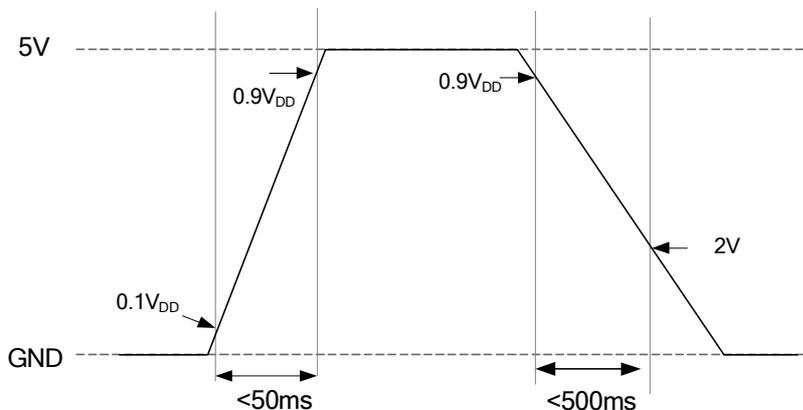


**Figure 5-2 Power On/Off Sequence in 5V only mode**

# 6. SMBus Slave Interface

The SMBus interface of RTS5411T is default disabled by firmware after power reset. To enable the SMBus, the external SPI flash is required.

## 6.1 Pull-Up Resistor for SMBus

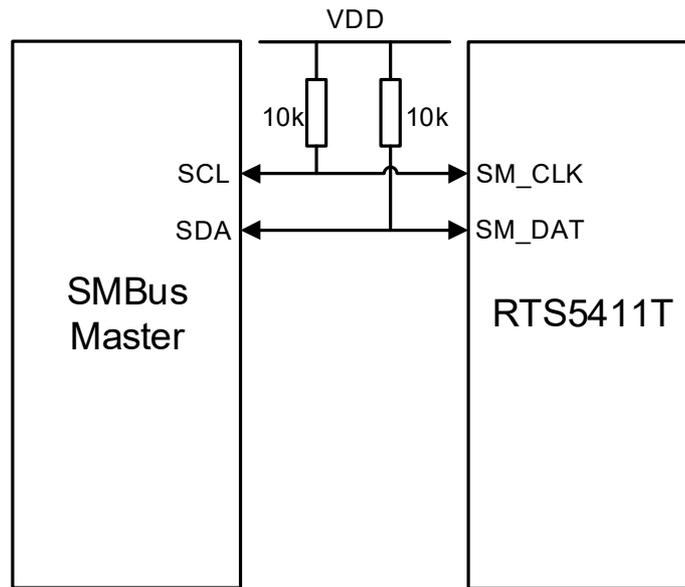External pull-up resistors (10 kΩ recommended) are required on the SM_DAT and SM_CLK pins when implementing SMBus.
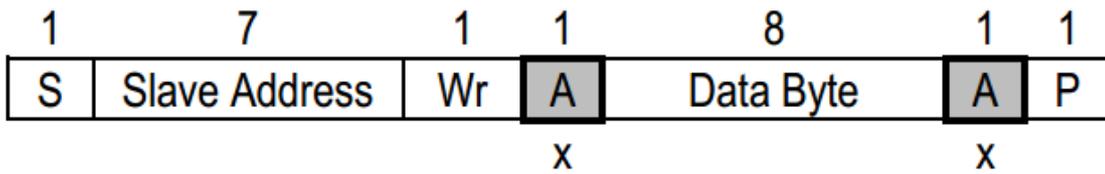


**Figure 6-1.  SMBus Slave Connection**

## 6.2 SMBus Bus Protocol

There are three **Bus Protocols** (defined in *SMBus Specification Revision 1.0*) supported by the SMBus interface of RTS5411T：

- Receive Byte
- Block Write
- Block Read

These bus protocols are shown in Figure 6-3, Figure 6-4 and Figure 6-5. The shading shown in the figures during a read or write indicates the hub is driving data on the SM_DAT line; otherwise, host data is on the SM_DAT line. Not all protocol elements will be present in every command. For instance, not all packets are required to include the Packet Error Code.

**Note**: Data bytes are transferred MSB first.

| 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Data Byte | A | P |
|   |   |   | x |   | x |   |

| | | |
|---|---|---|
| S | Start Condition | |
| Sr | Repeated Start Condition | |
| Rd | Read (bit value of 1) | |
| Wr | Write (bit value of 0) | |
| x | Shown under a field indicates that that field is required to have the value of 'x' | |
| A | Acknowledge (this bit position may be '0' for an ACK or '1' for a NACK) | |
| P | Stop Condition | |
| PEC | Packet Error Code | |
| ☐ | Master-to-Slave | |
| ▨ | Slave-to-Master | |
| ... | Continuation of protocol | |

**Figure 6-2.  SMBus Bus Protocol**

## 6.2.1 Receive Byte

The *Receive Byte* is similar to a Send Byte, the only difference being the direction of data transfer. A simple device may have information that the host needs. It can do so with the Receive Byte protocol. The same device may accept both Send Byte and Receive Byte protocols. A NACK (a '1' in the ACK bit position) signifies the end of a read transfer.
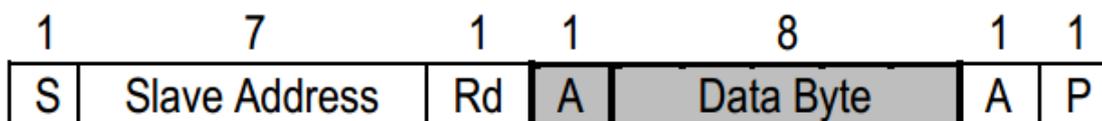
| 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| S | Slave Address | Rd | A | Data Byte | A | P |

**Figure 6-3.  Receive Byte**

## 6.2.2 Block Write/Block Read

The **Block Write** begins with a slave address followed by a write bit, which is sent by I2C master. After the command code following the slave address, the I2C master sent a byte count which describes how many bytes will be transmitted later. For example, there are 20 bytes to be send by I2C master, the byte count field should be set as 20 (14h) which followed by the 20-byte data. The byte count does not include the PEC byte. The byte count may not set as zero. A Block Read or Block Write is allowed to transfer **a maximum of 32 data bytes**.
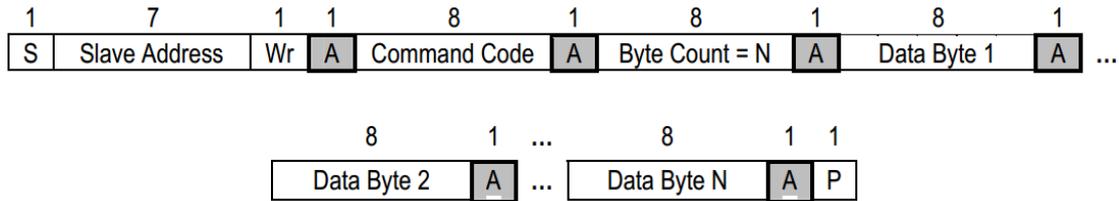
| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | |
|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | Byte Count = N | A | Data Byte 1 | A | ... |

| 8 | 1 | ... | 8 | 1 | 1 |
|---|---|---|---|---|---|
| Data Byte 2 | A | ... | Data Byte N | A | P |

**Figure 6-4.  Block Write**

A **Block Read** differs from Block Write in that the repeated START condition exists to satisfy the requirement for a change in the transfer direction. A NACK immediately preceding the STOP condition signifies the end of the read transfer.
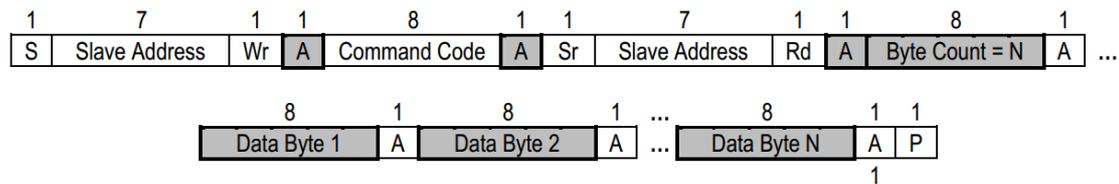
| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | Sr | Slave Address | Rd | A | Byte Count = N | A | ... |

| 8 | 1 | 8 | 1 | ... | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|
| Data Byte 1 | A | Data Byte 2 | A | ... | Data Byte N | A | P |
| | | | | | | | 1 |

**Figure 6-5.  Block Read**

## 6.3 SMBus Transfer Protocol

There are three Transfer Protocols supported by the SMBus interface of the RTS5411T：

- Get Device Status
- Block-out Transfer
- Block-in Transfer

### 6.3.1 Slave Address

The SMBus slave address of RTS5411T is default set to be 1101010b.

The value of slave address should be written to SLAVE_ADDR register when the initialization process of the firmware, then HW will automatically compare it with the received slave address.

### 6.3.2 Get Device Status

A **Get Device Status** is implemented by **Receive Byte**, which is used by the master to polling the transfer status for the addressed device
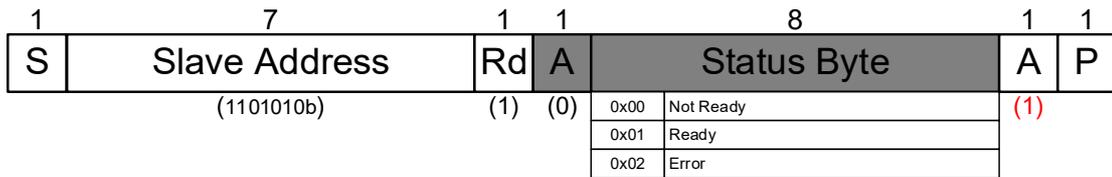
**Figure 6-6.  Get Device Status**

## 6.3.3 Block-out Transfer

A *Block-out Transfer* is implemented by *Block Write* and *Receive Byte*, which is used by the master to send a block data. The maximum transfer size is 32-byte.
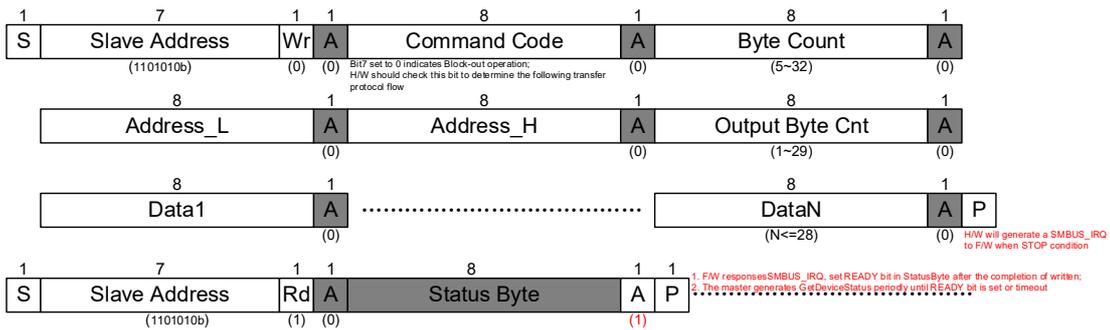


**Figure 6-7.  Block-out Transfer**

## 6.3.4 Block-in Transfer

A *Block-in Transfer* is implemented by Block Write, Block Read and Receive Byte, which is used by the master to receive a block data. The maximum transfer size is 32-byte.
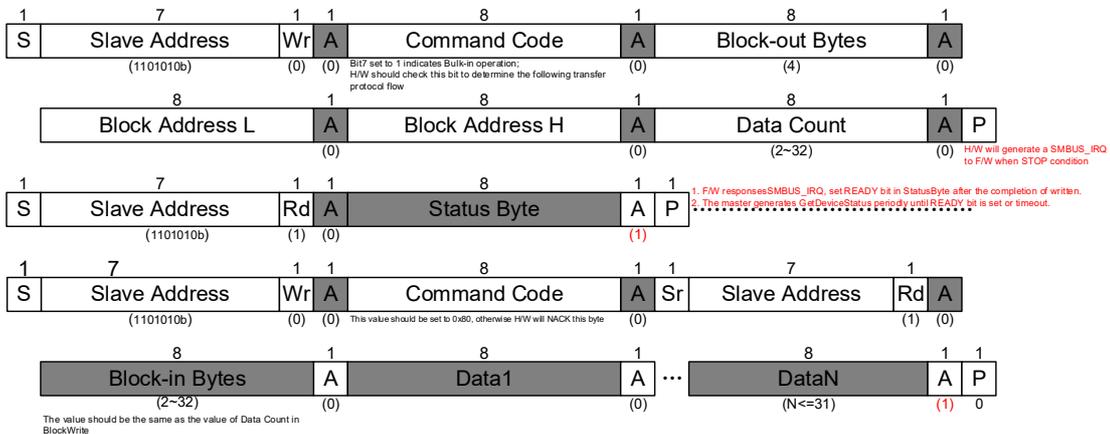


**Figure 6-8.  Block-in Transfer**

## 6.3.5 Invalid Protocol Response Behavior

The only valid protocols are Get Device Status, Bulk-out Transfer and Bulk-in Transfer (described above), where RTS5411T only responds to the 7-bit firmware configured slave addresses (1101010b). Any invalid protocol will result ERROR bit set in Status Byte, which indicates that an error has happened.

## 6.4 Bus Reset Sequence

The SMBus slave interface resets and returns to the idle state upon a START condition followed immediately by a STOP condition.

## 6.5 SMBus Timing

The SMBus slave interface complies with the *SMBus Specification Revision 1.0*. See Section 2.1, *AC Specifications* on page 3 for more information.
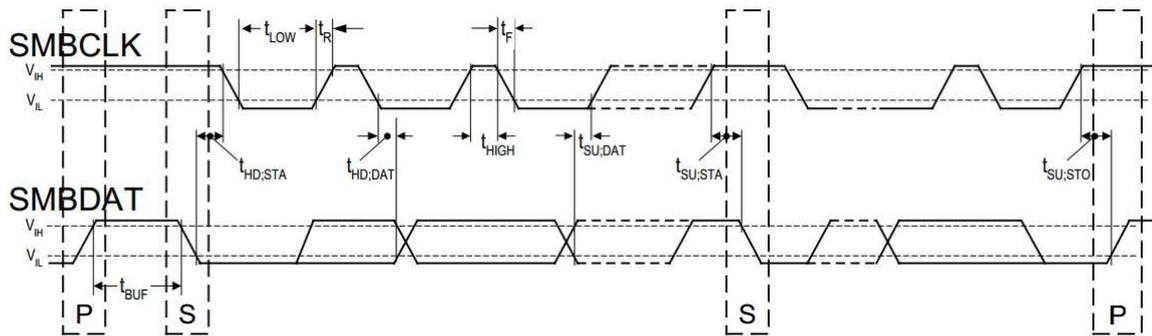


**Figure 6-9.  SMBus Slave Time Diagram**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $F_{SMB}$ | SMBus Operating Frequency | 10 | 100 | kHz |
| $F_{BUF}$ | Bus free time between Stop and Start Condition | 4.7 | - | μs |
| $T_{HD:STA}$ | Hold time after (Repeated) Start Condition. After this period, the first clock is generated. | 4.0 | - | μs |
| $T_{SU:STA}$ | Repeated Start Condition setup time | 4.7 | - | μs |
| $T_{SU:STO}$ | Stop Condition setup time | 4.0 | - | μs |
| $T_{HD:DAT}$ | Data hold time | 300 | - | ns |
| $T_{SU:DAT}$ | Data setup time | 250 | - | ns |
| $T_{TIMEOUT}$ | Detect clock low timeout | 25 | 35 | ms |
| $T_{LOW}$ | Clock low period | 4.7 | - | μs |
| $T_{HIGH}$ | Clock high period | 4.0 | 50 | μs |
| $T_{LOW:SEXT}$ | Cumulative clock low extend time (slave device) | - | 25 | ms |
| $T_{LOW:MEXT}$ | Cumulative clock low extend time (master device) | - | 10 | ms |
| $T_F$ | Clock/Data Fall Time | - | 300 | ns |
| $T_R$ | Clock/Data Rise Time | - | 1000 | ns |
| $T_{POR}$ | Time in which a device must be operational after power-on reset | | 500 | ms |

**Table 6-1. SMBus AC specifications**

# 7. I2C Master and slave interface

## 7.1 I2C Slave interface

The operation flow and date transaction format of I2C slave is similar with SMBus slave, reference SMBus Slave interface for reference.

## 7.2 I2C Master interface

### 7.2.1 Supported Mode and Speed

RTS5411T support the following three bus speed mode:

➢ Standard-mode (Sm), with a bit rate up to 100 kbit/s.

➢ Fast-mode (Fm), with a bit rate up to 400 kbit/s.

➢ Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s.

### 7.2.2 Transfer Protocol Implementation

RTS5411T support four types transfer format

➢ Write

➢ Read

➢ Read Random

➢ Send Address

**Write transfer**

Master-transmitter transmits to slave-receiver. The transfer direction is not changed as depicted in the figure below. The slave receiver acknowledges each byte.
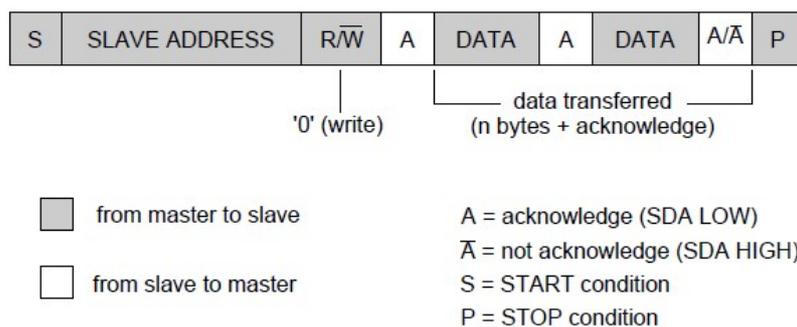


**Figure 7-1 Write transfer format**

**Read transfer**

Master reads slave immediately after first byte (see Figure below). At the moment of the first acknowledge, the master-transmitter becomes a master-receiver and the slave-receiver becomes a slave-transmitter. The first byte data is still generated by the slave, and then I2C master generates subsequent acknowledges. At the end, STOP condition is generated by the master, which sends a not-acknowledge (A) just before the STOP condition.
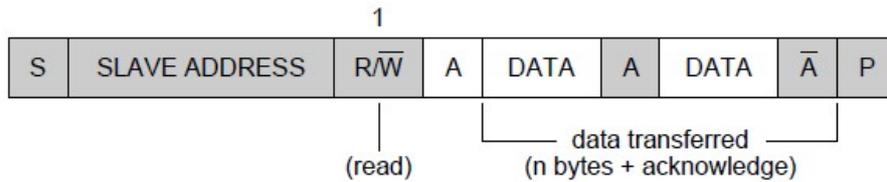
**Figure 7-2 Read transfer format**

**Read Random transfer**

Read Random transfer format initiate two START condition, one is START , the other is Start repeat (Sr), during the start and Sr the transfer direction changed. During a change of direction within a transfer, the START condition and the slave address are both repeated, but with the R/W bit reversed. As describe in the figure below ,the R/W bit after the first START is write and the data length n is 0 to 4 bytes. And the following start repeat R/W bit is read. The purpose of this format is to send command for the following Read operation.
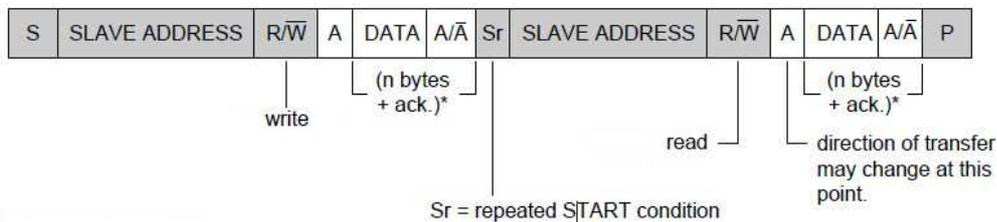


**Figure 7-3 Read Random transfer format**

**Send Address**

The Send Address transfer format is only with the slave address and without data, STOP condition following the R/W bit. This operation is used to set I2C slave device slave address.

## 7.2.3 Stretching the SCK

RTS5411T support the I2C slave stretch SCK when the slave is busy. Besides, the hub will stretch the SCK if the memory to send or receive data being full or empty.

## 7.2.4 Slave Response Timeout

The Slave Response Timeout is configurable for RTS5411T.

## 7.3 I2C Timing

The I2C-bus timing characteristics, bus-line capacitance and noise margin are given in Table7-1. Figure 7-4 shows the timing definitions for the I2C-bus.
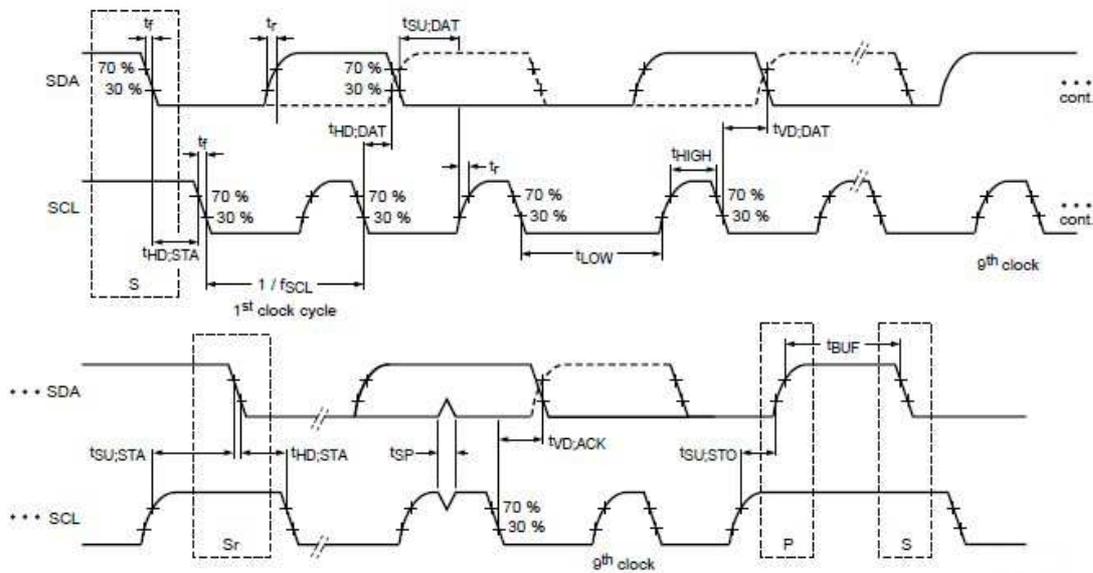
**Figure 7-4 Definition of timing on the I2C bus**

**Table 7-1 I2C Master Timing Specification**

| Symbol | Parameter | Standard-mode | | Fast-mode | | Fast-mode Plus | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| $t_{HD;STA}$ | hold time(repeated) START condition | 4.0 | - | 0.6 | - | 0.26 | - | µs |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | - | 1.3 | - | 0.5 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | 4.0 | - | 0.6 | - | 0.26 | - | µs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | 4.7 | - | 0.6 | - | 0.26 | - | µs |
| $t_{HD;DAT}$ | data hold time | 5.0 | - | - | - | - | - | µs |
| $t_{SU;DAT}$ | data set-up time | 250 | - | 100 | - | 50 | - | ns |
| $t_r$ | rise time of both SDA and SCL signals | - | 1000 | 20+0.1Cb | 300 | - | 120 | ns |
| $t_f$ | fall tome of both SDA and SCL signals | - | 300 | 20+0.1Cb | 300 | - | 120 | ns |
| $t_{SU;STO}$ | set-up tome for STOP condition | 4.0 | - | 0.6 | - | 0.26 | - | µs |
| $t_{BUF}$ | bus free time between a STOP and START condition | 4.7 | - | 1.3 | - | 0.5 | - | µs |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $C_b$ | capacitive load for each bus line | - | 400 | - | 400 | - | 550 | pF |
| $t_{VD;DAT}$ | data valid time | - | 3.45 | - | 0.9 | - | 0.45 | μs |
| $t_{VD;ACK}$ | data valid acknowledge time | - | 3.45 | - | 0.9 | - | 0.45 | μs |
| $V_{nL}$ | noise margin at LOW level | $0.1V_{DD}$ | - | $0.1V_{DD}$ | - | $0.1V_{DD}$ | - | V |
| $V_{nH}$ | noise margin at LOW level | $0.2V_{DD}$ | - | $0.2V_{DD}$ | - | $0.2V_{DD}$ | - | V |

## 8. QFN-76 Package Dimensions
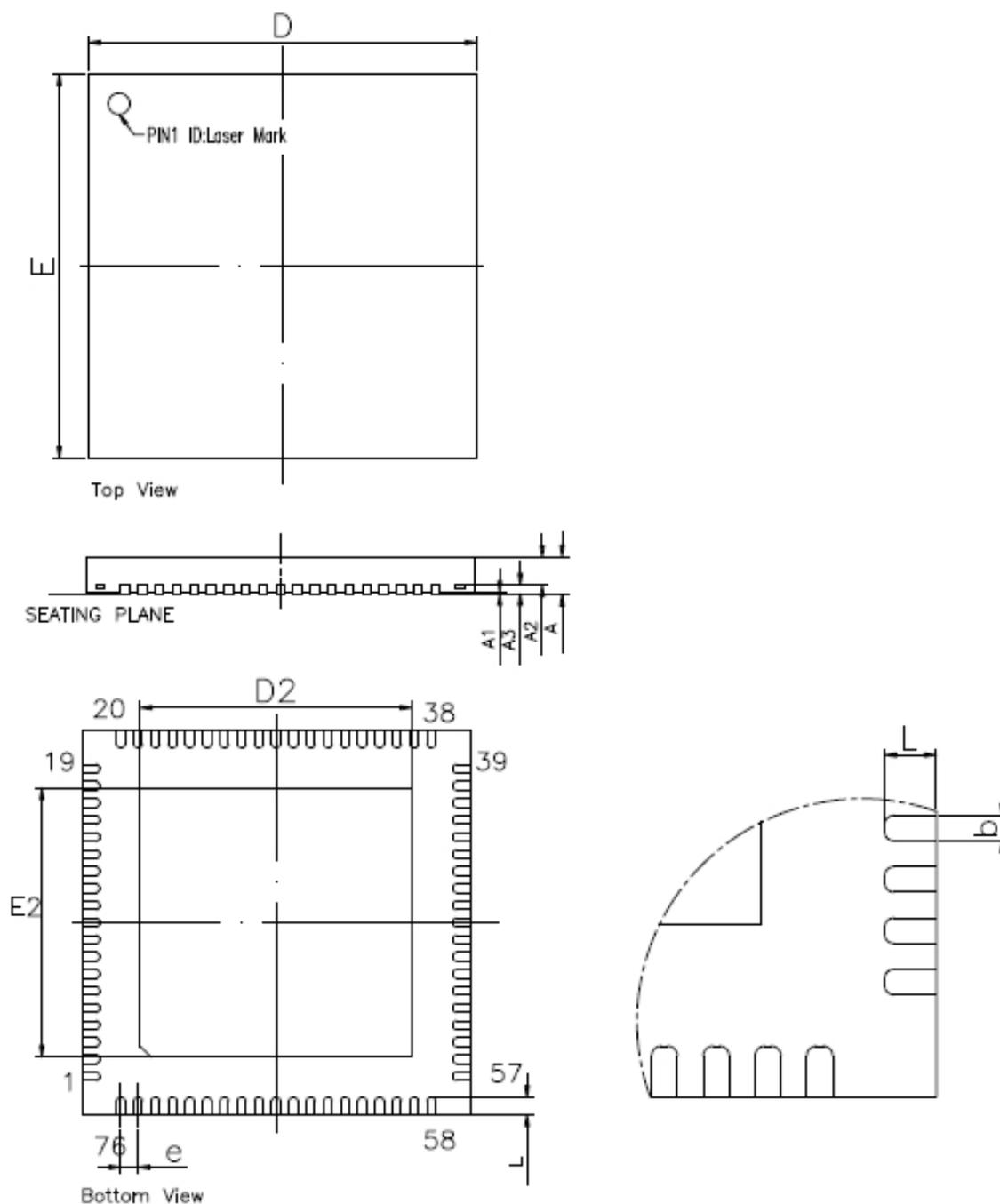
| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.80 | 0.85 | 0.90 | 0.031 | 0.033 | 0.035 |
| $A_1$ | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| $A_2$ | --- | 0.65 | 0.70 | --- | 0.026 | 0.028 |
| $A_3$ | 0.2 REF | | | 0.008 REF | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D/E | 9.00 BSC | | | 0.354 BSC | | |
| $D_2/E_2$ | 5.13 | 5.38 | 5.63 | 0.202 | 0.212 | 0.222 |
| e | 0.40 BSC | | | 0.016 BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).

2. REFERENCE DOCUMENTL：JEDEC MO-220.

3. BSC/REF tolerance +/-0.1mm

● **QFN76 pin (9x9) recommended PCB footprint dimensions**
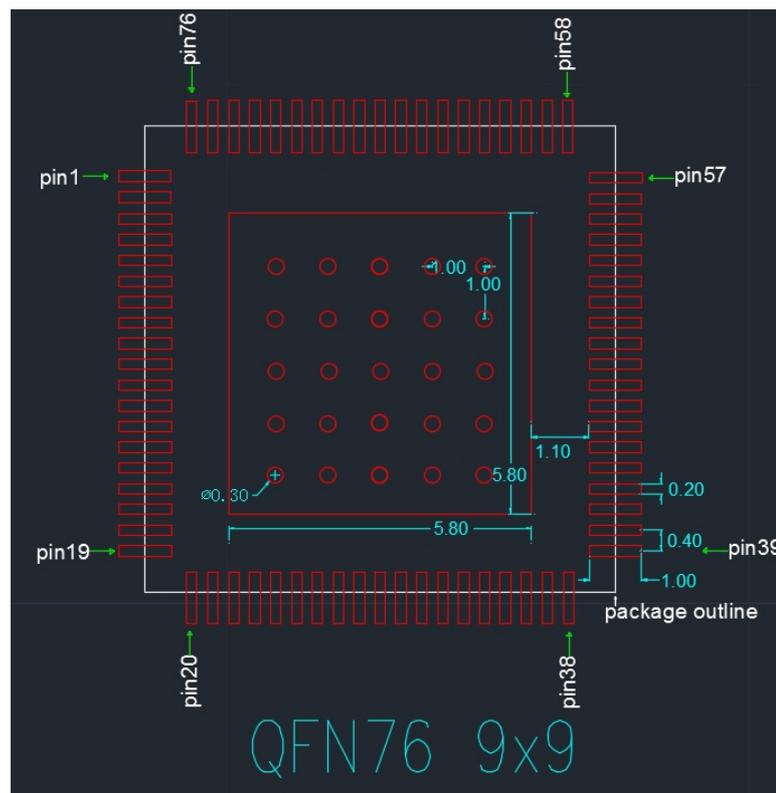


Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).

## 9. Ordering Information

| Part Number | Package | Status |
| --- | --- | --- |
| RTS5411T-GR | QFN-76 Green package | MP available |
| RTS5411T-GRT | QFN-76 Green package with Tape and Reel | MP available |