Application Note: SY58874U

Boost PFC Regulator

Preliminary Specification

General Description

SY58874U is a single-stage Boost PFC Regulator. Constant t_{ON} operation is applied to achieve high PF and no multiplier is need. Quasi-Resonant switching is applied to achieve high efficiency and better EMI performance.

Ordering Information

SY58874□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY58874UFAC	SO8	----

Features

- Integrated 520V MOSFET
- Quasi-Resonant (QR) mode to achieve low switching losses
- PF>0.95, THD<10%
- Output Over Voltage Protection
- Low BOM Cost
- RoHS Compliant and Halogen Free
- Compact Package: SO8

Applications

- Adaptors
- Pre-stage for Two-stage AC/DC Converter
- LED Lighting

Typical Applications

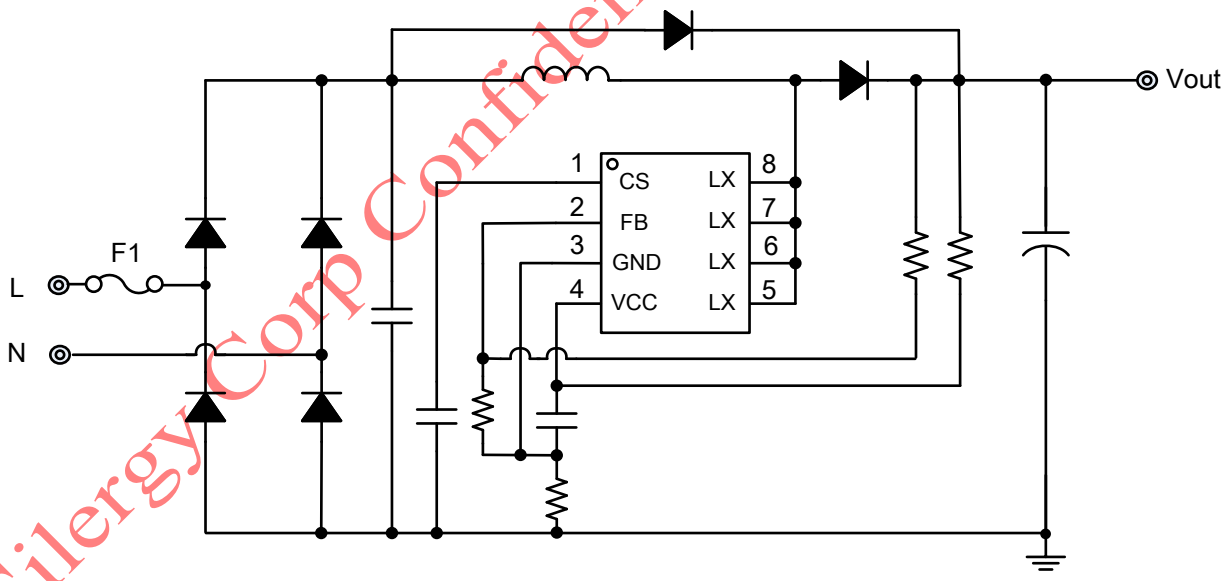
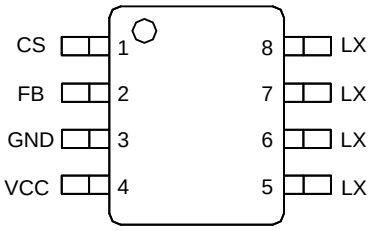


Fig.1 Schematic Diagram

Pinout (top view)



(SO8)

Top Mark: BYW*xyz*(device code: BYW, ***x=year code, y=week code, z= lot number code*)**

Pin Name	Pin number	Pin Description
CS	1	Peak current limit set pin.
FB	2	Voltage feedback pin. Connect to a resistor divider to sense output voltage.
GND	3	Ground Pin.
VCC	4	Power supply pin.
LX	5-8	Internal HV MOSFET drain pin.

Block Diagram

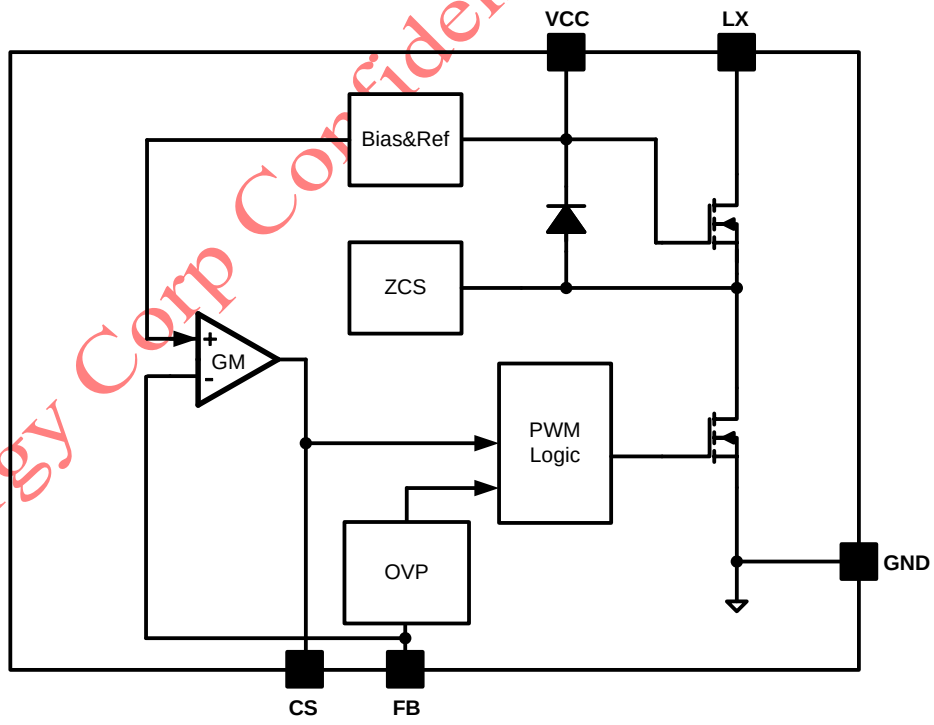


Fig.2 Simplified block diagram

Absolute Maximum Ratings (Note 1)

CS ---------- -0.3V~3.6V
FB ---------- -0.3V~16V
VCC ---------- -0.3V~20V
LX---------- 520V
Power Dissipation, @ T_A = 25°C SO8---------- 1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA}---------- 88°C/W
SO8, θ_{JC}---------- 45°C/W
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Electrical Characteristics

(V_{VCC}= 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VCC Turn-on Threshold	V_{VCC_ON}			14		V
VCC Turn-off Threshold	V_{VCC_OFF}			7.45		V
VCC Shunt Voltage	V_{VCC_SHUNT}	V_{VCC}>2mA		14.8		V
Start up Current	I_{ST}	V_{VCC}=12V		53		μA
Quiescent Current	I_Q			270		μA
CS Pin Section						
CS Limit	V_{CS_LIMIT}			530		mV
FB Pin Section						
Reference Voltage for Feedback	V_{REF}			1.225		V
Internal OVP Voltage Threshold	V_{REF_OVP}			1.4		V
Driver Section						
Min ON Time	T_{ON_MIN}			700		ns
Max ON Time	T_{ON_MAX}			20		μs
Min OFF Time	T_{OFF_MIN}			1.7		μs
Max OFF Time	T_{OFF_MAX}			50		μs
Integrated MOSFET Section						
BV of HV MOSFET	V_{BV}		520			V
Rdson of HV MOSFET	R_{DSON}			3.4		Ω
Thermal Section						
Thermal Shut Down Temperature	T_{SD}			160		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VCC pin voltage gradually higher than V_{VCC_ON} voltage then turn down to 12V.

Operation

SY58874U is a constant voltage boost PFC regulator targeting at Pre-stage for Two-stage AC/DC Converter.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at valley of drain voltage.

SY58874U provides reliable protections such as Over Voltage Protection (OVP), Over Temperature Protection (OTP), etc.

SY58874U is available with SO8 package.

Applications Information

Start up

After AC power or DC BUS is powered on, the capacitor C_{VCC} across VCC and GND pin is charged up by BUS voltage through a start up resistor R_{ST}. Once V_{VCC} rises up to V_{VCC_ON}, the internal blocks start to work. Then IC can be supplied at every switching cycle. The supply current is balanced with IC consumption current to maintain V_{VCC} above V_{VCC_OFF}.

The whole start up procedure is divided into two sections shown below. t_{STC} is the C_{VCC} charged up section, and t_{STO} is the time V_{VCC} continue rising and clamped at V_{VCC_Shunt}.

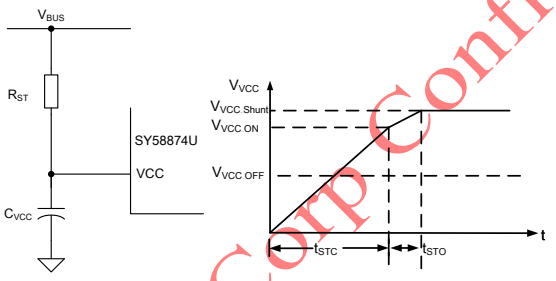


Fig.3 Start up

The start up resistor R_{ST} and C_{VCC} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST}.

$$R_{ST} < \frac{V_{BUS}}{I_{ST}}$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VCC} to obtain an ideal start up time t_{ST}.

$$C_{VCC} = \frac{\left(\frac{V_{BUS}}{R_{ST}} - I_{ST}\right) \times t_{ST}}{V_{VCC-ON}}$$

Proprietary self-bias technique allows C_{VCC} to be charged every switching cycle. There is no need to add auxiliary winding for power supply. C_{VCC} can be chosen with small value and small package to save cost.

Shut down

After AC power or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When power supply for IC is not enough, V_{VCC} will drop down. Once V_{VCC} is below V_{VCC_OFF}, the IC will stop working.

Quasi-resonant Operation

QR mode operation provides low turn-on switching losses in MOSFET.

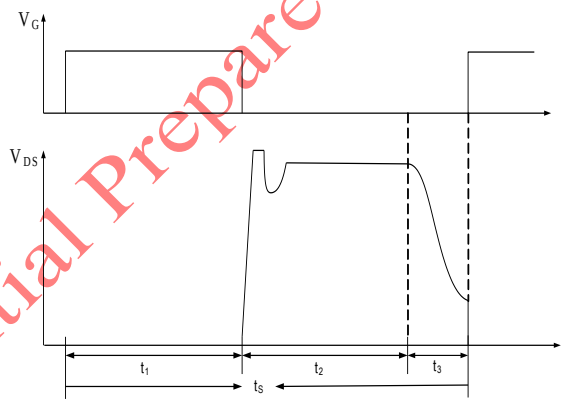


Fig.4 QR mode

When the voltage across drain and source of the MOSFET is at voltage valley, the MOSFET would be turned on.

Boost output voltage regulation

SY58874U regulates the boost output voltage using a internal transconductance error amplifier (GM). The inverting terminal of the GM is pinned out to FB, the non-inverting terminal is connected to an internal 1.225V voltage reference, and the GM output is pinned out to CS.

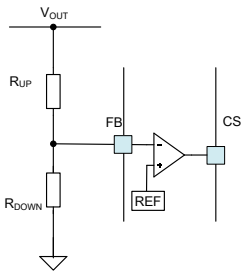


Fig.5 simplified output voltage feedback circuit

A resistor divider (R_{UP} and R_{DOWN}) scales down the boost output voltage (V_{OUT}) and connects to the FB pin. If the output voltage is less than the regulation, then the control voltage (V_{CS}) increases the on time of the driver, which increases the power transferring from the input to the output. If V_{OUT} is higher than the regulation, the V_{COMP} decreases the on time to limit the power transferring.

$$V_{OUT} = V_{REF} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}}$$

Over Voltage Protection (OVP)

Because of the extremely low bandwidth of PFC's voltage loop, there is a risk of overshoots at output side during startup, load steps, and line steps. For reliable operation, the over voltage protection (OVP) is necessary to prevent output voltage from exceeding the ratings of the PFC stage components.

SY58874U detects the over voltage condition and disables the driver until V_{OUT} decreases to a safe level, which ensures that V_{OUT} is within the PFC stage component ratings. An internal comparator connected to the FB pin provides the OVP protection.

$$V_{OUT\_OVP} = V_{REF\_OVP} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}}$$

Where V_{REF_OVP} is the Internal OVP voltage threshold.

Over Temperature Protection (OTP)

SY58874U has over temperature protection. When the junction temperature rises up over T_{SD}, the IC stops switching..

Power Device Design

MOSFET and Diode

When the operation condition is minimum voltage input and full load output, the semiconductor devices suffer the maximum current stress.

$$I_{L\_PK\_MAX} = \frac{\sqrt{2} \times 2 \times P_{OUT}}{\eta \times V_{AC\_MIN}}$$

$$I_{MOS\_PK\_MAX} = I_{D\_PK\_MAX} = I_{L\_PK\_MAX}$$

$$I_{L\_RMS\_MAX} = \frac{2 \times P_{OUT}}{\sqrt{3} \times \eta \times V_{AC\_MIN}}$$

$$I_{MOS\_RMS\_MAX} = \frac{2}{\sqrt{3}} \times \frac{P_{OUT}}{\eta \times V_{AC\_MIN}} \times \sqrt{1 - \left(\frac{\sqrt{2} \times 8 \times V_{AC\_MIN}}{3 \times \pi \times V_{OUT}}\right)}$$

$$I_{D\_RMS\_MAX} = \frac{4}{3} \times \frac{P_{OUT}}{\eta \times \sqrt{V_{AC\_MIN} \times V_{OUT}}} \times \sqrt{\frac{2 \times \sqrt{2}}{\pi}}$$

$$I_{D\_AVG} = I_{OUT} = \frac{P_{OUT}}{V_{OUT}}$$

Where $I_{L\text{-}PK\text{-}MAX}$ and $I_{L\text{-}RMS\text{-}MAX}$ are maximum inductor peak current and RMS current , P_{OUT} is the output power , V_{OUT} is the output voltage , V_{AC_MIN} is the minimum input AC voltage , η is the estimated efficiency.

Inductor (L)

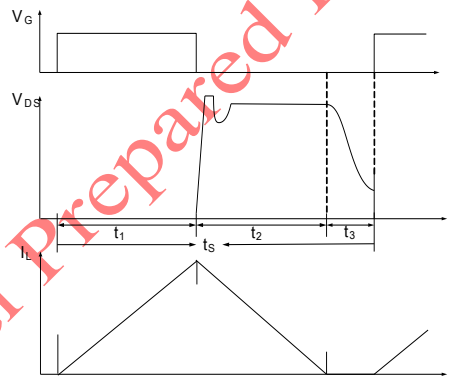


Fig.6 switching waveforms

The design flow is shown as below:

(a) Preset frequency f_S

(b) Compute relative t_S, t_1

$$t_S = \frac{1}{f_S}$$

$$t_1 = \frac{V_{OUT} - \sqrt{2} \times V_{AC}}{V_{OUT}} \times t_S$$

(c) Compute the peak current of inductor

$$I_{L\_PK} = \frac{\sqrt{2} \times 2 \times P_{OUT}}{\eta \times V_{AC}}$$

(d) Design inductance L

$$L_M = \frac{\sqrt{2} \times V_{AC\_RMS} \times t_1}{I_{L\_PK}}$$

Inductor Design (N)

Necessary parameters:	
inductance	L
CS limit	V_{CS_LIMIT}

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

$$\Delta B = 0.3 \sim 0.35T$$

(c) Compute current limit resistor R_S

$$R_S = \frac{V_{CS\_LIMIT}}{I_{L\_PK\_MAX}}$$

(d) Compute primary turn N_P

$$N = \frac{L_M \times I_{L\_PK\_MAX}}{\Delta B \times A_e}$$

(e) Select an appropriate wire diameter

With $I_{L\text{-}RMS\text{-}MAX}$ select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(f) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the inductor until the ideal inductor is achieved.

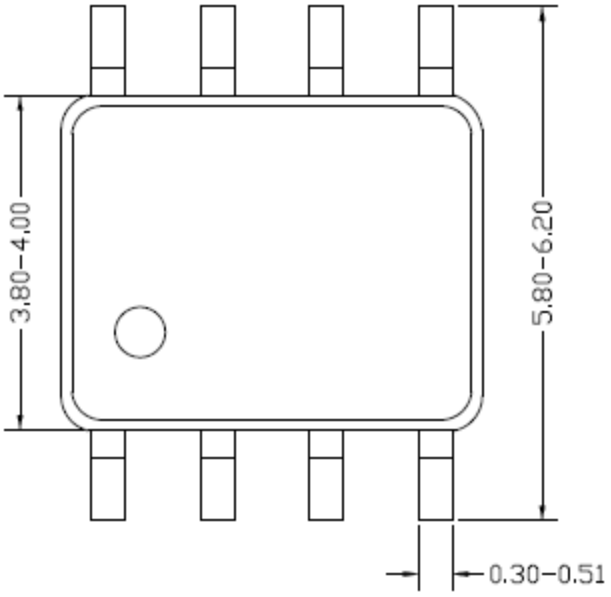
Output capacitor C_{OUT}

Preset the output voltage ripple ΔV_{OUT}, C_{OUT} is induced by

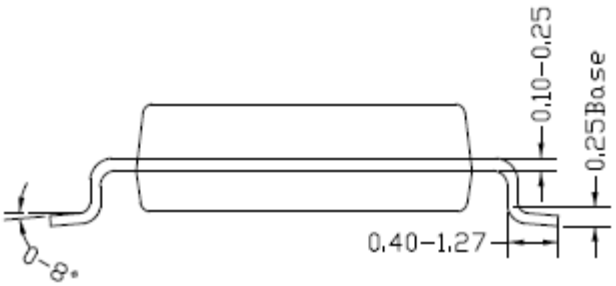
$$C_{OUT} = \frac{P_{OUT}}{2 \times \pi \times f_{AC} \times \Delta V_{OUT} \times V_{OUT}}$$

Where P_{OUT} is the rated output power, f_{AC} is the AC line frequency, ΔV_{OUT} is the demanded voltage ripple.

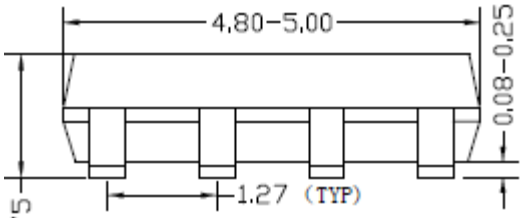
SO8 Package outline & PCB layout design



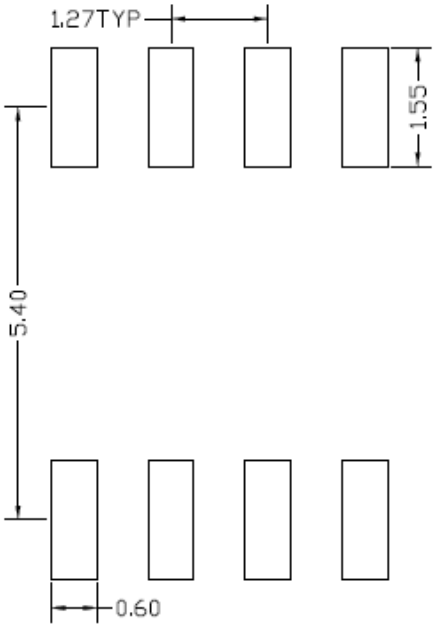
Top view



Side view



Front view



Recommended Pad Layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**