Application Note: SY5231

Secondary Side Synchronous Rectification

Advanced Design Specification

General Description

SY5231 is a high-performance synchronous rectification controller which is suitable for CCM, DCM and QR mode flyback converter. It can drive standard and logic-level N-channel MOSFET for secondary-side synchronous rectification.

SY5231 adopts DSEN voltage falling slope rate detecting technology to avoid SR MOSFET false turn on by parasitic ring under DCM or QR mode.

SY5231 adopts DSEN high voltage blanking time detective to enhance system ESD performance, it can prevent external noise false turn on SR MOSFET by making fast VDSEN falling slope rate.

SY5231 features extremely short turn off delay time under CCM operating mode. Meanwhile, it uses DSEN voltage regulation technology to fully utilize conducting time of SR MOSFET for high efficiency under DCM or QR mode.

Under light load condition, SY5231 will enter power save mode to improve light load efficiency.

The SY5231 is available in a SOT23-6 package.

Features

- Suitable for CCM, DCM and QR Mode Flyback Converter
- DSEN Pin Sensing up to 200V
- DSEN Falling Slope Rate Detecting to Avoid False Turn On of SR MOSFET by Parasitic Ring
- DSEN High Voltage Blanking Time detecting to enhance system ESD performance
- Dual Power Supply Channel for 3.3V to 21V Output Systems
- Maximum Allowed Switching Frequency Up to 500kHz
- 10 ns Typical Turnoff Propagation Delay
- 2A Sink, 0.5A Source Gate Driver Capability
- Compact Package: SOT23-6

Applications

- AC/DC Adapters
- USB Type-C and Power Delivery AC Adapters
- Server and Telecom Power Supply
- Auxiliary Power Supplies

Typical Application

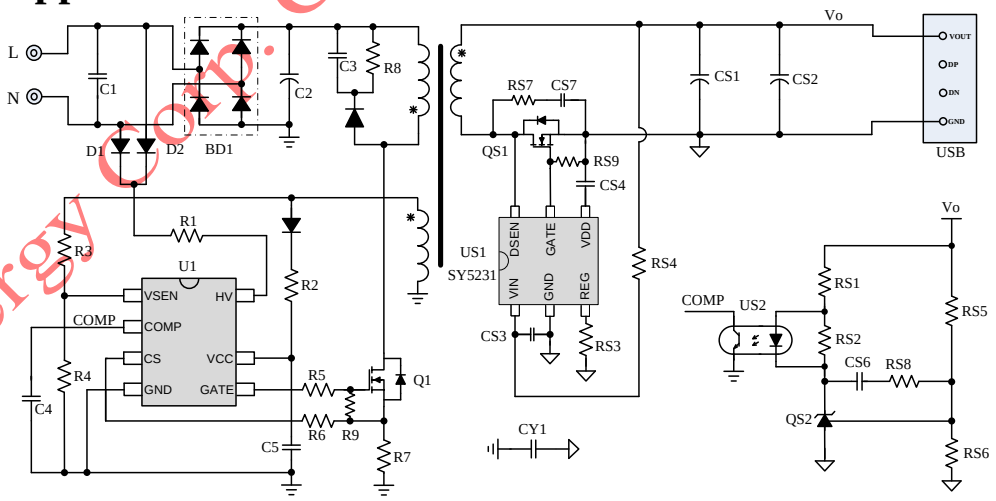


Fig. 1 Typical Application Circuit (SR MOSFET location: Low Side)

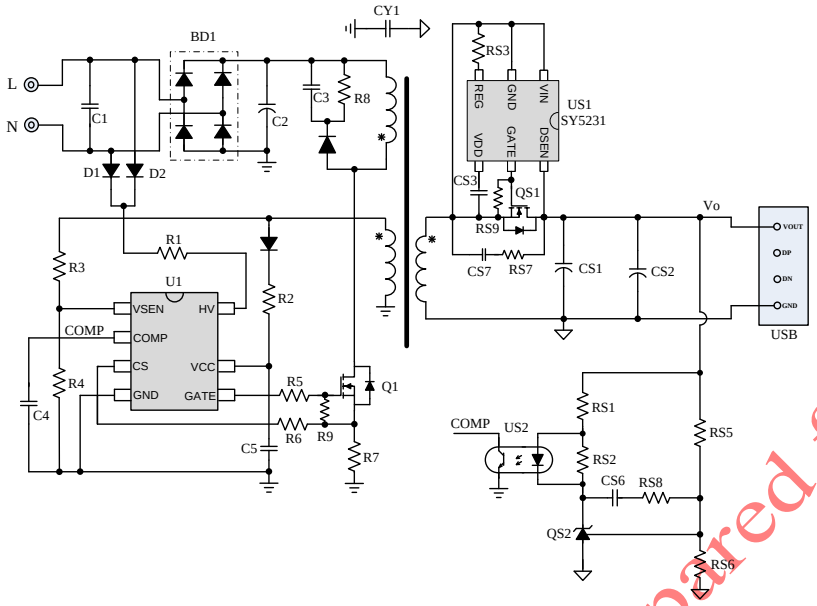
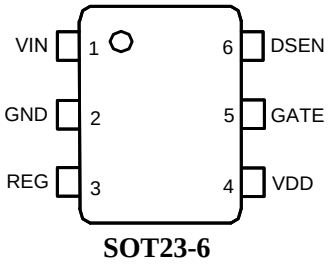


Fig. 2 Typical Application Circuit (SR MOSFET location: High Side)

Ordering Information

SY5231□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code



SOT23-6

Pinout (top view)

Ordering Number	Package	Top Mark
SY5231ABC	SOT23-6	D2xyz

x=year code, y=week code, z= lot number code

Pinout (top view)

Pin number	Pin Name	Pin Description
1	VIN	Power supply pin, connect it to the output of converter when SR MOSFET is located at low side. Connect it to GND pin when SR MOSFET is located at high side
2	GND	Connect this pin to SR MOSFET Source terminal
3	REG	Connect a resistor between this pin and GND to set the falling slope ref time threshold
4	VDD	Output of internal LDO, power supply for control unit and GATE drive circuit. Connect a 0.1μF or larger ceramic capacitor between VDD and GND pin
5	GATE	Connect this pin to the GATE terminal of SR MOSFET
6	DSEN	This pin should be connected to DRAIN of SR MOSFET to sense DRAIN voltage. This pin is also used as a self-supply channel

Absolute Maximum Ratings (Note 1)

VIN ---------- -0.3V~28V
REG ---------- -0.3V~16V
VDD ---------- -0.3V~16V
GATE ---------- -0.3V~16V
DSEN ---------- -1.5V~200V
I_{VDD} ---------- 20mA
Power Dissipation, @ TA = 25°C SOT23-6 ---------- 0.6W
Package Thermal Resistance (Note 2)
SOT23-6, θ_{JA} ---------- 170°C/W
SOT23-6, θ_{JC} ---------- 130°C/W
Junction Temperature Range ---------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

VIN ---------- 3.3V~21V
DSEN ---------- -1V~150V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

Electrical Characteristics

(V_{VIN}=12V, T_A=25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Pin						
Threshold of Switching to VIN Supply Channel	V_{VIN_VINSPY}	V_{VIN} is rising	4.7	4.85	5	V
Threshold of Switching to DSEN Supply Channel	$V_{VIN\_DSENSPY}$	V_{VIN} is falling	4.6	4.75	4.9	V
VDD Pin						
ON Threshold	V_{VDD_ON}		5	5.26	5.52	V
UVLO Hysteresis	V_{VDD_HYS}		2.35	2.5	2.75	V
VDD Regulation Voltage when VIN Pin is Active to Supply IC	$V_{VDD\_REG\_VIN}$		8.65	9.1	9.55	V
VDD Regulation Voltage when DSEN Pin is Active to Supply IC	$V_{VDD\_REG\_DSEN}$		4.75	5.1	5.35	V
Operating Current	I_{VDD_OP}	V_{VDD}=9V,C_{GATE}=2.2nF, F_{SW}=100kHz		3	3.5	mA
Maximum VDD Pin Capacitor Charging Current	$I_{VDD\_CHARGE\_MAX}$	VIN pin is active to charge VDD capacitor	12	17		mA
		DSEN pin is active to charge VDD capacitor	40	50		mA
Quiescent Current	I_{VDD_STBY}	Under Standby Mode		195	240	µA
DSEN Pin						
Ratio of PVS to DSEN	$K_{\_PVS\_RATIO}$			50		
PVS Initial Enable Threshold	$V_{PVS\_INITIAL\_EN}$		120	150	180	mV
Blanking Time for Sample PVS Pin Voltage	T_{PVS_BLK}		210	310	410	ns
Low Level Threshold to Sense VDSEN Falling Time	V_{DSEN_LTH}	V_{DSEN} is falling	0	20	40	mV
DESN Threshold to Force Turn off	$V_{DESN\_OFF\_TH}$		5	15	25	mV
Closed Loop V_{DSEN} Regulation Voltage Level	V_{DS_REG}	SR MOSFET is conducting	-54	-33	-22	mV
SR MOSFET Turn off Threshold	V_{OFF_TH}	V_{DSEN} is rising	-10	0	10	mV
Time Threshold IC Go into Sleep	$T_{STANDBY}$		16	20	24	us
REG Pin						
Resistor to Program Frequency Option	R_{REG}	R_{REG}=50k	75	100	125	ns
		R_{REG}=300k	225	300	375	ns
GATE Pin						
Gate Pin Clamped Current before UVLO ON	I_{CLP}	Vgs=1V	160	200	240	mA
Max. Source Current	I_{SOURCE_MAX}	V_{VDD}=9V, C_{LOAD}=2.2nF, Vgs from 1V to 8V	0.375	0.5		A

Max. Sink Current	I_{SINK_MAX}	V_{VDD}=9V, C_{LOAD}=2.2nF, Vgs from 8V to 1V	1.5	2		A
Minimum ON Time	T_{ON_MIN}		550	750	1050	ns
Minimum OFF Time	T_{OFF_MIN}		300	450	600	ns
Turn on Delay	T_{DELAY_ON}	C_{GATE}=2.2nF		30	50	ns
Turn off Delay	T_{DELAY_OFF}	C_{GATE}=2.2nF		10	20	ns
OTP						
Thermal Shutdown Temperature	T_{SD}		150	160	170	°C
Hysteresis to Resume Operating	T_{OTP_HYS}		15	20	25	°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on "2x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Block Diagram

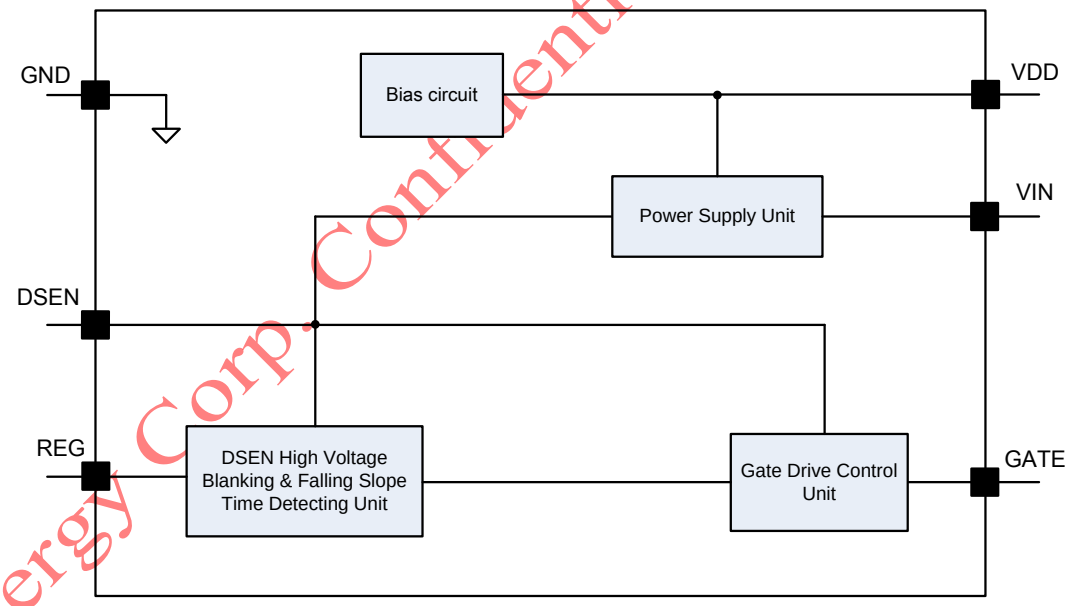
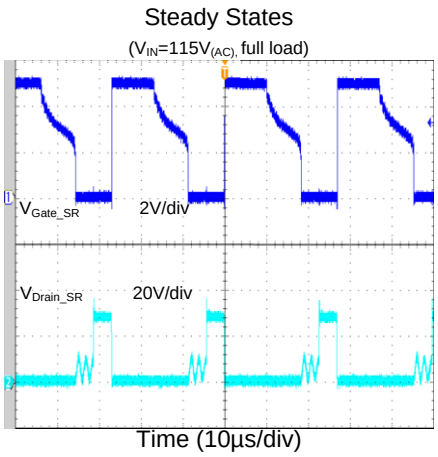


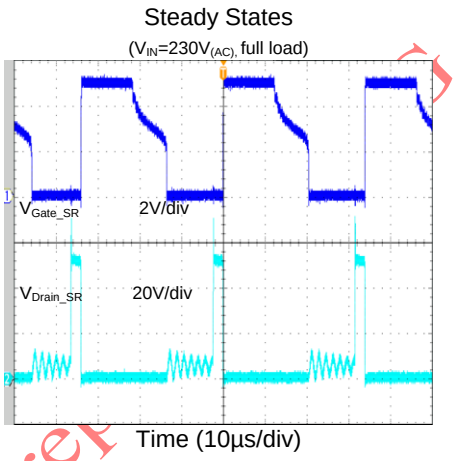
Fig.3 Block diagram

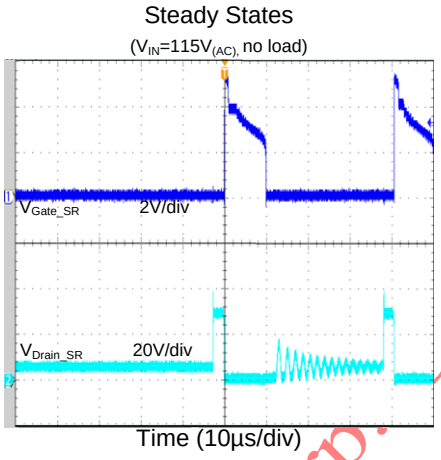
Typical Performance Characteristics

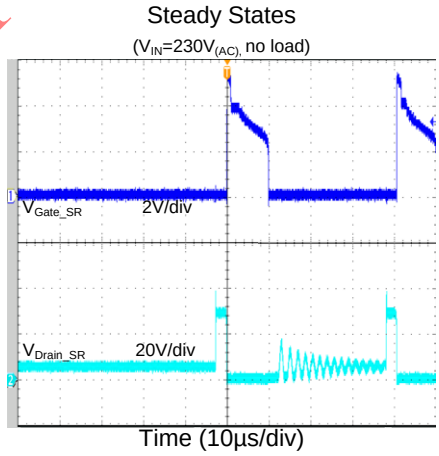
(Test condition: input voltage: 90Vac~264Vac; output spec: 5Vdc_3A, 20Vdc_3.25A; Ambient temperature: 25±5 ℃; Ambient humidity: 65±25 %.)

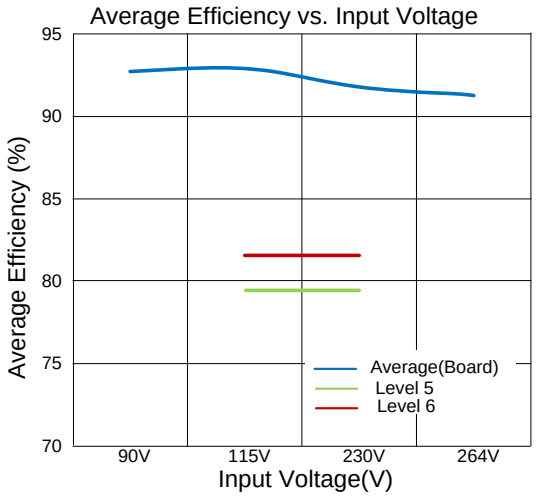
5Vdc_3A output







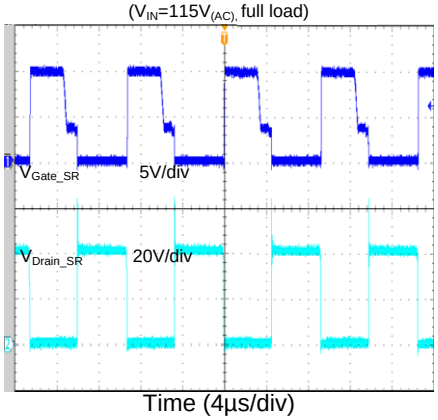




20Vdc_3.25A output

Steady States

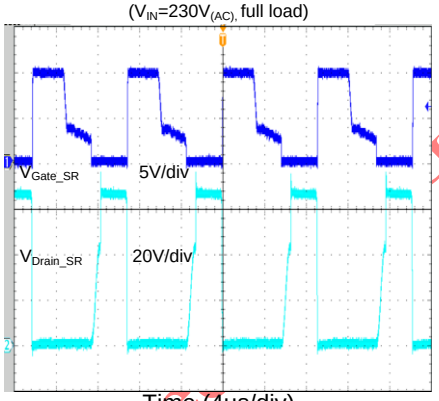
(V_{IN}=115$V_{(AC)}$, full load)



Time (4μs/div)

Steady States

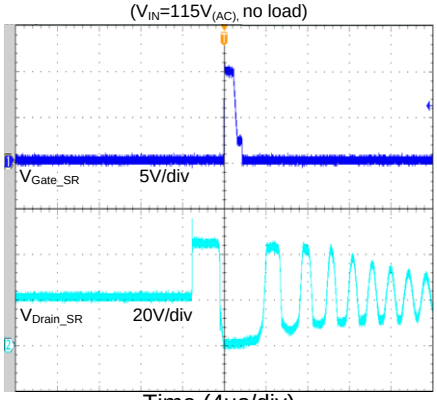
(V_{IN}=230$V_{(AC)}$, full load)



Time (4μs/div)

Steady States

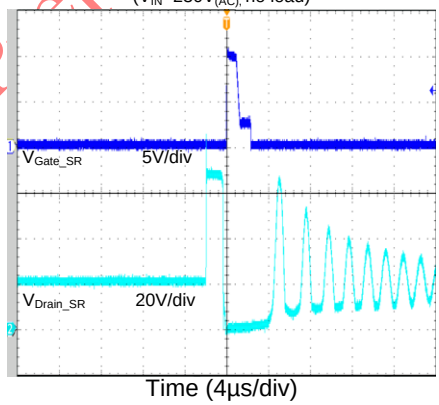
(V_{IN}=115$V_{(AC)}$, no load)



Time (4μs/div)

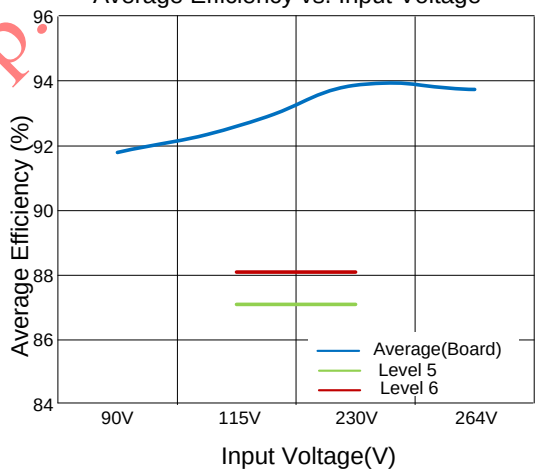
Steady States

(V_{IN}=230$V_{(AC)}$, no load)



Time (4μs/div)

Average Efficiency vs. Input Voltage



Operation Principles

Gate Pin Clamped before UVLO ON

In application, the primary side IC operate, the drain to source voltage of SR MOSFET will pulled up rapidly before IC UVLO ON when primary side MOSFET turn on. If the Cgd of SR MOSFET is big, the SR MOSFET gate voltage will be pulled up to make false turn on.

To resolve the problem, the gate voltage of SR MOSFET should be pulled down before IC UVLO ON.

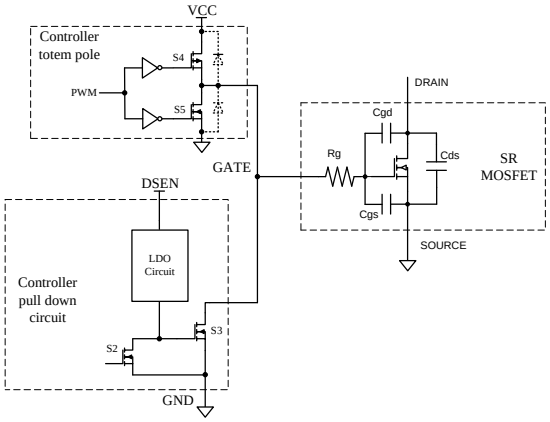


Fig. 4 Circuit diagram of SR controller & MOSFET

Before IC UVLO ON, the Gate of switcher S2 is low. DSEN voltage will charge the Vgs of switcher S3. S3 will pull down the gate voltage of SR MOSFET. The pulled down current of S3 is 200mA (@Vgs=1V of POWER MOSFET) to achieve better performance.

After IC UVLO ON, the Vgs of S2 is high. S2 will discharge the Vgs of S3, then S3 do not influence the GATE pin voltage. The GATE pin will be controlled only by IC totem pole. As in Fig.4.

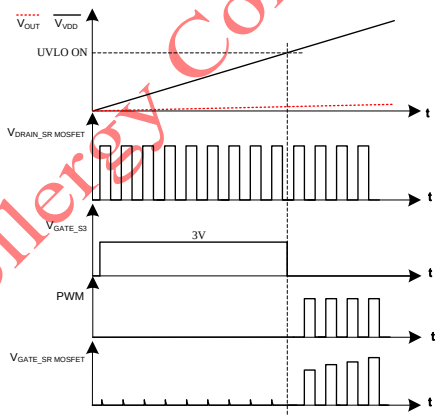


Fig. 5 Timing diagram of gate pin clamped

SR Turn On

Traditional method is to set a SR MOSFET turn on threshold V_{ON_TH}, when DSEN voltage is falling and down to V_{ON_TH}, then turn on SR MOSFET after a short delay as shown. However, under DCM or QR operating mode, after secondary current decrease to ZERO, a resonant waveform will appear. Sometimes, the amplitude of this resonant waveform can be large enough, which will cause DSEN voltage drops below turn on threshold V_{ON_TH}, SR MOSFET may be falsely turned on by parasitic resonant.

To solve the above issue, V_{DSEN} falling slope rate is detected. When primary MOSFET is turned off, V_{DSEN} falling slope rate is very high, SR will turn on; while during resonant phase, V_{DSEN} falling slope rate is relatively low, SR will not turn on.

SY5231 use resistor divide circuit to sense the DSEN voltage, the V_{PVS} is 0.02 times of V_{DSEN}. It set 2 thresholds to indirectly sense V_{PVS} falling slope rate, the V_{PVS} is the time duration ($\triangle t$) when V_{PVS} is falling between high-level threshold V_{PVS_HTH} and low-level threshold V_{DSEN_LTH} (0mV) is measured, and the falling time duration ($\triangle t$) will be compared with a falling slope ref time threshold T_{REF}.

To prevent external noise (for example: ESD noise) false turn on SR MOSFET by making fast V_{DSEN} falling slope rate, the DSEN blanking time is adopt.

V_{PVS} is the resistor divide voltage of V_{DSEN}. If V_{PVS} is above V_{PVS_HTH} and lasting for T_{PVS_BLK} (300nS) and falling slope time $\triangle t<T_{REF}$, IC considers this action as primary MOSFET turn off event and then turn on SR MOSFET after a short delay. Otherwise, IC will not turn on SR MOSFET.

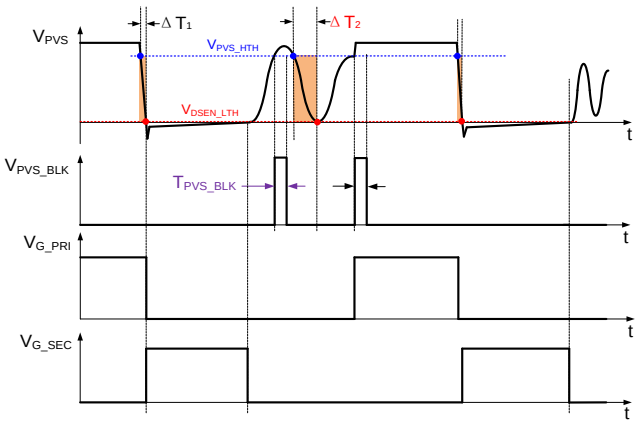


Fig.6 Time diagram of SR Off time enable strategy

V_{PVS_HTH} is a dynamically adjusted value, it is 0.85 times of DSEN high-level voltage value. The falling slope ref

time threshold T_{REF} is controlled by REG resistor as below;

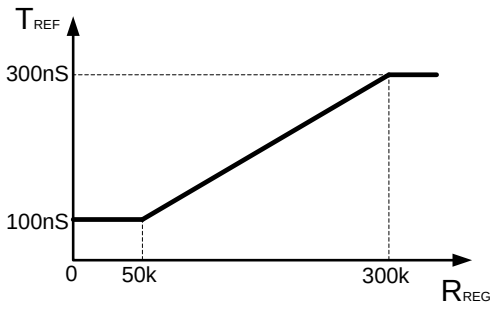


Fig. 7 Programmable curve of falling slope ref

SR Gate Control

Under DCM, the SR current will decrease before primary MOSFET is turned on. The closed loop V_{DS} regulation circuit will gradually decrease V_{GATE} once the V_{DS} is above the V_{DS_REG}(-30mV). As SR current becomes smaller, V_{GATE} drops near the SR MOSFET turn off threshold, I_D*R_{DSON} cannot be regulated to V_{DS_REG} anymore, V_{DS} will increase higher than V_{DS_REG}. If V_{DS} rises and cross V_{OFF_TH}, after a short delay time T_{OFF_DLY}, GATE voltage will be pulled down to ZERO by a large sink current to turn off SR MOSFET.

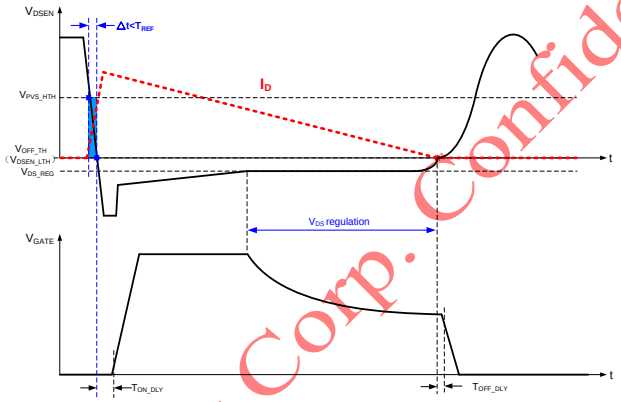


Fig. 8 SR control strategy in DCM

Under CCM, primary MOSFET will be turned on before secondary current decreases to ZERO, V_{DSEN} will rapidly increase due to primary MOSFET turn on event. IC will compare V_{DSEN} with another threshold V_{OFF_TH}, once V_{DSEN} is rising and crossing V_{OFF_TH}, after a short delay time T_{OFF_DLY}, GATE voltage will be pulled down to ZERO by a large sink current to achieve fast turn off SR MOSFET. The turn off delay time T_{OFF_DLY} is designed to be very short to minimize the power loss caused by primary and secondary MOSFET overlap.

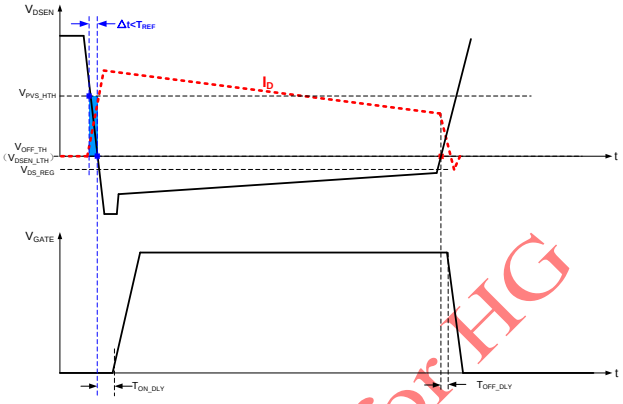


Fig. 9 SR control strategy in CCM

Min ON Time & Min OFF Time

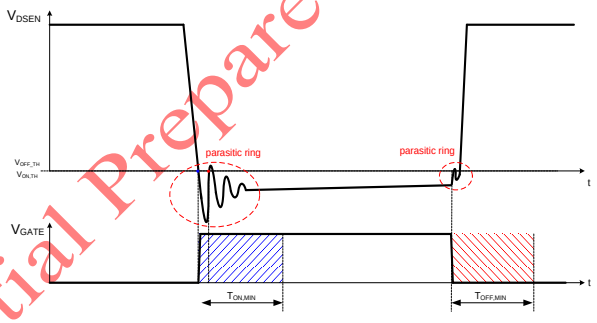


Fig. 10 timing diagram of Min ON time and Min OFF time

When primary MOSFET is turned off, DRAIN voltage of secondary SR MOSFET will drop rapidly to about -700mV, due to resonant between parasitic inductors and capacitors, a ringing will appear on DRAIN voltage waveform, the V_{DSEN} reach the turn off threshold V_{OFF_TH}.

To void false turn off SR MOSFET, a blanking time T_{ON_MIN} is applied when SR MOSFET is turned on. During this blanking time, GATE pin output state is latched off.

After SR MOSFET is turned off, a ringing will appear on DRAIN voltage waveform. To void IC internal logic circuit false action, a blanking time T_{OFF_MIN} is also applied.

Dual Channel Power Supply

When the output voltage is as low as 3V, which is not high enough to drive the SR MOSFET, the DSEN pin supply is preferred. When the output voltage is high, the power supply efficiency of DSEN pin is lower than VIN pin, the VIN pin supply is preferred.

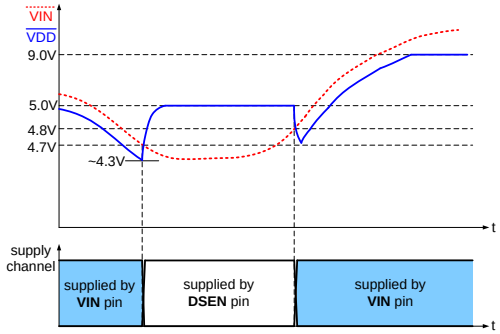


Fig. 11 Timing diagram of dual channel supply

SY5231 adopts dual channel power supply. Before VDD voltage reaches ON threshold V_{VDD_ON}, SY5231 is supplied by DSEN pin. As VDD rises and reach ON threshold, VIN pin voltage will be monitored. If VIN voltage is higher than V_{IN_INSPY}, then power supply channel will switch to VIN pin. As VIN increase higher, VDD will follow VIN (with about 0.5V voltage drop), finally VDD will be clamped to 9V. As VIN is decreasing and crossing V_{DSEN_VINSPY}, then the power supply channel will switch to DSEN pin and VDD will be regulated to 5V. Timing diagram is shown in Fig. 11.

Power Saving Mode

Under light load conditions, SY5231 will enter power saving mode to improve light load efficiency.

During each switching cycle, after SR MOSFET is turned off, a timer will start to count, if the timer has counted to 20us before next SR turn on instant, IC will enter power saving mode, and reduce the power consumption. IC will exit power saving mode by SR MOSFET turn on event.

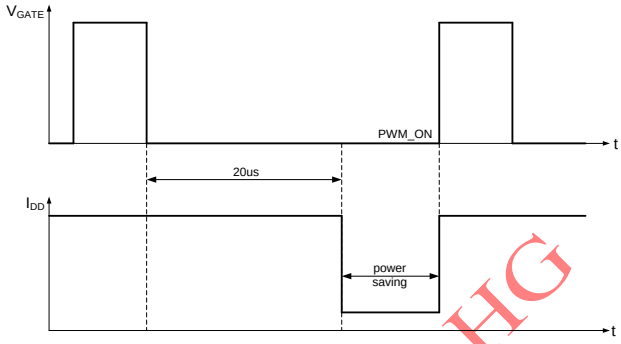


Fig. 12 timing diagram of power saving mode

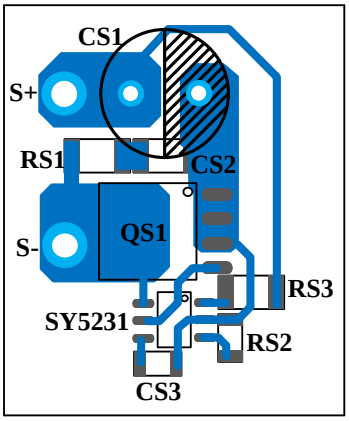
OTP

IC die temperature is monitored, if the die temperature rises above 160℃, IC will stop driving SR MOSFET and keep GATE voltage to 0V. When die temperature drops below 140℃, IC will resume normal operating again.

Layout

(a) To achieve better EMI and Efficiency performance, the output connector should be connected to the output cap first, then to the SR Power pin.

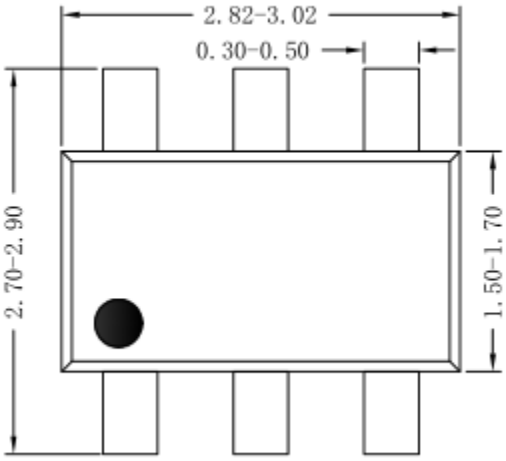
(b) The circuit loop of all switching circuit should be kept small: secondary power loop, secondary RC snubber circuit loop and IC power supply loop.



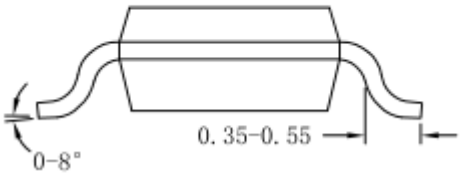
Design Notice

1. To prevent SR turn off later at no load, the SR freewheeling time should be more than 1μs.
2. To achieve better EMI performance and reduce secondary rectifier loss, the circuit loop of secondary winding terminal, the output cap and SR MOSFET should be short.
3. GND pin should be connected to Source of SR MOSFET shortly.
4. DSEN pin should be connected to Drain of SR MOSFET shortly.
5. When big current ring happened at secondary winding after Minton, the gate voltage has ring because of the close loop control. To resolve this issue, external parasitic inductance should be reduced by optimizing the layout, or increasing the RC snubber.
6. To improve the system ESD performance, at least 10Ω resistor should be in series between VIN pin and Output cap, and at least 100nF cap should be in parallel between VIN pin and SOURCE pin.

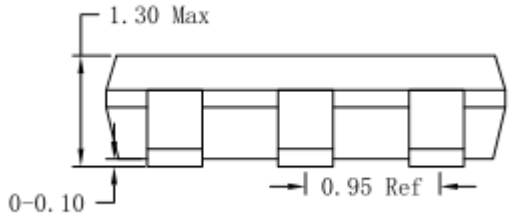
SOT23-6 Package Outline & PCB layout



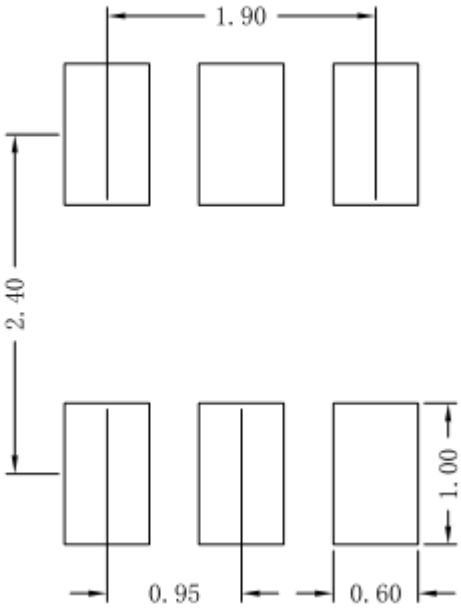
Top View



Side View



Side View



Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**