Application Note: SY5033A

CCM+QR SSR Flyback Controller

Advanced Design Specification

General Description

SY5033A is a peak current mode SSR flyback controller targeting at wide output range fast charger application. It features wide VCC operating range (10~90V) which can eliminate external LDO circuit. It features HV start up circuit and low quiescent current which can achieve low no load loss. It adopts pseudo fixed frequency control which can eliminate slope compensation under CCM. It combines CCM and QR mode together to achieve optimized efficiency. It adopts adaptive peak current limit to achieve LPS requirement. It also provides comprehensive and reliable protections including BO, output OVP/UVP, VCC OVP, OLP, external OTP, OTP, Secondary SR MOS SCP, etc.

SY5033A is available with compact SO8 package.

Features

- Wide VCC Operating Range: 10~90V
- HV Start up
- Mixed CCM+QR Control Strategy
- Pseudo Fixed Frequency Control to Eliminate Slope Compensation under CCM
- 65kHz Fixed Switching Frequency under CCM
- 90kHz Switching Frequency Limit under QR Mode
- Frequency Fold Back for High Average Efficiency
- Minimum Switching Frequency Limited to 28kHz
- Burst Control for High Light Load Efficiency
- Adaptive Peak Current Limit for LPS
- Comprehensive Protections Including BO, Output OVP/UVP, VCC OVP, OLP, External OTP, OTP, Secondary SR MOS SCP, etc
- Gate Drive Capability: +75mA/-600mA
- Internal Soft Start Process
- Compact Package: SO8

Applications

- Fast Charger
- AC/DC Adapter

Typical Applications

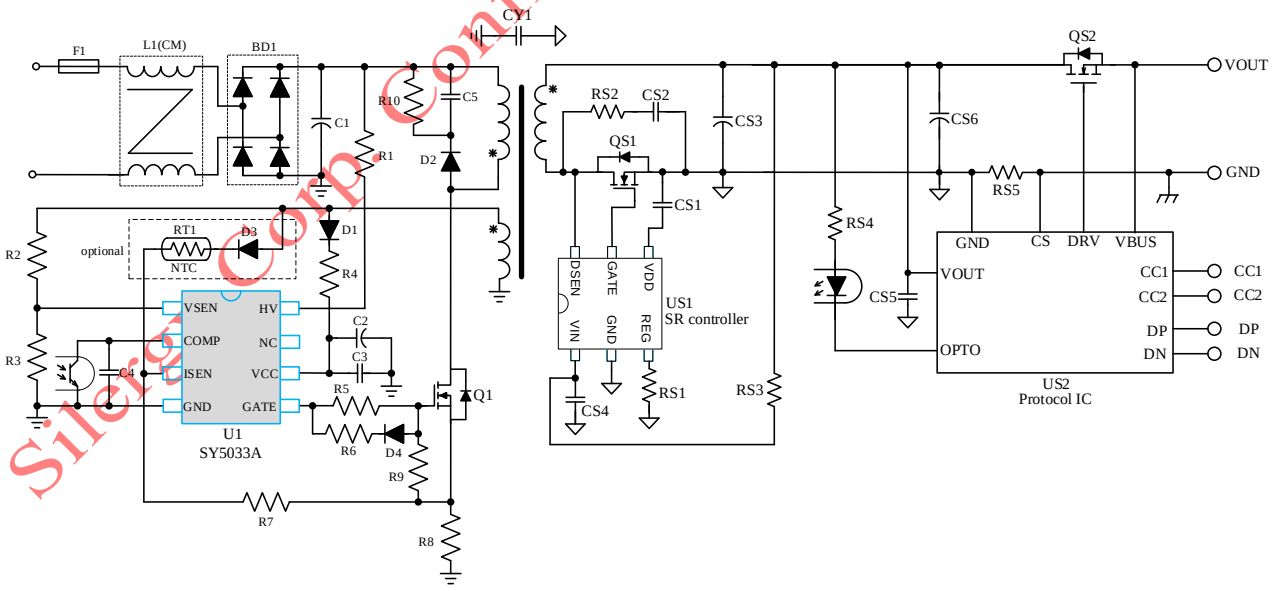


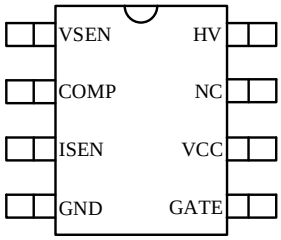
Fig.1 Typical Application Circuit

Silergy Corp Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

Ordering Information

SY5033□(□□□)
- Package Code
- Optional Spec Code



Pinout (Top view)

Ordering Number	Package	Top Mark
SY5033AFAP	SO8	GHQxyz

x=year code, y=week code, z= lot number code

Pinout

Pin Number	Pin Name	Pin Description
1	VSEN	Multiple functions including valley detecting, input voltage sense and output voltage sense
2	COMP	This pin is connected to an opto-coupler for output voltage feed back
3	ISEN	Primary peak current sense and programmable external OTP
4	GND	Ground
5	GATE	Gate drive
6	VCC	Power supply
7	NC	
8	HV	HV start up

Absolute Maximum Ratings (Note 1)

HV ---------- -0.3V~900V
VCC ---------- -0.3V~100V
GATE ---------- -0.3V~15V
VSEN, ISEN ---------- -0.3V~20V
COMP ---------- -0.3V~3.6V
Power Dissipation, at T_A = 25°C SO8 ---------- 1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA} ---------- 125°C/W
SO8, θ_{JC} ---------- 60°C/W
Junction Temperature Range ---------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

V_{CC} ---------- 10V~90V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

Electrical Characteristics

(V_{CC} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
HV Pin Section						
Break Down Voltage	V_{HV_BR}		900			V
Leakage Current	I_{HV_LK}	V_{HV}=400V_{DC}			1	μA
HV Current to Charge VCC	I_{HV}	V_{HV}=100V_{DC}		2.3		mA
VCC Pin Section						
Turn ON Threshold	V_{CC_ON}	V_{CC} rising up		18		V
HV Current Source Enable Threshold	V_{CC_MIN}	V_{CC} falling down		9.0		V
Turn OFF Threshold	V_{CC_OFF}	V_{CC} falling down		8.0		V
OVP Threshold	V_{CC_OVP}			94		V
Current Sink under Over Voltage Condition	I_{CC_OVP}	V_{CC}=V_{CC_OVP}+0.1V		3		mA
Start up Current	I_{CC_ST}	V_{CC}=V_{CC_ON}-0.5V			100	μA
Quiescent Current	I_{CC_Q}			280		μA
Operating Current	I_{CC_OPT}	C_L=1nF, F_{SW}=65kHz		2.2		mA
Current Sink under Fault Condition	I_{CC_FAULT}			0.65		mA
ISEN Pin Section						
Max Peak Current Limit	V_{ISEN_MAX}			500		mV
Min Peak Current Limit	V_{ISEN_MIN}			138		mV
Primary OCP Threshold	V_{ISEN_OCP}			650		mV
Leading Edge Blanking	T_{ISEN_LEB}			450		ns
Blanking time for ISEN Short Detecting	$T_{ISENSCP\_BLK}$	Low line condition		3.9		μs
Threshold Voltage for ISEN Short Detecting	V_{ISEN_SCP}			50		mV
External OTP Threshold	V_{ISEN_EXOTP}			0.5		V
VSEN Pin Section						
Blanking Time for Output Voltage Sense after MOS is Turned OFF	T_{VOSEN_BLK}	I_{COMP}=120uA		1.45		μs
Output OVP Threshold	V_{VSEN_OVP}			2.0		V
Output UVP Threshold	V_{VSEN_UVP}			150		mV
Output UVP Blanking Time during Start up	T_{STBLK_UVP}			17.8		ms
Brown out Threshold Current	I_{BO}			100		μA
Brown in Hysteresis Current	I_{BI_HYS}			12		μA
Brown out Debounce Time	T_{BO_DBC}			64		ms
High line condition (Force QR) Threshold Current	I_{LINE_H}			300		μA
Back to Low Line Condition Hysteresis Current	$I_{LINE\_L\_HYS}$			54		μA
COMP Pin Section						
OLP Debounce Time	T_{OLP_DBC}			64		ms
Switching Frequency Section						

Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

Frequency under CCM	F_{SW_CCM}			65		kHz
Frequency Limit under QR Mode	$F_{SW\_MAX\_QR}$			90		kHz
Minimum Switching Frequency	F_{SW_MIN}			28		kHz
Frequency Modulation Amplitude	$A_{FSW\_MOD\_AMP}$	Under CCM		±6%		
Frequency Modulation Period	T_{FSW_MOD}			500		μs
Maximum ON Time	T_{ON_MAX}			18		μs
Maximum OFF Time	T_{OFF_MAX}			240		μs
GATE Pin Section						
High Level Clamp	V_{GATE_CLAMP}	V_{CC}=20V		13.5		V
Max Source Current	I_{SOURCE_MAX}			75		mA
Max Sink Current	I_{SINK_MAX}			600		mA
Internal OTP Section						
OTP threshold	T_{OTP}			150		°C
Hysteresis to Recovery	T_{OTP_HYS}			23		°C
Soft Start Section						
Soft start time	T_{SS}			3.5		ms
Auto-recovery Control						
Re-start timer	T_{RST}			2		s

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note2: Θ_{JA} is tested on Silergy EVB, the EVB is two layer and 1oz copper is used.

Note 3: Increase VCC pin voltage gradually higher than V_{CC_ON} voltage then turn down to 12V.

Silergy Corp. Confidential Prepared for Meizu

Block Diagram

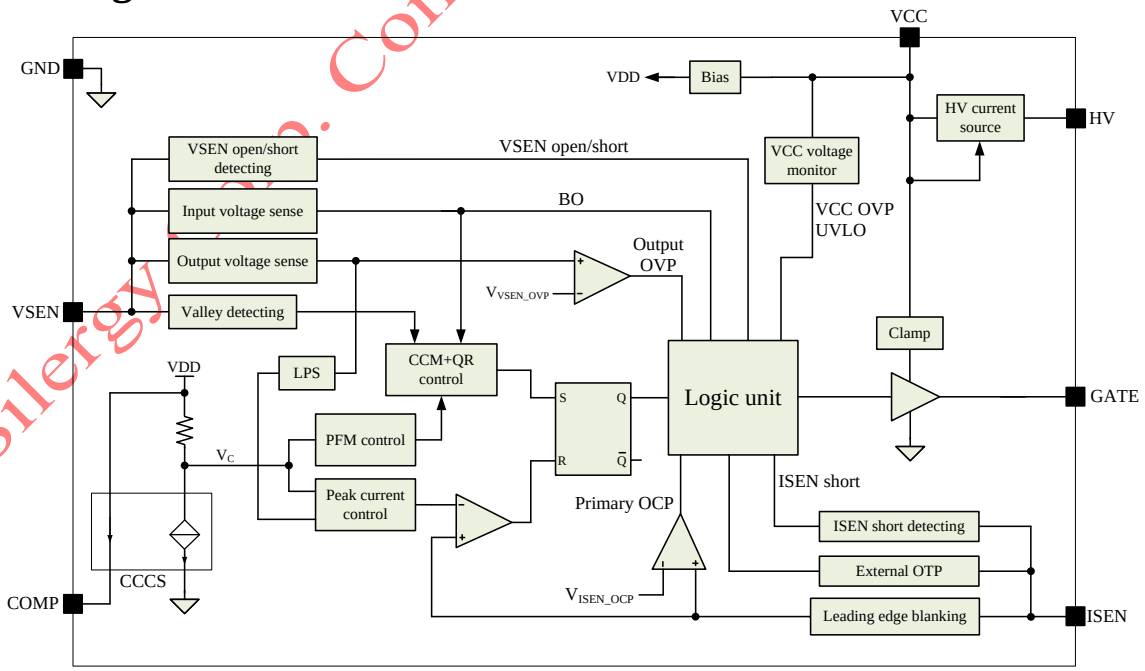
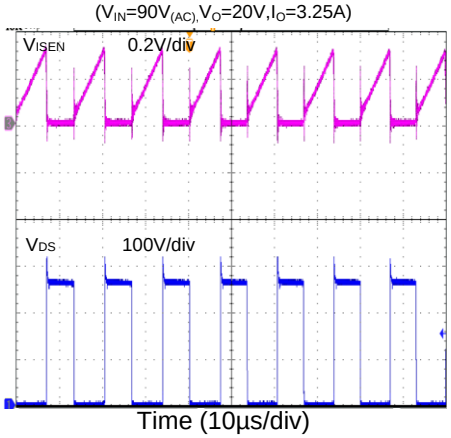


Fig.2 Block diagram

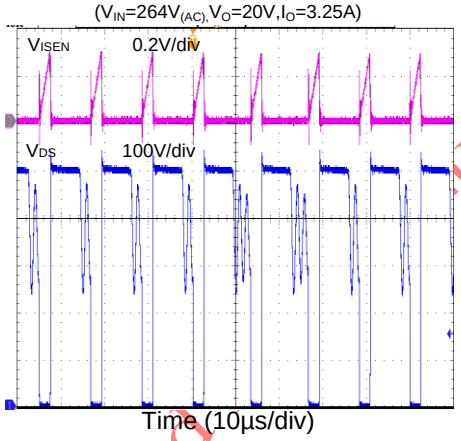
© 2023 Silergy Corp. All Rights Reserved.

Typical Performance Characteristics

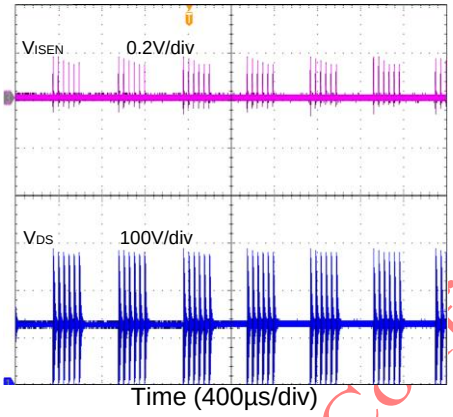
Steady state
(V_{IN}=90$V_{(AC)}$,V_O=20V,I_O=3.25A)



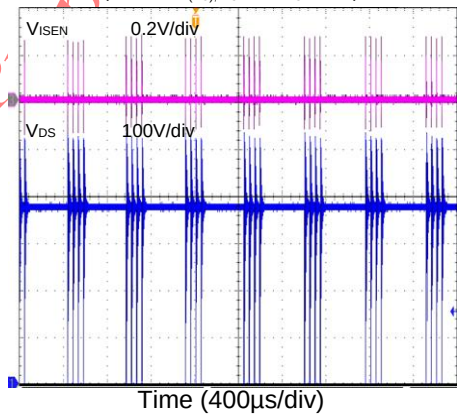
Steady state
(V_{IN}=264$V_{(AC)}$,V_O=20V,I_O=3.25A)



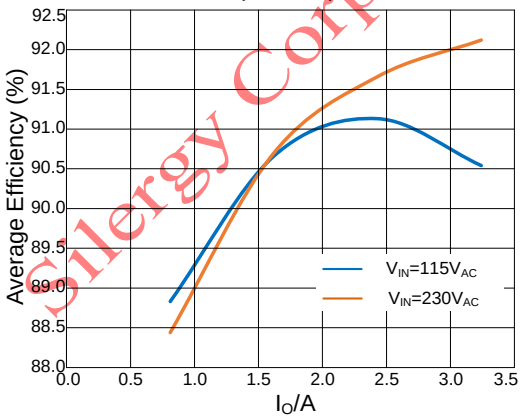
Steady state
(V_{IN}=90$V_{(AC)}$,V_O=20V,I_O=0.1A)



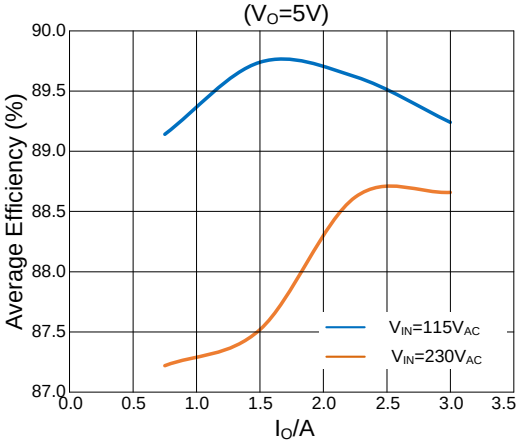
Steady state
(V_{IN}=264$V_{(AC)}$,V_O=20V,I_O=0.1A)



Efficiency Curve
(V_O=20V)



Efficiency Curve
(V_O=5V)



Silergy Corp. Confidential Prepared

© 2023 Silergy Corp. All Rights Reserved.

Operation Principles

HV start up

SY5033A features HV start up to simplify start up circuit and achieve low no load loss. HV pin is recommended to connected to BUS+ through a resistor R_{HV}. R_{HV} is used to improve the reliability of HV pin and the recommended resistance is 10kΩ~20kΩ.

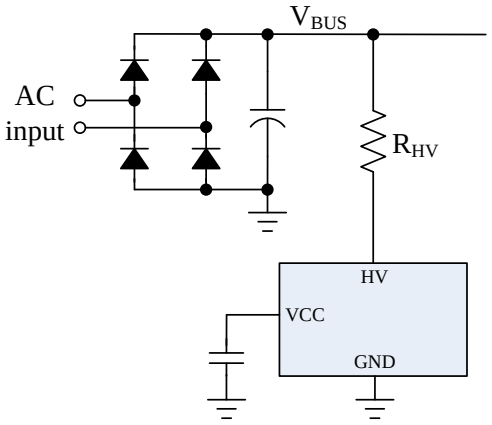


Fig.1 HV start up circuit

Wide VCC operating range

SY5033A features wide VCC operating range from 10V to 90V, which is dedicated for fast charger applications. The traditional external LDO circuit for IC power supply can be eliminated to achieve simple peripheral circuit. A ceramic capacitor C_1 is recommended to be mounted as close as possible to IC's VCC and GND pin on PCB layout.

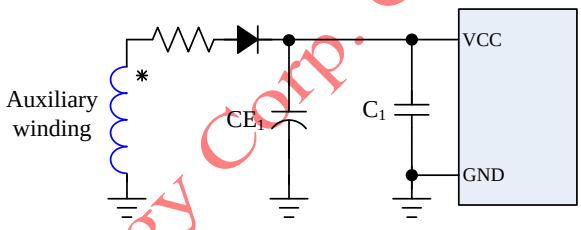


Fig.2 Simple IC power supply circuit

CCM+QR mixed operating principle

SY5033A adopts mixed control method that combine CCM and QR mode together. CCM frequency is fixed to 65kHz, while QR mode frequency is limited to 90kHz. Transformer is designed that under low line input and heavy load condition, IC operates under CCM. While under other conditions, IC will operate under QR mode (valley switching). Due to this mixed control method, optimized efficiency and transformer size can be achieved.

Under light load condition, IC operates under burst mode to further improve light load efficiency. Burst mode is controlled by COMP pin internal control voltage V_C. When V_C is lower than sleep mode threshold, IC will stop switching and enter sleep mode. Under sleep mode, the current consumed by IC is maintained to very low level (typical=280uA). When V_C is higher than another exit sleep threshold, IC will exit sleep mode and resume normal operating. The lighter the load is, the longer IC will stay in sleep mode.

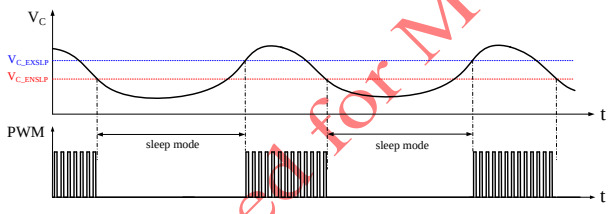


Fig.3 Timing diagram of burst mode control

Force QR at high line input condition

CCM under high line input condition is generally not allowed due to lower converter efficiency and higher voltage spike if secondary SR switcher is used. SY5033A adopts force QR mode control to guarantee QR mode (valley turn on) under high line input condition and steady state.

SY5033A senses input voltage by VSEN pin negative current I_{VSEN} (flowing out of VSEN pin) when primary power MOS is turned on. When primary power MOS is turned on, VSEN pin will be internally clamped to 0V, since the negative voltage on auxiliary winding is proportional to BUS voltage, the current flowing out of VSEN pin will be proportional to BUS voltage. SY5033A will compare the current flowing out of VSEN pin with high line threshold current I_{LINE_H} (typical=300uA), if the current flowing out of VSEN pin is larger than I_{LINE_H}, input high line condition is recognized by IC and force QR mode is enabled. When VSEN pin negative current is lower than another threshold current I_{LINE_H}-$I_{LINE\_L\_HYS}$, low line input condition will be recognized by IC and force QR will be disabled, CCM operating will be allowed. The upper resistor of VSEN pin resistor divider connected between auxiliary winding will set input high line condition threshold voltage. Input high line condition threshold V_{IN_H} (RMS) is calculated as below equation:

$$V_{IN\_H} = \frac{I_{LINE\_H}}{\sqrt{2}} \times \frac{N_P}{N_A} \times R_H$$

Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

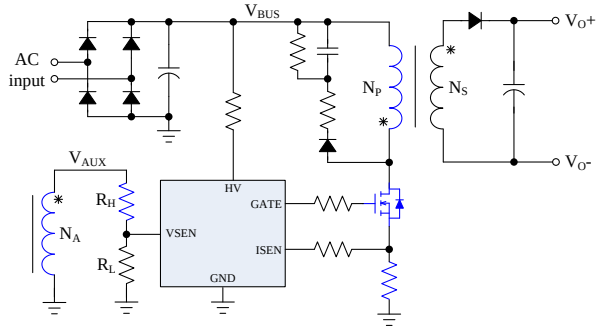


Fig.4 Illustration of input voltage detecting

BO (brown out) protection

During Vin start up, when V_{CC} rises to V_{CC_ON} threshold, IC will check if input voltage is higher than BI(brown in) threshold firstly. The 1st switching pulse is aimed to detect input voltage condition. If VSEN pin negative current I_{VSEN} is larger than BI threshold, IC will continue normal switching. Otherwise, IC will stop switching and enter auto-recovery mode.

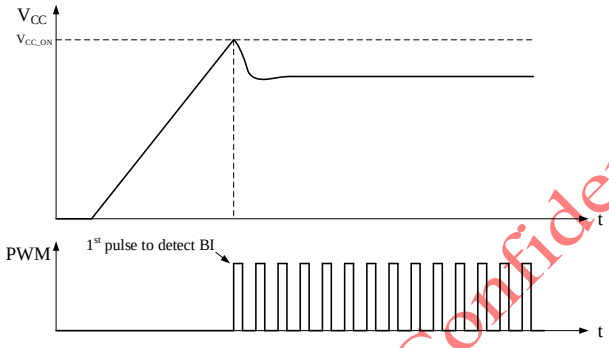


Fig.5 1st detecting pulse when Vin start up

Under abnormal conditions, if AC input voltage becomes lower and lower, input current will become larger and larger, there is high risk of AC components such as NTC resistor, EMI choke and bridge rectifier which may be over heated and finally break down. SY5033A adopts BO protection (input under voltage protection) to avoid over heating of AC input components. It detects BUS voltage by VSEN pin negative current I_{VSEN} when primary power MOS is turned on. IC will compare I_{VSEN} with internal BO threshold current I_{BO}, if I_{VSEN} is lower than I_{BO}, and sustained longer than BO debounce time T_{BO_DBC}, IC will stop switching and enter auto-recovery mode. The input BO threshold can be calculated according to below equation:

$$V_{IN\_BO} = \frac{I_{BO}}{\sqrt{2}} \times \frac{N_P}{N_A} \times R_H$$

Generally, input BO threshold voltage is defined between 60Vac and 70Vac.

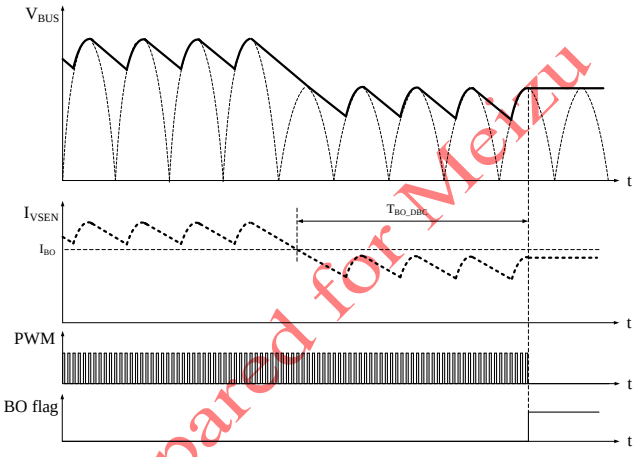


Fig.6 Timing diagram of BO protection

Programmable output OVP/UVP

SY5033A will sense output voltage by VSEN pin cycle by cycle, and programmable output OVP/UVP can be achieved. When primary power MOS is turned off, voltage on auxiliary winding V_{AUX} will be proportional to output voltage V_O. VSEN pin will sense the output voltage by a resistor divider (R_H and R_L) connected between auxiliary winding.

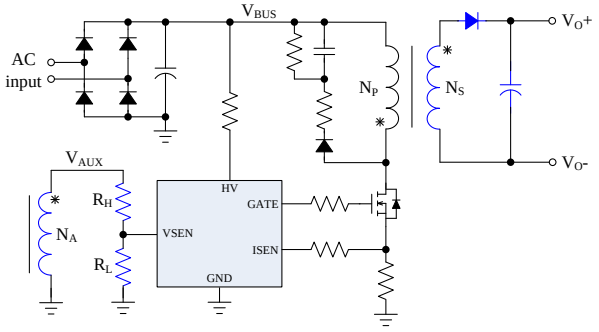


Fig.7 Circuit diagram of output voltage sense

The relationship between VSEN pin voltage and output voltage is shown as below equation:

$$V_{VSEN} = V_O \cdot \frac{N_A}{N_S} \cdot \frac{R_L}{R_H + R_L}$$

Since voltage spike will present on VSEN pin when primary side power MOS is turned off as shown in below figure, to avoid false trigger of output OVP by the voltage

Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

spike, a blanking time T_{VOSEN_BLK} is adopted. Output voltage will only be sampled after T_{VOSEN_BLK} elapse. Primary side RCD snubber should be carefully tuned to make sure that voltage spike sustained time will not exceed T_{VOSEN_BLK}.

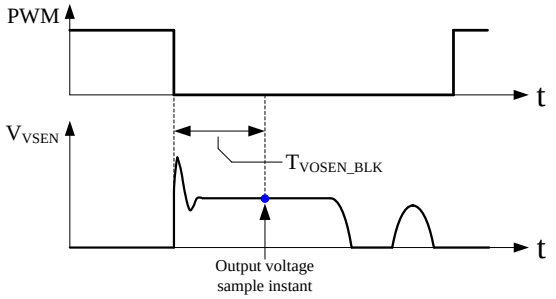


Fig.8 Illustration of blanking time for output voltage sense

When VSEN pin voltage rises above OVP threshold V_{VSEN_OVP}, IC will stop switching and enter auto-recovery mode. Output OVP threshold is calculated as below equation.

$$V_{O\_OVP} = V_{VSEN\_OVP} \cdot \frac{N_S}{N_A} \cdot \frac{R_H + R_L}{R_L}$$

For fast charger applications, output voltage varies according to protocol controller, so output OVP level should be determined by the maximum output voltage. For example, a fast charger claims output voltage range from 3.3V to 20V, then output OVP level is equal to 20V multiplied by 120% (V_{O_OVP}=24V).

Note: VSEN pin upper resistor R_H should be determined firstly according to input BO threshold voltage (customer predefined), and then lower resistor R_L of VSEN pin resistor divider is calculated according to below equation.

$$R_L = R_H \cdot \frac{1}{\frac{N_A}{N_S} \cdot \frac{V_{O\_OVP}}{V_{VSEN\_OVP}} - 1}$$

Programmable external OTP

SY5033A features programmable external OTP on ISEN pin. The circuit diagram is shown as fig.9. A fast-switching signal diode D_1, a NTC resistor RT_1 and a fine tune resistor R_{TUNE} are used to achieve external OTP. When primary power MOS is turned off, the volage on auxiliary winding will be proportional to output voltage. The relationship between ISEN pin voltage and output voltage is shown as below equation:

$$V_{ISEN} = \left(\frac{N_A}{N_S} \cdot V_O - V_{D1}\right) \cdot \frac{R_{OCP} + R_{ISEN}}{R_{RT1} + R_{TUNE} + R_{OCP} + R_{ISEN}}$$

The voltage on ISEN pin will be sensed and compared with external OTP threshold V_{ISEN_EXOTP} (typical=0.5V), if ISEN pin voltage is higher than the OTP threshold for 4 consecutive switching cycles, external OTP will be triggered. When external OTP is triggered, IC will enter auto-recovery mode. The resistance of NTC resistor to trigger external OTP is calculated by below equation:

$$R_{NTC(OTP)} = (R_{OCP} + R_{ISEN}) \cdot \left(\frac{\frac{N_A}{N_S} \cdot V_O - V_{D1}}{V_{ISEN\_EXOTP}} - 1\right) - R_{TUNE}$$

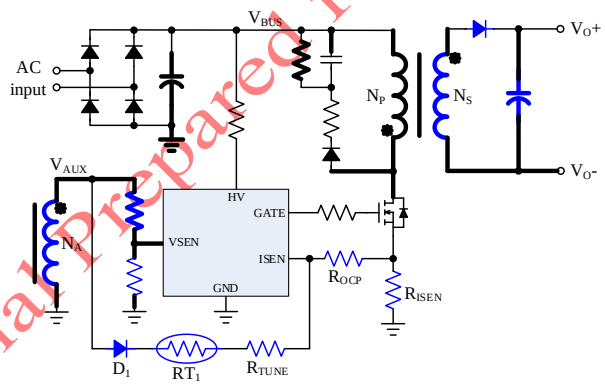


Fig.9 Circuit diagram of external OTP

OLP (Over Load Protection)

When output over load happens, COMP pin internal voltage V_C will be pulled up to high level, and primary peak current will reach the maximum value. SY5033A will compare V_C with internal OLP threshold, when V_C is higher than the OLP threshold, a timer will begin to count, and if V_C is continuously higher than OLP threshold which result in OLP timer elapse, SY5033A will stop switching and enter auto-recovery mode.

Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

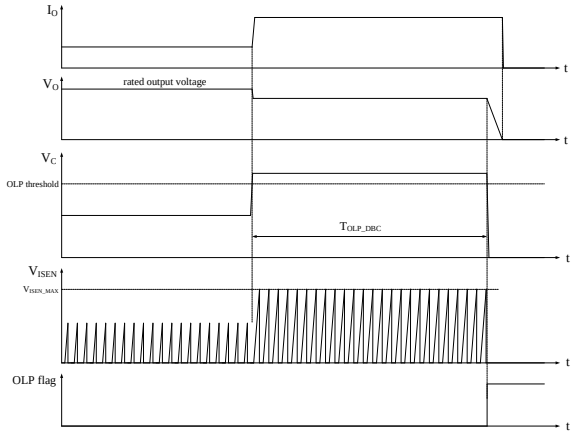


Fig.10 Timing diagram of OLP

Secondary SR MOS short circuit protection

Under secondary SR MOS short circuit condition, when primary power MOS is turned on, primary current of flyback converter will increase with very high di/dt rate, during ISEN pin leading edge blanking time, primary peak current sense voltage V_{ISEN} will rise to very high level without limit. SY5033A adopts a primary OCP threshold V_{ISEN_OCP}, when V_{ISEN} is larger than V_{ISEN_OCP}, and last for 4 consecutive switching cycles, secondary SR MOS short circuit protection will be triggered, IC will stop switching and enter auto-recovery mode.

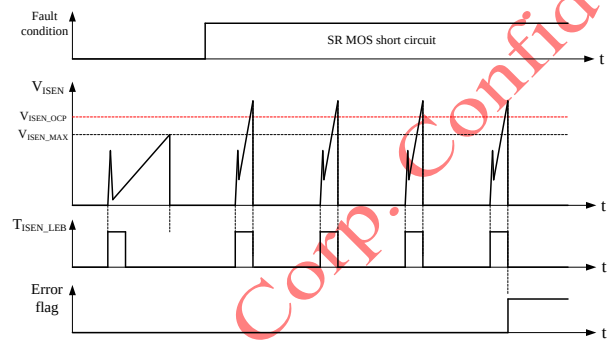


Fig.11 Timing diagram of primary OCP

ISEN pin short circuit protection

SY5033A will check if ISEN pin is shorted to GND during each switching cycle. When primary side power MOS is turned on, a blanking time $T_{ISENSHORT\_BLK}$ is adopted, after this blanking time elapse, IC will compare ISEN pin voltage with internal threshold voltage V_{ISEN_SHORT} (typical=50mV), if ISEN pin voltage is lower than this threshold voltage and last for 2 switching cycles, ISEN pin shorted to GND fault is detected, IC will stop switching and then enter auto-recovery mode.

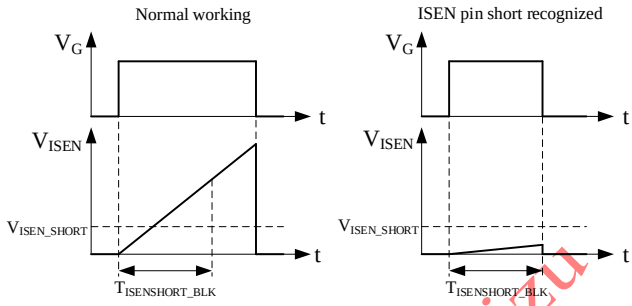


Fig.12 Illustration of ISEN short circuit detecting

Internal OTP

SY5033A monitors die temperature under normal operating mode. Once die temperature rises above internal OTP threshold, IC will stop switching and enter auto-recovery mode. Once die temperature drops below recovery threshold (T_{OTP} -T_{OTP_HYS}), IC will resume normal operating.

Power Supply Design Guard

BUS capacitor calculation

Generally, bulk capacitor C_{BUS} is selected according to below rules:

1~2uF per watt of input power

$$C_{BUS,MIN} = (1.0 \cdot P_{IN})\,uF$$

$$C_{BUS,MAX} = (2.0 \cdot P_{IN})\,uF$$

To be more accurate, BUS capacitor can be selected according to predefined voltage ripple $\triangle V_{BUS}$ on BUS capacitor under minimum AC input voltage and full load condition as shown in below figure.

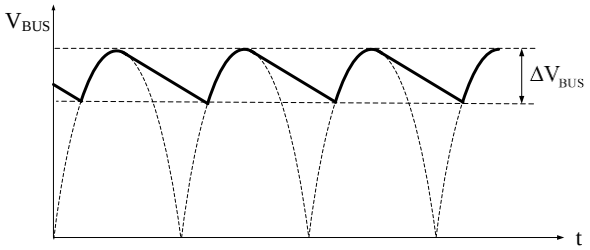


Fig.13 Illustration of voltage ripple on BUS capacitor

When voltage ripple $\triangle V_{BUS}$ is selected, then BUS capacitor can be calculated as below equation:

Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

$$C_{BUS}=\frac{P_O}{\eta\cdot\pi\cdot f_{AC}\cdot\Delta V_{BUS}}\cdot\frac{\arcsin(1-\frac{\Delta V_{BUS}}{\sqrt{2}\cdot V_{IN,MIN}})+\frac{\pi}{2}}{2\sqrt{2}\cdot V_{IN,MIN}-\Delta V_{BUS}}$$

Where P_O is rated output power, $\triangle V_{BUS}$ is predefined voltage ripple on BUS capacitor, η is converter efficiency, f_{AC} is frequency of AC input voltage and $V_{IN,MIN}$ is the minimum AC input voltage.

Transformer parameter calculation

1) Primary/secondary turns ratio: N_{PS}

Maximum allowed N_{PS} is limited by the voltage stress of primary power MOSFET:

$$N_{PS}\le\frac{V_{MOS,BR}\cdot K_{DR}-\sqrt{2}\cdot V_{IN,MAX}-\Delta V_{SN}}{V_{O,MAX}}$$

Where $V_{MOS,BR}$ is the breakdown voltage of primary MOSFET, K_{DR} is V_{DS} de-rating factor of MOSFET, ΔV_{SN} is voltage spike generated when primary MOS is turned off, and $V_{O,MAX}$ is the maximum output voltage.

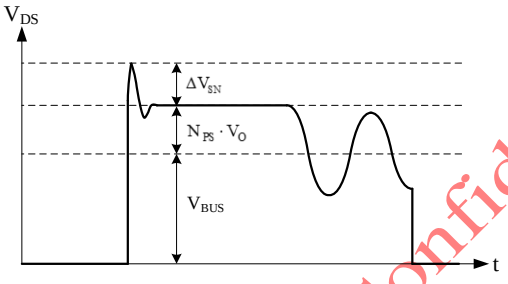


Fig.14 Illustration of voltage spike on primary MOS

2) Primary inductance: L_M

Primary inductance of transformer is related with primary current ripple. Generally, primary side current ripple is defined as shown in below figure. And current ripple factor is defined as below equation:

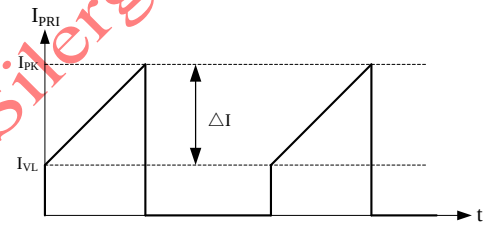


Fig.15 Illustration of primary current ripple

$$K_{RP}=\frac{0.5\cdot\Delta I}{I_{PK}-0.5\cdot\Delta I}$$

K_{RP}<1: CCM
K_{RP}=1: DCM (QR mode)

Generally, to get optimized transformer size and efficiency for universal input application, under low input and full load condition, CCM operating is selected, and under high input and full load condition, QR mode is selected.

Based on design experience, under lowest input voltage and full load condition, it is recommended to choose K_{RP} between 0.3~0.5 for optimized performance. And for an initial start, K_{RP}=0.4 is selected. Once K_{RP} is selected, primary inductance of transformer is calculated as below equation:

$$L_M=\frac{V_{BUS,MIN}^{\ 2}\cdot D_{MAX}^{\ 2}\cdot\eta}{2\cdot P_O\cdot f_{SW}\cdot K_{RP}}$$

Where f_{SW} is rated CCM switching frequency, P_O is rated output power, η is converter efficiency. D_{MAX} is maximum duty cycle at $V_{BUS,MIN}$ and rated output power, and D_{MAX} is calculated as below equation:

$$D_{MAX}=\frac{N_{PS}\cdot V_O}{V_{BUS,MIN}+N_{PS}\cdot V_O}$$

3) Turns of primary winding

(a) Select the magnetic core type, identify the effective cross-sectional area A_E

(b) Preset the maximum magnetic flux density B_{MAX} at minimum BUS voltage and full load condition:

B_{MAX}=0.2T~0.3T

(c) Calculate maximum primary peak current I_{PK} at rated output power:

$$I_{PK}=\frac{V_O\cdot I_O\cdot(1+K_{RP})}{V_{BUS,MIN}\cdot D_{MAX}\cdot\eta}$$

(d) Calculate primary turns: N_P

$$N_P=\frac{L_M\cdot I_{PK}}{B_{MAX}\cdot A_E}$$

Where A_E is effective cross-sectional area of core

4) Turns of secondary winding: N_S

$$N_S=\frac{N_P}{N_{PS}}$$

5) Turns of auxiliary winding: N_A

Turns of auxiliary winding is decided by minimum VCC pin voltage under normal operating. Minimum VCC pin voltage occurs under minimum output voltage. Generally,

Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

minimum VCC pin voltage should be guaranteed to be above 10V. Turns of auxiliary winding can be initially calculated as below equation:

$$N_A = \frac{10 \cdot N_S}{V_{O,MIN}}$$

VCC pin voltage should be checked under minimum output voltage and null load condition, and turns of auxiliary winding should be fine-tuned according to actual test results.

Peak current sense resistor calculation

Under minimum AC input voltage condition, when BUS voltage is maximum value and primary peak current reaches ISEN pin maximum setpoint, maximum output current is reached (OCP point). Under OCP point, primary peak current is calculated as below equations:

$$D_{OCP} = \frac{N_{PS} \cdot V_O}{\sqrt{2} \cdot V_{IN,MIN} + N_{PS} \cdot V_O}$$

$$I_{PK,MAX} = \frac{P_O \cdot K_{OCP}}{\sqrt{2} \cdot V_{IN,MIN} \cdot D_{OCP} \cdot \eta} + \frac{\sqrt{2} \cdot V_{IN,MIN} \cdot D_{OCP}}{2 \cdot L_M \cdot f_{SW}}$$

Where K_{OCP} is OCP proportion, K_{OCP} is generally set to 120%~130%.

$$K_{OCP} = \frac{I_{O,OCP}}{I_O}$$

After maximum primary peak current has been calculated, the peak current sense resistor R_{ISEN} can be easily derived by below equation:

$$R_{ISEN} = \frac{V_{ISEN,MAX}}{I_{PK,MAX}}$$

Where $V_{ISEN,MAX}$ is ISEN pin current sense limit voltage (typical=0.5V).

Customer needs to fine tune the current sense resistor according to the converter actual OCP point. If OCP point is larger than target level, R_{ISEN} should be tuned a little larger, If OCP point is smaller than target level, R_{ISEN} should be tuned a little smaller.

Secondary SR MOS Selection

Under the conditions of the maximum BUS voltage and maximum output voltage, the reverse voltage of secondary rectification diode will reach the maximum level. The maximum value of SR MOS reverse voltage is calculated as below equation:

$$V_{DS(SR),MAX} = \frac{\sqrt{2} \cdot V_{IN,MAX}}{N_{PS}} + V_{O,MAX} + V_{SPIKE}$$

Where $V_{IN,MAX}$ is maximum AC input voltage, N_{PS} is the primary/secondary turns ratio of transformer, $V_{O,MAX}$ is maximum output voltage and V_{SPIKE} is the voltage spike generated when primary MOS is turned on.

Maximum peak current of SR MOS is calculated as equation below:

$$I_{D(SR),MAX} = I_{PK,MAX} \cdot N_{PS}$$

Where $I_{PK,MAX}$ is the maximum primary peak current at $V_{BUS,MIN}$ and OCP point.

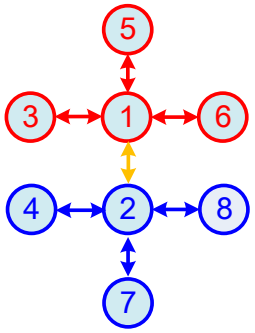
Layout Considerations

A proper PCB design must follow below guidelines:

(a) To achieve good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS capacitor first, then to the switching circuit.

(b) The loop of all switching circuit should be kept as small as possible: primary power loop, secondary power loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ①: Ground of BUS capacitor

Ground ②: Ground of primary IC (SY5033A)

Ground ③: Ground node of auxiliary winding

Ground ④: Ground node of VSEN pin resistor divider

Ground ⑤: Ground of primary side Y capacitor

Ground ⑥: Ground of current sense resistor

Ground ⑦: Ground of VCC pin capacitor

Ground ⑧: Ground of receiver of opto-coupler.

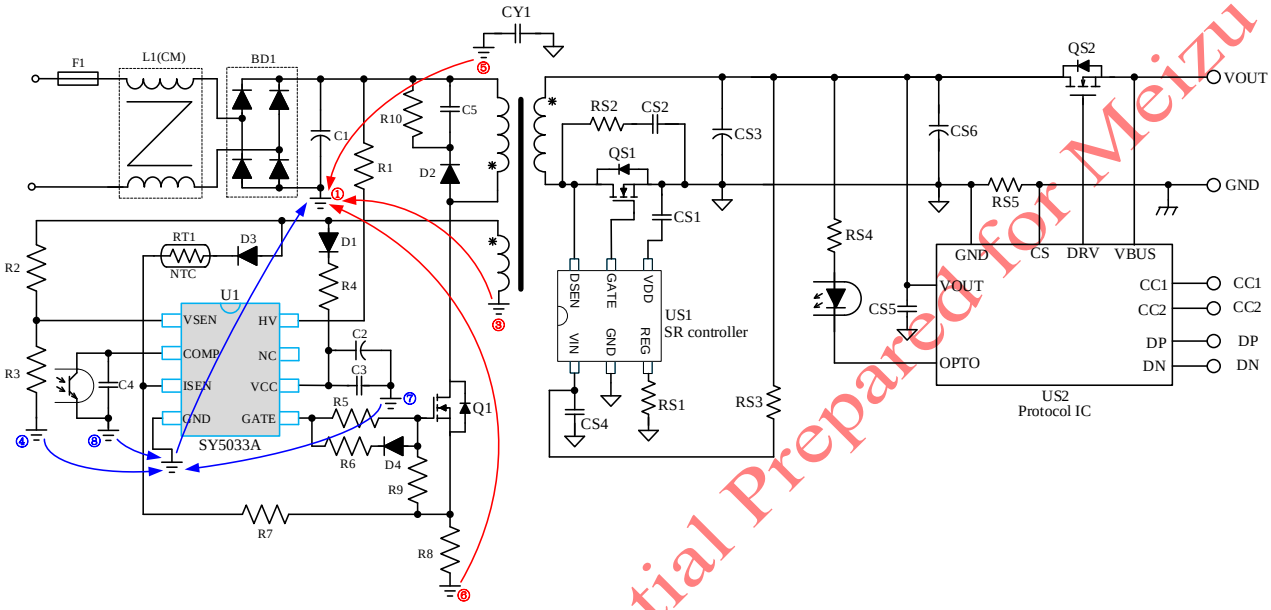
Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

(d) Bias supply trace should be connected to the bias supply capacitor first and then to the GND pin. The bias supply capacitor should be put right beside the IC.

(e) The ceramic capacitor C3 should be mounted as close as possible to IC's VCC and GND pin.

(f) The resistor divider connected to VSEN pin is recommended to be put close to the IC.



Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

Design Example of 65W Quick Charger

A design example of typical application is shown below step by step.

Input/output specification

Parameter	Symbol	Value
Input voltage range	V_{IN}	90~264Vac
AC input frequency	f_{AC}	50Hz
Rated output power	P_O	65W
PDO output	V_O	5V/3A, 9V/3A, 15V/3A, 20V/3.25A
Output OVP threshold	$V_{O,OVP}$	24V
OCP proportion	K_{OCP}	130%

Preset parameter

Parameter	Symbol	Value
Break down voltage of power MOS	$V_{MOS,BR}$	650V
V_{DS} de-rating factor of power MOS	K_{DR}	90%
Spike on V_{DS} during power MOS turn off	ΔV_{SN}	80V
Converter efficiency	η	88%
Primary current ripple factor	K_{RP}	0.4
Voltage ripple on BUS capacitor	ΔV_{BUS}	63V
Input high line condition threshold	$V_{IN,H}$	180Vac
Transformer effective cross-sectional area	A_E	96.6 mm^2 (RM10)
Voltage spike on SR MOS	V_{SPIKE}	7V

1) BUS capacitor selection

Voltage ripple on BUS capacitor is set to: ΔV_{BUS}=63V

$$C_{BUS}=\frac{P_O}{\eta\cdot\pi\cdot f_{AC}\cdot\Delta V_{BUS}}\cdot\frac{\arcsin(1-\frac{\Delta V_{BUS}}{\sqrt{2}\cdot V_{IN,MIN}})+\frac{\pi}{2}}{2\sqrt{2}\cdot V_{IN,MIN}-\Delta V_{BUS}}=\frac{65}{88\%\times3.14\times50\times63}\cdot\frac{\arcsin(1-\frac{63}{\sqrt{2}\times90})+\frac{\pi}{2}}{2\sqrt{2}\times90-63}=81.8uF$$

Select BUS capacitor: C_{BUS} = 82uF

Minimum BUS voltage:

$$V_{BUS,MIN}=\sqrt{2}\cdot V_{IN,MIN}-\Delta V_{BUS}=\sqrt{2}\times90-63=64V$$

2) Transformer design

(a)Calculate primary/secondary turns ratio: N_{PS}

Maximum output voltage: $V_{O,MAX}$=20V

$$N_{PS}\le\frac{V_{MOS,BR}\cdot K_{DR}-\sqrt{2}V_{IN,MAX}-\Delta V_{SN}}{V_{O,MAX}}=\frac{650\times0.9-\sqrt{2}\cdot264-80}{20}=6.58$$

N_{PS} is selected to: $N_{PS}=6$

(b) Calculate maximum duty cycle D_{MAX} at minimum BUS voltage and rated output power condition

Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

$$D_{MAX} = \frac{N_{PS} \cdot V_{O,MAX}}{V_{BUS,MIN} + N_{PS} \cdot V_{O,MAX}} = \frac{6 \times 20}{64 + 6 \times 20} = 65.2\%$$

(c) Calculate primary inductance: L_M

$$L_M = \frac{V_{BUS,MIN}^{\ 2} \cdot D_{MAX}^{\ 2} \cdot \eta}{2 \cdot P_O \cdot f_{SW} \cdot K_{RP}} = \frac{64^2 \times 65.2\%^2 \times 88\%}{2 \times 65 \times 65k \times 0.4} = 453.3uH$$

Select $L_M = 450uH$

(d)Calculate primary peak current at minimum BUS voltage and rated output power condition:

$$I_{PK} = \frac{P_O}{V_{BUS,MIN} \cdot D_{MAX} \cdot \eta} + \frac{V_{BUS,MIN} \cdot D_{MAX}}{2 \cdot L_M \cdot f_{SW}} = \frac{65}{64 \times 65.2\% \times 88\%} + \frac{64 \times 0.652}{2 \times 450u \times 65k} = 2.48A$$

(e)Calculate primary winding turns: N_P

Transformer core effective cross-sectional area: $A_E = 96.6 \cdot 10^{-6} m^2$

Maximum allowed flux density at rated output power: $B_{MAX} = 0.27T$

$$N_P = \frac{L_M \cdot I_{PK}}{B_{MAX} \cdot A_E} = \frac{450u \times 2.48}{0.27 \times 96.6 \times 10^{-6}} = 42.8$$

Select primary winding turns: N_P=42

(f) Calculate secondary winding turns: N_S

$$N_S = \frac{N_P}{N_{PS}} = \frac{42}{6} = 7$$

Select secondary turns: N_S=7

(g) Calculate auxiliary winding turns: N_A

Minimum VCC pin voltage is set to: $V_{CC(AUX)}$=10V

$$N_A = \frac{V_{CC(AUX)} \cdot N_S}{V_{O,MIN}} = \frac{10 \times 7}{3.3} = 21.2$$

Select auxiliary winding turns: N_A=21

Note: Auxiliary winding turns should be fine-tuned according to actual VCC pin voltage under minimum output voltage and no-load condition

(h) If other transformer core type is selected, then re-calculate (e)~(g).

3) Current sense resistor calculation:

(a)Calculate duty cycle under minimum input voltage (maximum BUS voltage): D_{OCP}

$$D_{OCP} = \frac{N_{PS} \cdot V_{O,MAX}}{\sqrt{2} \cdot V_{IN,MIN} + N_{PS} \cdot V_{O,MAX}} = \frac{6 \times 20}{\sqrt{2} \times 90 + 6 \times 20} = 48.5\%$$

(b)Calculate primary side peak current at OCP point: $I_{PK,MAX}$

Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

$$I_{PK,MAX}=\frac{P_O\cdot K_{OCP}}{\sqrt{2}\cdot V_{IN,MIN}\cdot D_{OCP}\cdot\eta}+\frac{\sqrt{2}\cdot V_{IN,MIN}\cdot D_{OCP}}{2\cdot L_M\cdot f_{SW}}=\frac{65\times130\%}{\sqrt{2}\times90\times48.5\%\times88\%}+\frac{\sqrt{2}\times90\times48.5\%}{2\times450u\times65k}=2.61A$$

(c)Calculate current sense resistor: R_{ISEN}

$$R_{ISEN}=\frac{V_{ISEN,MAX}}{I_{PK,MAX}}=\frac{0.5}{2.61}=0.192\Omega$$

Note: ISEN pin current sense resistor R_{ISEN} should be fine-tuned according to the actual OCP point.

4) Secondary SR MOS selection

(a)Maximum reverse voltage calculation:

$$V_{DS(SR),MAX}=\frac{\sqrt{2}\cdot V_{IN,MAX}}{N_{PS}}+V_{O,MAX}+V_{SPIKE}=\frac{\sqrt{2}\times264}{6}+20+7=89.2V$$

Considering voltage derating, SR MOS with 100V rating is recommended.

(b)Maximum instantaneous SR MOS current:

$$I_{D(SR),MAX}=N_{PS}\cdot I_{PK,MAX}=6\times2.61=15.7A$$

5) Calculate VSEN pin resistor divider

(a)Firstly, calculate VSEN pin upper resistor: R_H

Predefined input voltage high line condition threshold: $V_{IN,H}$=180Vac

$$R_H=\frac{\sqrt{2}\cdot V_{IN,H}}{I_{IN,H}}\cdot\frac{N_A}{N_P}=\frac{\sqrt{2}\cdot180}{300u}\cdot\frac{21}{42}=424.3k\Omega$$

Select R_H=420kΩ

(b) After R_H is determined, then calculate lower resistor R_L:

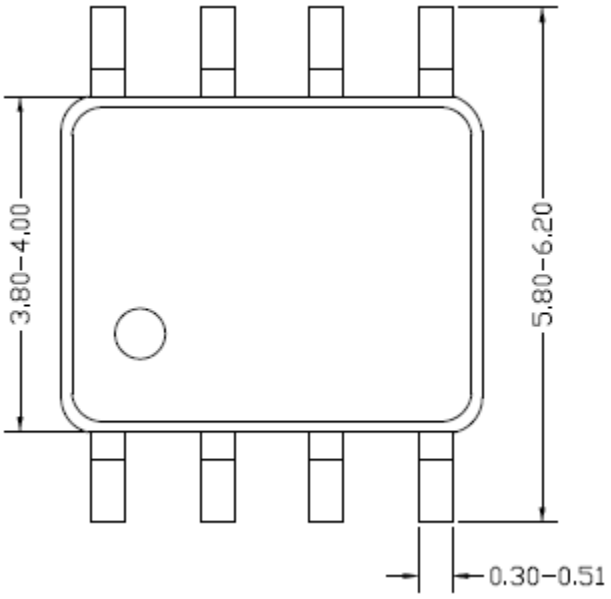
$$R_L=\frac{1}{\frac{V_{O,OVP}}{V_{VSEN,OVP}}\cdot\frac{N_A}{N_S}-1}\cdot R_H=\frac{1}{\frac{24}{2}\cdot\frac{21}{7}-1}\cdot420k=19.4k\Omega$$

Select R_L=19 kΩ

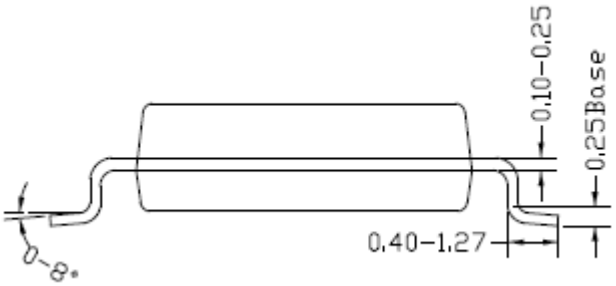
Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.

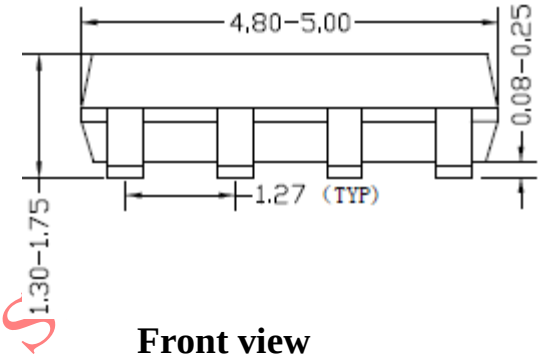
SO8 Package outline & PCB layout design



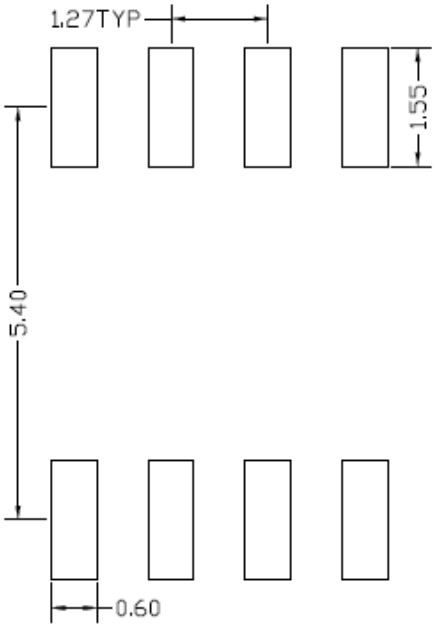
Top view



Side view



Front view



Recommended Pad Layout
(Reference only)

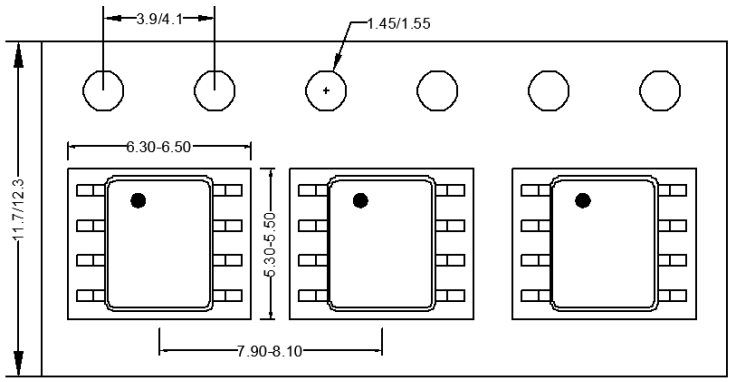
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Meizu
Confidential P
S

© 2023 Silergy Corp. All Rights Reserved.

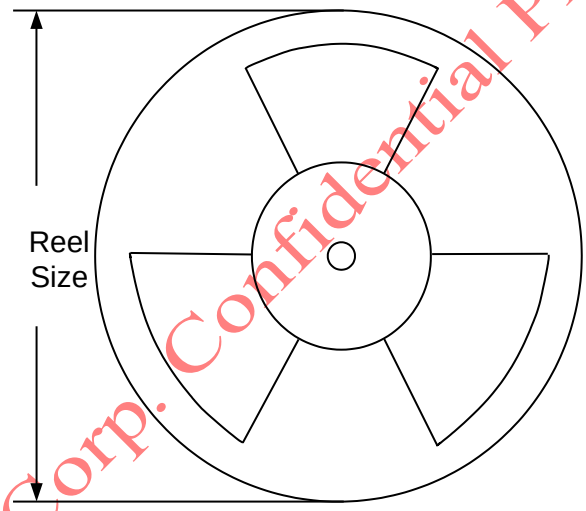
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Silergy Corp. Confidential Prepared for Meizu

© 2023 Silergy Corp. All Rights Reserved.