1. DESCRIPTION

The XD07 and XL07Z devices offer low offset and long-term stability by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common- mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

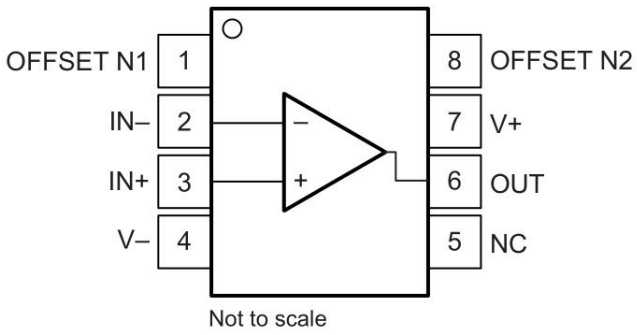
2. FEATURES

- Low noise
- No external components required
- Replace chopper amplifiers at a lower cost
- Wide input-voltage range:

  0 V to ±14 V (typ, ±15-V supply)
- Wide supply-voltage range: ±3 V to ±18V

3. PIN CONFIGURATIONS AND FUNCTIONS

XD07
XL07Z

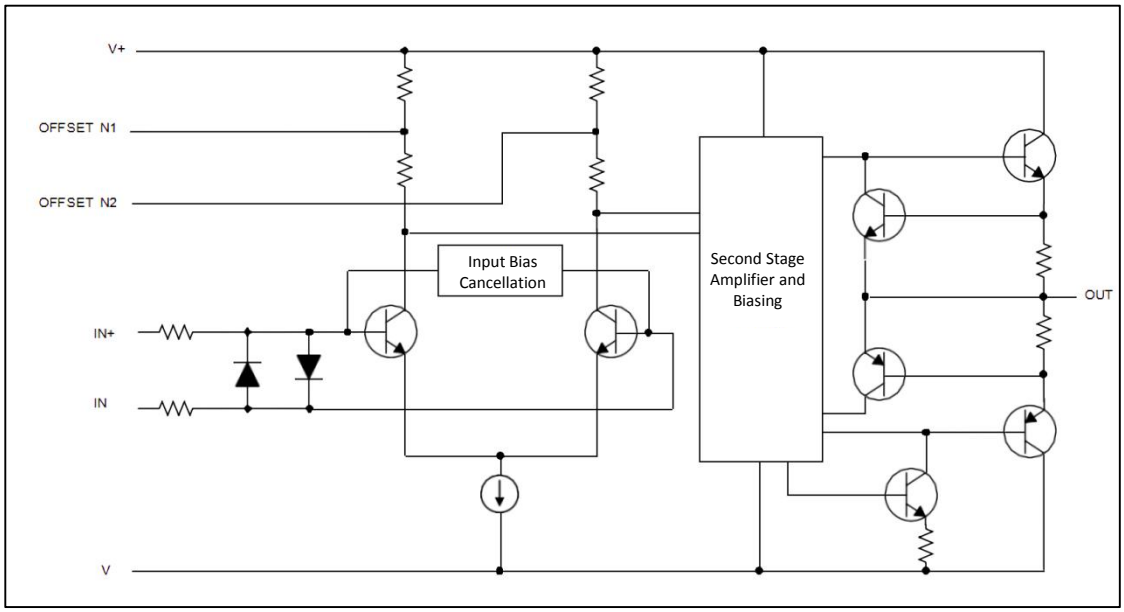


(Top View)

Table 2. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
OFFSET N1	1	Input	External input offset voltage adjustment
IN–	2	Input	Inverting input
IN+	3	Input	Noninverting input
V–	4	—	Negative supply
NC	5	—	Do not connect
OUT	6	Output	Output
V+	7	—	Positive supply
OFFSET N2	8	Input	External input offset voltage adjustment

4. FUNCTIONAL BLOCK DIAGRAM



Block Diagram

REMARK:

1) The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current- gain betas (β), collector or emitter resistors, and so on. The input offset pins allow the designer to adjust for these mismatches by external circuitry.
2) The slew rate is the rate at which an operational amplifier can change the output when there is a change on the input. The XL07Z have a 0.3-V/μs slew rate.
3) The XL07Z are powered on when the supply is connected. The devices can be operated as single-supply operational amplifiers or dual-supply amplifiers, depending on the application.

5. SPECIFICATIONS

5.1. Absolute Maximum Ratings (1)

			MIN	MAX	UNIT
V_S	Supply voltage(2)	Single supply		40	V
		Dual supply		±20	
	Input voltage	Differential(3)		±28	V
		Single-ended(4)		±20	
	Output short-circuit(5)		Continous		
T_J	Operating junction temperature		–40	85	°C
T_{stg}	Storage temperature		–55	125	°C

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltage values, unless otherwise noted, are with respect to the midpoint between V+ and V−.

[3] Differential voltages are at IN+ with respect to IN−.

[4] The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

[5] The output can be shorted to ground or to the negative power supply. Fast ramping shorts to the positive supply can cause permanent damage and eventual destruction.

5.2. Thermal Resistance Characteristics

THERMAL METRIC		XL07Z D (SOP) 8 PINS	XD07 P (DIP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.6	85	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.1	68.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.4	55.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.7	38.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.6	55.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

5.3. ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±1000	V
		Charged-devicemodel (CDM),per JEDEC specification JESD22-C101 [2]	±1000	

[1] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

[2] JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4. Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single supply	6		36	V
		Dual supply	±3		±18	
V_{CM}	Common-mode input voltage	V_S = ±15 V	–13		13	V
T_A	Operating ambient temperature		-40		85	℃

5.5. Electrical Characteristics

at TA = 25°C, VS = ±15 V, RL = 2 kΩ connected to mid-supply, and VCM = VOUT = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	XD07			±60		μV
			T_A = -40°C to 85°C		±85		
		XL07Z				±150	
			T_A = -40°C to 85°C			±250	
dV_{OS}/dT	Input offset voltage drift	T_A = -40°C to 85°C	XD07		±0.5		μV/°C
			XL07Z			±2.5	
	Long-term drift of input offset voltage				±0.4		μV/mo
	Offset adjustment range	R_s = 20 kΩ			±4		mV
PSRR	Power supply rejection ratio	V_S = ±3 V to ±18 V			7	32	μV/V
			T_A = -40°C to 85°C		10	51	
INPUT BIAS CURRENT							
I_B	Input bias current	XD07			±1.8		nA
			T_A = -40°C to 85°C		±2.2		
		XL07Z				±12	
			T_A = -40°C to 85°C			±14	
	Input bias current drift	XD07			±18		pA/°C
		XL07Z				±50	
I_{OS}	Input offset current	XD07			±0.8		nA
			T_A = -40°C to 85°C		±1.6		
		XL07Z				±6	
			T_A = -40°C to 85°C			±8	
	Input offset current drift	XD07			12		pA/°C
		XL07Z				±50	

Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.38		μV_{PP}
e_N	Input voltage noise density	f = 10 Hz			10.5		$nV/\sqrt{Hz}$
		f = 100 Hz			10.2		
		f = 1 kHz			9.8		
	Input current noise	f = 0.1 Hz to 10 Hz			15		pA_{pp}
i_N	Input current noise density	f = 10 Hz			0.35		$pA/\sqrt{Hz}$
		f = 100 Hz			0.15		
		f = 1 kHz			0.13		
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage			±13	±14		V
		T_A = -40°C to 85°C		±13	±13.5		
CMRR	Common-mode rejection ratio	XD07 V_{CM} = ±13 V		100	120		dB
			T_A = -40°C to 85°C	97	120		
		XL07Z V_{CM} = ±13 V		94	110		
			T_A = -40°C to 85°C	94	106		
INPUT CAPACITANCE							
r_I	Input resistance			7	33		MΩ
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	1.4 V < V_O < 11.4 V, R_L = 500 kΩ	XD07	100	400		V/mV
			XL07Z		400		
		V_O = ±10 V		120	400		
			T_A = –40°C to +85°C	100	400		
FREQUENCY RESPONSE							
	Unity gain bandwidth			0.4	0.6		MHz
SR	Slew rate	V_S = 5 V, R_L = 2 kΩ			0.3		V/µs
OUTPUT							
	Voltage output swing			±11.5	±12.8		V
		T_A = -40°C to 85°C		±11	±12.6		
		R_L = 10 kΩ		±12	±13		
		R_L = 1 kΩ			±12		
POWER SUPPLY							
P_D	Power dissipation	No load			80	150	mW
		V_S = ±3 V, no load			4	8	

[1] The specifications listed in the Electrical Characteristics apply to XD07 and XL07Z.

[2] Because long-term drift cannot be measured on the individual devices before shipment, this specification is not intended to be a warranty. This specification is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first 30 days of operation.

5.6. Typical Charateristic

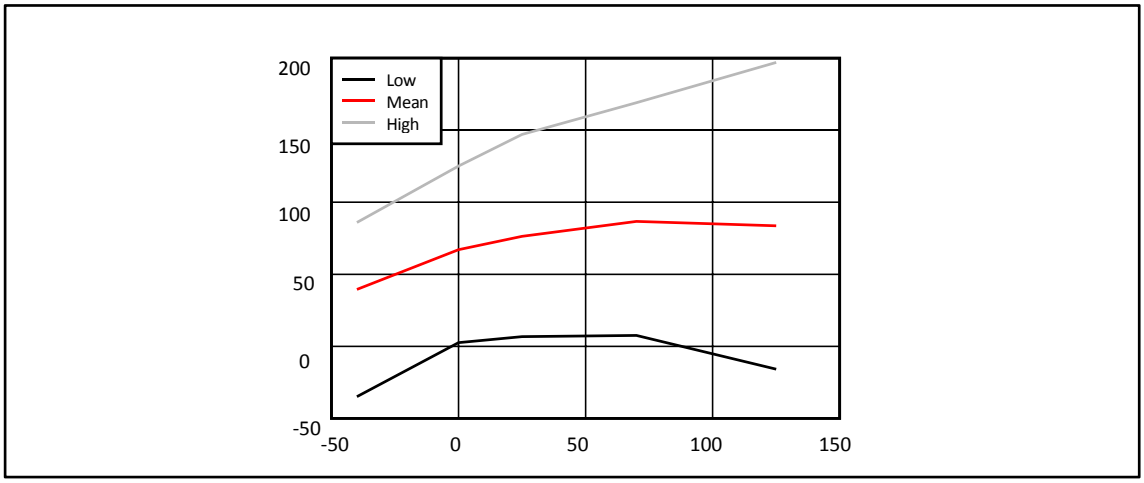


Figure 5-1. Input-Offset Voltage vs Temperature

6. Detailed Description

6.1. Overview

These devices offer low offset and long-term stability by means of a low-noise, chopperless, bipolar-input- transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common- mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

These devices are characterized for operation from -40°C to 85°C.

6.2. Application Information

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current- gain betas (β), collector or emitter resistors, and so on. The input offset pins allow the designer to adjust for these mismatches with external circuitry. Figure 4 shows how these input mismatches can be adjusted by putting resistors or a potentiometer between the null pins. Use a potentiometer to fine tune the circuit during testing or for applications that require precision offset control. For more information about designing using the input-offset pins, see the Nulling Input Offset Voltage of Operational Amplifiers application report.

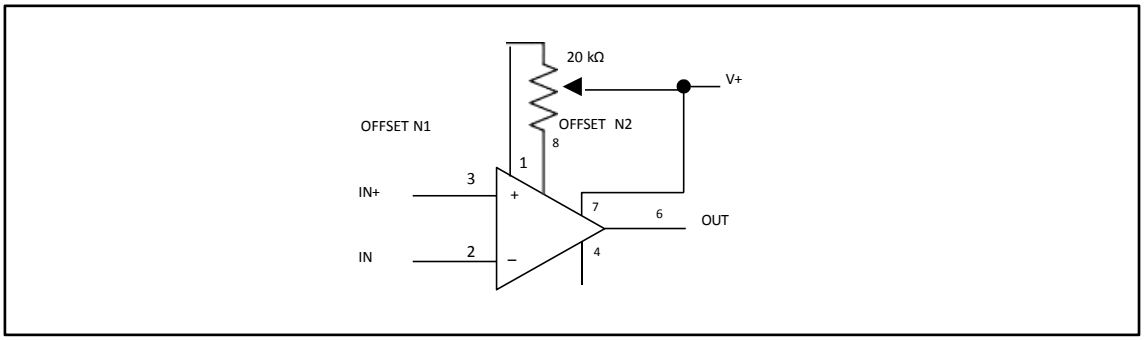


Figure 6-1. Input Offset-Voltage Null Circuit

6.3. Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal is used to drive a relatively high current load. This circuit is also called a buffer amplifier or unity gain amplifier. The inputs of an operational amplifier have a very high resistance that puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so the amplifier can provide as much current as necessary to the output load.

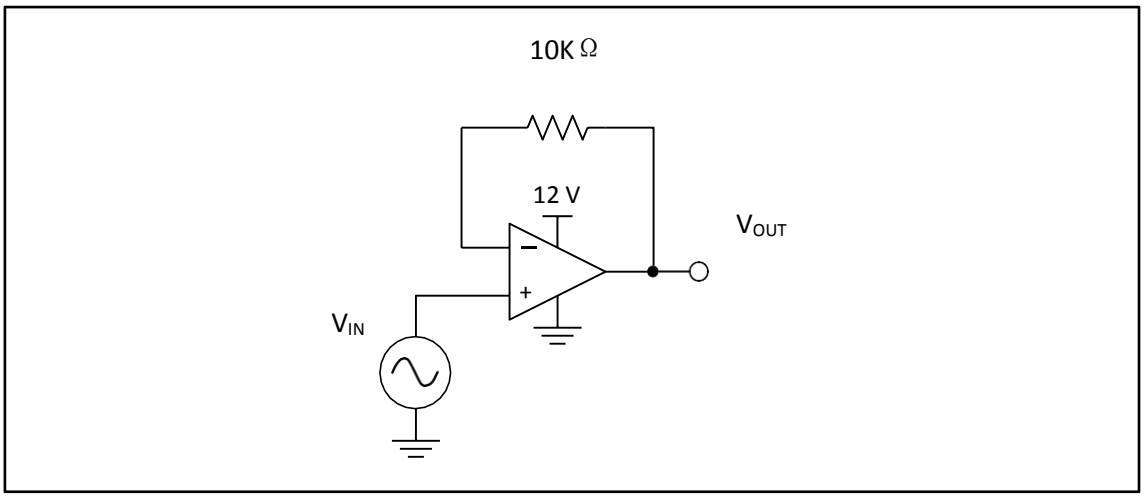


Figure 6-2. Voltage Follower Schematic

6.3.1. Design Requirements

- Output range of 2 V to 11 V
- Input range of 2 V to 11 V

6.3.2. Output Voltage Swing

The output voltage of an operational amplifier is limited by the internal circuitry to some level less than the supply rails. For this amplifier, the output voltage swing is within ±12 V, which accommodates the input and output voltage requirements.

6.3.3. Supply and Input Voltage

For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The chosen amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 11 V, the supply voltage must be 12 V. Using a negative voltage on the lower rail, rather than ground, allows the amplifier to maintain linearity for inputs below 2 V.

6.3.4. Application Curves

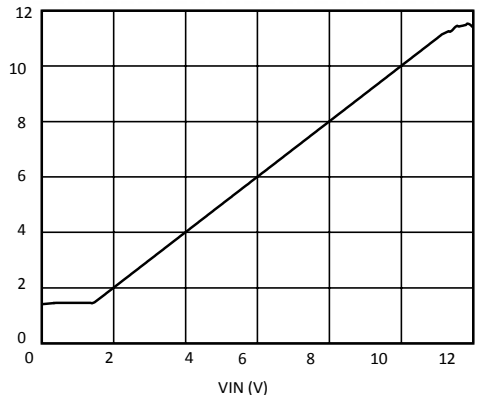


Figure 6-3. Output Voltage vs Input

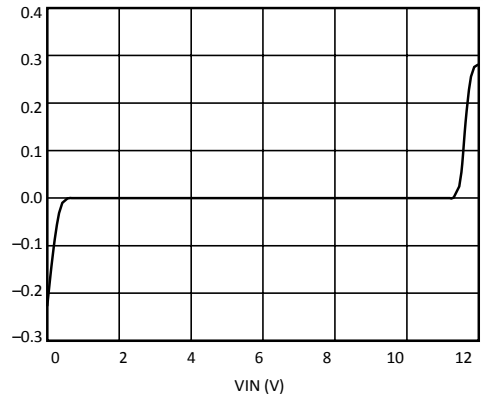


Figure 6-4. Current Drawn by the Input of the Voltage Follower (IIO) vs Input Voltage

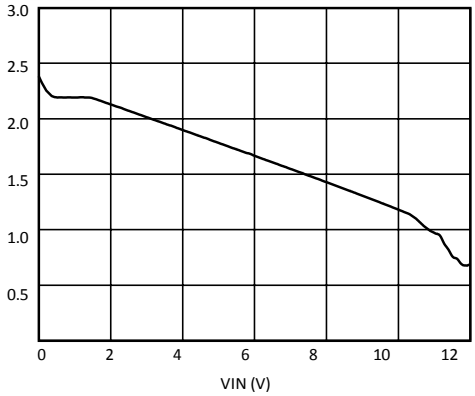


Figure 6-5. Current Drawn from Supply (ICC) vs Input Voltage

6.4. Power Supply Recommendations

The XL07x operate from ±3 V to ±18 V supplies; many specifications apply from -40°C to 85°C.

CAUTION
Supply voltages larger than ±20 V can permanently damage the device. See also *Section 5.1*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more details on bypass capacitor placement.

6.5. Layout

6.5.1. Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. On multilayer PCBs, one or more layers are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicularly, as opposed to in parallel, with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

6.5.2. Layout Example

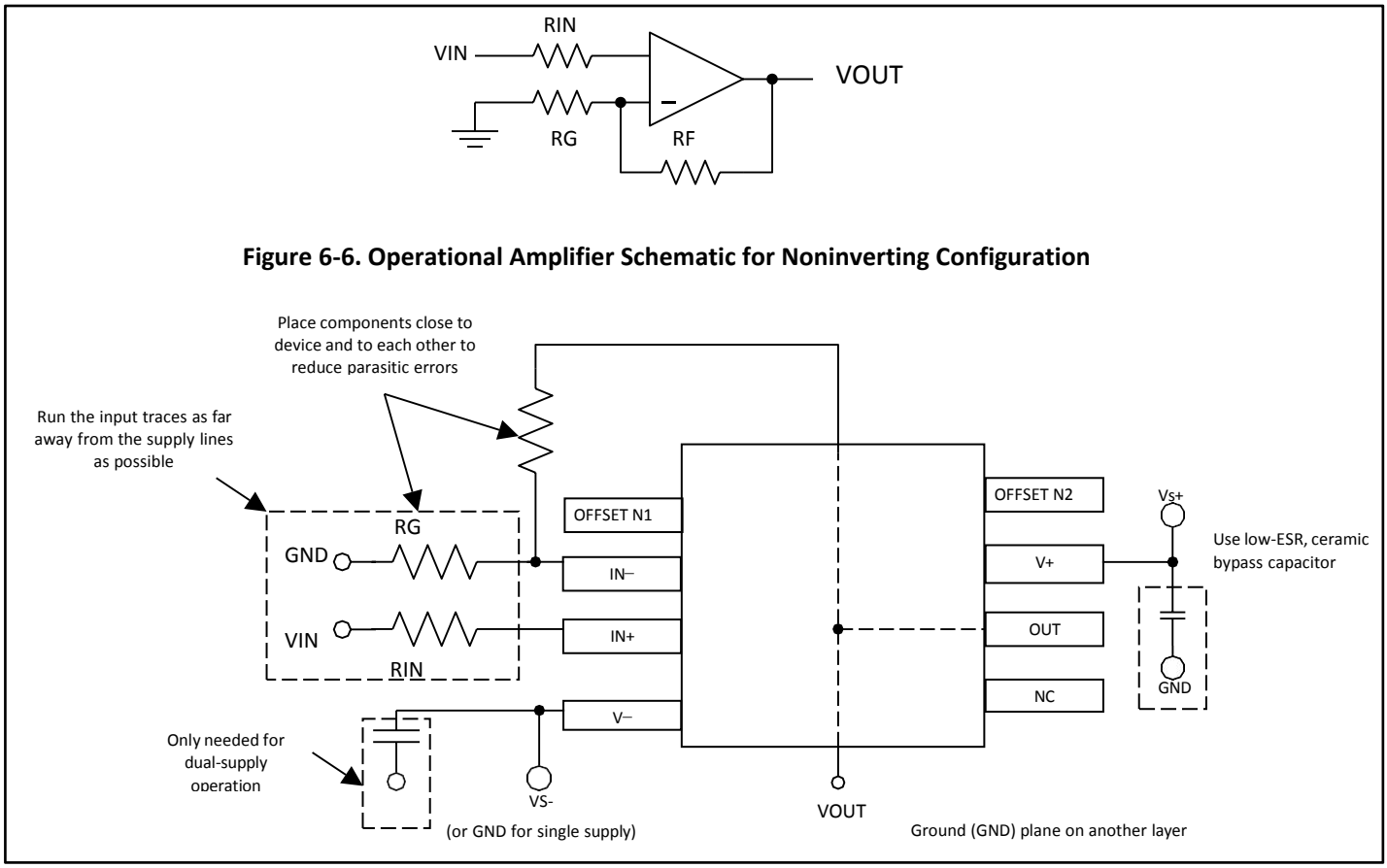


Figure 6-6. Operational Amplifier Schematic for Noninverting Configuration

Figure 6-7. Operational Amplifier Board Layout for Noninverting Configuration

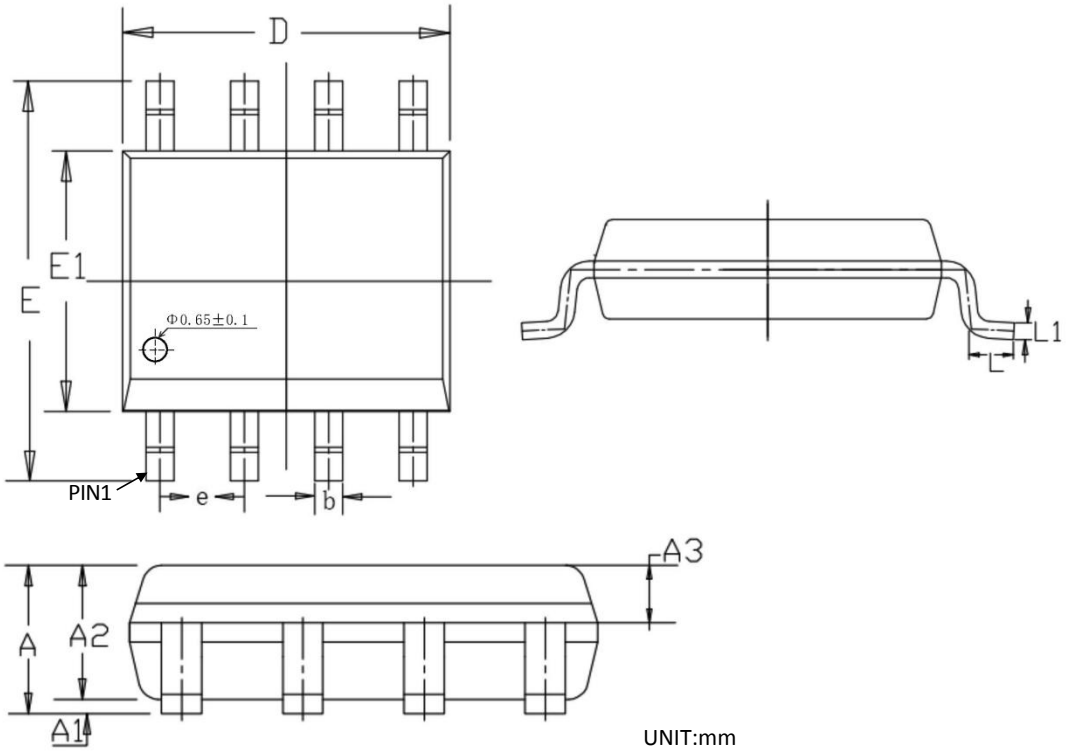
7. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL07Z	XL07Z	SOP8	4.90 * 3.90	-40 to +85	MSL3	T&R	2500
XD07	XD07	DIP8	9.25 * 6.38	-40 to +85	MSL3	Tube 50	2000

8. DIMENSIONAL DRAWINGS

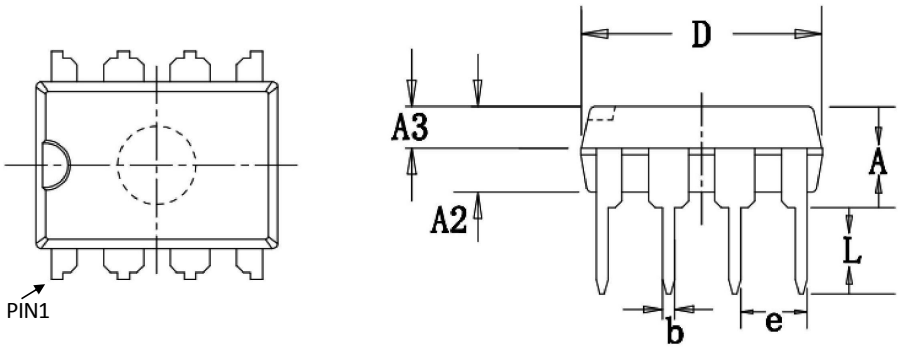
SOP8

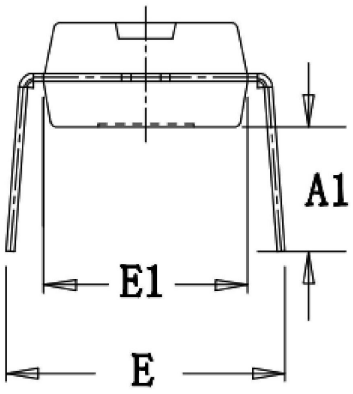


UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D(长度)	4.800	4.900	5.000
D	5.800	6.000	6.200
E	3.800	3.900	4.000
E1	0.450	0.600	0.750
L	—	0.25BSC	—

DIP8





UNIT:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1	3.786	3.886	3.986
A2	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	–	0.490
e	2.510	2.540	2.570
D	9.150	9.250	9.350
E	7.800	8.500	9.200
E1	6.280	6.380	6.480
L	3.000	–	–