

1. DESCRIPTION

XL549 is an 8-bit serial A/D converter chip, which adopts CMOS technology and realizes A/D conversion by 8-bit switching capacitor successive approximation method. It can be serial interface with general microprocessor and controller through CLK, CS and DATAOUT, and constitute a variety of cheap measurement and control application systems. With a 4MHz on-chip system clock and hardware and software control circuit, the conversion time is up to 17 μ s, and the XL549 sampling is 40,000 times /s.

The maximum total out-of-balance error of other functions is $\pm 0.5\text{LSB}$, and the typical power consumption is 6mW. Differential reference voltage high resistance input, anti-interference, can be calibrated according to the proportional scale conversion range, $V_{\text{REF+}}-V_{\text{REF-}}\geq 1\text{V}$, can be used for small signal sampling.

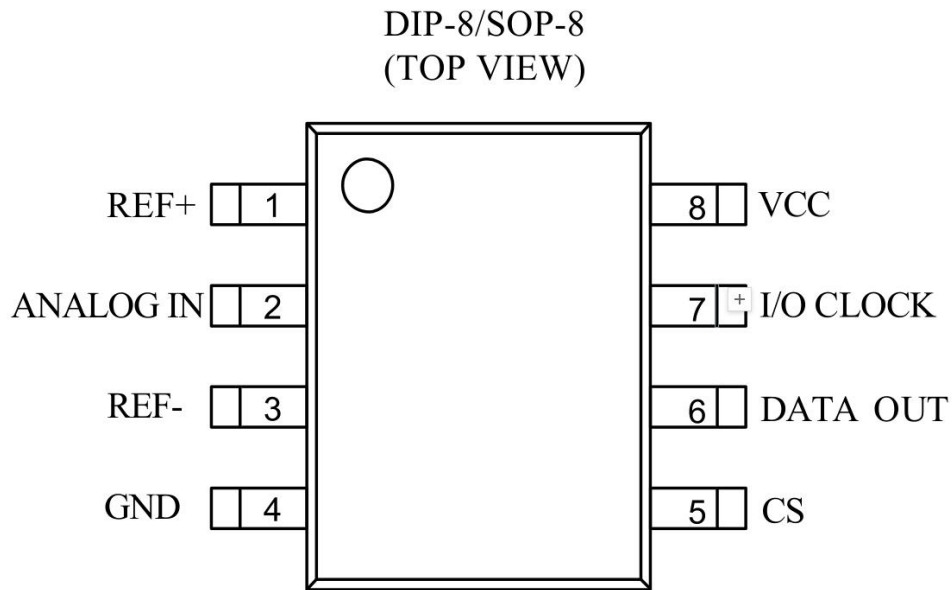
2. FEATURES

- Adopts three-wire serial mode and microprocessor interface
- 8-bit resolution AD converter
- Typical internal system clock of 4MHz
- On-chip sampling and holding circuit, conversion time $\leq 17\mu\text{s}$
- Differential voltage input
- Wide operating voltage 3V-6.5V
- Low power consumption 15mW
- Total offset error is $\leq \pm 0.5\text{LSB}$
- Sampling speed 40000 times /S
- An internal 4MHz system clock is provided on chip and is independent of the external I/OCLOCK for operation control
- Available package : SOP8 (XL549) , DIP8 (XD549)

3. TYPICAL APPLICATION

- Handheld device
- Portable monitors and power management
- Industrial signal monitoring
- Measurement and control instrument

4. PIN CONFIGURATIONS AND FUNCTIONS



Pin Functions

| Pin | Symbol | Description |
|-----|-----------|---|
| 1 | REF+ | Positive reference voltage input $2.5V \leq REF+ \leq V_{CC} + 0.1$ |
| 2 | ANALOG IN | Analog signal input |
| 3 | REF- | Negative reference voltage input, $-0.1V \leq REF- \leq 2.5V$ |
| 4 | GND | ground |
| 5 | CS | Chip selection end |
| 6 | DATA OUT | Data conversion interface output |
| 7 | I/O CLOCK | External clock input |
| 8 | VCC | supply voltage |

5. LIMITING PARAMETER

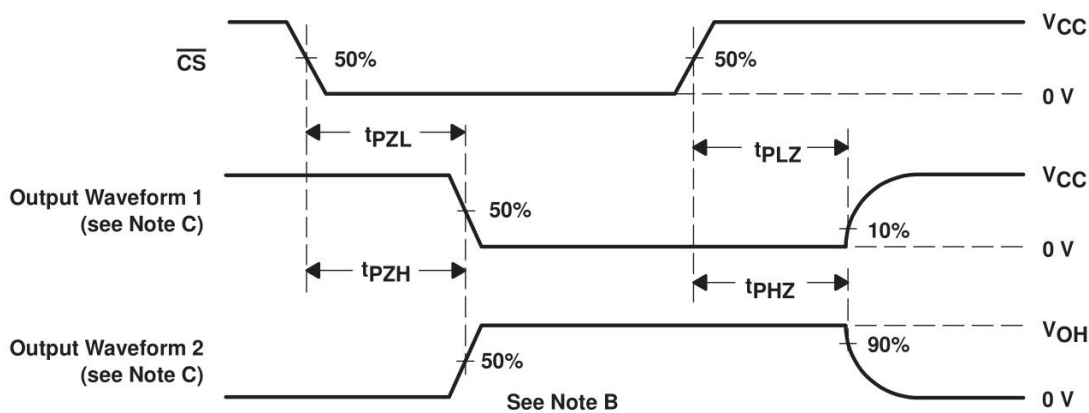
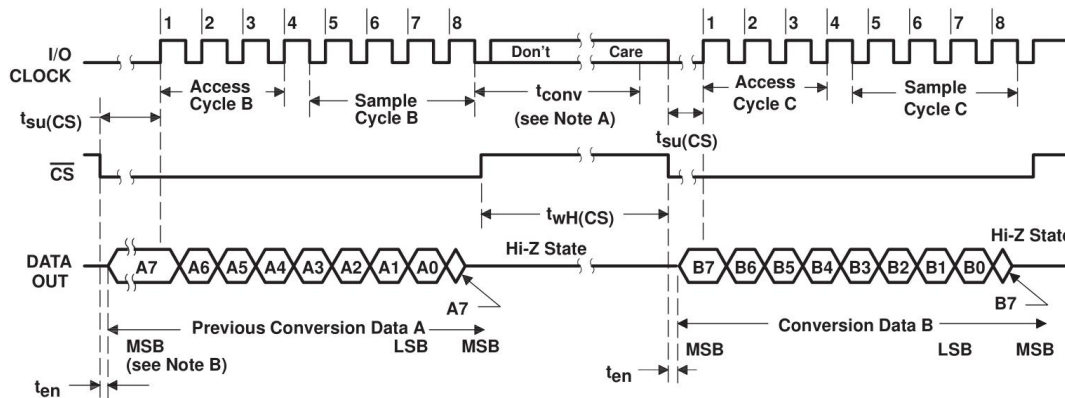
| | |
|--|-----------------------|
| Supply voltage, VCC | 6.5 V |
| Input voltage range at any input | -0.3 V to VCC + 0.3 V |
| Output voltage range | -0.3 V to VCC + 0.3 V |
| Peak input current range (any input) | ± 10 mA |
| Peak total input current range (all inputs) | ± 30 mA |
| Operating free-air temperature range, TA | 0°C to 70°C |
| Storage temperature range, Tstg | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

6. ELECTRICAL CHARACTERISTIC

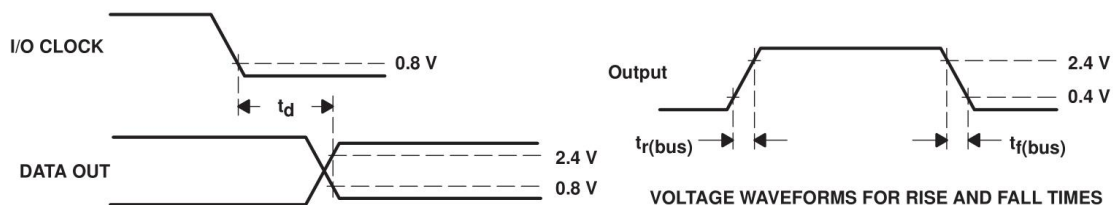
(VIN=5V, unless otherwise noted, TA=-40 ° C to 85 ° C, typical values measured at ambient temperatures of 25 ° C)

| Symbol | Parameter | Conditions | Min | TYPE | Max | Unit |
|----------------------------------|---|---------------------|--------------|------|------|------------------|
| VCC | Supply voltage | | 3 | 5 | 6 | V |
| VOH | High-level output voltage | VCC=4.75V | 2.4 | | | V |
| VOL | Low-level output voltage | VCC=4.75V | | | 0.4 | V |
| IOZ | High-impedance off-state output current | VO=VCC | | | 10 | μA |
| | | VO=0 | | | -10 | |
| IIH | High-level input current, control inputs | VI=VCC | 0.005 2.5 | | | μA |
| IIL | Low-level input current, control inputs | VI=0 | -0.005 | | -2.5 | μA |
| II(on) | Analog channel on-state input current during sample cycle | Analog input at VCC | 0.4 | | | μA |
| | | Analog input at 0 V | 1.8 | | -1 | μA |
| ICC | Operating supply current | CS at 0V | 1.9 3 | | 2.5 | mA |
| ICC +Iref | Linearity error | Vref+=VCC | | | | mA |
| EL | Full-scale error | | | | ±0.5 | LSB |
| EZS | Zero-scale error | | | | ±0.5 | LSB |
| EFS | Conversion time | | | | ±0.5 | LSB |
| tconv | Conversion time | | | 12 | 17 | μA |
| Total access and conversion time | | | | 19 | 25 | μA |
| ta | Channel acquisition time(sample cycle) | | | 4 | | I/O clock cycles |
| tv | Time output data remains valid after I/O CLOCK↓ | | | 10 | | ns |
| td | Time output data output valid | | | 400 | | ns |
| ten | Output enable time | | | 1.4 | | μA |
| tdis | Data bus fall time | | | 150 | | ns |
| tr(bus) | | | | 300 | | ns |
| Tf(bus) | | | | 300 | | ns |

7. TIMING CHART AND DESCRIPTION



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

The usual control sequence is:

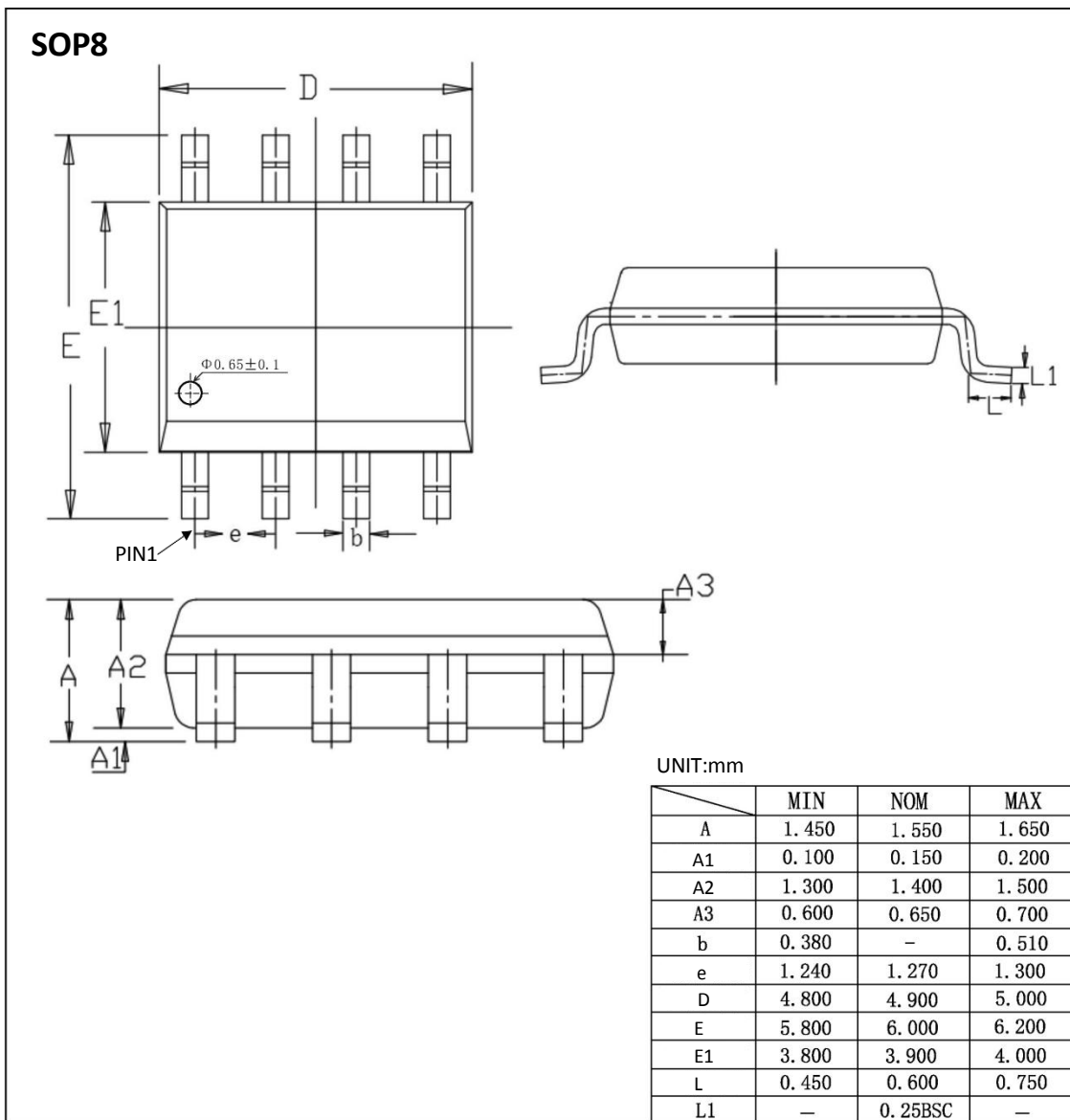
- (1) Set CS low. After measuring the CS falling edge, the internal circuit waits for two internal clock rising edges and a falling edge, then confirms the change, and finally automatically outputs the highest bit (D7) of the previous conversion result to the DATAOUT terminal.
- (2) The falling edge of the first four I/O CLOCK cycles moves out of the second, third, fourth, and fifth bits (D6, D5, D4, D3), and the on-chip sampling hold circuit starts sampling the analog input at the fourth I/O CLOCK falling edge.
- (3) The falling edge of the next three I/O CLOCK cycles moves out of the 6, 7, 8 (D2, D1, D0) transitions
- (4) The falling edge of the on-chip sampling-hold circuit at the 8th I/O CLOCK cycle moves out the 6th, 7th, 8th (D2, D1, D0) conversion bits. The hold function will last for 4 internal clock cycles and then begin A/D conversion for 32 internal clock cycles. After the eighth I/O CLOCK, CS must be high, or I/O CLOCK must remain low for 36 internal system clock cycles Completion of work to be maintained and converted. If there is a valid interference pulse on I/O CLOCK when CS is low, the microprocessor/controller will lose synchronization with the device's I/O timing. An effective low level occurs if CS is high.
- (5) To sample the analog signal at a specific time, the falling edge of the 8th I/O CLOCK clock should correspond to that time, because the chip starts sampling at the falling edge of the 4th I/O CLOCK clock, but starts saving at the falling edge of the 8th I/O CLOCK clock.

8. ORDERING INFORMATION

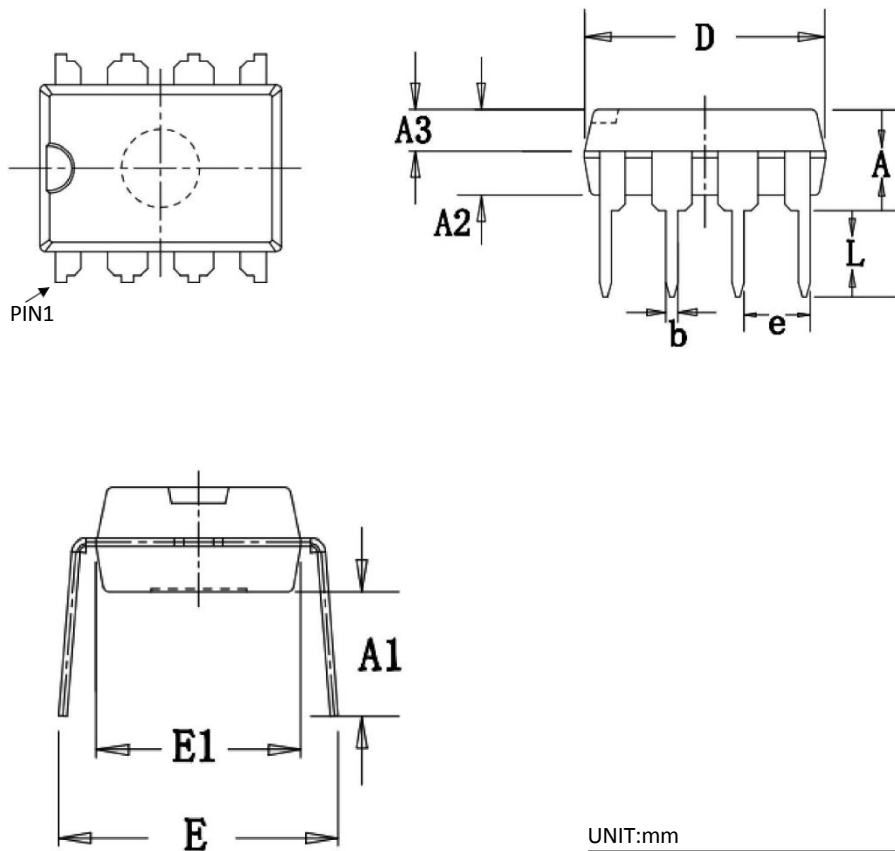
Ordering Information

| Part Number | Device Marking | Package Type | Body size (mm) | Temperature (°C) | MSL | Transport Media | Package Quantity |
|-------------|----------------|--------------|----------------|------------------|------|-----------------|------------------|
| XL549 | XL549 | SOP8 | 4.90 * 3.90 | - 40 to 85 | MSL3 | T&R | 2500 |
| XD549 | XD549 | DIP8 | 9.25 * 6.38 | - 40 to 85 | MSL3 | Tube 50 | 2000 |

9. DIMENSIONAL DRAWINGS



DIP8



UNIT:mm

| | MIN | NOM | MAX |
|----|-------|-------|-------|
| A | 3.600 | 3.800 | 4.000 |
| A1 | 3.786 | 3.886 | 3.986 |
| A2 | 3.200 | 3.300 | 3.400 |
| A3 | 1.550 | 1.600 | 1.650 |
| b | 0.440 | — | 0.490 |
| e | 2.510 | 2.540 | 2.570 |
| D | 9.150 | 9.250 | 9.350 |
| E | 7.800 | 8.500 | 9.200 |
| E1 | 6.280 | 6.380 | 6.480 |
| L | 3.000 | — | — |

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