1. DESCRIPTION

XL548 and XD548 are 8-bit serial A/D converter chip, which adopts CMOS technology and realizes A/D conversion by 8-bit switching capacitor successive approximation method. It can be serial interface with general microprocessor and controller through CLK, CS and DATAOUT, and constitute a variety of cheap measurement and control application systems. With a 4MHz on-chip system clock and hardware and software control circuit, the conversion time is up to 17μs, and the XL548 sampling is 45,500 times /s.

The maximum total out-of-balance error of other functions is ± 0.5LSB, and the typical power consumption is 6mW. Differential reference voltage high resistance input, anti-interference, can be calibrated according to the proportional scale conversion range, VREF+-VREF-≥1V, can be used for small signal sampling.

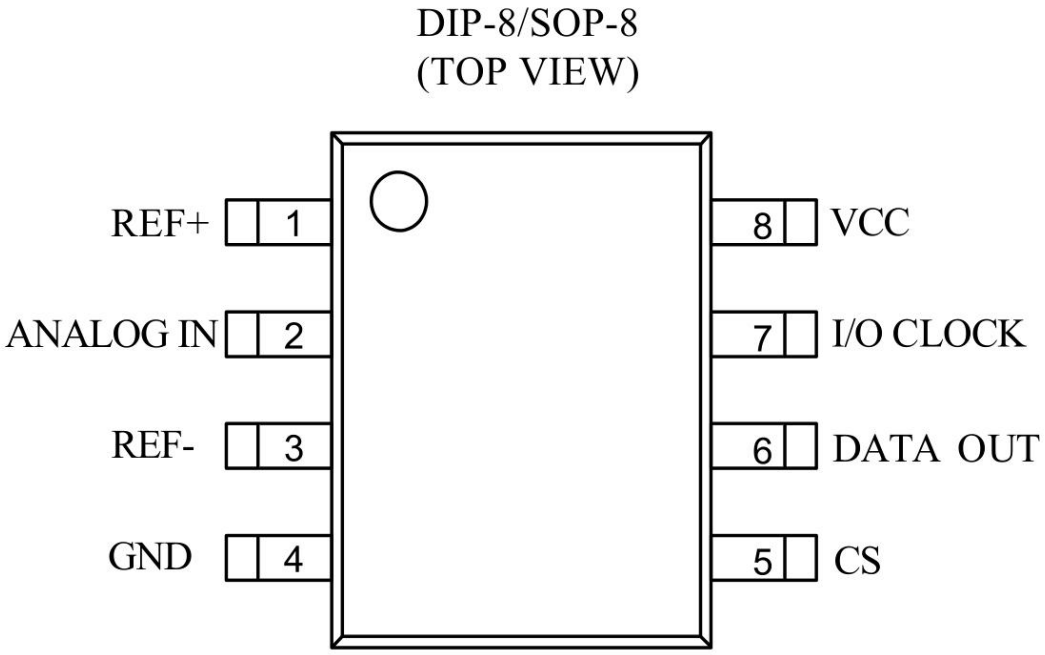
2. FEATURES

- Adopts three-wire serial mode and microprocessor interface
- 8-bit resolution AD converter
- A typical internal system clock of 4MHz
- On-chip sampling and holding circuit, conversion time ≤17us
- Differential voltage input
- Wide operating voltage 3V-6.5V
- Low power consumption 15mW
- Total offset error ≤±0.5LSB
- Sampling speed 45,500 times /S
- An internal 4MHz system clock is provided on chip and is independent of the external I/OCLOCK for operation control
- Package option: XL548 (SOP8) , XD548 (DIP8)

3. TYPICAL APPLICATION

- Handheld device
- Portable monitors and power management
- Industrial signal monitoring
- Measurement and control instrument

4. PIN CONFIGURATIONS AND FUNCTIONS



Pin Functions

Pin	Symbol	Description
1	REF+	Positive reference voltage input 2.5V≤REF+≤Vcc+0.1
2	ANALOG IN	Analog signal input
3	REF—	Negative reference voltage input, -0.1V≤REF-≤2.5V
4	GND	Ground
5	CS	Chip selection end
6	DATA OUT	Data conversion interface output
7	I/OCLOCK	External clock input
8	VCC	Supply voltage

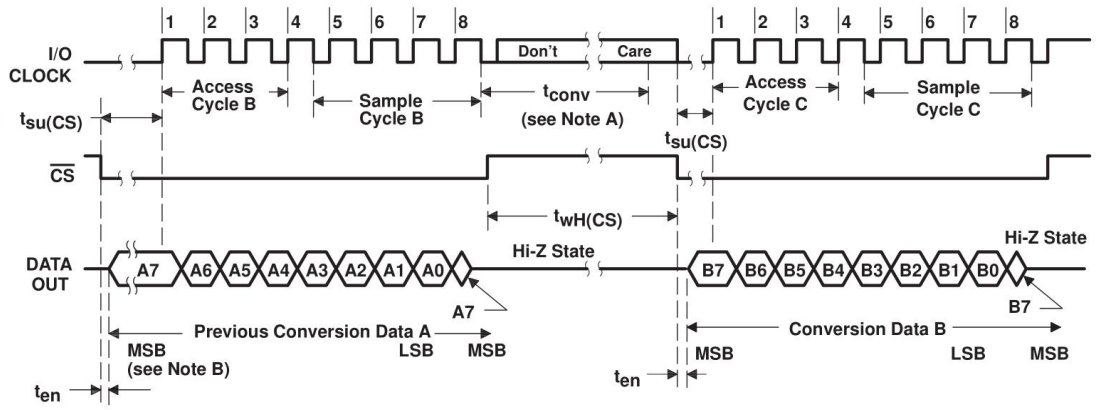
5. LIMITING PARAMETER

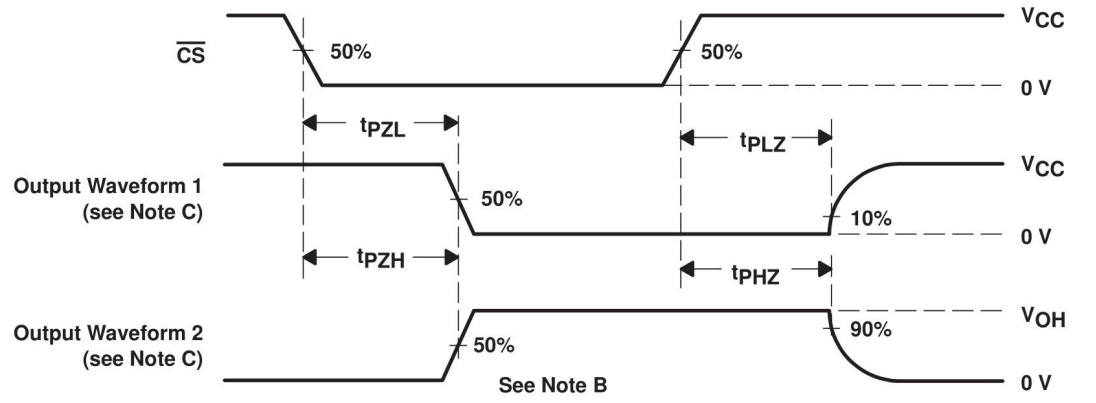
VCC end to GND voltage..... —0.5V to 6.5V
All input pins to GND voltage..... —0.5V to 6V
OUT pin to GND voltage.....V to VCC+0.3V
Vref+ Pin to GND voltage.....V toVCC+0.1V
Vref- Pin to GND voltage.....V
Peak current of all input pins.....±20mA
Storage temperature..... —65℃ to +150℃
Operating ambient temperature..... —40℃ to +85℃
Welding temperature (10 seconds).....+260℃
Maximum junction temperature.....+150℃

6. ELECTRICAL CHARACTERISTIC

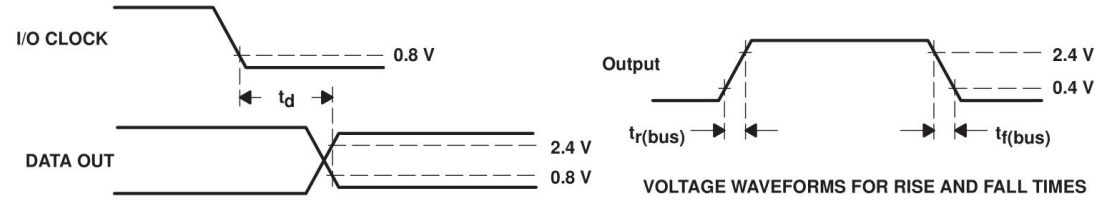
Symbol	Parameter	Conditions	Min	TYPE	Max	Unit
VCC	Supply voltage		3	5	5.5	V
V_{OH}	High-level output voltage	VCC = 4.5 V, IOH = – 1.6 mA	2.4			V
		VCC = 4.5 V to 5.5 V, IOH = – 20 uA	VCC–0.1			
VOL	Low-level output voltage	VCC = 4.5 V, IOL = 1.6 mA			0.4	V
		VCC = 4.5 V to 5.5 V, IOL = 20uA			0.1	
I_{OZ}	Off-state (high-impedance-state) output current	VO = VCC, CS at VCC			10	A
		VO = 0, CS at VCC			–10	
I_{IH}	High-level input current	VI = VCC		0.05		A
I_{IL}	Low-level input current	VI = 0		– 0.005	– 2.5	A
I_{CC}	Operating supply current	CS at 0 V		0.8	2.5	mA
$I_{Leakage}$	Analog input leakage current	VI = VCC			1	A
		VI = 0			–1	
	Maximum static analog	Vref+ = VCC, Vref – = GND			10	A
tsu(CS)	Setup time, CS low before first I/O CLOCK				1.425	s
th(CS)	Hold time, CS low after last I/O CLOCK				0	ns
twH	Pulse duration, I/O CLOCK high				190	ns
twL(I/O)	Pulse duration, I/O CLOCK low				190	ns
tt(CS)	Transition time				10	ns

7. TIMING CHART AND DESCRIPTION





VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

The usual control sequence is:

(1) Set CS low. After measuring the CS falling edge, the internal circuit waits for two internal clock rising edges and a falling edge, then confirms the change, and finally automatically outputs the highest bit (D7) of the previous conversion result to the DATAOUT terminal.

(2) The falling edge of the first four I/OCLOCK cycles moves out of the second, third, fourth, and fifth bits (D6, D5, D4, D3), and the on-chip sampling hold circuit starts sampling the analog input at the fourth I/OCLOCK falling edge.

(3) The falling edge of the next three I/OCLOCK cycles moves out of the 6, 7, 8 (D2, D1, D0) transitions

(4) The falling edge of the on-chip sampling-hold circuit at the 8th I/OCLOCK cycle moves out the 6th, 7th, 8th (D2, D1, D0) conversion bits. The hold function will last for 4 internal clock cycles and then begin A/D conversion for 32 internal clock cycles.After the eighth I/OCLOCK, CS must be high, or I/OCLOCK must remain low for 36 internal system clock cycles.Completion of work to be maintained and converted. If there is a valid interference pulse on I/OCLOCK when CS is low, the microprocessor/controller will lose synchronization with the device's I/O timing.

(5) To sample the analog signal at a specific time, the falling edge of the 8th I/OCLOCK clock should correspond to that time, because the chip starts sampling at the falling edge of the 4th I/OCLOCK clock, but starts saving at the falling edge of the 8th I/OCLOCK clock.

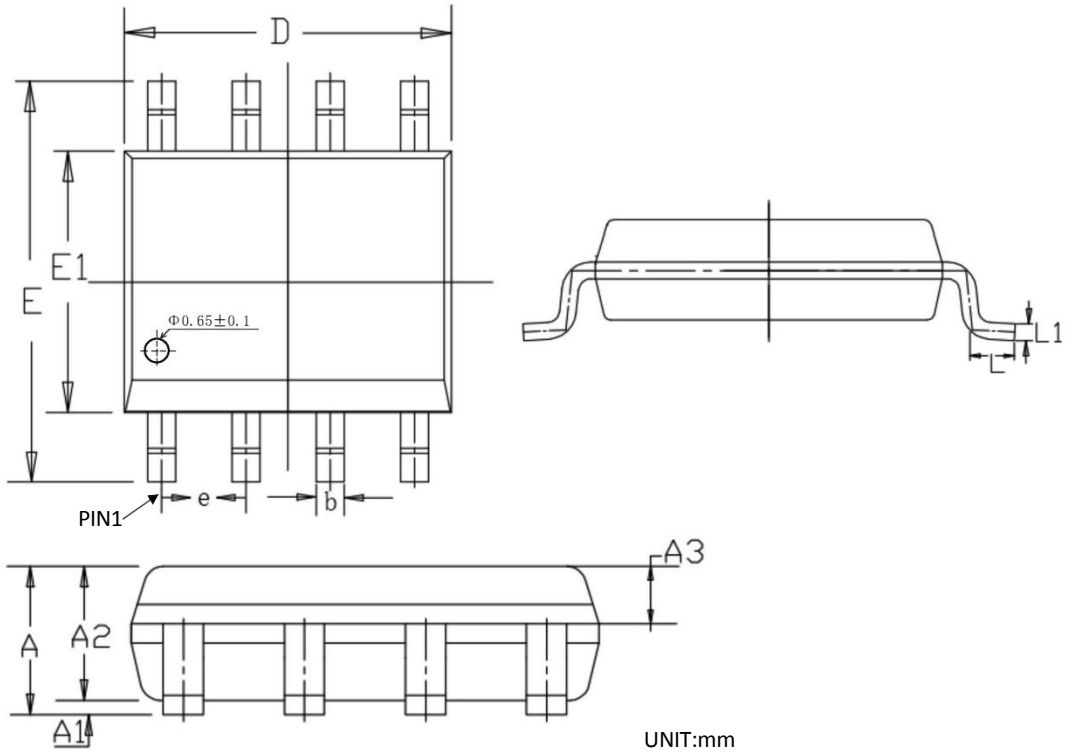
8. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL548	XL548	SOP8	4.90 * 3.90	- 40 to 85	MSL3	T&R	2500
XD548	XD548	DIP8	9.25 * 6.38	- 40 to 85	MSL3	Tube 50	2000

9. DIMENSIONAL DRAWINGS

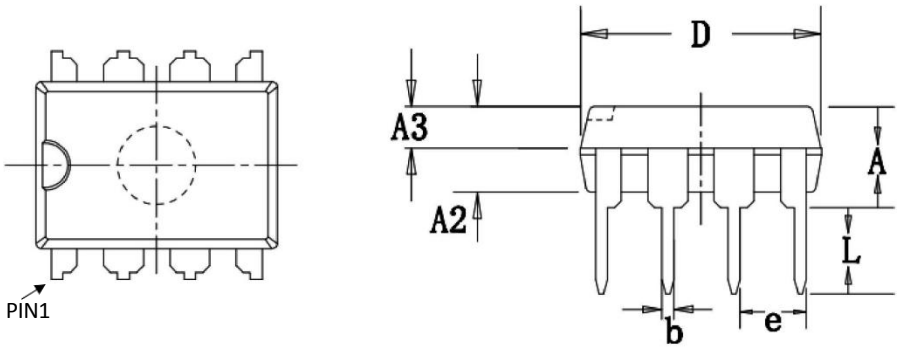
SOP8

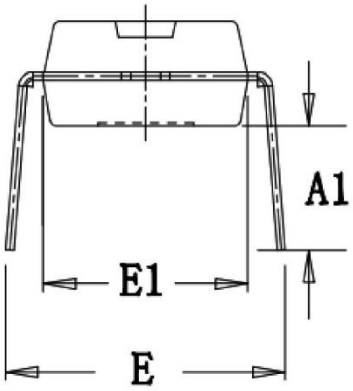


UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—

DIP8





UNIT:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1	3.786	3.886	3.986
A2	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	–	0.490
e	2.510	2.540	2.570
D	9.150	9.250	9.350
E	7.800	8.500	9.200
E1	6.280	6.380	6.480
L	3.000	–	–