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SEMICONDUCTOR



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PLED

TLV702XXDBVR(MS)

Product specification

产品描述

TLV702XXDBVR(MS) 系列是一组低压差 (LDO) 转换器, 具有 1.2V 至 5.5V 宽电压输入范围、低压差、低功耗和小型化封装的等特性。

TLV702XXDBVR(MS) 低至 2uA 低静态电流特性, 特别适合用于电池供电、长时间待机系统设备应用, 能帮助降低系统设备的待机功耗, 有效延长待机时间和电池使用寿命。

TLV702XXDBVR(MS) 有带 EN 使能引脚的版本可选, 将 EN 脚拉低可进入关断模式, 此关断模式下静态电流可降至仅 100nA (典型值)。TLV702XXDBVR(MS) 系列支持输出电容采用陶瓷电容器, 在 1.2V 至 5.5V 的宽输入电压范围内和整个输出负载电流 0mA-300mA 范围内稳定工作。

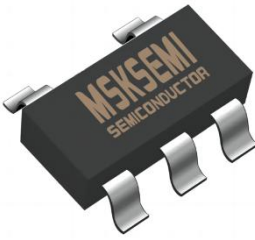
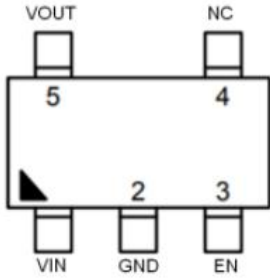
产品特性

- 2uA 静态电流 (无负载)
- $\pm 2\%$ 输出电压精度
- 300mA 输出电流能力
- 100nA 关断电流 (可选版本)
- 宽范围输入电压: 1.2V 至 5.5V
- 低压差: 0.18V ($V_o=3.3V/I_o=300mA$ 条件下)
- 支持固定输出电压: 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V
- 支持陶瓷电容或者钽电容
- 限流保护
- 过温保护

产品应用

- 手持式、电池供电设备
- 低功耗微处理器
- 笔记本电脑、掌上型电脑和 PDA
- 无线通讯设备
- 音频/视频设备
- 车载导航系统

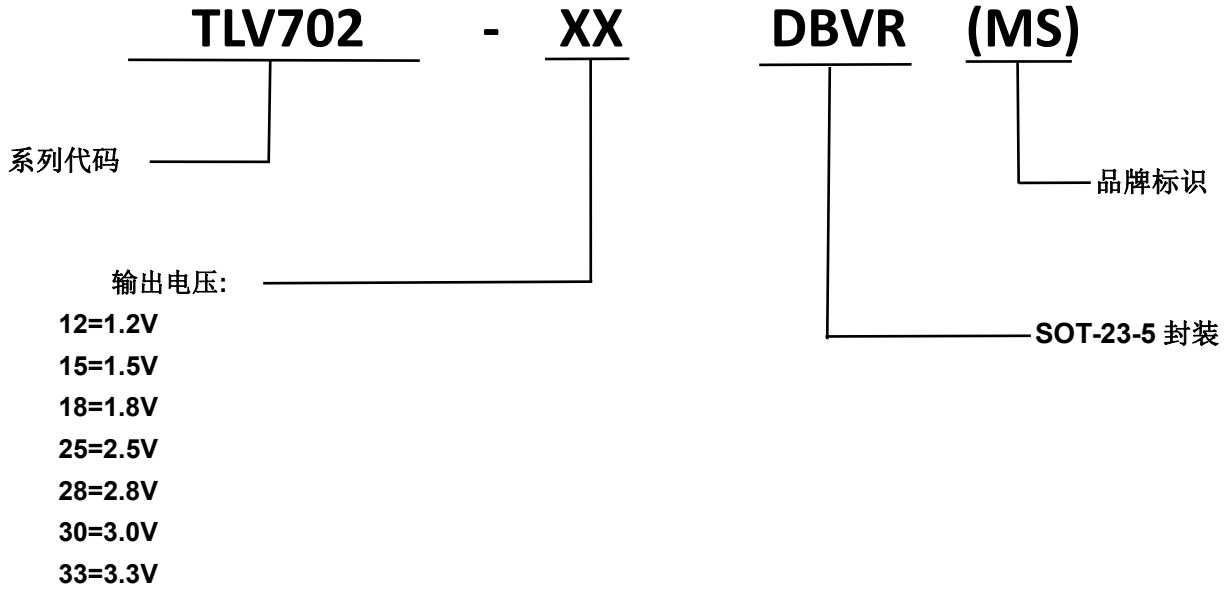
封装脚位图

SOT-23-5	Pin Configurations
	

引脚功能描述

脚位号	名称	功能描述
2	GND	接地
5	VOUT	电压输出端口
1	VIN	电源输入端口
3	EN	使能控制
4	NC	浮空脚

产品信息



TLV70212DBVR(MS)	TLV70215DBVR(MS)
AADB ****	AADG ****
TLV70218DBVR(MS)	TLV70225DBVR(MS)
AABB ****	AAET ****
TLV70228DBVR(MS)	TLV70230DBVR(MS)
AAC6 ****	AADC ****
TLV70233DBVR(MS)	
AAC7 ****	

典型应用电路

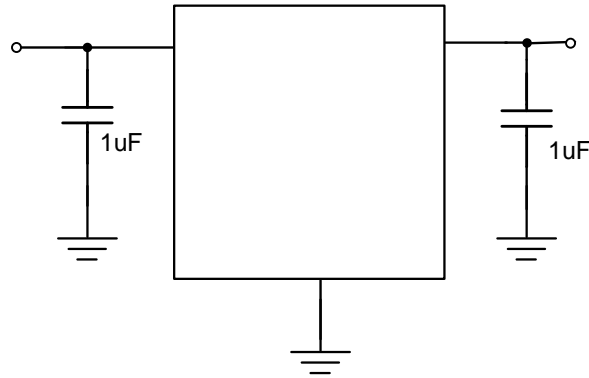


图 1: 固定输出应用电路

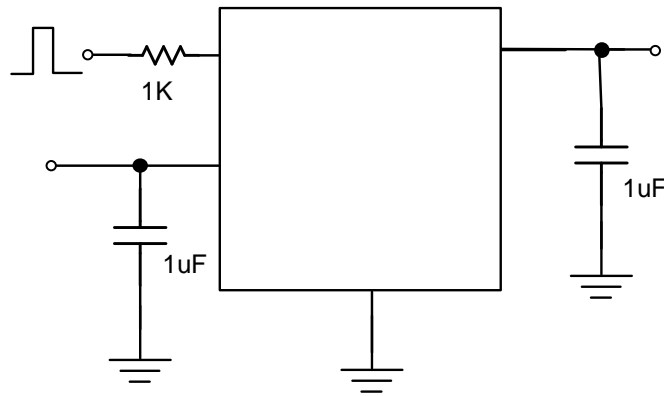


图 2: 带使能脚的固定输出应用电路

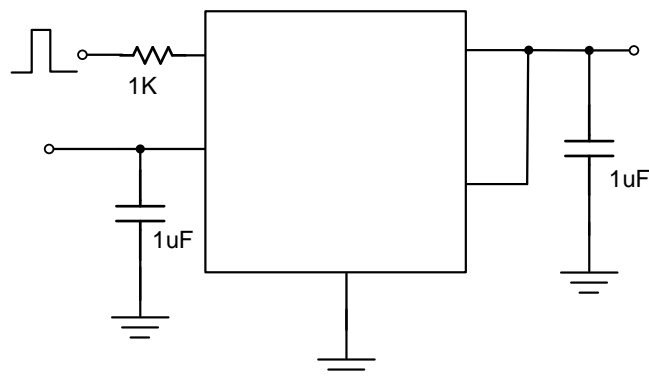


图 3: 固定输出带使能功能和输出电压检测功能之应用电路

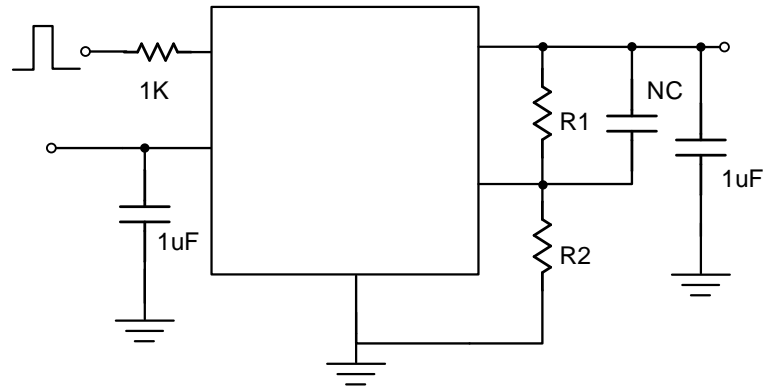
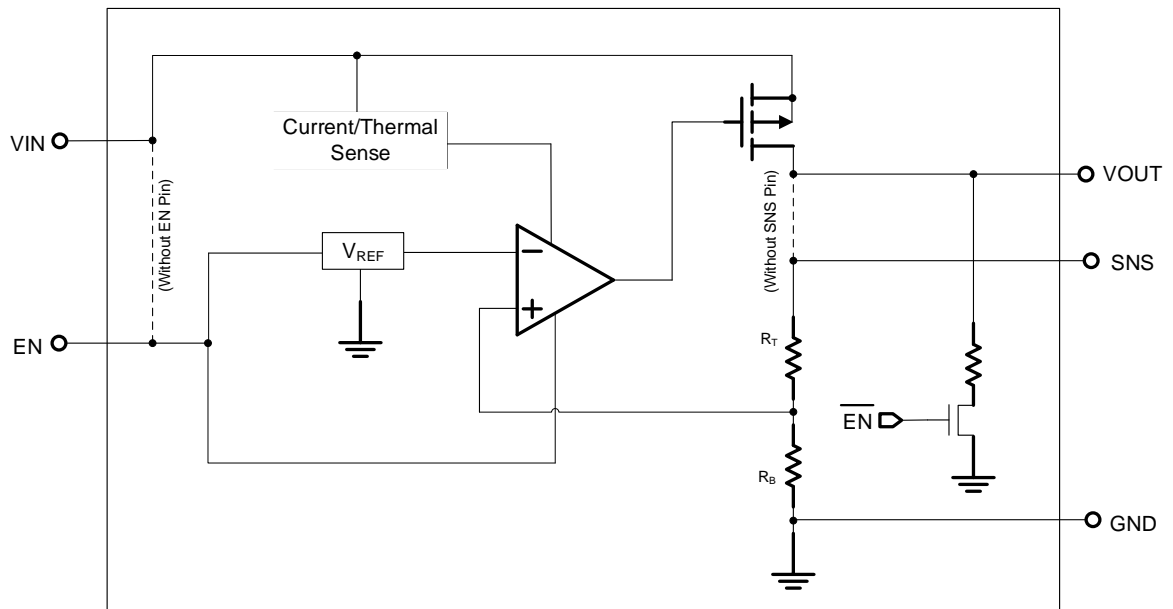


图 4: 带使能脚和输出电压检测可调电压输出应用电路

产品功能框图



最大耐压值 (Note 1)

VIN 至 GND	-0.3V to 7V
VOUT, EN 至 GND	-0.3V to 6V
VOUT 至 VIN	-6V to 0.3V
封装热阻 (Note 2)	
θ_{JA}	200 °C /W
引脚焊锡温度 (Soldering, 10 sec.)	260 °C
结点温度	150 °C
存储温度范围	-60 °C to 150 °C
ESD 静电	
HBM	2KV
MM	200V
CDM	2KV

建议应用条件

输入电压 VIN	1.2V to 5.5V
应用结温范围	-40 °C to 125 °C
应用环温范围	-40 °C to 85 °C

电气特性

($V_{IN} = 5V$, $V_{EN} = 5V$ $T_A = 25^\circ C$ 除另有说明外)

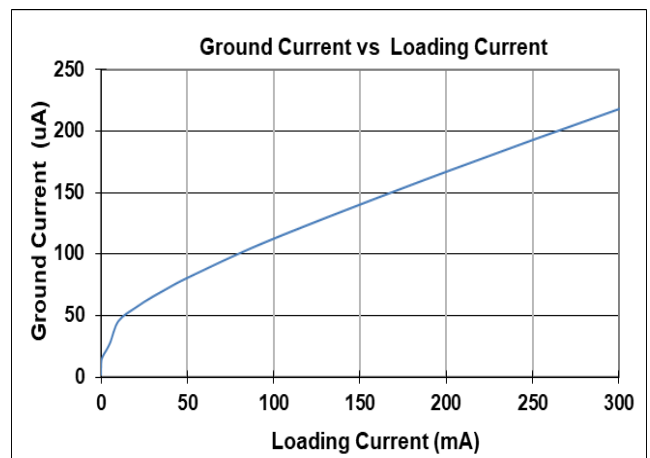
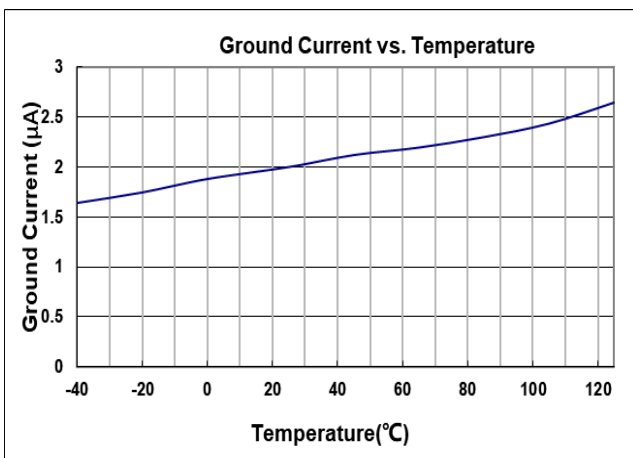
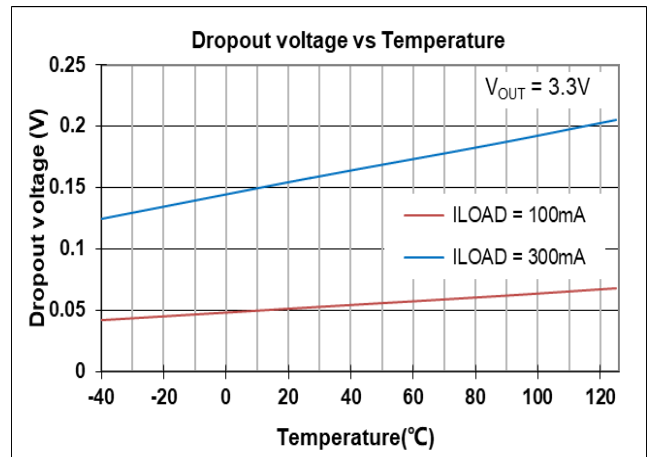
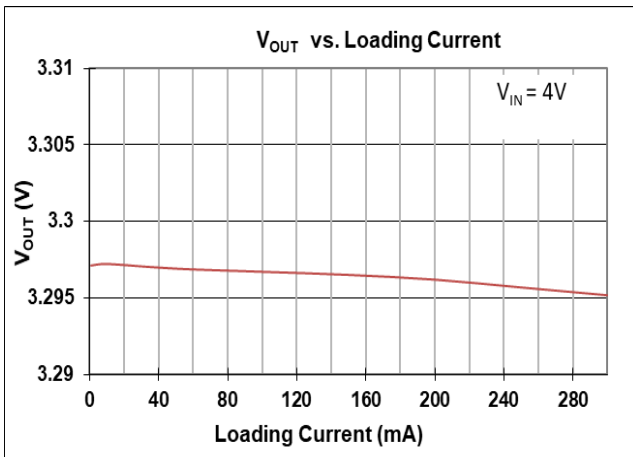
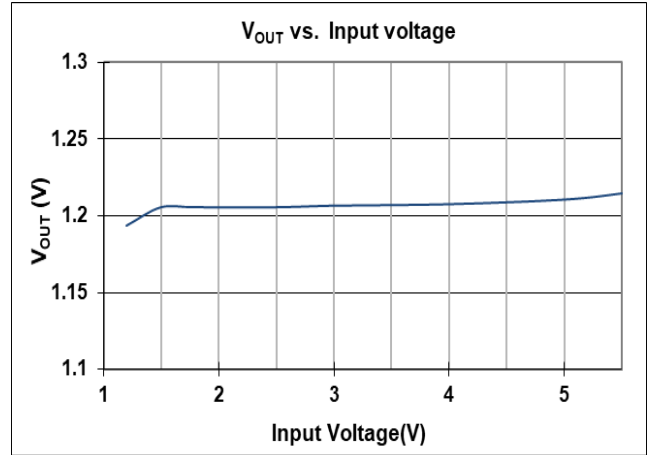
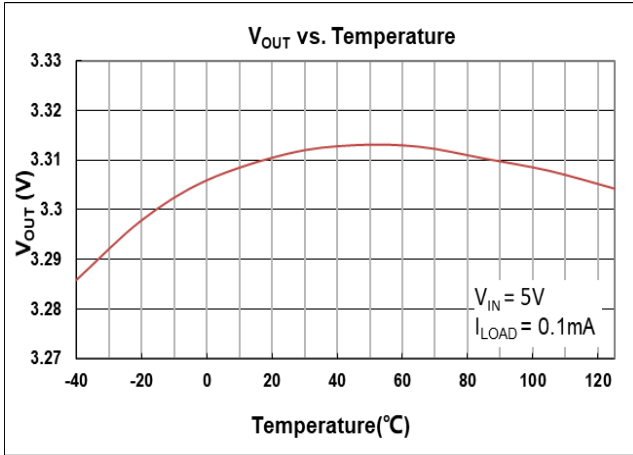
参数	符号	测试条件	最小值	典型值	最大值	单位	
输入电压	V_{IN}		1.2	--	5.5	V	
输出电压精度		$I_{LOAD} = 0.1mA$	-2		2	%	
SNS 输入电流	I_{SNS}	$SNS = V_{OUT}$		0.5		μA	
Dropout 电压 ($I_{LOAD} = 300mA$) (Note 3)	V_{DROP_3V}	$V_{OUT} \geq 3V$		0.18		V	
	$V_{DROP_2.8V}$	$V_{OUT} = 2.8V$		0.23			
	$V_{DROP_2.5V}$	$V_{OUT} = 2.5V$		0.23			
	$V_{DROP_1.8V}$	$V_{OUT} = 1.8V$		0.28			
	$V_{DROP_1.5V}$	$V_{OUT} = 1.5V$		0.36			
	$V_{DROP_1.2V}$	$V_{OUT} = 1.2V$		0.45			
静态电流	I_Q	$I_{LOAD} = 0mA$		2		μA	
关闭电流	I_{SD}	$V_{EN} = 0V$, $V_{OUT} = 0V$		0.1	0.5	μA	
使能电压阈值	V_{IH}	EN Rising	1.0			V	
	V_{IL}	EN Falling			0.4		
EN 输入电流	I_{EN}	$V_{EN} = 5V$		10	100	nA	
输入电压调整率	$\Delta LINE$	$I_{LOAD} = 30mA$, $1.5V \leq V_{IN} \leq 5.5V$ or $(V_{OUT} + 0.2V) \leq V_{IN} \leq 5.5V$		0.2		%	
负载电压调整率	$\Delta LOAD$	$10mA \leq I_{LOAD} \leq 0.3A$		0.2		%	
输出电流限流值	I_{LIM}	$V_{OUT} = 0V$	301	600		mA	
电源抑制比 ($I_{LOAD} = 5mA$)	PSRR	$V_{OUT} = 1.2V$, $V_{IN} = 2V$	$f = 100Hz$	--	80	--	dB
			$f = 1kHz$	--	75	--	
输出电流噪声 ($BW = 10Hz$ to $100kHz$, $C_{OUT} = 1\mu F$.)		$V_{IN} = 3.5V$, $I_{LOAD} = 0.1A$	$V_{OUT} = 1.2V$	--	80	--	μV_{RMS}
			$V_{OUT} = 2.8V$	--	120	--	
过温度关断温度	T_{SD}	$I_{LOAD} = 10mA$		--	155	--	$^\circ C$
过温度关断迟滞	ΔT_{SD}			--	15	--	$^\circ C$
放电电阻	R_{DC}	$EN = 0V$, $V_{OUT} = 0.1V$	--	30	--	Ω	

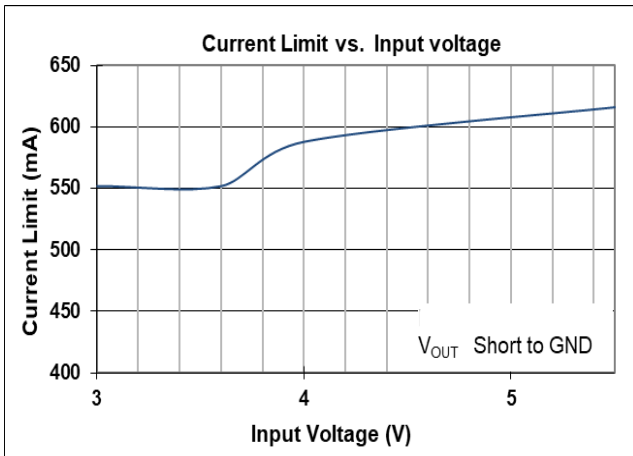
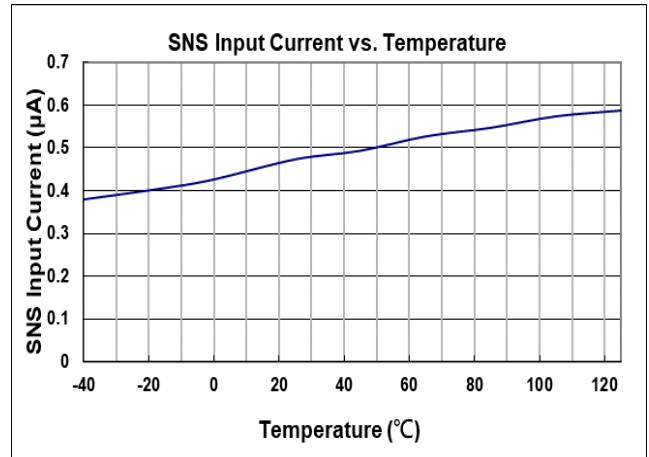
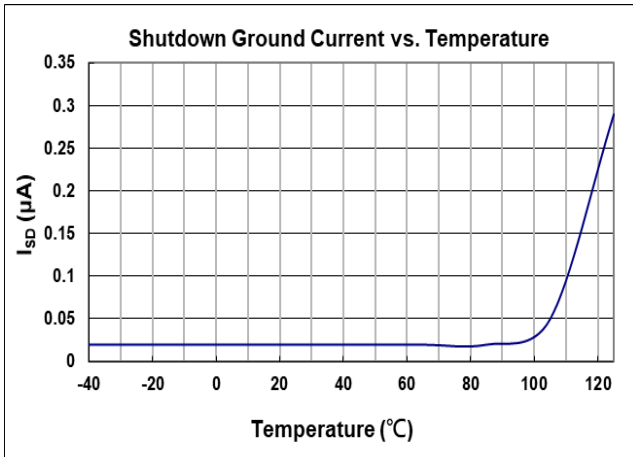
Note 1. 任何超过“最大耐压值”的应用可能会导致芯片遭受永久性损坏。这些是额定最大耐压值，仅表示在这个范围内芯片不会损伤，但不保证所有性指标都正常，在任何超过“最大耐压值”的场合使用，都可能导致芯片永久性损坏。在接近或等于最大耐压值情况下使用，可能会影响产品可靠性。

Note 2. θ_{JA} 测量条件： $T_A = 25^\circ C$ ，使用 EVB 板。

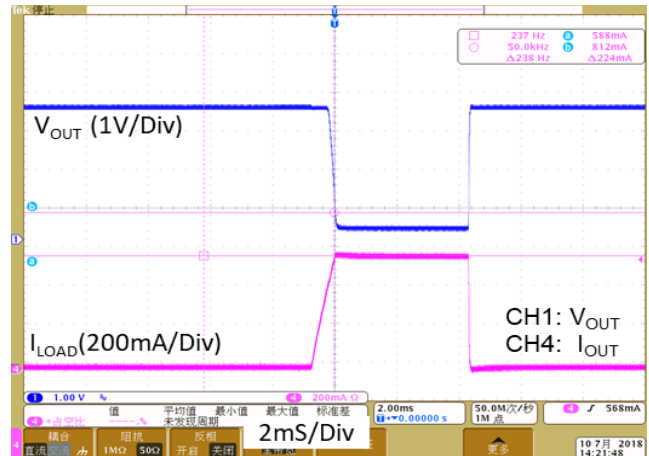
Note 3. $V_{DROP} = V_{IN} - V_{OUT}$ (V_{OUT} 达到 98%标准值)。

典型电气特性

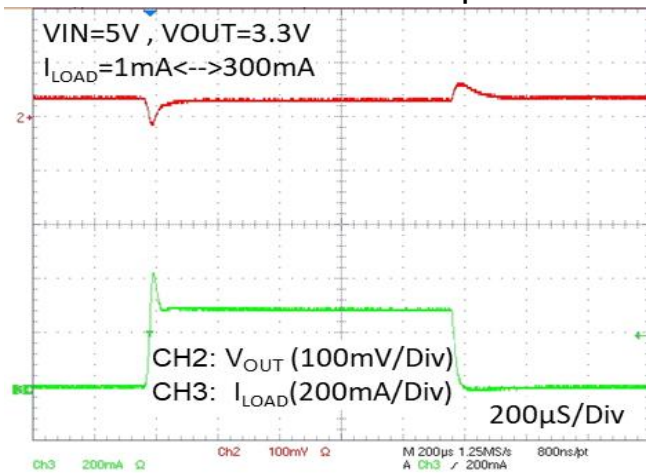




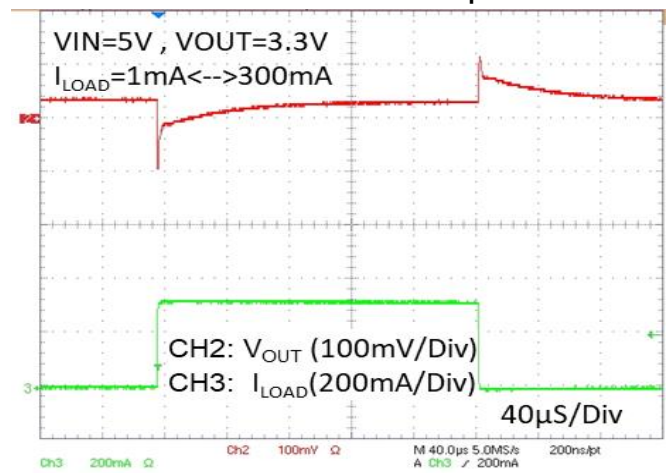
Current Limit Response



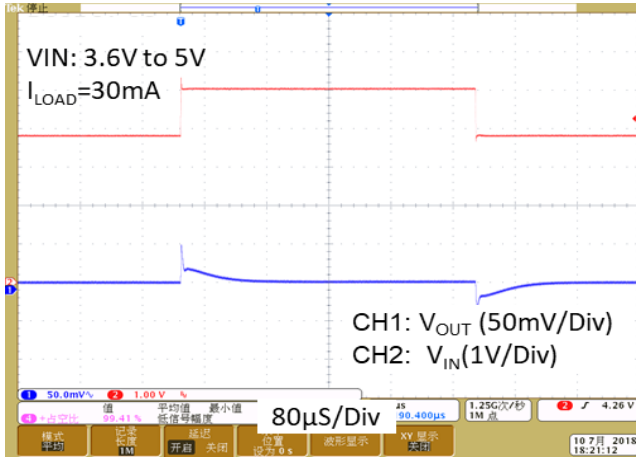
Load Transient Response I



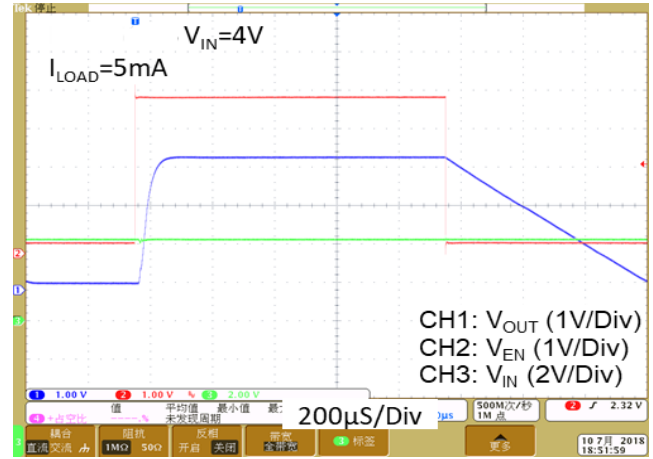
Load Transient Response II



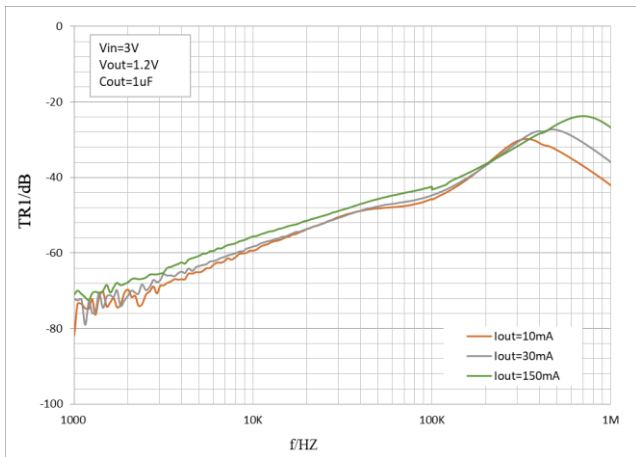
Line Transient Response



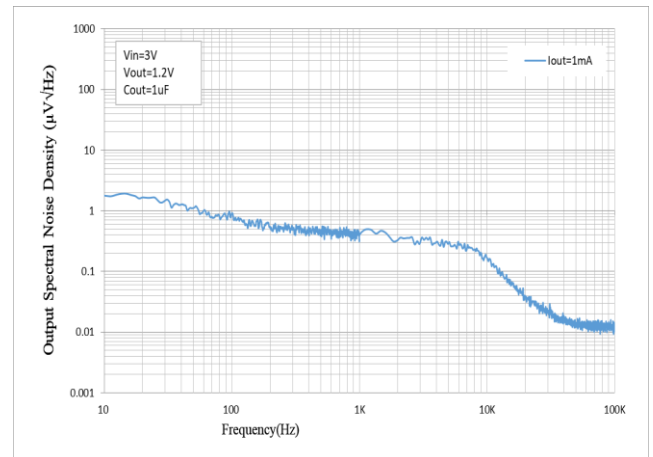
V_{OUT} Turn On/Off by EN



PSRR vs. Frequency



Noise Density Spectrum



应用指导

输入和输出电容

TLV702XXDBVR(MS) 系列产品应用, 需要选择合适的输入电容和输出电容, 以确保产品应用获得稳定可靠的性能。使用 1uF 或者更大容值的输入电容, 并将其靠近 IC 的 VIN 和 GND pin 脚摆放。输出电容可选用 1mΩ以上 ESR (等效串联阻抗), 有效容值 1uF 至 22uF 的电容。并将输出电容靠近 IC 的 V_{OUT} 和 GND 脚摆放。增加输出电容的容值和降低 ESR 能够提升电路的 PSRR 和瞬态响应能力。

Dropout 电压

TLV702XXDBVR(MS) 系列采用 PMOS 传输晶体管来实现低压差。当 $(V_{IN} - V_{OUT})$ 小于 (V_{DRO}) 时, PMOS 晶体管处于线性工作区域, 输入至输出阻抗即为 PMOS 的 $R_{DS(ON)}$, 在此状态下, PMOS 等效于一颗电阻, V_{DRO} 和输出电流近似成比例。和其他线性电压转换器一样, TLV702XXDBVR(MS) 系列的 PSRR 和瞬态响应能力会随着 $(V_{IN} - V_{OUT})$ 压差接近 V_{DRO} 而下降。

Layout 注意事项

将输入电容、输出电容和 LDO 放置在 PCB 的同一面, 并尽量将电容器靠近 IC 的输入输出脚摆放, 可实现电路最佳性能。输入电容和输出电容的接地连接必须拉回到 TLV702XXDBVR(MS) 的接地引脚, 并使用短而粗的铺线连接。避免使用长走线、窄走线、或者通过过孔走线, 这些会增加寄生电感和电阻, 导致电路性能变差, 特别是在瞬态工作条件下。

电流限制功能

TLV702XXDBVR(MS) 系列产品内部的电流限制器可持续监控及控制输出功率晶体管, 将输出电流限制至 600mA (典型值)。限流功能确保输出可以短路至地, 器件不会损坏。

OTP (过温度保护)

当产品的结点温度超过 155°C (典型值) 时, TLV702XXDBVR(MS) 会关闭 P-MOS 关闭输出。当结点温度往回降大约 15°C 时, TLV702XXDBVR(MS) 会重新自动重启工作。

热散功率

持续工作时, IC 的结点温度不应超过其额定值。最大的热散功率取决于 IC 封装的热阻、PCB 布图、周围气流速率以及结点和环境温度的差异。最大热散功率计算如下:

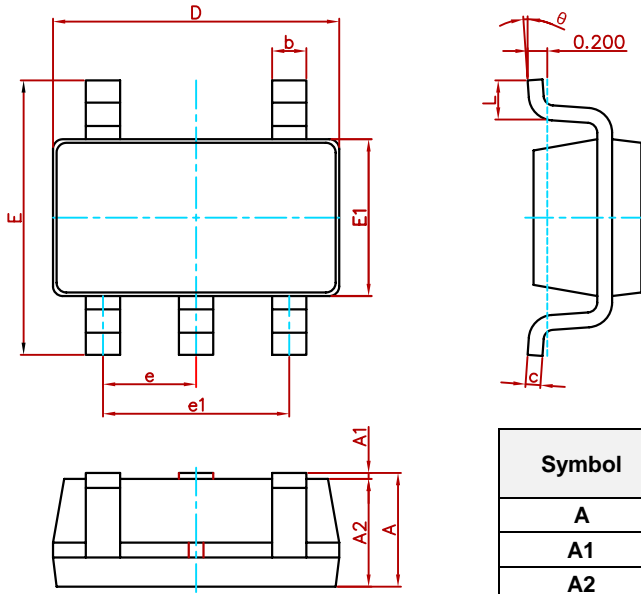
环温 $T_A = 25^\circ\text{C}$, 使用 MSKSEMI PCB,

$$PD(\text{Max}) = (125^\circ\text{C} - 25^\circ\text{C}) / (200^\circ\text{C}/\text{W}) = 0.5\text{W}$$

热散功率(PD)等于输出电流和 LDO 上的压降的乘积, 计算公式如下:

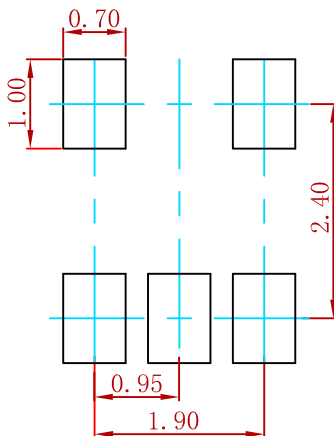
$$PD = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.05 mm.
 3. The pad layout is for reference purposes only.

订购信息

订单型号	封装形式	包装/数量
TLV70212DBVR(MS)	SOT-23-5	盘装/3000pcs
TLV70215DBVR(MS)	SOT-23-5	盘装/3000pcs
TLV70218DBVR(MS)	SOT-23-5	盘装/3000pcs
TLV70225DBVR(MS)	SOT-23-5	盘装/3000pcs
TLV70228DBVR(MS)	SOT-23-5	盘装/3000pcs
TLV70230DBVR(MS)	SOT-23-5	盘装/3000pcs
TLV70233DBVR(MS)	SOT-23-5	盘装/3000pcs

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