Ultra Low Jitter Oscillator

Features

- Frequency range
- 1MHz~200Mhz @3.3V
- 1MHz~125MHz @1.8V
- Supply voltage 1.65V ~ 3.63V
- Output Clock Tri-State Mode
- CMOS output clock
- Operating temperature -40~125ºC
- RoHS compliant & Pb free
- AEC-Q100 compliant (option)
- SMD seam sealing ceramic package
- 2.0mm x1.6mm,2.5mm x2.0mm, 3.2mm x2.5mm

Applications

- SATA, SAS, Ethernet, PCI Express, video, wireless.
- Computing, storage, networking, telecom, Industrial control.

Table1. Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Output Frequency Range	F	1	-	200	MHz	V_{DD}=3.3V
		1	-	125		V_{DD}=1.8V
Frequency Stability	F_stab	-20	-	+20	PPM	-40~85
		-30	-	+30		-40~105
		-100	-	+100		-40~125
Operating Temperature Range	T_use	-40	-	+125	ºC	
Supply Volage	V_{DD}	1.65	1.8	1.95	V	
		2.97	3.3	3.63		
Current Consumption	I_{DD}	-	-	3.4	mA	15pF Load, f=27MHz, V_{DD}=3.3V
		-	-	22	mA	15pF Load, f=40MHz, V_{DD}=3.3V
OE mode disable current	I_od	-	-	10	uA	When OE=GND, output is Pulled Down
PDB mode standby Current	I_std		-	10	uA	When OE=GND, output is Pulled Down
Duty Cycle	DC	45		55	%	
Rise/Fall Time	Tr, Tf	-	1.5	-	nS	15pF load, 10%~90% V_{DD}, high drive (V_{DD}=3.3V)
Output Voltage High	V_{OH}	V_{DD} -0.4	-	-	V_{DD}	I_{OH}=-4mA, I_{OL}=4mA, Standard Drive
Output Voltage Low	V_{OL}	-	-	0.4	V_{DD}	
Input Voltage High	V_{IH}	70%	-	-	V_{DD}	Pin1, OE
Input Volage Low	V_{IL}	-	-	30%	V_{DD}	Pin1, OE
Startup Time	T_start	-	5	7	mS	Measure from the time V_{DD} reaches its rated minimum value.
OE Enable/Disable Time	T_oe	-	-	10	nS	OE function; Ta=25 ºC, 15pFload. Add one clock period to this measurement for a usable clock output.
Resume Time	T_resume	-	-	7	mS	In PDB mode, Ta=25 ºC, 15pFload
PK-PK Period Jitter	T_jitt	-	200	300	pS	F=27MHz, V_{DD}= 3.3V
			220	400	pS	F=27MHz, V_{DD} =1.8V
RMS Phase Jitter	T_phj	-	-	0.7	pS	F=27MHz, integration bandwidth=12kHz to 5MHz, V_{DD} =1.8V
First year Aging	F_aging	-1.5	-	+1.5	PPM	25 ºC
10-year Aging		-5	-	+5	PPM	

Notes:
1: All electrical specifications in the above table are specified with 15pF output load and for all V_{DD} unless otherwise stated.

Table2. Pin Configuration

Pin	Symbol	Functionality	
1	OE	Output Enable	H or Open, Specified frequency output L: output is high impedance. Only output driver is disabled.
		PDB mode	H or Open, Specified frequency output L: output is low. Device goes to sleep mode. Supply current reduces to I_std.
2	GND	Power	Electrical ground
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage

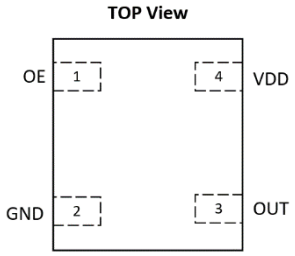


Table3. Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-60	150	ºC
VDD	-0.5	7	V
Electrostatic Discharge	-	2000	V
Soldering Temperature		260	ºC
Junction Temperature		150	ºC

Phase Noise Plot

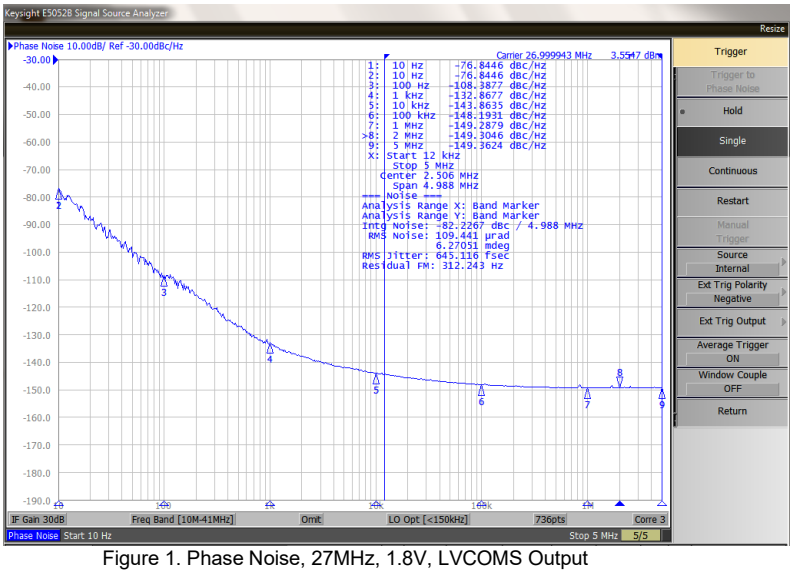


Figure 1. Phase Noise, 27MHz, 1.8V, LVCOMS Output

REV: V1.6

Test Circuit and Waveform

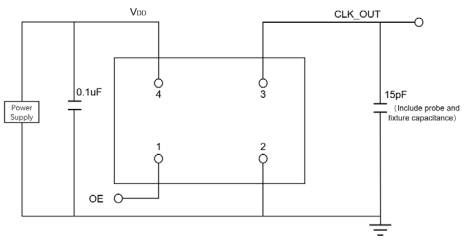


Figure 2. Test Circuit

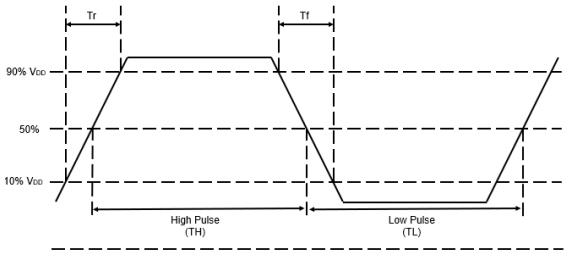


Figure 3. Waveform

Notes:

2. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagram

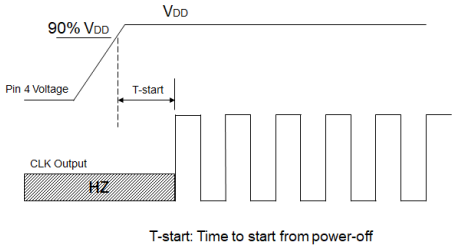


Figure 4. Startup Timing (OE mode)

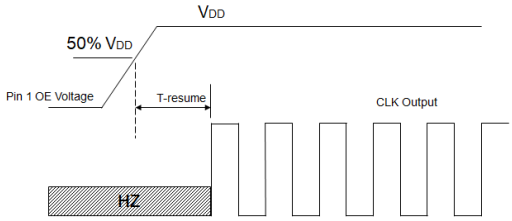


Figure 5. Standby Resume Timing (PDB mode)

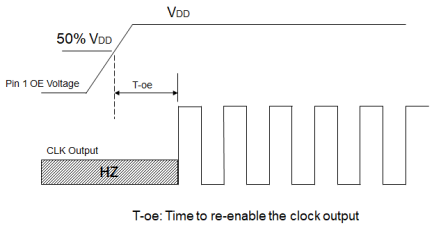


Figure 6. OE Enable Timing

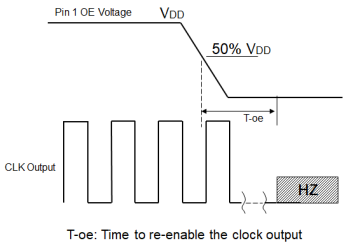
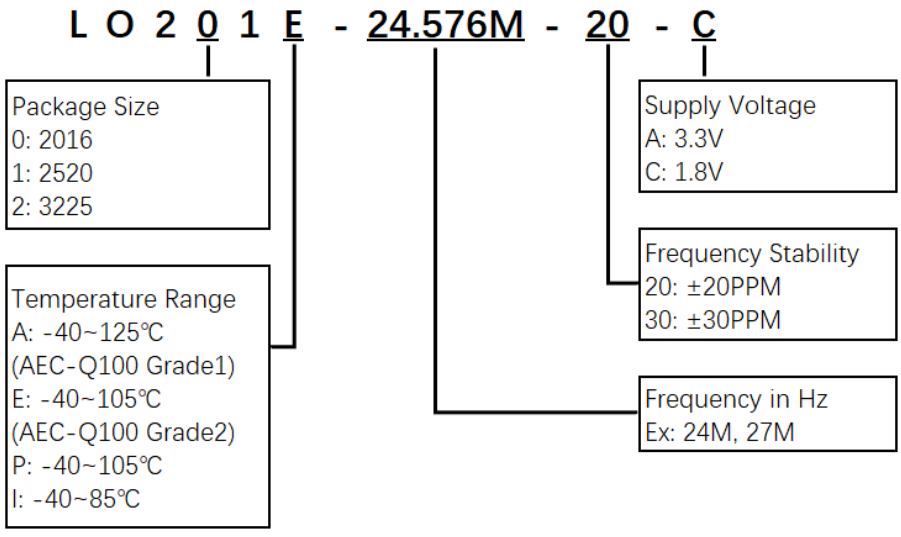


Figure 7. OE Disable Timing

Ordering Information



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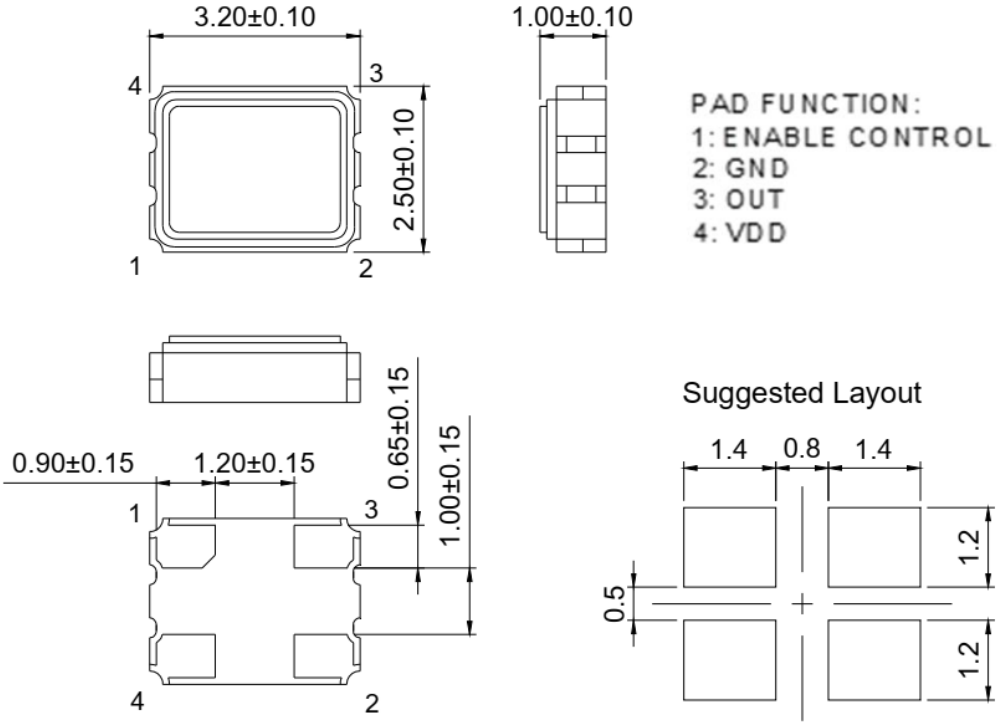
Dimensions

3225



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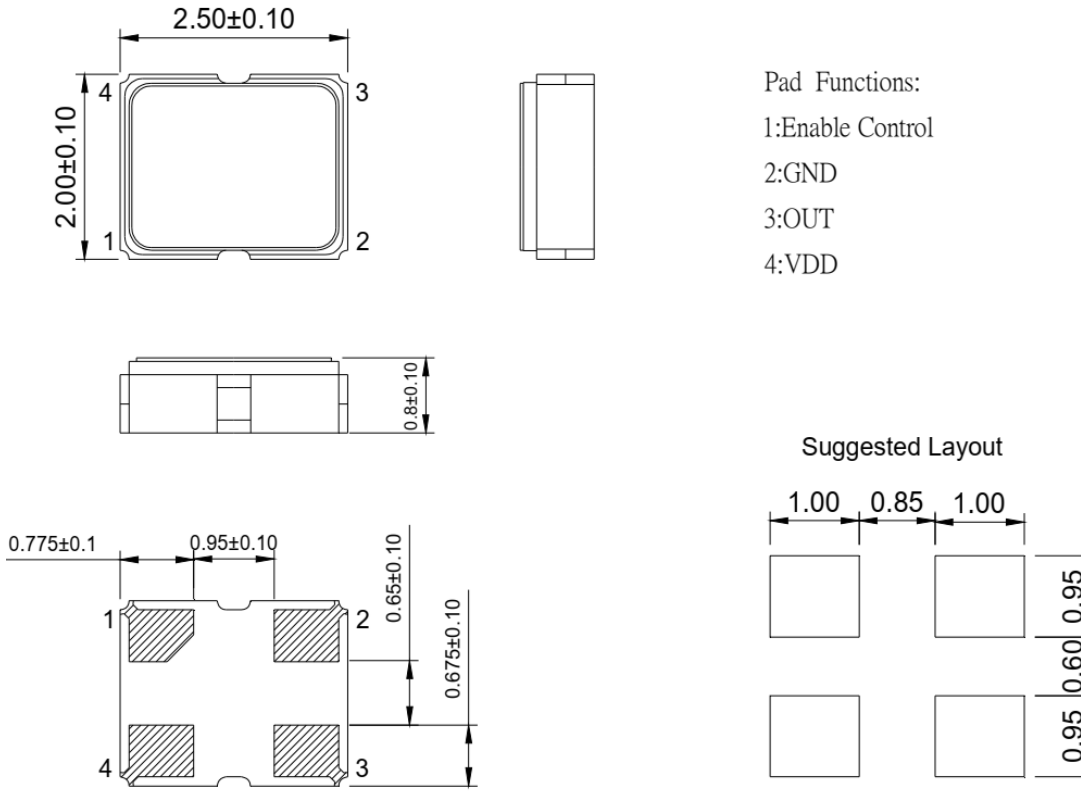

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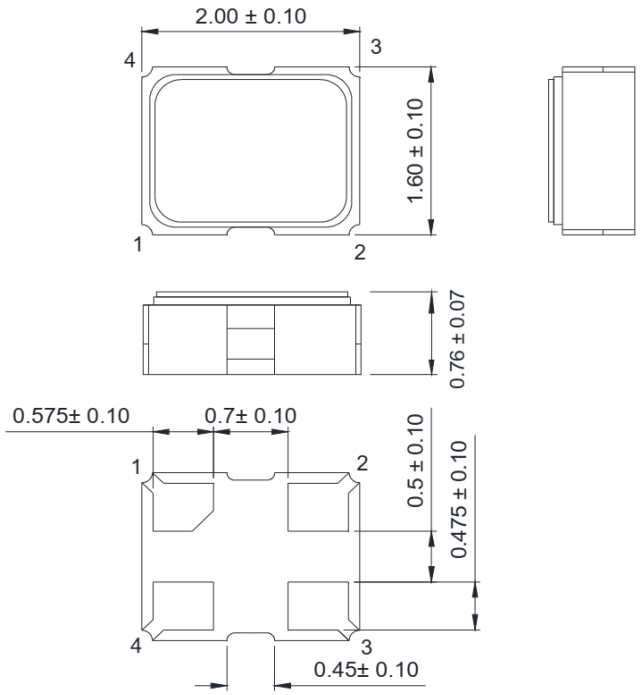
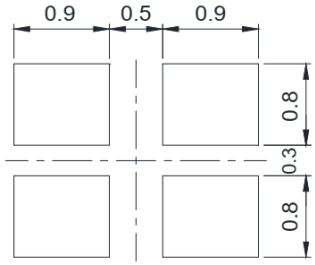
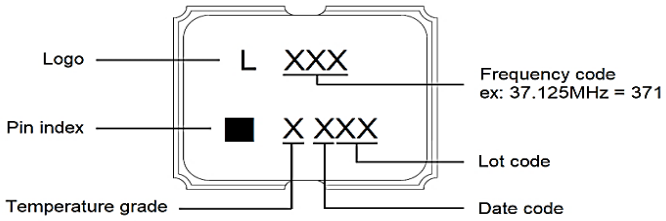


PAD FUNCTION:
1: ENABLE CONTROL
2: GND
3: OUT
4: VDD

Suggested Layout



Marking



Temperature Grade	Temperature Range	Frequency Stability (PPM)
A	-40~125℃(AEC-Q100 Grade1)	±100
E	-40~105℃ (AEC-Q100 Grade2)	±30
P	-40~105℃	±30
I	-40~85℃	±20

Revision History

Revision Number	Date of Release	Changes
1.0	03/29/2021	1) Preliminary datasheet
1.1	04/29/2021	1) Ordering information 2) Marking
1.2	05/21/2021	1) Add dimensions
1.3	09/09/2021	1) Add temperature range -40~125℃
1.4	10/26/2021	1) Add I temperature Grade
1.5	12/06/2021	1) Update the AEC-Q100 Grade 1
1.6	11/15/2022	1) Modify the PPM in the marking information 2) Updated the electrical characteristics. 3) Updated the phase noise plot.