HF500A-30

Fixed-Frequency, EMI Optimized Flyback Regulator with Multi-Mode Control and Over-Power Line Compensation

DESCRIPTION

The HF500A-30 is a fixed-frequency, current-mode regulator with built-in slope compensation. The device combines a 700V MOSFET and a full-featured controller into one chip for a low-power, offline, flyback, switch-mode power supply with EMI optimization.

At medium and heavy loads, the regulator operates at a fixed frequency with frequency jittering. Jittering helps reduce EMI energy on the switching frequency and its harmonics. Under light-load conditions, the regulator holds the peak current and reduces its switching frequency to 25kHz to offer excellent efficiency. At very light loads, the regulator enters burst mode to achieve low standby power consumption.

Full protection features include brown-in and brownout, VCC under-voltage lockout (UVLO), overload protection (OLP), short-circuit protection (SCP), VCC over-voltage protection (OVP), input OVP, and over-temperature protection (OTP).

The HF500A-30 features over-power line compensation to ensure that the overload protection point is independent of the input voltage.

The HF500A-30 is available in a PDIP8-7B package.

Table 1 shows the maximum output power.

Table 1: Maximum Output Power (1)

	$85V_{AC}$ to $265V_{AC}$	
	Adapter (2)	Open Frame (3)
P_{OUT} (W)	18	27

Notes:

1) The junction temperature can limit the maximum output power.
2) Maximum continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
3) Maximum continuous power in an open frame design at 50°C ambient temperature.

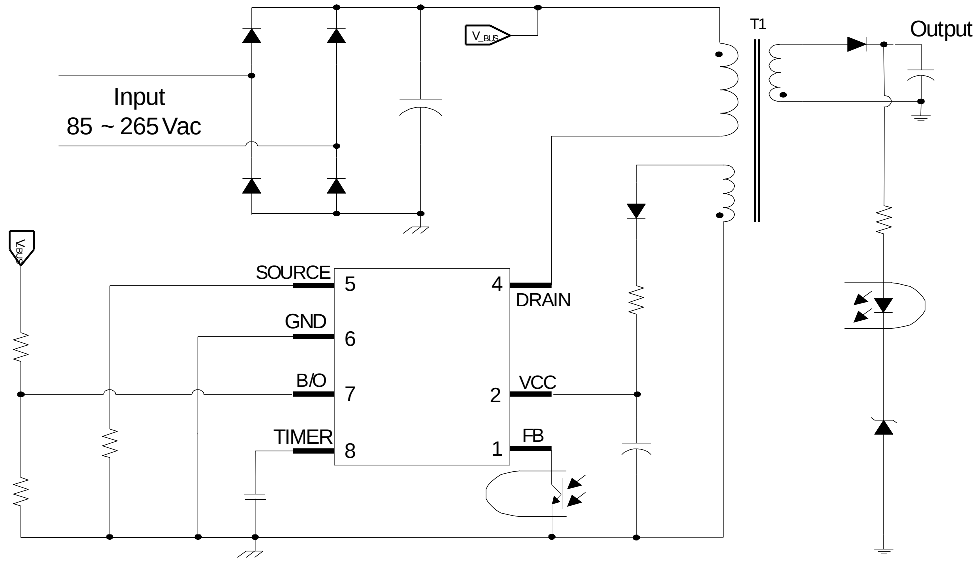
FEATURES

- 700V/1.4Ω Integrated MOSFET
- Fixed-Frequency, Current-Mode Control Operation with Built-In Slope Compensation
- EMI (Radiated Emissions) Optimization
- Frequency Foldback Down to 25kHz at Light Loads
- Burst Mode for Low Standby Power Consumption
- Frequency Jittering for a Reduced EMI Signature
- Over-Power Compensation
- Internal High-Voltage Current Source
- VCC Under-Voltage Lockout (UVLO) with Hysteresis
- Configurable Input B/O and Over-Voltage Protection (OVP)
- VCC Over-Voltage Protection (OVP)
- Overload Protection (OLP) with Configurable Delay
- Latch-Off Protection on TIMER
- Over-Temperature Protection (OTP) (Auto-Restart with Hysteresis)
- Short-Circuit Protection (SCP)
- Configurable Soft Start (SS)
- Available in a PDIP8-7B Package

APPLICATIONS

- Power Supplies for Home Appliances
- Set-Top Boxes
- Standby and Auxiliary Power
- Adapters

TYPICAL APPLICATION



ORDERING INFORMATION

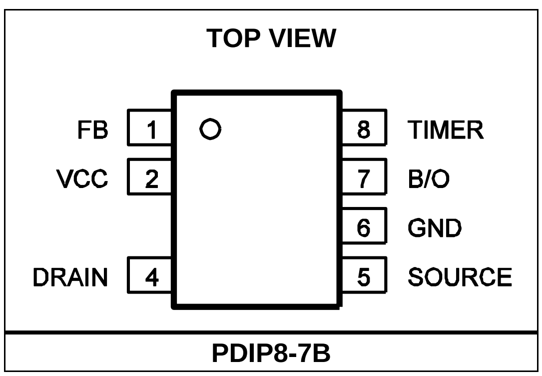
Part Number*	Package	Top Marking
HF500AGP-30	PDIP8-7B	*See Below*

TOP MARKING

MPS YYWW
H500A-30
LLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
H500A-30: Part number
LLLLLLLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	FB	**Feedback.** A pull-down optocoupler controls the output regulation.
2	VCC	**Power supply of the IC.** VCC triggers over-voltage protection (OVP) if the voltage on VCC rises above V_{OVP}.
4	DRAIN	**Drain of the internal MOSFET.** DRAIN is the input for the high-voltage current source at start-up
5	SOURCE	**Source of the internal MOSFET.** SOURCE is the input of the primary current-sense signal.
6	GND	**Ground.**
7	B/O	**Brown-in/brownout, input OVP, and over-power compensation (OPC) detection.** The voltage on the B/O pin is used to detect brown-in/brownout, input OVP, and over-power compensation. This pin's functions are disabled if B/O is pulled above V_{DIS}.
8	TIMER	**Combined soft start, frequency jittering, and timer functions for overload protection (OLP) and brown-out protection.** The IC is latched by pulling TIMER down. TIMER allows for external OVP and over-temperature protection (OTP) detection.

ABSOLUTE MAXIMUM RATINGS (4)

DRAIN breakdown voltage..........-0.3V to +700V
VCC to GND ....-0.3V to +30V
FB, TIMER, SOURCE, B/O to GND...................
....-0.3V to +7V
Continuous power dissipation (T_A = 25°C) (5)
.... 1.19W
Junction temperature ....150°C
Lead temperature ....260°C
Storage temperature .... -60°C to +150°C
ESD capability human body model (all pins except DRAIN) 4.0kV
ESD capability machine model 200V

ESD Ratings

Human body model (HBM) .... ±2kV
Charged device model (CDM)....................±2kV

Recommended Operating Conditions (6)

Operating junction temp (T_J).... -40°C to +125°C
Operating VCC range ....9V to 24V

Thermal Resistance (7)

	θ_{JA}	θ_{JC}	
PDIP8-7B..............................	105......	45...	°C/W

Notes:

4) Exceeding these ratings may damage the device.
5) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
6) The device is not guaranteed to function outside of its operating conditions.
7) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 16V, T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Start-Up Current Source (DRAIN)						
Supply current from DRAIN	I_{DRAIN_0}	V_{CC} = 0V, V_{DRAIN} = 120V/400V	1.4	3.6	6.2	mA
	I_{DRAIN_11}	V_{CC} = 11V, V_{DRAIN} = 120V/400V	1.4	5	7.9	
Leakage current from DRAIN	I_{LK}	V_{CC} = 10V, V_{DRAIN} = 400V		4.5	10.5	µA
Breakdown voltage	V_{BR}	T_J = 25°C	700			V
Internal MOSFET (DRAIN)						
On-state resistance	$R_{DS(ON)}$	V_{CC} = 10.5V, I_D = 0.1A, T_J = 25°C		1.4	1.6	Ω
Supply Voltage Management (VCC)						
VCC level (increasing) where the internal regulator stops	VCC_{OFF}		11	12	13	V
VCC level (decreasing) where the IC shuts down and the internal regulator turns on	VCC_{UVLO}		6	7	8	V
VCC UVLO hysteresis	VCC_{OFF} - VCC_{UVLO}		4	4.8		V
VCC recharge level when protection occurs	VCC_{PRO}		4.7	5.3	5.9	V
VCC decreasing level where the latch-off phase ends	VCC_{LATCH}			2.5		V
Internal IC consumption	I_{CC}	V_{FB} = 3V, V_{CC} = 12V		0.9	1.2	mA
Internal IC consumption, latch-off phase	$I_{CCLATCH}$	V_{CC} = 12V, T_J = 25°C		700	900	µA
Voltage on VCC (upper limit) where the regulator latches off (OVP)	V_{OVP}		25	27	29	V
Blanking duration on the OVP comparator	t_{OVP}			60		µs
Oscillator						
Oscillator frequency	f_{OSC}	V_{FB} > 1.85V, T_J = 25°C	62	65	68	kHz
Frequency jittering amplitude in percentage of f_{OSC}	A_{JITTER}	V_{FB} > 1.85V, T_J = 25°C	±5	±6.5	±8	%
Frequency jittering entry level	V_{FB_JITTER}				1.95	V
Frequency jittering modulation period	t_{JITTER}	C_{TIMER} = 47nF		3.7		ms
Protections (B/O)						
Brown-in threshold voltage on B/O	V_{B/O_IN}	$V_{B/O}$ increasing	0.95	1	1.05	V
Brownout threshold voltage on B/O	V_{B/O_OUT}	$V_{B/O}$ decreasing	0.85	0.9	0.95	V
Brown-in/brownout hysteresis	$\Delta V_{B/O}$		0.065	0.1	0.14	V

ELECTRICAL CHARACTERISTICS *(continued)*

VCC = 16V, T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timer duration for line cycle dropout	$t_{B/O}$	C_{TIMER} = 47nF	34	55		ms
Input OVP threshold on B/O	$OVP_{B/O}$		4.2	4.5	4.8	V
Input OVP delay time	$t_{OVPB/O}$			90		µs
Voltage on B/O to disable B/O and input OVP function	V_{DIS}		5.4	6	6.6	V
Clamp voltage on B/O	V_{B/O_CLA}		7			V
Input impedance	$R_{B/O}$		1.2			MΩ
Current Sense (SOURCE)						
Current limit point	V_{ILIM}		0.93	1	1.07	V
Short-circuit protection point	V_{SCP}		1.3	1.5	1.7	V
Current limitation during frequency foldback	V_{FOLD}	V_{FB} = 1.85V	0.63	0.68	0.73	V
Current limitation when entering burst	V_{IBURL}	V_{FB} = 0.7V		0.1		V
Current limitation when exiting burst	V_{IBURH}	V_{FB} = 0.8V		0.13		V
Leading-edge blanking for V_{ILIM}	t_{LEB1}			350		ns
Leading-edge blanking for V_{SCP}	t_{LEB2}			270		ns
Slope of the compensation ramp	S_{RAMP}		18	25	31	mV/µs
Feedback (FB)						
Internal pull-up resistor	R_{FB}	T_J = 25°C	12	13.5	15	kΩ
Internal pull-up voltage	V_{DD}			4.3		V
V_{FB} to internal current-set point division ratio	K_{FB1}	V_{FB} = 2V	2.5	2.8	3.1	
V_{FB} to current-set point division ratio	K_{FB2}	V_{FB} = 3V	2.8	3.1	3.4	
FB level (decreasing) where the regulator enters burst mode	V_{BURL}		0.63	0.7	0.77	V
FB level (increasing) where the regulator exits burst mode	V_{BURH}		0.72	0.8	0.88	V
Overload Protection (FB)						
FB level where the regulator enters OLP after a dedicated time	V_{OLP}			3.7		V
Time duration before OLP when FB reaches the protection point	t_{OLP}	C_{TIMER} = 47nF	32			ms

ELECTRICAL CHARACTERISTICS *(continued)*

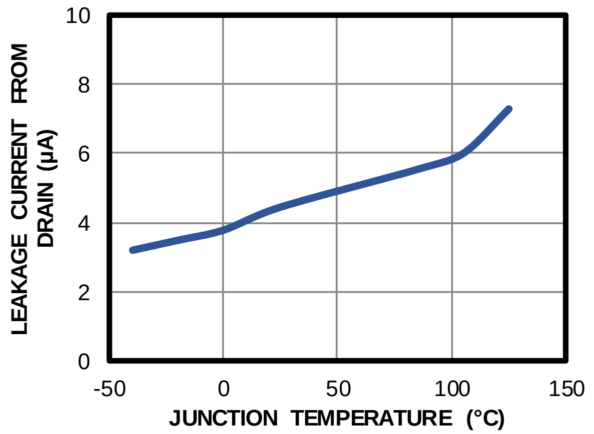
VCC = 16V, T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Over-Power Compensation (B/O)						
Compensation voltage	V_{OPC}	$V_{B/O}$ = 1.1V, V_{FB} = 2.5V, T_J = 25°C		0		mV
		$V_{B/O}$ = 1.3V, V_{FB} = 2.5V, T_J = 25°C		19		
		$V_{B/O}$ = 2.9V, V_{FB} = 2.5V, T_J = 25°C	153	200	247	
		$V_{B/O}$ = 3.5V, V_{FB} = 2.5V, T_J = 25°C	205	270	335	
		$V_{B/O}$ > V_{DIS}, T_J = 25°C		0		
FB voltage (lower limit) when compensation is removed	$V_{OPC(OFF)}$		0.55			V
FB voltage (upper limit) when compensation is fully applied	$V_{OPC(ON)}$				2.5	V
Frequency Foldback						
FB voltage (lower threshold) when frequency foldback starts	$V_{FB(FOLD)}$			1.8		V
Minimum switching frequency	$f_{OSC(MIN)}$	T_J = 25°C	20.5	25	30	kHz
FB voltage (lower threshold) when frequency foldback ends	$V_{FB(FOLDE)}$			1		V
Latch-Off Input (Integration in TIMER)						
Lower threshold when the regulator is latched	$V_{TIMER(LATCH)}$		0.7	1	1.2	V
Blanking duration on latch detection	t_{LATCH}			42		µs
Over-Temperature Protection (OTP)						
Thermal shutdown threshold	T_{OTP}			150		°C
Thermal shutdown hysteresis	$T_{OTP(HYS)}$			25		°C

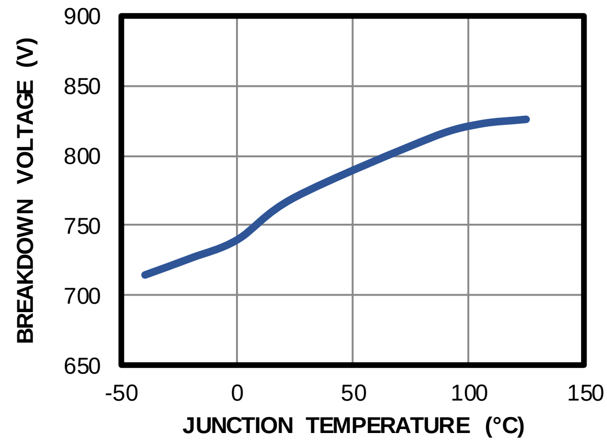
TYPICAL CHARACTERISTICS

Leakage Current from DRAIN vs. Junction Temperature

V_{DRAIN} = 400V

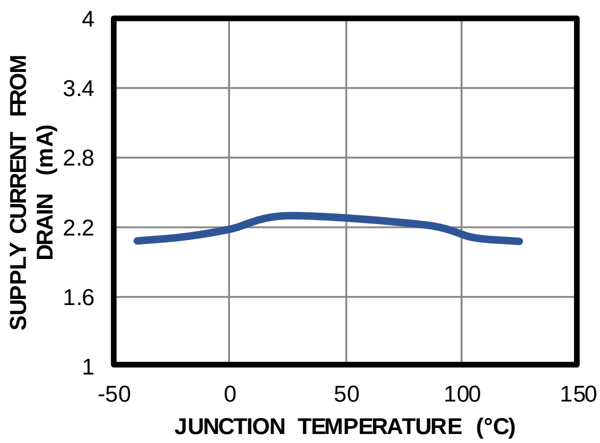


Breakdown Voltage vs. Junction Temperature



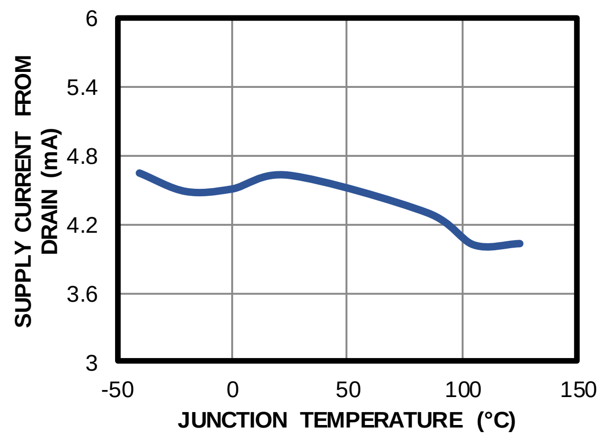
Supply Current from DRAIN vs. Junction Temperature

V_{CC} = 0V

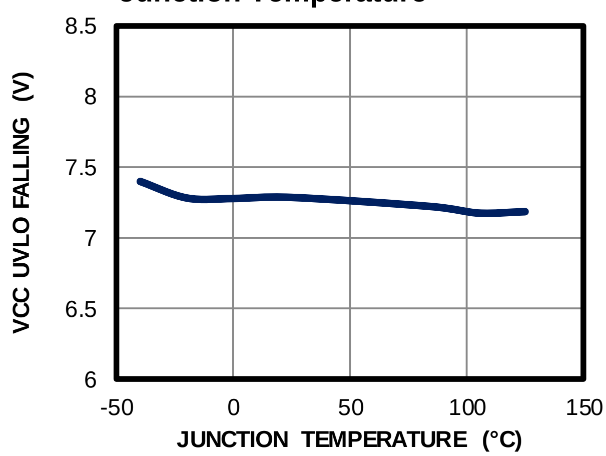


Supply Current from DRAIN vs. Junction Temperature

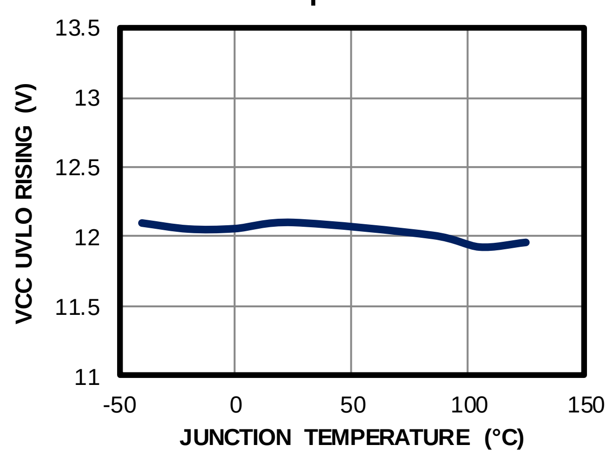
V_{CC} = 11V



VCC UVLO Falling Threshold vs. Junction Temperature

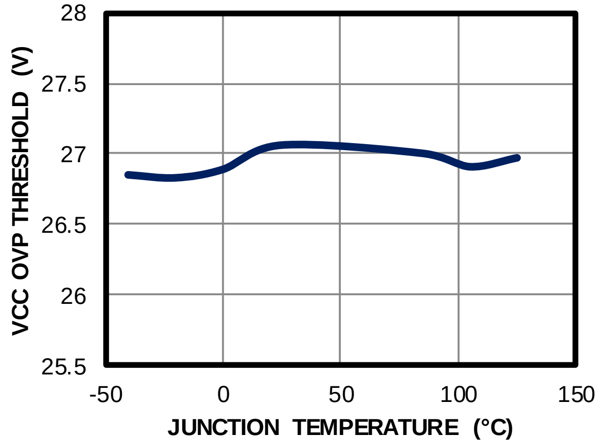


VCC UVLO Rising Threshold vs. Junction Temperature

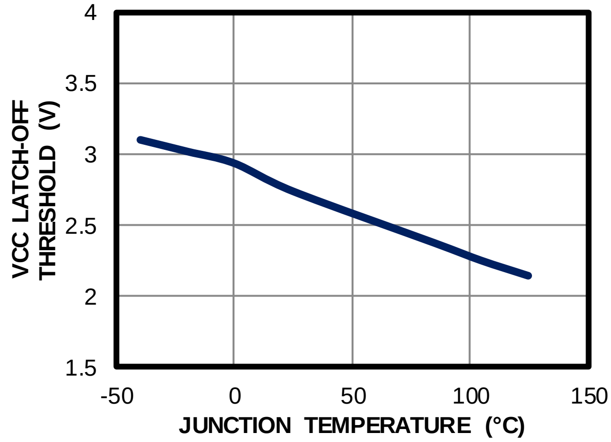


TYPICAL CHARACTERISTICS *(continued)*

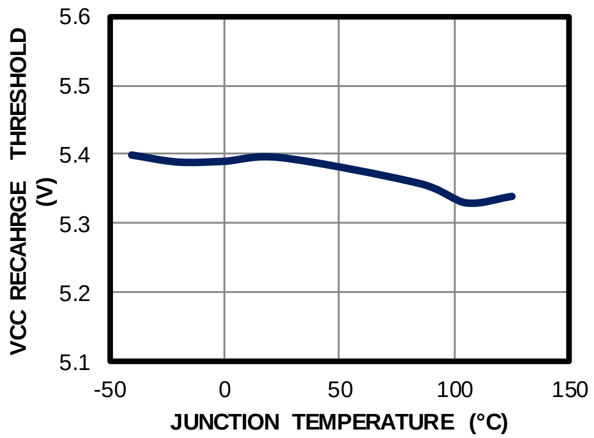
VCC OVP Threshold vs. Junction Temperature



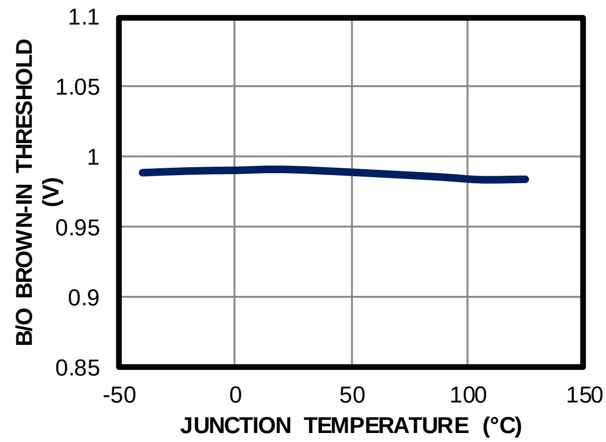
VCC Latch-Off Threshold vs. Junction Temperature



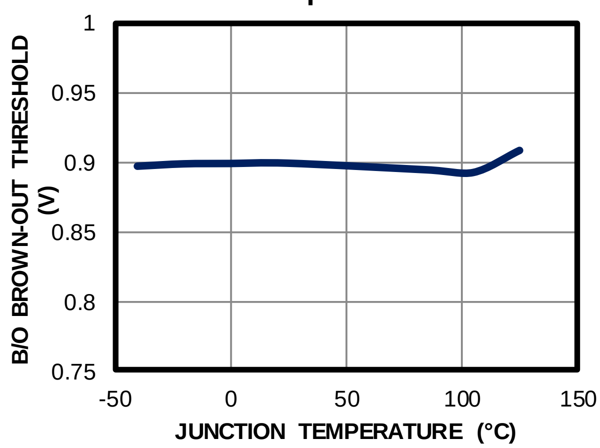
VCC Recharge Threshold vs. Junction Temperature



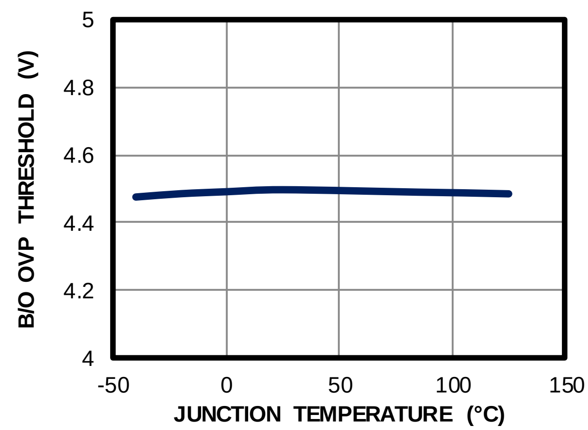
B/O Brown-In Threshold vs. Junction Temperature



B/O Brownout Threshold vs. Junction Temperature

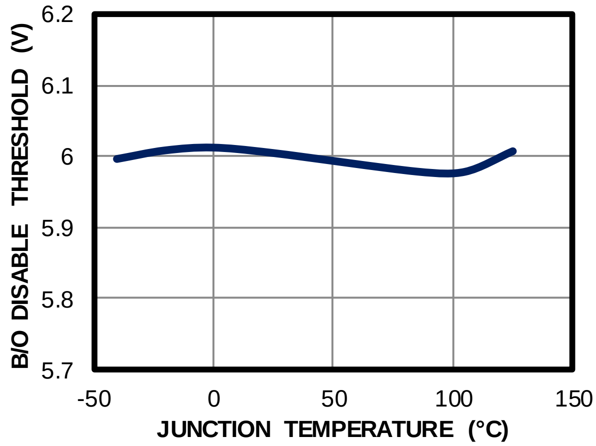


B/O OVP Threshold vs. Junction Temperature

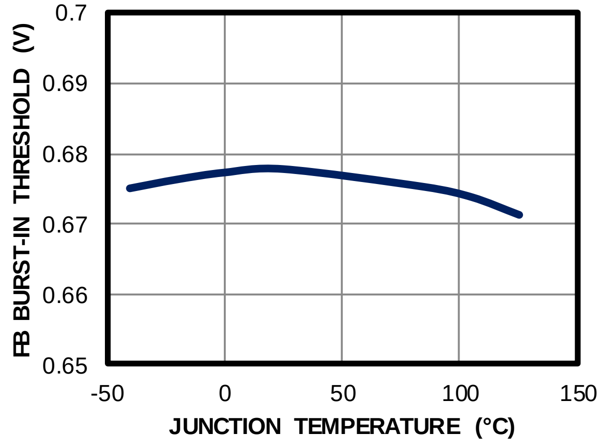


TYPICAL CHARACTERISTICS *(continued)*

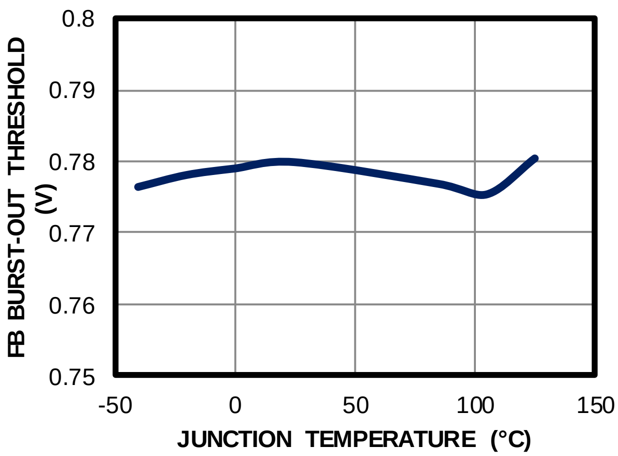
B/O Disable Threshold vs. Junction Temperature



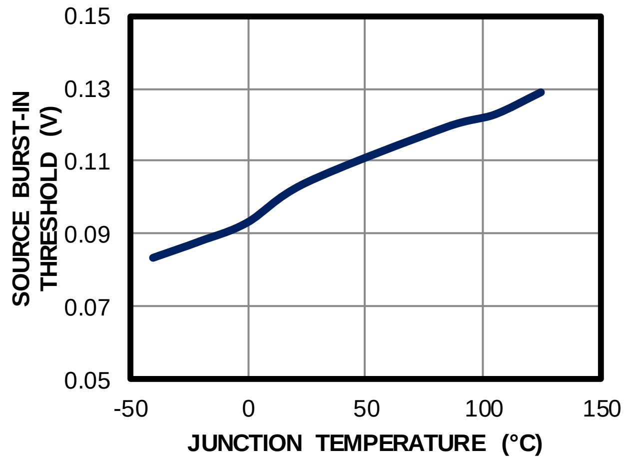
FB Burst-In Threshold vs. Junction Temperature



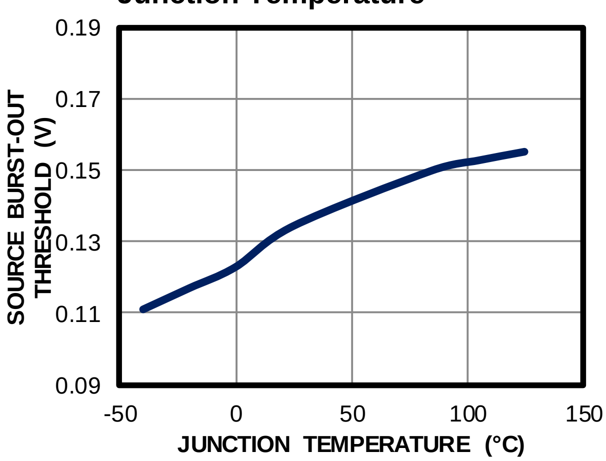
FB Burst-Out Threshold vs. Junction Temperature



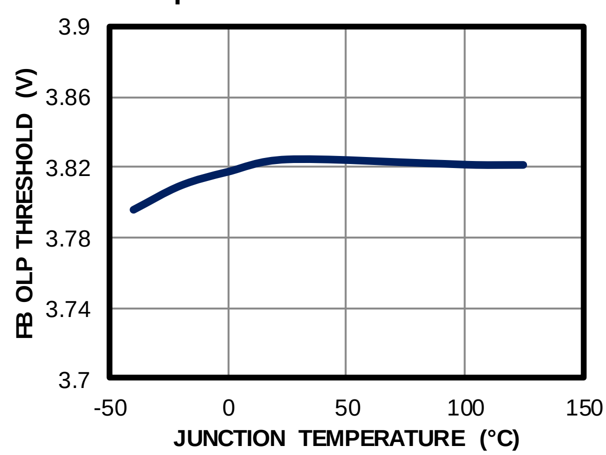
SOURCE Burst-In Threshold vs. Junction Temperature



SOURCE Burst-Out Threshold vs. Junction Temperature

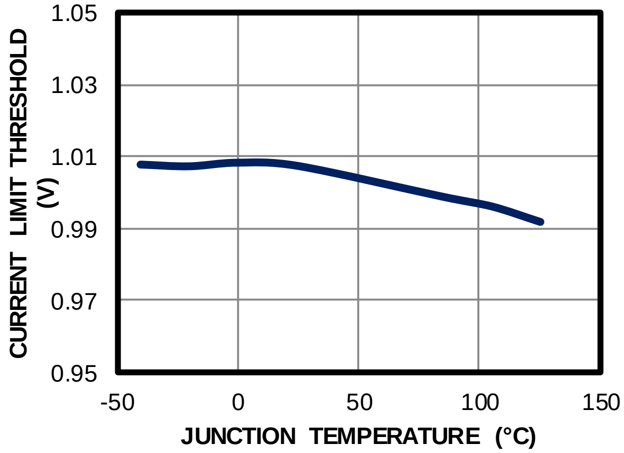


FB OLP Threshold vs. Junction Temperature

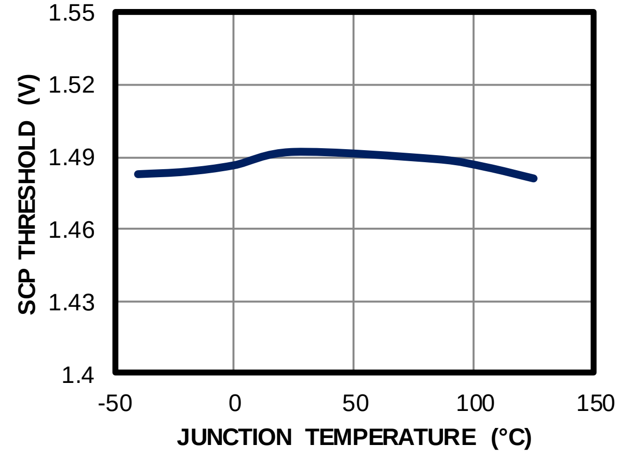


TYPICAL CHARACTERISTICS *(continued)*

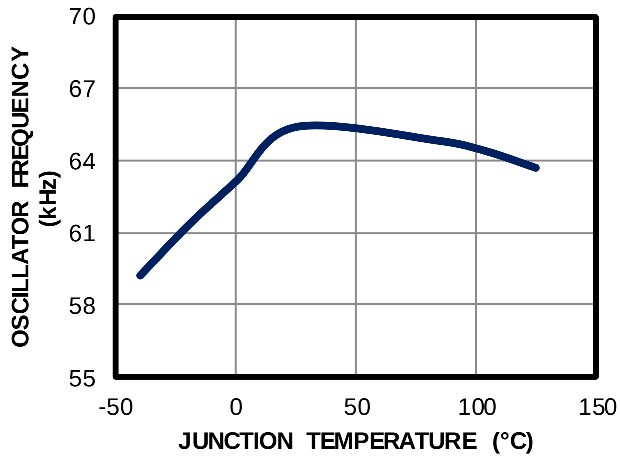
Current Limit Threshold vs. Junction Temperature



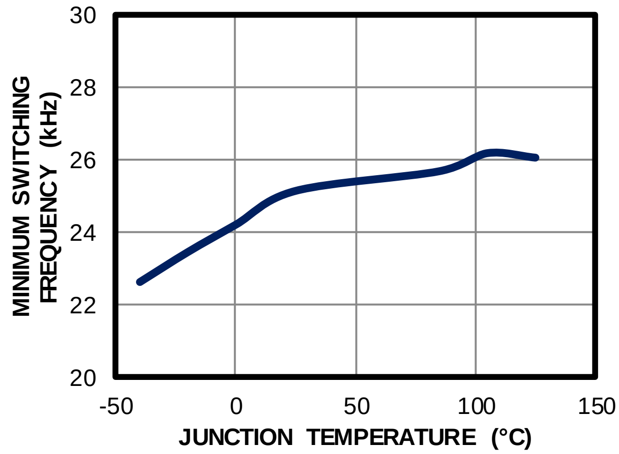
SCP Threshold vs. Junction Temperature



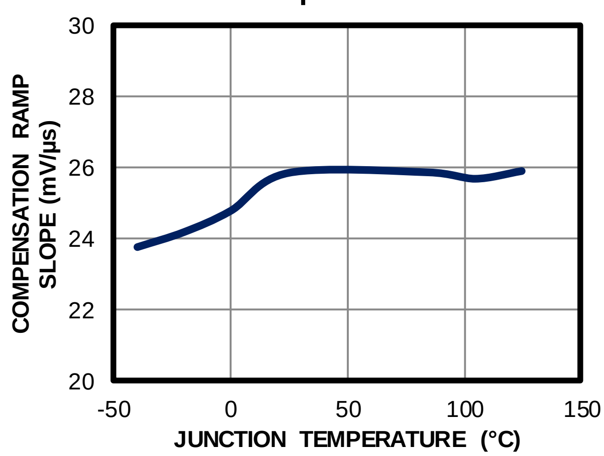
Oscillator Frequency vs. Junction Temperature



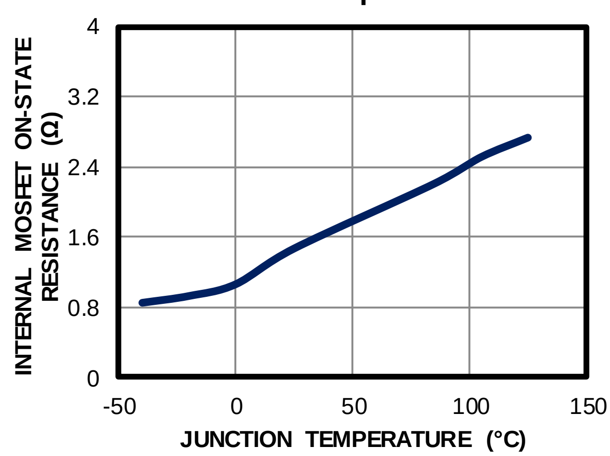
Minimum Switching Frequency vs. Junction Temperature



Compensation Ramp Slope vs. Junction Temperature



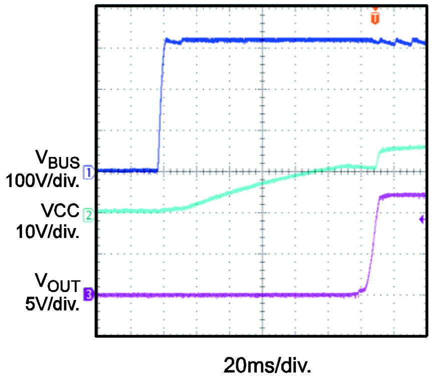
Internal MOSFET On-State Resistance vs. Junction Temperature



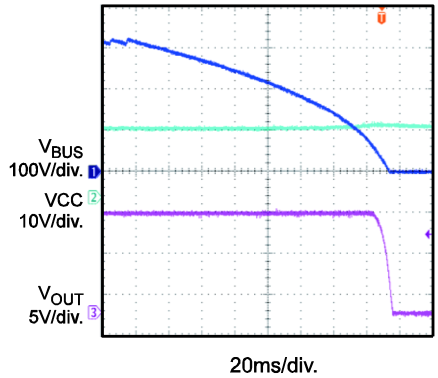
TYPICAL PERFORMANCE CHARACTERISICS

V_{IN} = 230V_{AC}, V_{OUT} = 12V, I_{OUT} = 2.5A, unless otherwise noted.

Input Power On

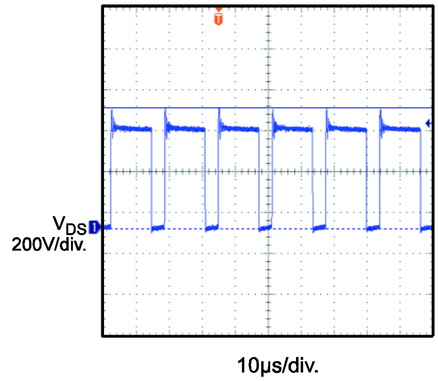


Input Power Off

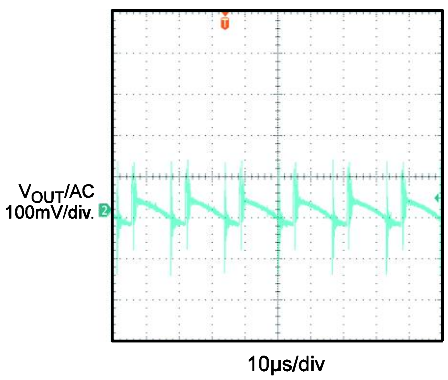


Stress

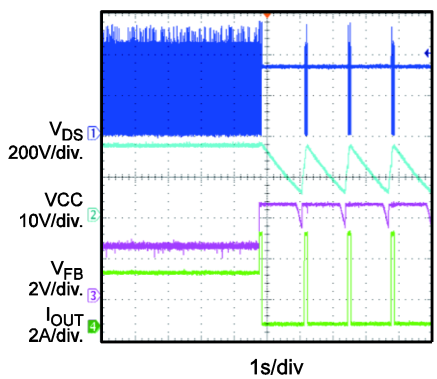
V_{IN}=265VAC



Output Ripple

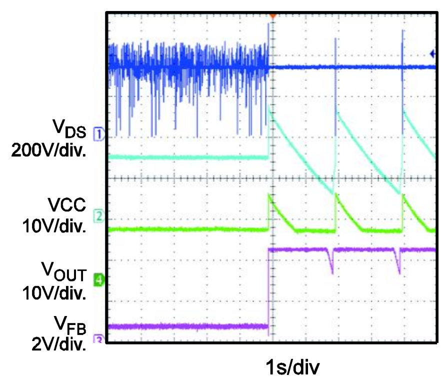


OLP Entry

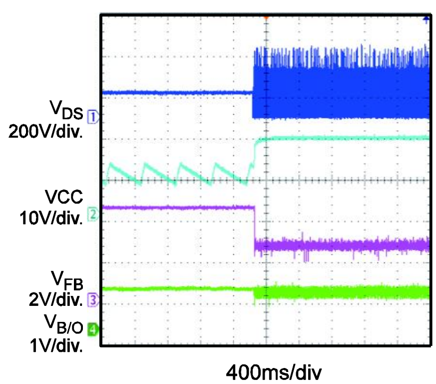


OVP Entry

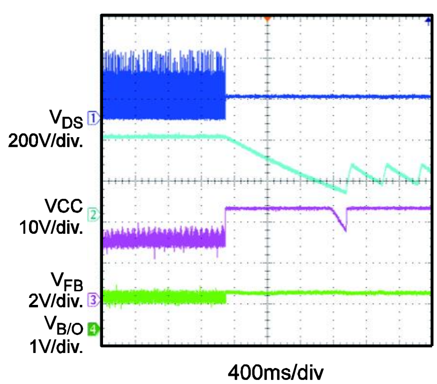
No Load



Brown-In

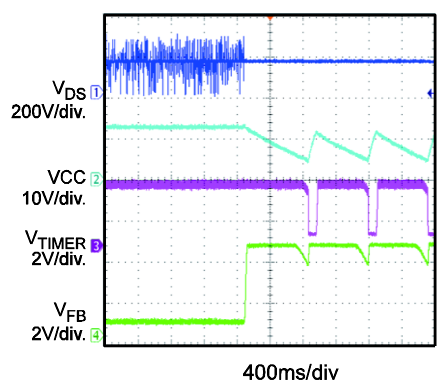


Brown-Out



OTP Entry

V_{IN}=115VAC, No Load



FUNCTIONAL BLOCK DIAGRAM

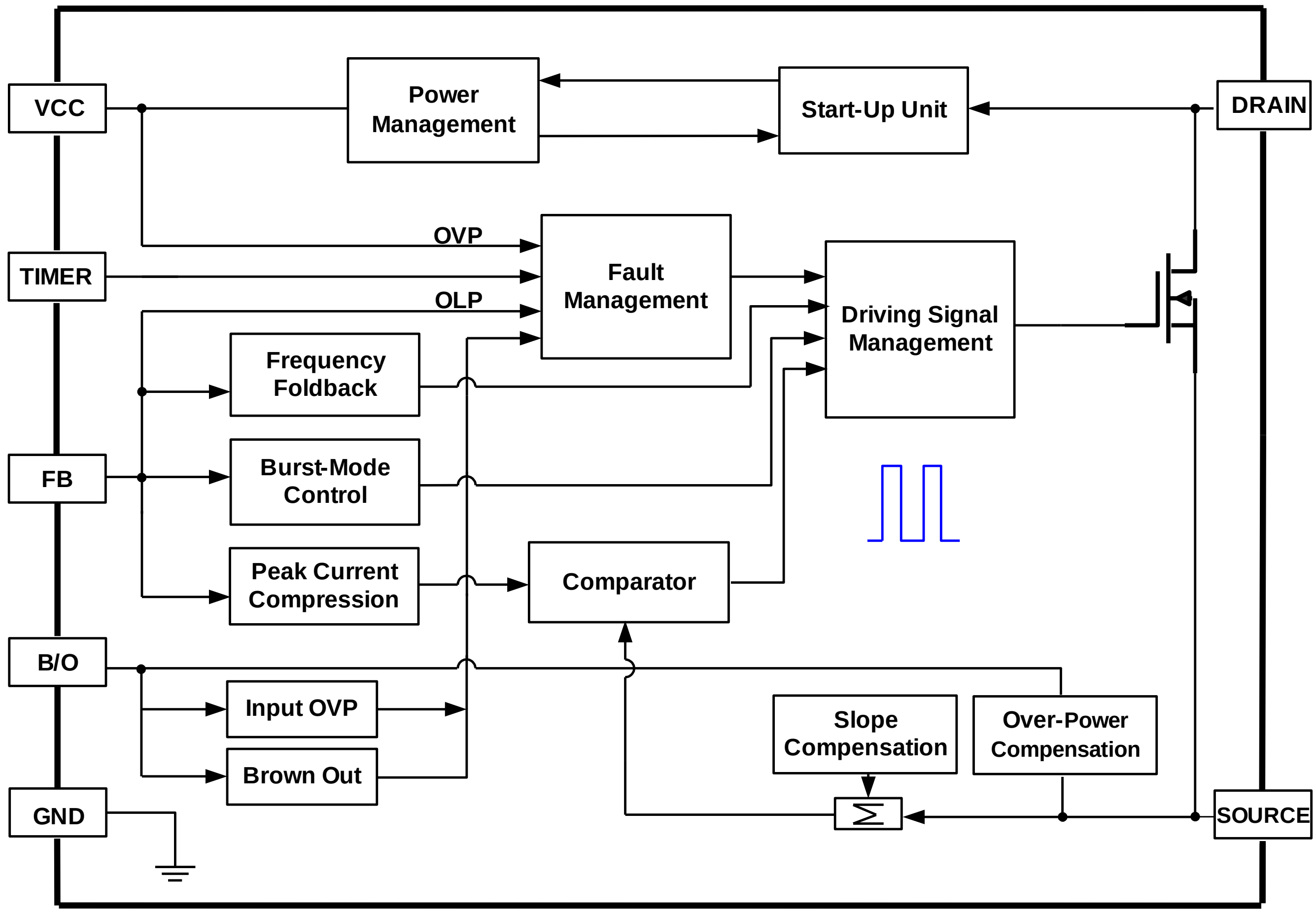


Figure 1: Functional Block Diagram

OPERATION

The HF500A-30 is a fixed-frequency, current-mode regulator with built-in slope compensation that incorporates all of the necessary features to build a reliable switch-mode power supply.

Under light-load conditions, the HF500A-30 freezes the peak current and reduces its switching frequency to 25kHz to minimize switching loss. When the output power falls below a given level, the regulator enters burst mode. To improve electromagnetic interference (EMI) performance, the HF500A-30 uses frequency jittering, and implements a slow driver speed to achieve an optimized radiated emission performance.

Fixed Frequency with Jittering

Frequency jittering reduces EMI by spreading out the energy (see Figure 2).

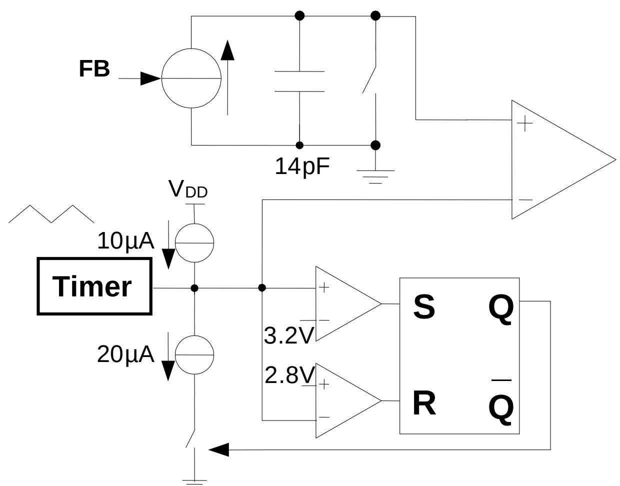


Figure 2: Frequency Jitter Circuit

An internal capacitor is charged with a controlled current source, which is fixed when the FB voltage (V_{FB}) exceeds 2V, and its voltage is compared to the TIMER voltage (V_{TIMER}). V_{TIMER} is a triangular wave between 2.8V and 3.2V with a charging/discharging current (see Figure 3). The switching frequency can be calculated with Equation (1):

$$f_{SW} = \frac{1\cdot 10^{6}}{5.28\cdot V_{TIMER}/V + 0.2} Hz \qquad (1)$$

t_{JITTER} can be estimated with Equation (2):

$$t_{JITTER} = 8\cdot C_{TIMER}/nF\cdot 10^{-5} s \qquad (2)$$

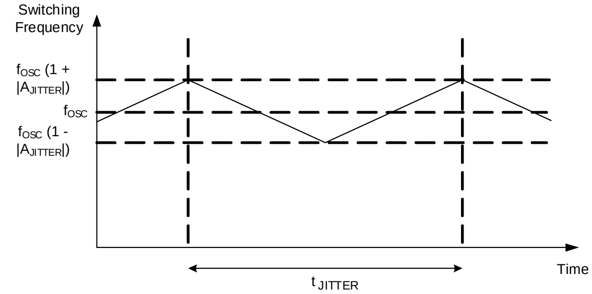


Figure 3: Frequency Jittering

Frequency Foldback

To achieve high efficiency for all load conditions, the HF500A-30 implements frequency foldback while under light-load conditions.

When the load drops to a particular threshold, the regulator holds the V_{FOLD} peak current steady and reduces the charging current. The switching frequency drops to $f_{OSC(MIN)}$ to reduce switching loss. If the load continues to drop, the peak current decreases with a fixed frequency to avoid audible noise. Figure 4 shows the frequency and peak current vs. V_{FB}.

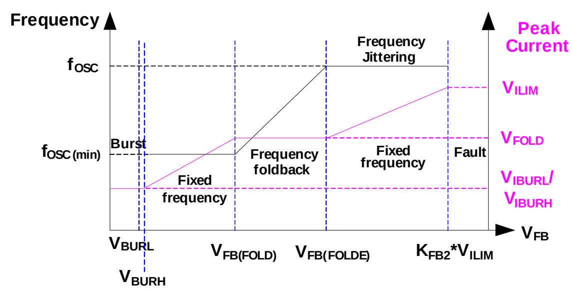


Figure 4: Frequency and Peak Current vs. V_{FB}

Current-Mode Operation with Slope Compensation

The primary peak current is controlled by V_{FB}. When the peak current reaches the level determined by V_{FB}, the MOSFET turns off. The HF500A-30's internal synchronous slope compensation (S_{RAMP}) prevents sub-harmonic oscillation when the duty cycle exceeds 50% in continuous conduction mode (CCM). This allows the HF500A-30 to work across a wide input voltage range.

High-Voltage Start-Up Current Source

Initially, the IC is self-supplied by the internal high-voltage current source, which is drawn from DRAIN. The IC turns off the current source once the voltage on VCC reaches VCC_{OFF}.

If the voltage on VCC falls below VCC_{UVLO}, the switching pulse stops, and the current source turns on again. The auxiliary winding takes over the power supply for the IC when the output voltage rises normally to the set voltage. The lower threshold of VCC is pulled down from VCC_{UVLO} to VCC_{PRO} if a fault condition occurs. The fault conditions includes overload protection (OLP), short-circuit protection (SCP), brown-out, over-voltage protection (OVP), and over-temperature protection (OTP) (see Figure 5).

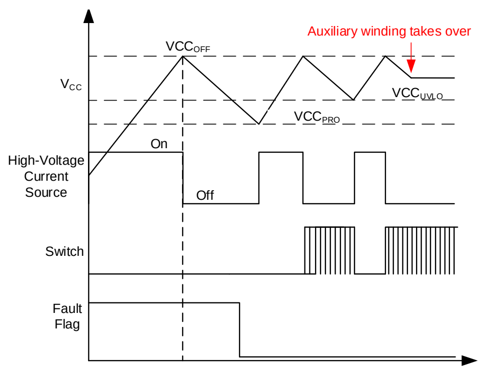


Figure 5: VCC Power Supply Process

Soft Start (SS)

The HF500A-30 adopts a soft-start procedure that gradually increases the current limit and switching frequency to reduce the stress on the power components.

During soft start, the TIMER capacitor is slowly charged in two steps. The TIMER voltage controls the current limit and switching frequency (see Figure 6).

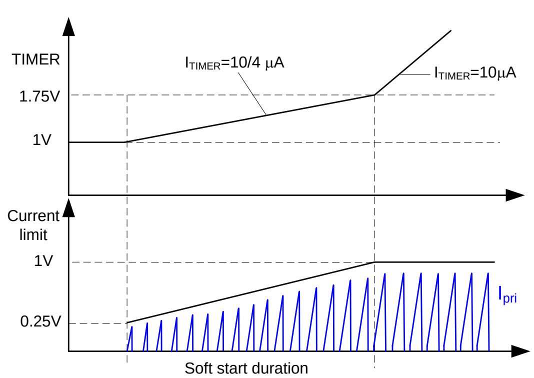


Figure 6: Soft Start

The TIMER capacitor determines the start-up duration, calculated with Equation (3):

$$t_{SOFT\_START} = 0.3 \cdot C_{TIMER} / nF \cdot 10^{-3} s \quad (3)$$

Burst-Mode Operation

The HF500A-30 uses burst-mode operation to minimize power dissipation under no-load or light-load conditions. As the load decreases, V_{FB} decreases. The HF500A-30 stops switching when V_{FB} drops below the low threshold (V_{BURL}), which indicates a sufficiently high output voltage. Switching resumes once V_{FB} rises to the high threshold (V_{BURH}), which indicates an insufficient output voltage. This regulates the output voltage. Burst-mode operation alternately enables and disables the MOSFET's switching cycle, which reduces switching loss under no-load or light-load conditions.

Timer-Based Overload Protection (OLP)

If the switching frequency is fixed in a flyback converter, the maximum output power is limited by the peak current. When the load current exceeds the design value, the output voltage drops below its set value due to the maximum power limit. The current flowing through the primary and secondary optocoupler is reduced, and V_{FB} is pulled high (see Figure 7).

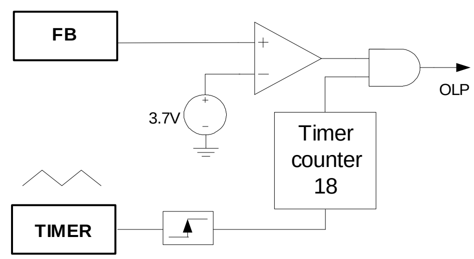


Figure 7: Overload Protection Block

If V_{FB} rises above V_{OLP}, this is considered an error flag. The timer starts counting the rising edge of the internal oscillator, which is controlled by the TIMER pin. The timer resets once the error flag is removed. When the timer has counted to 18 cycles, the device triggers overload protection (OLP). This timer-based OLP prevents OLP from mistriggering when the power supply is starting up, or during a load transition (see Figure 8).

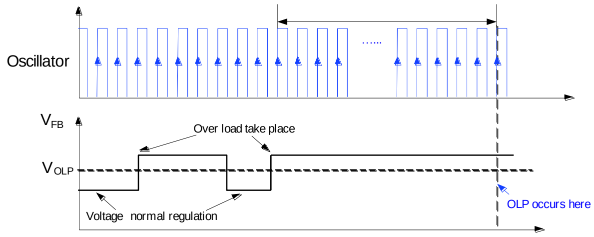


Figure 8: Overload Protection Function

Over-Power Compensation (OPC)

An internal offset proportional to the input voltage is added to the current-sense voltage. The input voltage (V_{IN}) is sampled by the B/O pin through a resistor divider. This equalizes the peak current across the entire V_{IN} range by reducing the peak current under high input voltages. This results in an overall constant OLP point, regardless of V_{IN}. Figure 9 shows the compensation in relation to the voltage on the FB and B/O pins.

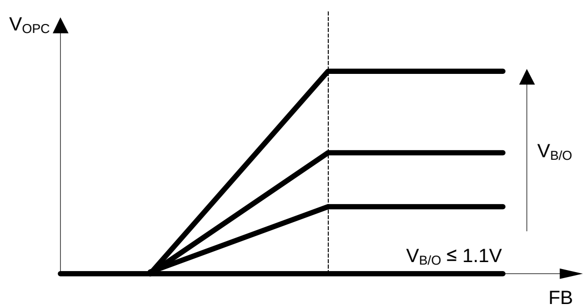


Figure 9: Compensation Voltage vs. FB and B/O

The maximum OPC voltage (V_{OPC}) can be calculated with Equation (4):

$$V_{OPC} = 0.094 \cdot (V_{B/O} - 1.1V) \quad (4)$$

Input Brown-In/Brownout and Input Over-Voltage Protection (OVP)

Input brown-in/brownout and input over-voltage protection (OVP) are detected by monitoring the B/O pin.

For the brown-in function, the HF500A-30 does not work until the B/O voltage exceeds V_{B/O_IN}.

If the B/O voltage drops below V_{B/O_OUT}, this is considered a brownout flag. If this condition lasts for a certain time ($t_{B/O}$), brownout is triggered, and the HF500A-30 stops operating.

Input OVP is triggered when the B/O voltage exceeds $OVP_{B/O}$ for a certain time ($t_{OVPB/O}$). If input OVP occurs, the HF500A-30 stops operating.

If the voltage on B/O exceeds V_{DIS}, the input brownout and input OVP functions are disabled.

If the B/O functions are not required, connect the B/O pin to VCC through a resistor to ensure that the voltage on B/O exceeds V_{DIS} during normal operation.

Short-Circuit Protection (SCP)

The HF500A-30 features short-circuit protection (SCP). The device senses the SOURCE voltage and stops switching if V_{SOURCE} reaches V_{SCP} after a short leading-edge blanking time (t_{LEB2}). Normal operation resumes when the fault is removed.

Over-Temperature Protection (OTP)

If the inner temperature of the HF500A-30 exceeds T_{OTP}, over-temperature protection (OTP) is triggered. The device's switching cycle is turned off by the OTP logic, and the VCC lower threshold is pulled down from VCC_{UVLO} to VCC_{PRO}. The HF500A-30 resumes operation once the temperature drops below the hysteresis value ($T_{OTP(HYS)}$).

VCC Over-Voltage Protection (OVP)

The HF500A-30 enters an auto-restart fault condition if the VCC voltage rises above the over-voltage protection (OVP) threshold (V_{OVP}) for a certain time (t_{OVP}). Typically, VCC OVP is used for indirect output OVP. This occurs when the optocoupler fails, and the output voltage fails to regulate.

TIMER Protection

The HF500A-30 latches off if the TIMER pin's voltage drops below $V_{TIMER(LATCH)}$ for a certain time (t_{LATCH}). This allows the TIMER pin to set additional protections, such as external OVP and OTP.

Leading-Edge Blanking (LEB)

An internal leading-edge blanking (LEB) unit that contains two LEB times (t_{LEB1} and t_{LEB2}) is used to prevent premature switching pulse termination. Premature switching pulse termination can occur due to a current spike when the MOSFET turns on. This spike is caused by parasitic capacitance. During the blanking time, the current comparator is disabled and cannot turn off the MOSFET (see Figure 10).

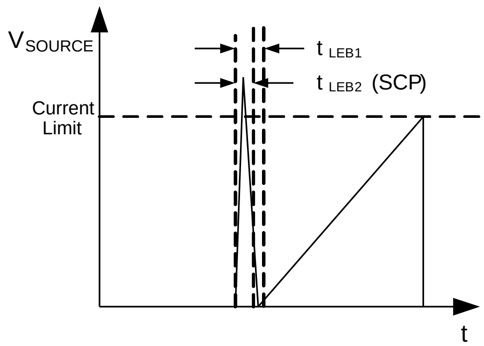


Figure 10: Leading-Edge Blanking

APPLICATION INFORMATION

Selecting the VCC Capacitor

When the input voltage is applied, the VCC capacitor is charged up by the internal high-voltage current source. VCC should be held above VCC_{UVLO} until the output voltage builds up, so that VCC is supplied by the auxiliary winding. Otherwise, VCC_{UVLO} terminates the switching, and the output voltage cannot be set normally. For most applications, choose a VCC capacitor value between 10µF and 47µF. The value for the VCC capacitor can be estimated with Equation (5):

$$C_{VCC} > \frac{I_{CC} * t_{RISE}}{VCC_{OFF} - VCC_{UVLO}} \quad (5)$$

Where I_{CC} is the internal IC consumption, and t_{RISE} is the output voltage rising period.

Primary-Side Inductor Design (L_M)

The HF500A-30 uses internal slope compensation to support CCM and duty cycles exceeding 50%. Use K_P to indicate the CCM depth. K_P is the ratio between the primary inductor's ripple current and the peak current ($0 < K_P \leq 1$) (see Figure 11). When $K_P = 1$, this indicates discontinuous conduction mode (DCM). An optimal K_P value is between 0.7 and 0.9 for the universal input range, and DCM should be implemented if the input voltage is $230V_{AC}$. A large inductance leads to a smaller K_P. This reduces the RMS current but increases the transformer size and the switching loss consumption, especially with high-line inputs.

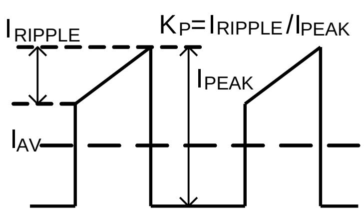


Figure 11: Typical Primary Current Waveform

The input power (P_{IN}) at the minimum input can be estimated with Equation (6):

$$P_{IN} = \frac{V_O \cdot I_O}{\eta} \quad (6)$$

Where V_O is the output voltage (V_{OUT}), I_O is the rated output current (I_{OUT}), and η is the estimated efficiency.

η is typically between 0.75 and 0.85, depending on the input range and output voltage.

For CCM at the minimum input voltage, calculate the converter duty cycle with Equation (7):

$$D = \frac{(V_O + V_F) \cdot N}{(V_O + V_F) \cdot N + V_{IN(MIN)}} \quad (7)$$

Where V_F is the secondary diode's forward voltage, N is the transformer turns ratio, and $V_{IN(MIN)}$ is the minimum voltage on the bulk capacitor.

The MOSFET on time (t_{ON}) can be calculated with Equation (8):

$$t_{ON} = D \cdot t_S \quad (8)$$

Where t_S is the switching cycle period ($1/f_{OSC}$).

The average value of the primary current (I_{AV}) can be calculated with Equation (9):

$$I_{AV} = \frac{P_{IN}}{V_{IN(MIN)}} \quad (9)$$

The primary current peak (I_{PEAK}) can be calculated with Equation (10):

$$I_{PEAK} = \frac{I_{AV}}{(1 - \frac{K_P}{2}) \cdot D} \quad (10)$$

The primary current ripple (I_{RIPPLE}) can be calculated with Equation (11):

$$I_{RIPPLE} = K_P \cdot I_{PEAK} \quad (11)$$

The primary current valley (I_{VALLEY}) can be calculated with Equation (12):

$$I_{VALLEY} = (1 - K_P) \cdot I_{PEAK} \quad (12)$$

L_M can be calculated with Equation (13):

$$L_M = \frac{V_{IN(MIN)} \cdot t_{ON}}{I_{RIPPLE}} \quad (13)$$

Current-Sense Resistor

Figure 12 shows the peak current comparator logic. When the sum of the sensing resistor voltage and the slope compensator reaches

V_{LIMIT}, the comparator goes high to reset the RS trigger, and the MOSFET turns off.

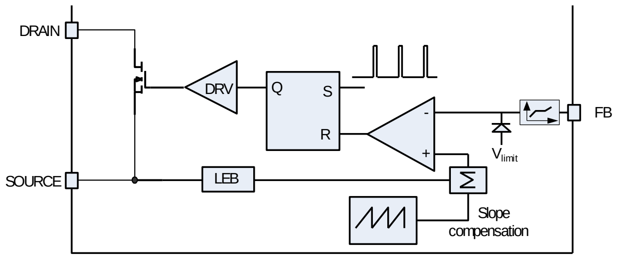


Figure 12: Peak Current Comparator Circuit

Figure 13 shows the peak current comparator's subsequent waveform.

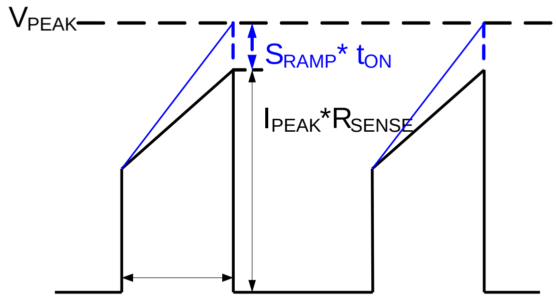


Figure 13: Peak Current Comparator

The maximum current limit is V_{ILIM}. The slope compensation ramp is S_{RAMP}. Given a certain margin, V_{PEAK} should be 95% of V_{ILIM} at full loads. Calculate the voltage on the sensing resistor (V_{SENSE}) with Equation (14):

$$V_{SENSE} = 95\% \cdot V_{ILIM} - S_{RAMP} \cdot t_{ON} \quad (14)$$

The value of the sense resistor (R_{SENSE}) can be estimated with Equation (15):

$$R_{SENSE} = \frac{V_{SENSE}}{I_{PEAK}} \quad (15)$$

Select a current-sense resistor with an appropriate power rating. Estimate the current-sense resistor's power loss with Equation (16):

$$P = \left[\left(\frac{I_{PEAK} + I_{VALLEY}}{2}\right)^2 + \frac{1}{12}\left(I_{PEAK} - I_{VALLEY}\right)^2\right] \cdot D \cdot R_{SENSE} \quad (16)$$

Jitter Period

Frequency jitter is used as an effective method to reduce EMI by dissipating energy. The nth order harmonic noise bandwidth can be calculated with Equation (17):

$$B_{Tn} = n \cdot (2 \cdot \Delta f + f_{JITTER}) \quad (17)$$

Where Δf is the frequency jitter amplitude.

If B_{Tn} exceeds the resolution bandwidth (R_{BW}) of the spectrum analyzer (200Hz for noise frequencies below 150kHz, and 9kHz for noise frequencies between 150kHz and 30MHz), the spectrum analyzer receives less noise energy.

Equation (2) on page 14 describes the jitter period (t_{JITTER}). A lower jitter frequency (f_{JITTER}) is more effective for EMI reduction. However, the measurement bandwidth requires f_{JITTER} to exceed R_{BW} for effective EMI reduction. f_{JITTER} should also be lower than the control loop gain crossover frequency to avoid disturbing the output voltage regulation.

The TIMER capacitor must be selected wrr. A larger-value capacitor may cause start-up to fail at full loads because of the longer soft start-up duration calculated with Equation (3) on page 15. However, a smaller-value capacitor causes the timer period to decrease, which overloads the timer count capability. This may cause logic problems. For most applications, it is recommended for f_{JITTER} to be between 200Hz and 400Hz.

Ramp Compensation

In peak current control, sub-harmonic oscillations occur when the duty cycle exceeds 50% in CCM. The HF500A-30 solves this problem with internal ramp compensation. The ratio between the primary current slew rate and secondary current slew is called α. Calculate α with Equation (18):

$$\alpha = \frac{\frac{D_{MAX} \cdot V_{IN(MIN)}}{(1-D_{MAX}) \cdot L_M} \cdot R_{SENSE} - m_a}{\frac{V_{IN(MIN)}}{L_M} \cdot R_{SENSE} + m_a} \quad (18)$$

Where m_a is the minimum internal slope value of the compensation ramp (about 18mV/µs).

For stable operation, α must be less than 1.

Design Example

Table 1 lists a design example of the HF500A-30 for power adapter applications.

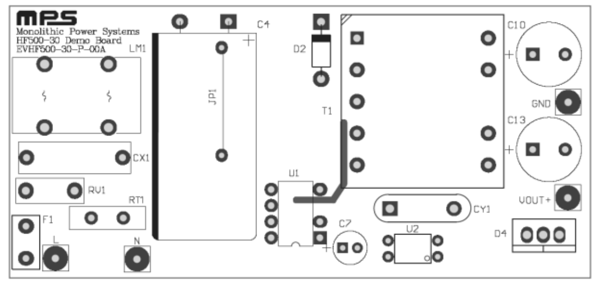
Table 1: Design Specifications

V_{IN}	85V_{AC} to 265V_{AC}
V_{OUT}	12V
I_{OUT}	2.5A

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, good EMI performance, and good thermal performance. For the best results, refer to Figure 13 and follow the guidelines below:

1. To reduce EMI noise, minimize the loop area formed by the input capacitor, the transformer's primary winding, the MOSFET drain and source of the HF500A-30, and the sensing resistor.
2. Minimize the voltage jumping area (e.g. the MOSFET drain and the anode of the secondary diode) for better EMI. DRAIN is a fused lead pin, which helps with thermal radiation when it is connected to copper. If required, make a tradeoff between EMI and thermal performance.
3. Minimize the snubber circuit loop to reduce EMI.
4. Minimize the secondary loop area of the output diode and output filter to reduce EMI noise.
5. Provide sufficient copper areas at the cathode terminal of the output diode to act as a heat sink.
6. Place the AC input far away from the switching nodes to minimize any noise coupling that may bypass the input filter.
7. Place the bypass capacitor as close to the IC as possible.
8. Use a single-point connection at the negative terminal of the input filter capacitor for the IC's ground and biased winding return.



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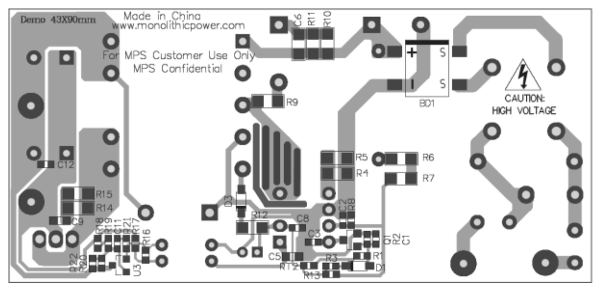


Bottom

Figure 13: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

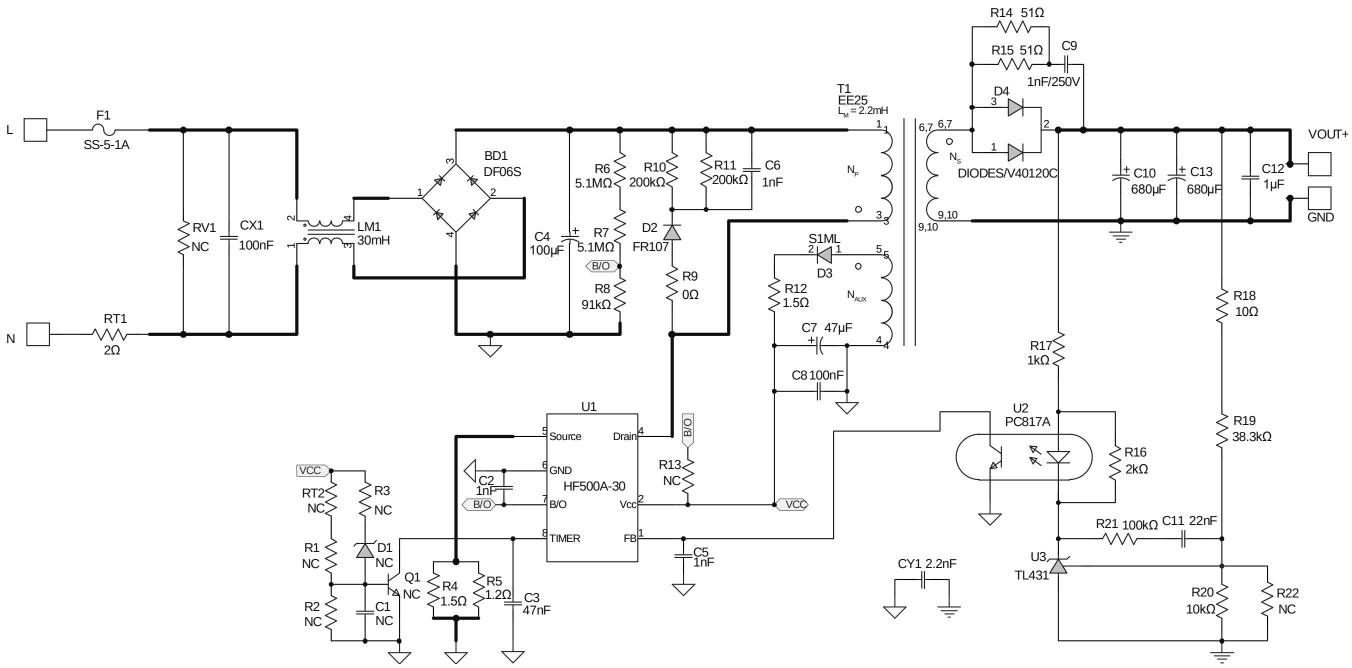
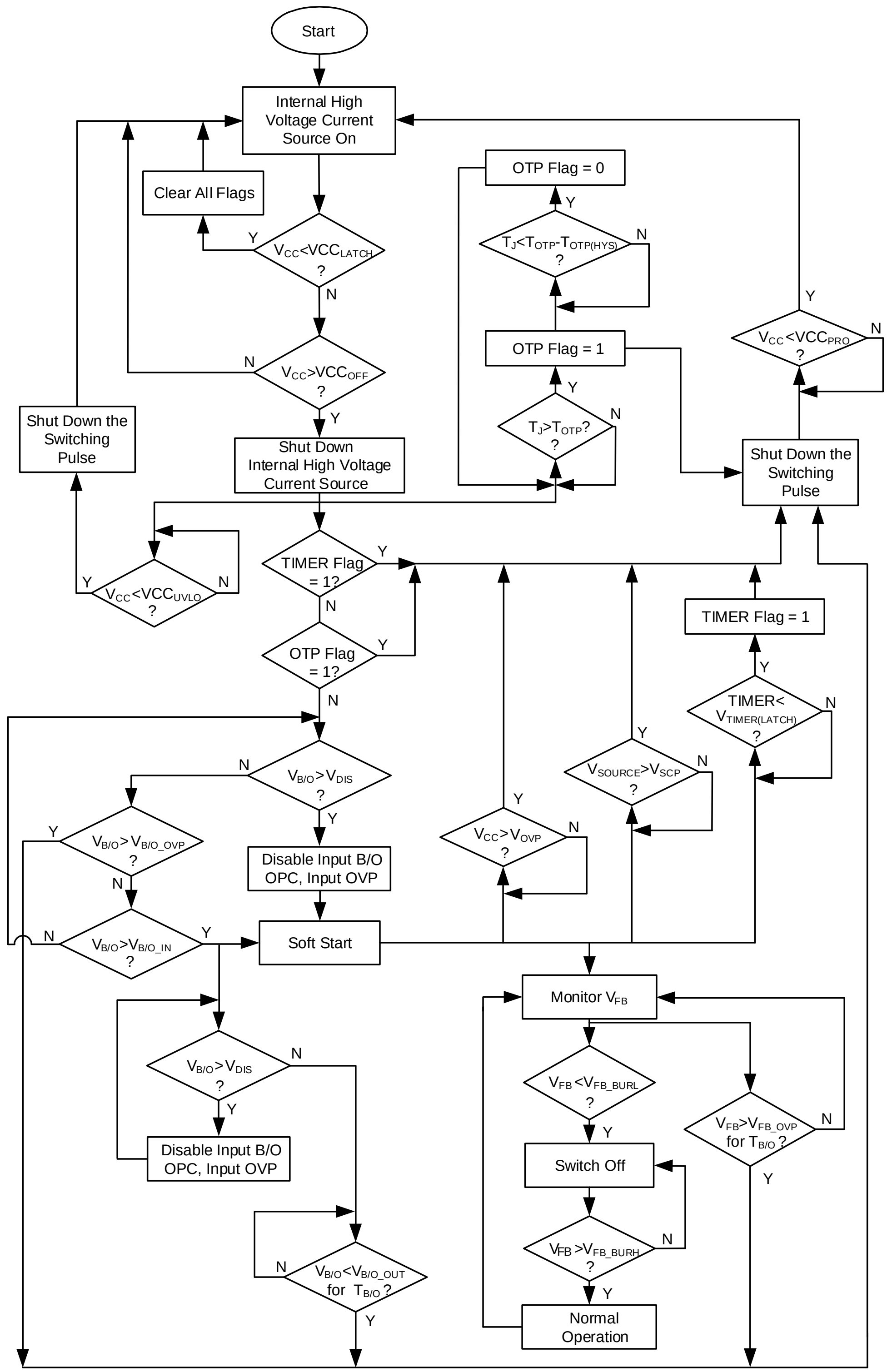


Figure 14: Typical Application Circuit

FLOWCHART

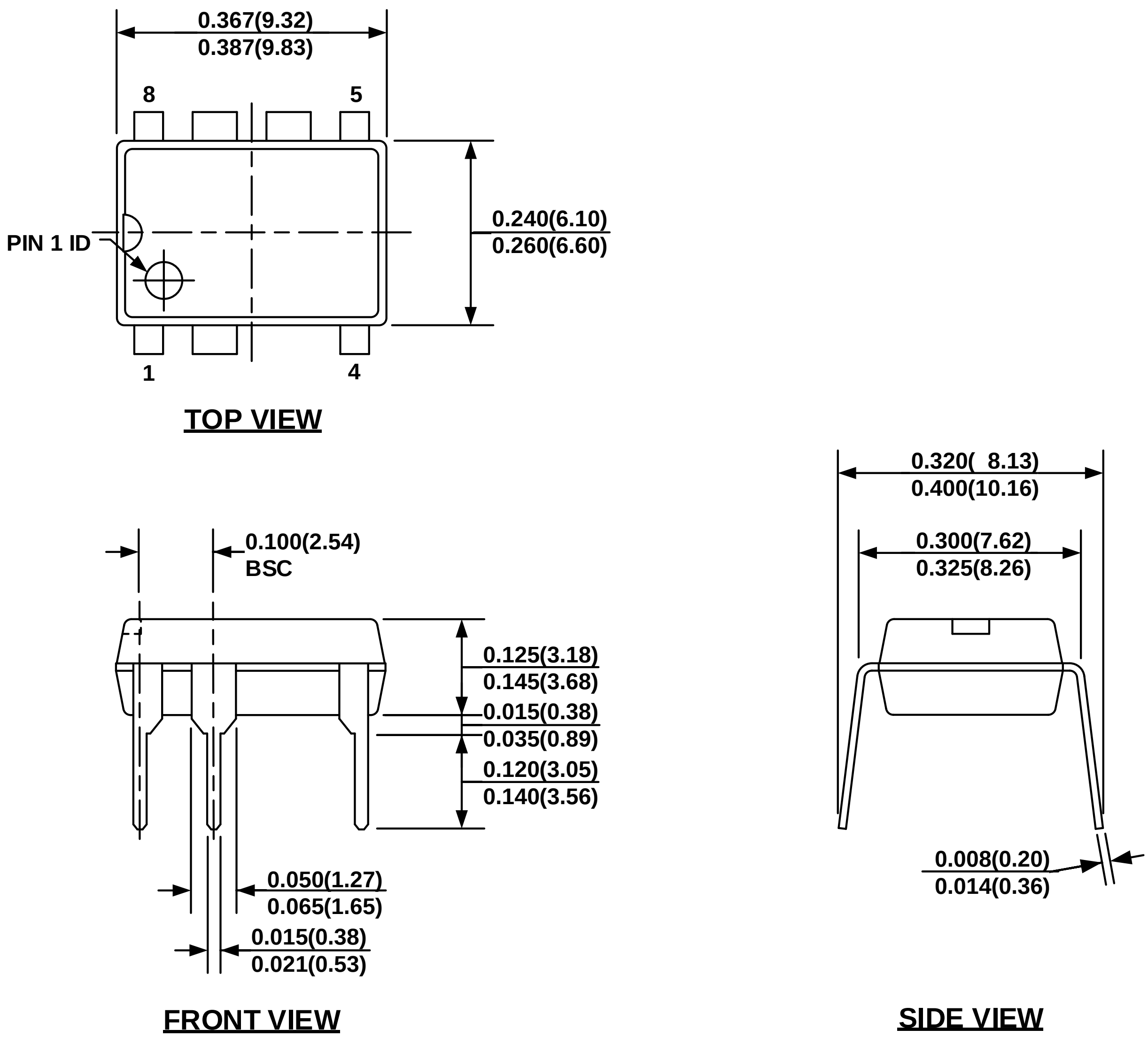


VCC UVLO, brown-out, OVP, OLP and OTP are auto-restart. Only TIMER faults are latch-off.
VCC should drop to VCC_{LATCH} to release the latch condition (usually by disconnecting the input).

Figure 15: Flowchart

PACKAGE INFORMATION

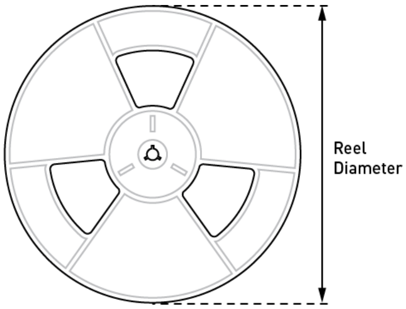
PDIP8-7B



NOTE:

1) CONTROL DIMENSION ARE IN INCHES. DIMENSIONS IN BRACKETS ARE IN MILLIMETERS.
2) PACKAGE LENGTH AND WIDTH DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
3) JEDEC REFERENCE IS MS-001.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
HF500AGP-30	PDIP8-7B	N/A	50	N/A	N/A	N/A	N/A

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/26/2021	Initial Release	-