



## ULN2803

## LINEAR INTEGRATED CIRCUIT

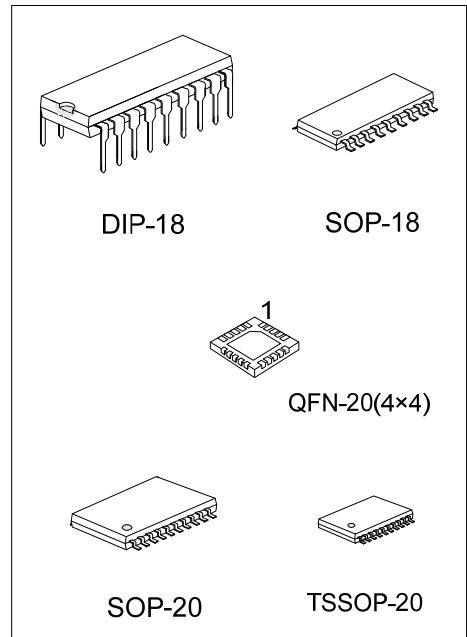
### EIGHT DARLINGTON ARRAYS

#### DESCRIPTION

The UTC **ULN2803** is high-voltage, high-current Darlington drivers comprised of eight NPN Darlington pairs.

#### FEATURES

- \*Output current (single output) 500mA MAX.
- \*High sustaining voltage output 50V MIN.
- \*Output clamp diodes
- \*Inputs compatible with various types of logic

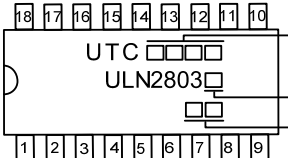
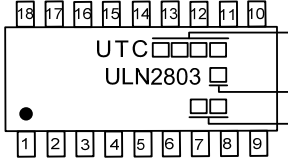
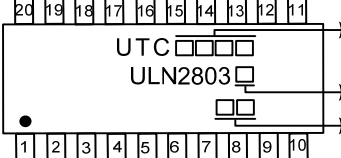
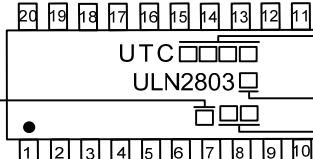
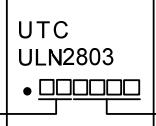


#### ORDERING INFORMATION

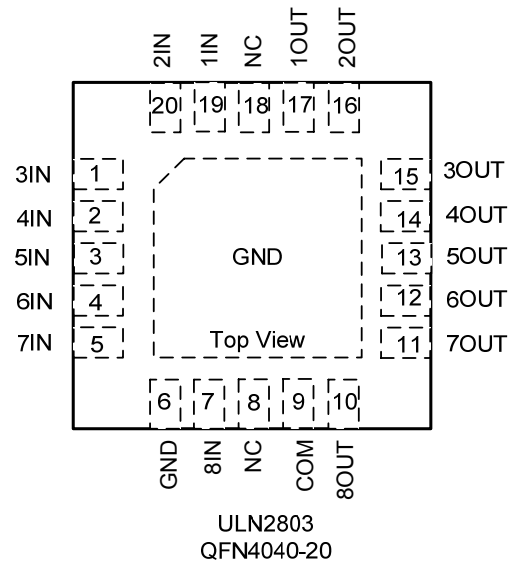
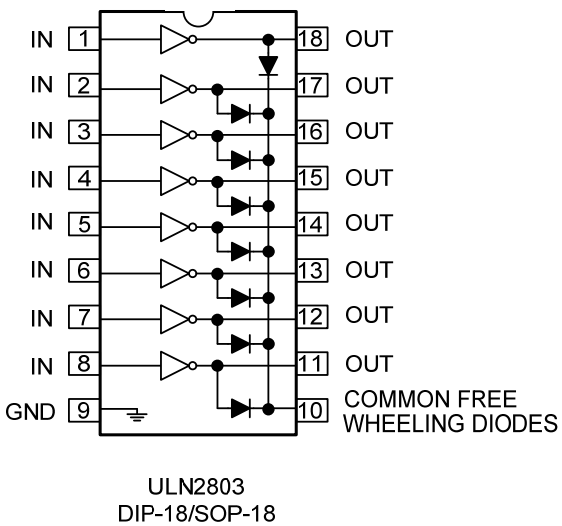
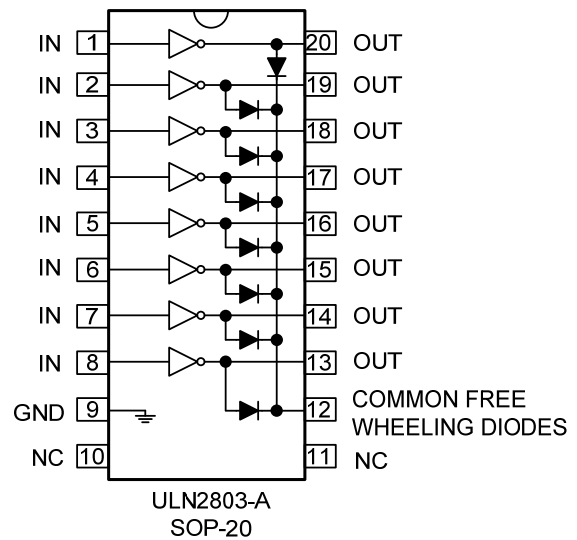
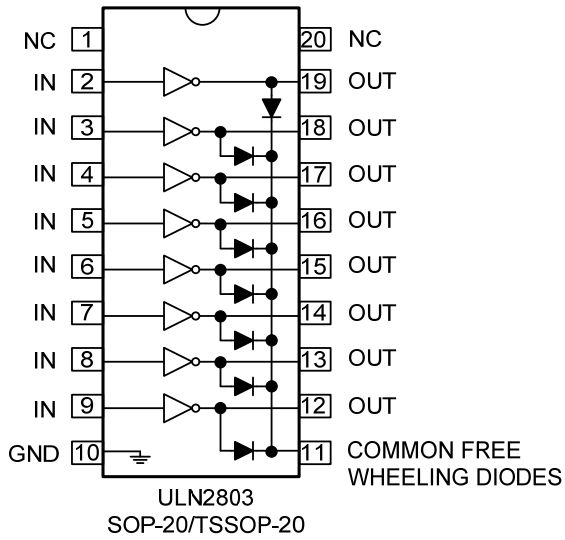
Ordering Number		Package	Packing
Lead Free	Halogen Free		
ULN2803L-D18-T	ULN2803G-D18-T	DIP-18	Tube
ULN2803L-S18-R	ULN2803G-S18-R	SOP-18	Tape Reel
ULN2803L-S20-R	ULN2803G-S20-R	SOP-20	Tape Reel
ULN2803L-S20-A-R	ULN2803G-S20-A-R	SOP-20	Tape Reel
ULN2803L-P20-R	ULN2803G-P20-R	TSSOP-20	Tape Reel
ULN2803L-Q20-4040-R	ULN2803G-Q20-4040-R	QFN-20(4x4)	Tape Reel

<p>ULN2803G-S20-A-R</p> <p>(1)Packing Type (2)Pin Code (3)Package Type (4)Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) x: refer to PIN CONFIGURATIONS (3) T: Tube, R: Tape Reel (4) G: Halogen Free and Lead Free, L: Lead Free</p>
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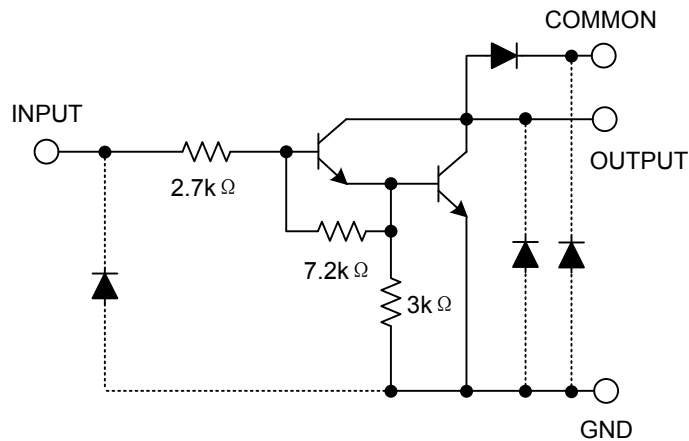
### MARKING

PACKAGE	MARKING
DIP-18	 <p>             18 17 16 15 14 13 12 11 10 → Date Code              UTC □□□□ → L: Lead Free              ULN2803 □ → G: Halogen Free              □ □ → Lot Code              1 2 3 4 5 6 7 8 9           </p>
SOP-18	 <p>             18 17 16 15 14 13 12 11 10 → Date Code              UTC □□□□ → L: Lead Free              ULN2803 □ → G: Halogen Free              □ □ → Lot Code              1 2 3 4 5 6 7 8 9           </p>
SOP-20 / TSSOP-20 (For ULN2803)	 <p>             20 19 18 17 16 15 14 13 12 11 → Date Code              UTC □□□□ → L: Lead Free              ULN2803 □ → G: Halogen Free              □ □ → Lot Code              1 2 3 4 5 6 7 8 9 10           </p>
SOP-20 (For ULN2803-A)	 <p>             20 19 18 17 16 15 14 13 12 11 → Date Code              UTC □□□□ → L: Lead Free              ULN2803 □ → G: Halogen Free              □ □ → Lot Code              Pin Code ← 1 2 3 4 5 6 7 8 9 10           </p>
QFN4040-20	 <p>             UTC              ULN2803              • □□□□□□ → Lot Code → Date Code           </p>

### ■ PIN CONFIGURATIONS



### ■ SCHEMATICS (EACH DRIVER)



Note: The input and output parasitic diodes cannot be used as clamp diodes.

### ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Input Voltage		$V_{IN}$	-0.5 ~ 30	V
Output Sustaining Voltage		$V_{CE(SUS)}$	-0.5 ~ 50	V
Output Current		$I_{OUT}$	500	mA/ch
Clamp Diode Reverse Voltage		$V_R$	50	V
Clamp Diode Forward Current		$I_F$	500	mA
Power Dissipation	DIP-18	$P_D$	1.47	W
	SOP-18		0.92 / 1.31 (Note 2)	W
	SOP-20			W
	TSSOP-20			W
	QFN4040-20			0.6
Operating Temperature		$T_{OPR}$	-40 ~ +85	°C
Storage Temperature		$T_{STG}$	-40 ~ +150	°C

Notes: 1. Absolute maximum ratings are stress ratings only and functional device operation is not implied. The device could be damaged beyond Absolute maximum ratings.

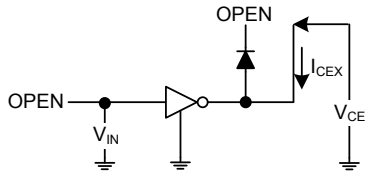
2. On glass epoxy PCB (75x144x1.6mm Cu 20%).

### ■ ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ , unless otherwise specified)

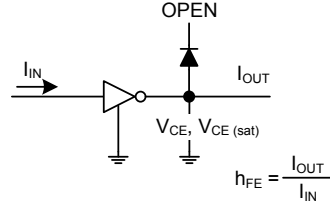
PARAMETER		SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Leakage Current		$I_{CEX}$	1	$V_{CE}=50\text{V}, T_A=25^\circ\text{C}$ $V_{CE}=50\text{V}, T_A=85^\circ\text{C}$			50 100	$\mu\text{A}$
Collector-Emitter Saturation Voltage		$V_{CE(SAT)}$	2	$I_{OUT}=350\text{mA}, I_{IN}=500\mu\text{A}$ $I_{OUT}=200\text{mA}, I_{IN}=350\mu\text{A}$ $I_{OUT}=100\text{mA}, I_{IN}=250\mu\text{A}$		1.3 1.1 0.9	1.6 1.3 1.1	V
Input Current	ON	$I_{IN(ON)}$	3	$V_{IN}=3.85\text{V}, I_{OUT}=350\text{mA}$		0.93	1.35	mA
	OFF	$I_{IN(OFF)}$	4	$I_{OUT}=500\mu\text{A}, T_A=85^\circ\text{C}$	50	65		$\mu\text{A}$
Input Voltage (output on)		$V_{IN(ON)}$	5	$V_{CE}=2.0\text{V}$ $I_{OUT}=200\text{mA}$ $I_{OUT}=250\text{mA}$ $I_{OUT}=300\text{mA}$			2.4 2.7 3.0	V
Clamp Diode Reverse Current		$I_R$	6	$V_R=50\text{V}, T_A=25^\circ\text{C}$ $V_R=50\text{V}, T_A=85^\circ\text{C}$			50 100	$\mu\text{A}$
Clamp Diode Forward Voltage		$V_F$	7	$I_F=350\text{mA}$			2.0	V
Input Capacitance		$C_{IN}$				15	25	pF
Turn-On Delay		$t_{ON}$	8	$V_{OUT}=50\text{V}, R_L=125\Omega, C_L=15\text{pF}$		0.1	1	$\mu\text{s}$
Turn-Off Delay		$t_{OFF}$	8	$V_{OUT}=50\text{V}, R_L=125\Omega, C_L=15\text{pF}$		0.2	1	$\mu\text{s}$

### ■ TEST CIRCUIT

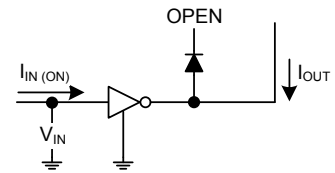
1.  $I_{CEX}$



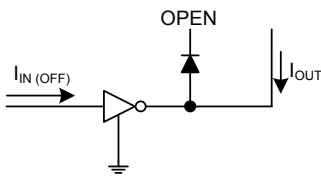
2.  $V_{CE(sat)}$ ,  $h_{FE}$



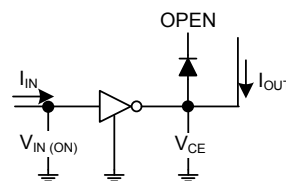
3.  $I_{IN(ON)}$



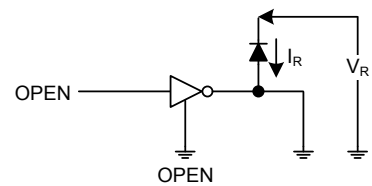
4.  $I_{IN(OFF)}$



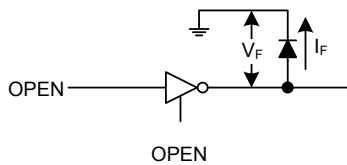
5.  $V_{IN(ON)}$



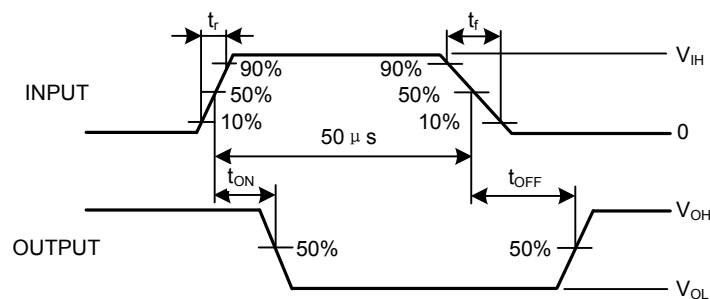
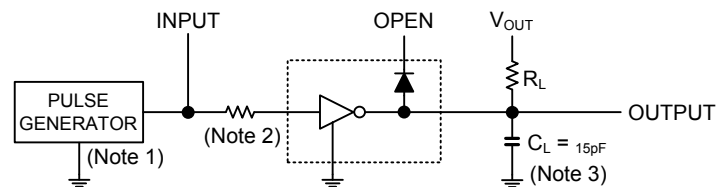
6.  $I_R$



7.  $V_F$

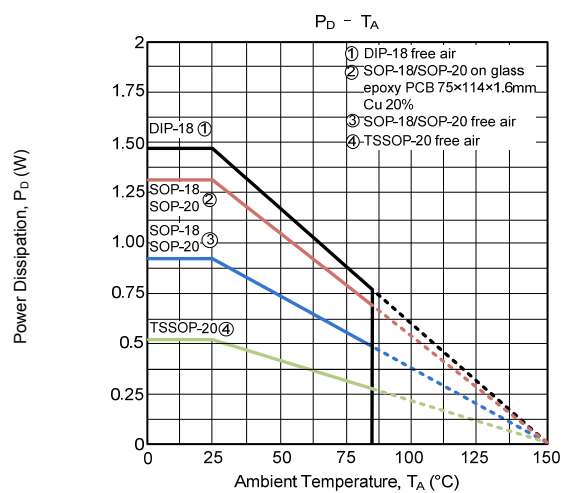
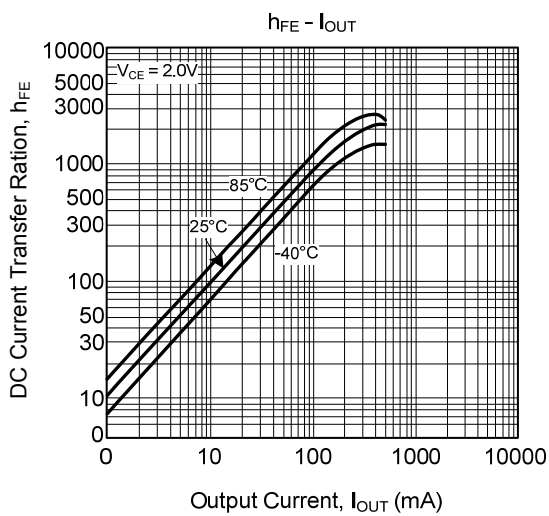
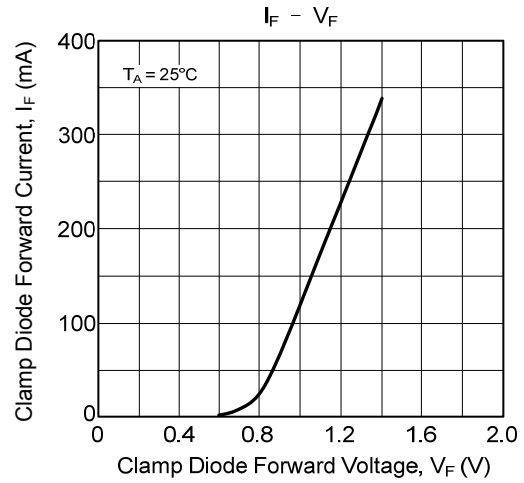
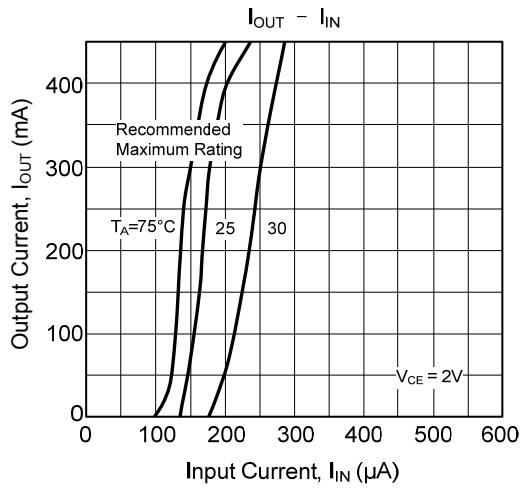
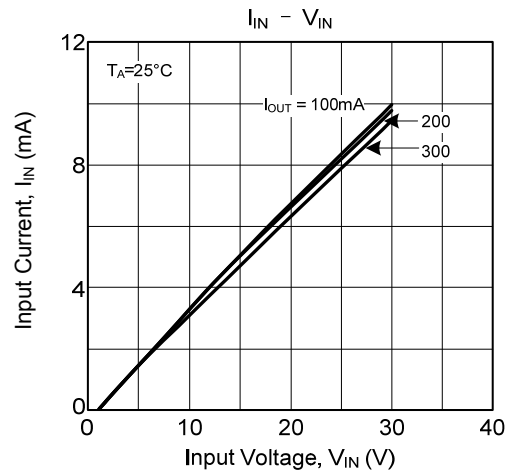
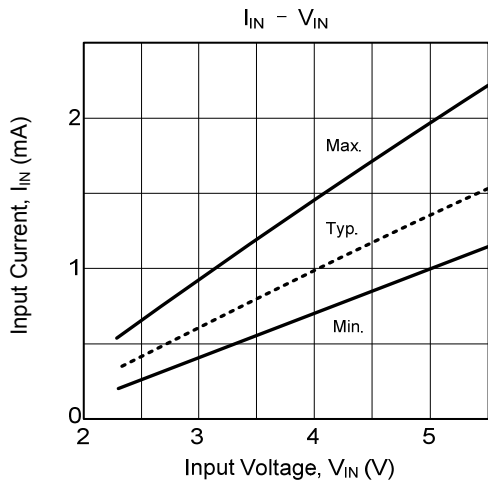


8.  $t_{ON}$ ,  $t_{OFF}$



- Notes: 1. Pulse width  $50\mu s$ , duty cycle 10%  
 Output impedance  $50\Omega$ ,  $t_r \leq 5ns$ ,  $t_f \leq 10ns$   
 2.  $R_1: 0$ ,  $V_{IH}: 3V$   
 3.  $C_L$  includes probe and jig capacitance.

## TYPICAL CHARACTERISTICS



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