MP6005A

420kHz, 8V to 80V Input Voltage Range, High-Efficiency Flyback/Forward Controller

DESCRIPTION

The MP6005A is a peak current mode flyback and forward controller. It is specifically designed for wide-input, high-frequency flyback application, and active-clamped forward application.

The MP6005A operates within a wide 8V to 80V input voltage range. Current mode control provides simple loop compensation and cycle-by-cycle current limit. The MP6005A provides a 420kHz frequency to minimize external components. The 2A GATE driver minimizes the power loss of the external MOSFET. The 0.8A SYNC driver provides a high-efficiency solution for active-clamped forward topology.

The MP6005A also features frequency dithering, soft start, overload protection (OLP) and over-voltage protection (OVP).

The MP6005A is available in a QFN-10 (3mmx3mm) package.

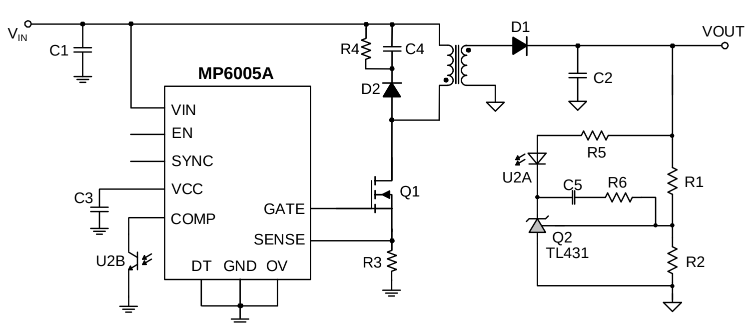
FEATURES

- Wide 8V to 80V Input Voltage Range
- 420kHz Fixed Switching Frequency
- 2A GATE and 0.8A SYNC Drivers
- Internal V_{CC} Supply Compatible with 16V External Power
- 160mV Switching Current-Sense (CS) Limit
- Synchronous SYNC Driver for High-Efficiency, Active-Clamped Forward Solution
- Hiccup Protection for Overload Protection (OLP), Short-Circuit Protection (SCP), Over-Voltage Protection (OVP) and Thermal Shutdown
- EMI Reduction with Frequency Dithering
- Available in a QFN-10 (3mmx3mm) Package

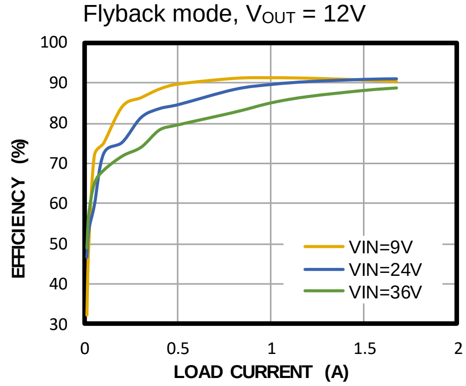
APPLICATIONS

- Security Cameras
- Video Telephones
- Wireless Access Points (WAPs)
- Point-of-Sale (POS) Systems
- Power over Ethernet (PoE) Systems
- Industrial Isolated Power Supplies

TYPICAL APPLICATION



Efficiency
Flyback mode, V_{OUT} = 12V



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6005AGQ	QFN-10 (3mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6005AGQ-Z).

TOP MARKING

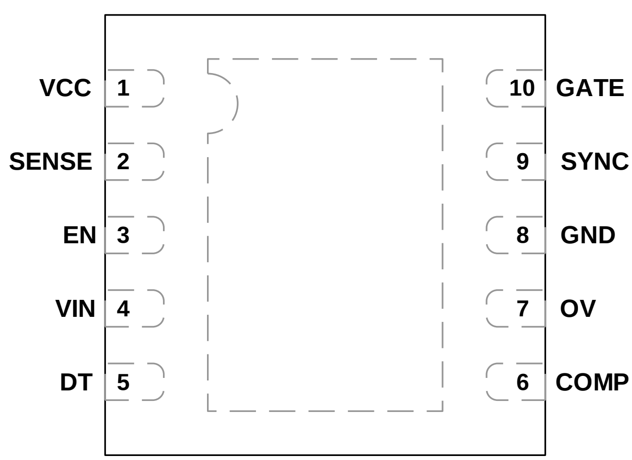
BKLY

LLL

BKL: Product code of MP6005AGQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-10 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VCC	**Internal circuit supply pin.** VCC is powered through the internal LDO from VIN. Connect a capacitor from VCC to GND to bypass the internal regulator. The VCC capacitor must be at minimum 1μF for flyback application and 4.7μF for forward application. VCC also can be powered by an external power source to save internal LDO loss.
2	SENSE	**Current sense and frequency dither setting pin.** See the Current Sense and Over-Current Protection (OCP) section on page 14, as well as the Frequency Dithering section on page 14, for more details.
3	EN	**Controller on/off control pin.** The EN pin is internally connected to GND through a 2.5MΩ resistor.
4	VIN	**Input power supply pin.** Connect a bypass capacitor from VIN to GND.
5	DT	**Dead time setting pin.** The DT pin can configure the dead time between the GATE and SYNC pins. A resistor below 33kΩ must be connected from DT to GND. See the Dead Time Setting section on page 16 for more details.
6	COMP	**Feedback pin through the optocoupler**. COMP is internally pulled up to 5V through a 10kΩ resistor.
7	OV	**Over-voltage monitor pin.** When the voltage on the OV pin exceeds 2.5V, over-voltage protection (OVP) is triggered. Connect OV to GND if OVP is not required.
8	GND	**Ground.** The GND pin is the power return for the controller.
9	SYNC	**Synchronous MOSFET gate driver pin.**
10	GATE	**Main MOSFET gate driver pin.**

ABSOLUTE MAXIMUM RATINGS [1]

VIN .... -0.3V to +100V
VCC, GATE, SYNC .... -0.3V to +18V
EN ....-0.3V to +6.5V [2]
OV ....-0.5V to +5.5V [3]
All other pins.............................. -0.3V to +5.5V
EN sinking current .... 0.5mA [2]
OV sinking current ....±2mA [3]
Continuous power dissipation (T_A = 25°C)
QFN-10 (3mmx3mm)...................... 2.66W [4] [6]
Junction temperature .... 150°C
Lead temperature .... 260°C
Storage temperature................ -65°C to +150°C

Recommended Operating Conditions [5]

Supply voltage (V_{IN}) .... 8V to 80V
Maximum VCC, GATE, SYNC voltage.......±16V
Maximum EN sinking current .... 0.4mA [2]
Maximum OV sinking current.................. 1mA [3]
Operating junction temp (T_J). ... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-10 (3mmx3mm)
EV6005A-Q-00A [6] ....47.......8.....°C/W
JESD51-7 [7]............................50…...12....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) When the EN pull-up voltage is high, a current flows into the EN pin. The current should be limited by an external pull-up resistor. See the Enable Control Setting section on page 16 for more details.
3) OV is clamped by the internal circuit. The sink/source current should be limited.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on EV6005A-Q-00A, 2-layer 90mmx35mm PCB.
7) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, V_{EN} = 5V, T_J = -40°C to 125°C (8), typical value is tested at 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power supply and UVLO						
VIN UVLO rising threshold	V_{IN-R}	V_{IN} rising, start charging V_{CC}	4.5	5.5	6.5	V
VIN UVLO falling threshold	V_{IN-F}	V_{IN} falling	3.8	4.8	5.8	V
VCC regulation voltage	V_{CC}	Load = 0mA to 20mA		8.5		V
VCC dropout voltage	$V_{CC-DROP}$	V_{IN} = 8V, I_{VCC} = 10mA		1.5		V
VCC UVLO rising threshold	V_{CC-R}	V_{IN} exceeds V_{IN-R}, V_{CC} rising	5.4	5.7	6.0	V
VCC UVLO falling threshold	V_{CC-F}	V_{IN} exceeds V_{IN-R}, V_{CC} falling	5.0	5.3	5.6	V
Quiescent current	I_Q	DT = 0V, V_{COMP} = 0V, I_Q = I_{IN}-I_{COMP}, GATE and SYNC floating		550		μA
Shutdown current	I_{SD}	V_{EN} = 0V			1	μA
Enable Control						
EN turn-on threshold	V_{EN-R}	Start switching	1.93	2	2.07	V
EN turn-on hysteresis	V_{EN-HYS}	Stop switching		0.2		V
EN high micro-power threshold	V_{EN-H}	Start internal logic			1.0	V
EN low micro-power threshold	V_{EN-L}	Stop internal logic	0.4			V
EN input current	I_{EN}	V_{EN} = 5V		2		μA
EN turn-on delay		EN on to GATE output		500		μs
OVP Monitor						
OVP threshold	V_{OVP}		2.4	2.5	2.6	V
OV leakage current	I_{OV}	V_{OV} = 2V		10	50	nA
OVP hiccup off time				340		ms
Error Amplifier						
COMP high voltage	V_{COMP}	DT = 0V, float COMP		5		V
COMP internal pull-up resistor				10		kΩ
Soft Start						
Internal soft-start time	t_{SS}	When DT = 0V, test COMP from 1.5V to 3.5V		20		ms
Current Sense						
Maximum current sense limit	$I_{LIMIT-MAX}$		140	160	180	mV
SCP limit			240	300	360	mV
Current leading-edge blanking time	t_{LEB}			250		ns
Current-sense amplifier gain	G_{CS}			11		V/V
SENSE input bias current		V_{SENSE} = 160mV		10	50	nA
PWM Switching						
Switching frequency	f_{SW}		378	420	462	kHz
Dead Time, Dither (DT and SENSE Pin)						
DT pin detection current	I_{DT}		35	40	45	μA
SENSE pin detection current	I_{SENSE}		90	100	110	μA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{EN} = 5V, T_J = -40°C to 125°C (8), typical value is tested at 25°C, unless otherwise noted.

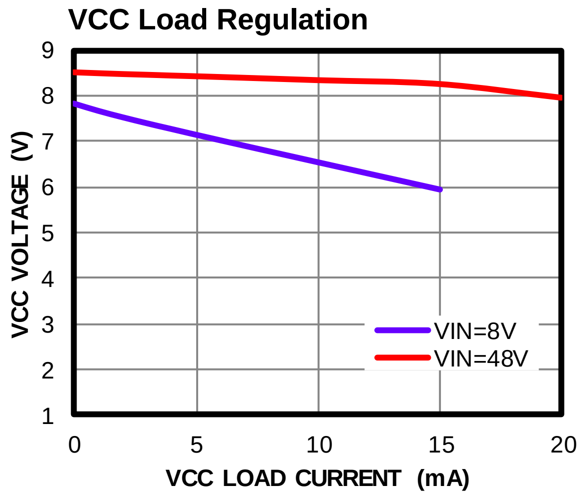
Parameter	Symbol	Condition	Min	Typ	Max	Units
DT pin and SENSE pin detection period	t_{DT}, t_{SENSE}			200		μs
DT pin and SENSE pin detection threshold voltage (9)	V_{DT}, V_{SENSE}	Voltage level 1 range			0.15	V
		Voltage level 2 range	0.25		0.4	V
		Voltage level 3 range	0.55		0.85	V
		Voltage level 4 range	1.1		1.5	V
GATE Driver Signal						
GATE driver impedance (sourcing)	I_{GATE}	I_{GATE} = -20mA		2		Ω
GATE driver impedance (sinking)	I_{GATE}	I_{GATE} = 20mA		1.7		Ω
GATE source current capability (10)		V_{CC} = 8.5V, GATE = 10nF, test gate rising speed		2		A
GATE sink current capability (10)		V_{CC} = 8.5V, GATE = 10nF, test gate falling speed		1.7		A
GATE output high voltage	V_{GATE}		V_{CC} - 0.05			V
GATE output low voltage	V_{GATE}				0.05	V
Minimum GATE on time	t_{ON-MIN}			250		ns
GATE maximum duty cycle	D_{MAX}			70		%
SYNC driver signal						
SYNC driver impedance (sourcing)	I_{SYNC}	I_{GATE} = -20mA		5		Ω
SYNC driver impedance (sinking)	I_{SYNC}	I_{GATE} = 20mA		2		Ω
SYNC source current capability (10)		VCC = 8.5V, SYNC = 10nF, test SYNC rising speed		0.8		A
SYNC sink current capability (10)		VCC = 8.5V, SYNC = 10nF, test SYNC falling speed		1.2		A
SYNC output high voltage	V_{SYNC}		V_{CC} - 0.05			V
SYNC output low voltage	V_{SYNC}				0.05	V
Protection						
Overload protection hiccup on time (10)				4.8		ms
Overload protection hiccup off time (10)				340		ms
Thermal shutdown temperature (10)	T_{SD}			150		°C
Thermal shutdown hysteresis (10)	T_{HYS}			20		°C

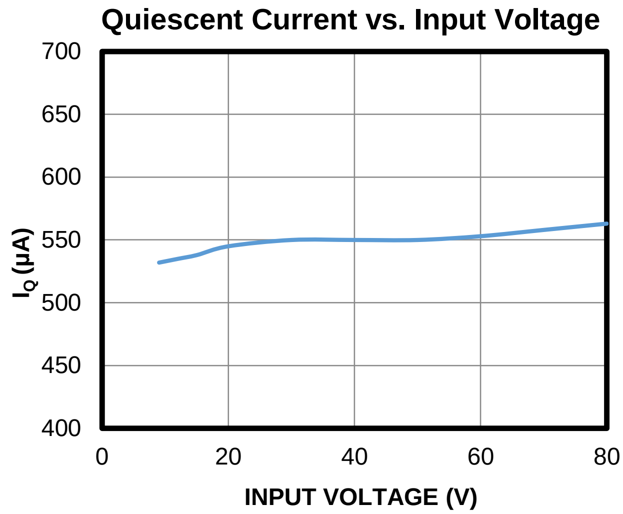
Notes:

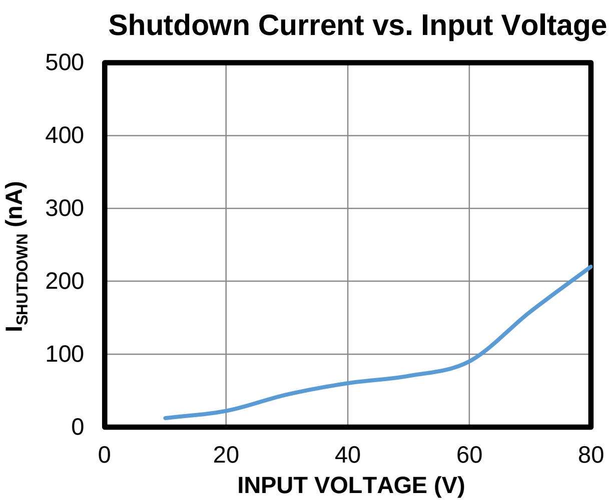
8) Not tested in production. Guaranteed by over-temperature correlation.
9) See Table 1 and Table 2 on page 14 for the different voltage options.
10) Guaranteed by engineering sample characterization.

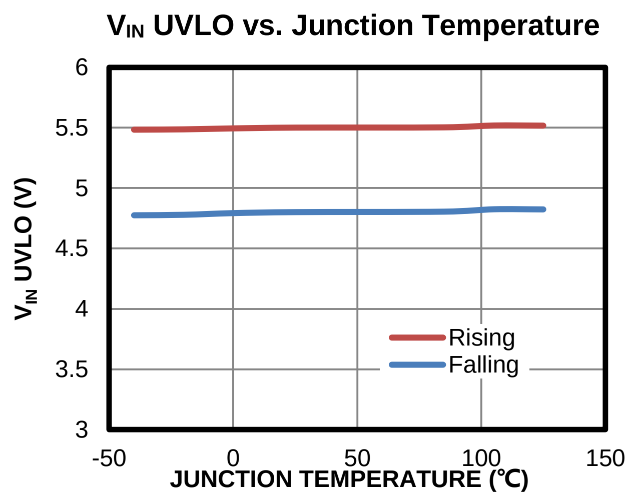
TYPICAL CHARACTERISTICS

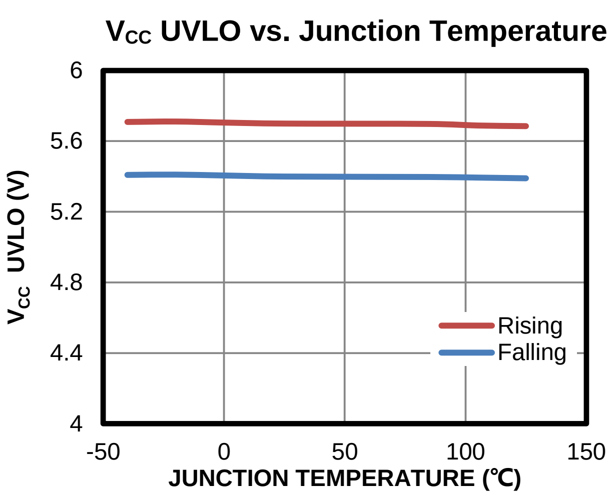
V_{IN} = 48V, V_{EN}= 5V, T_A = 25°C, unless otherwise noted.

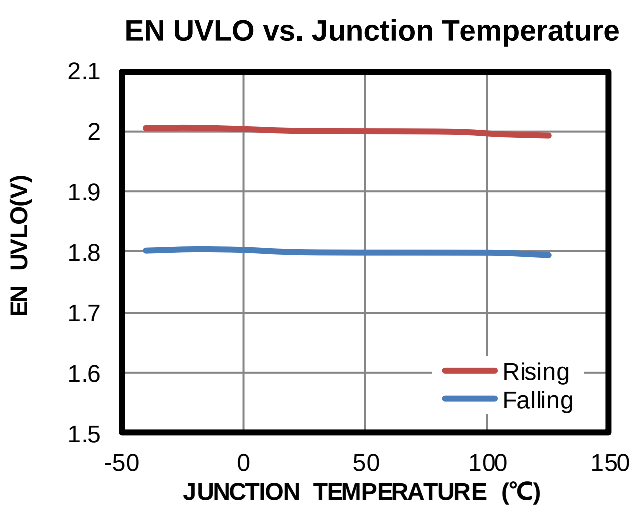






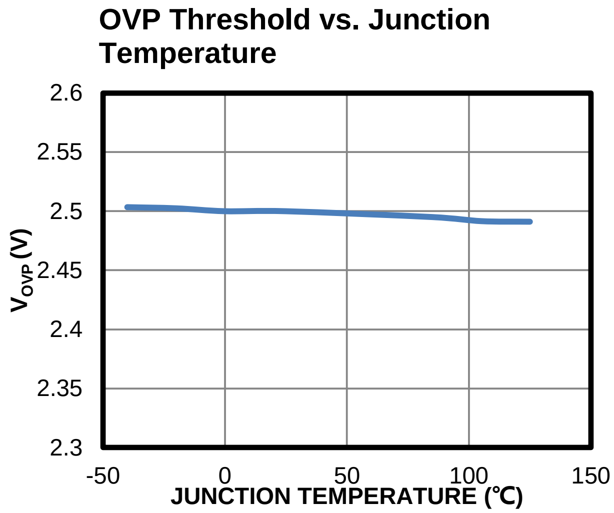


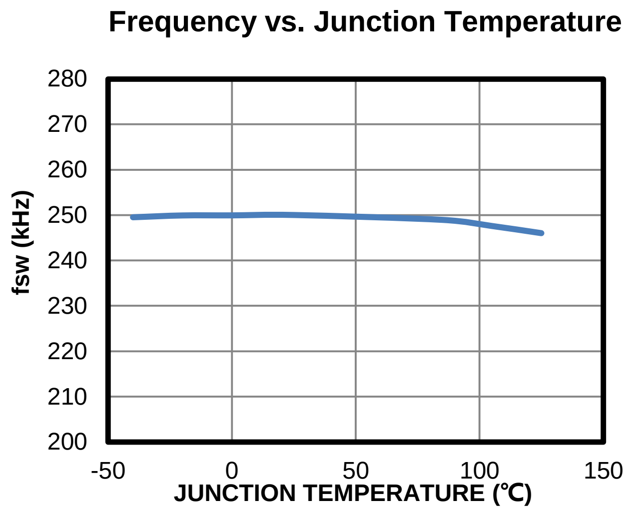


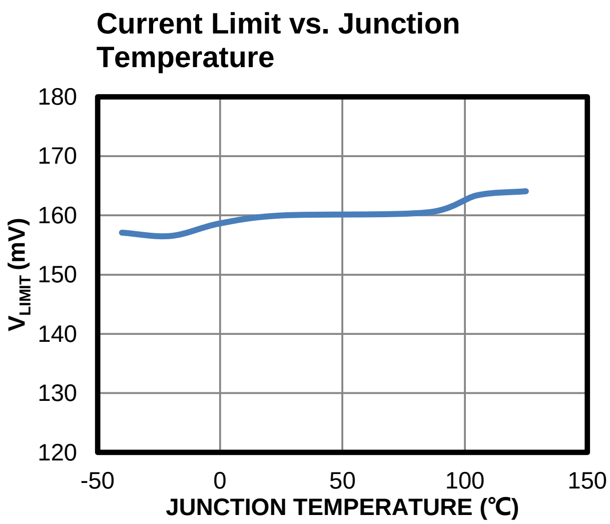


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

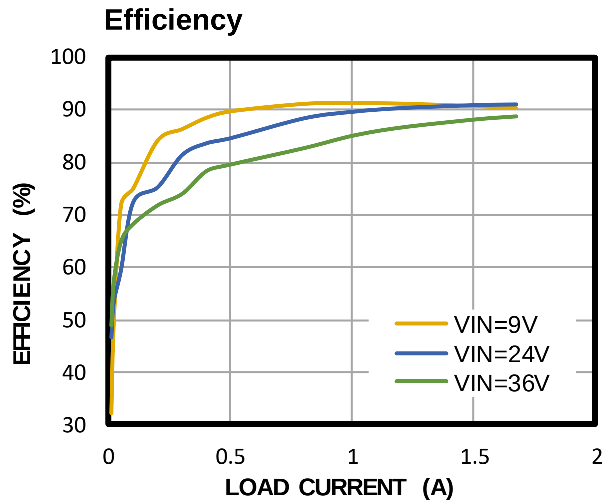


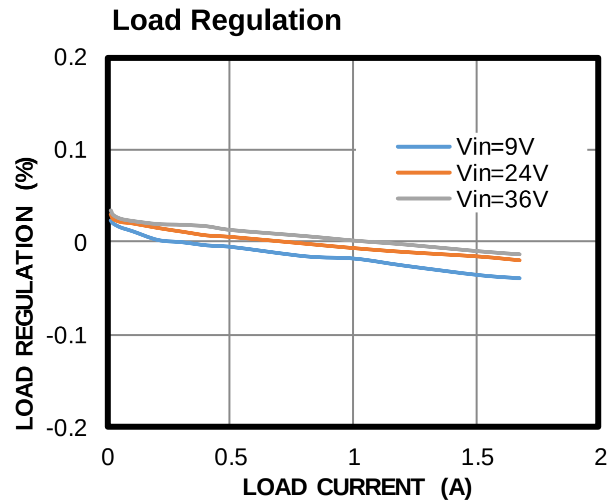


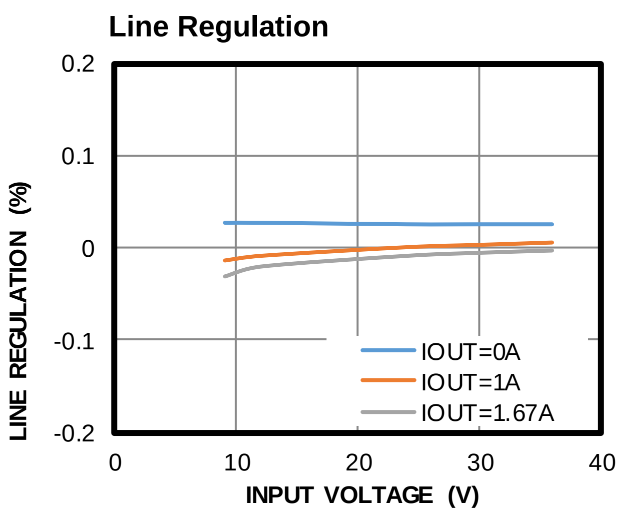


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{EN} = 5V, V_{OUT} = 12V, P_{OUT} = 20W, T_A = 25°C, unless otherwise noted.





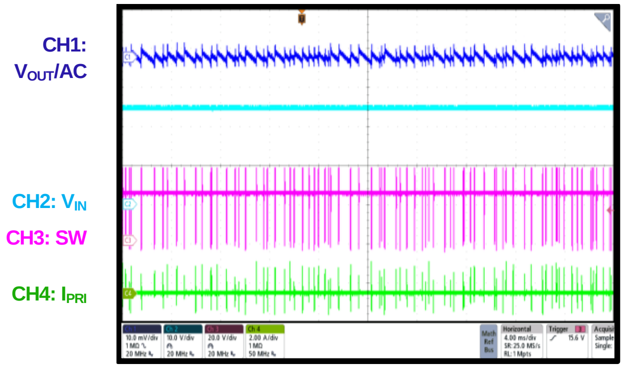


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{EN} = 5V, V_{OUT} = 12V, P_{OUT} = 20W, T_A = 25°C, unless otherwise noted.

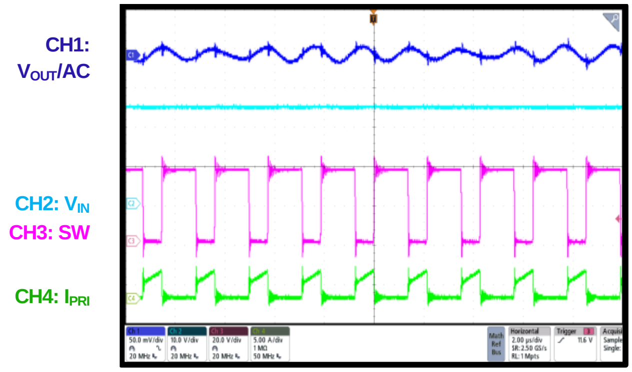
Steady State

I_{OUT} = 0A



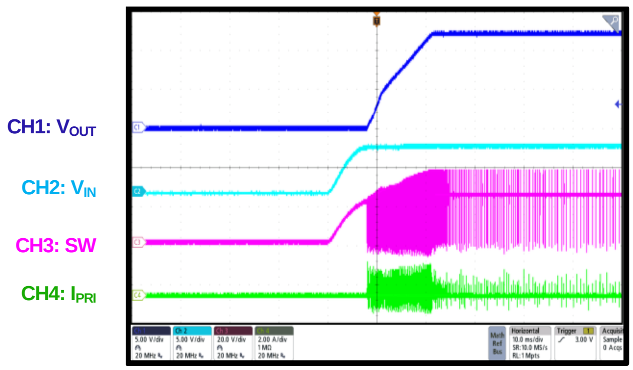
Steady State

I_{OUT} = 1.67A



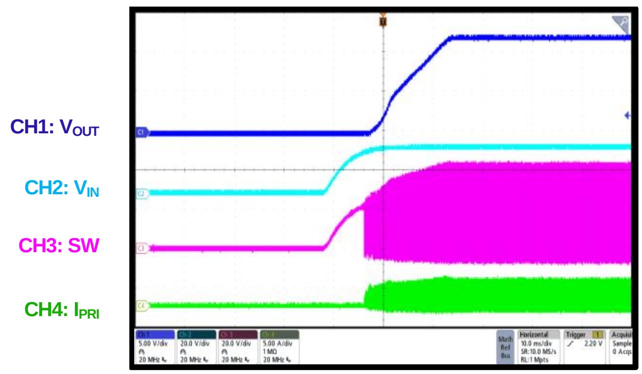
Start-Up through VIN

I_{OUT} = 0A



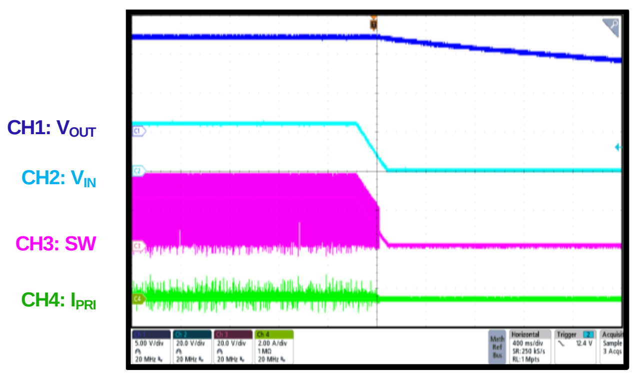
Start-Up through VIN

I_{OUT} = 1.67A



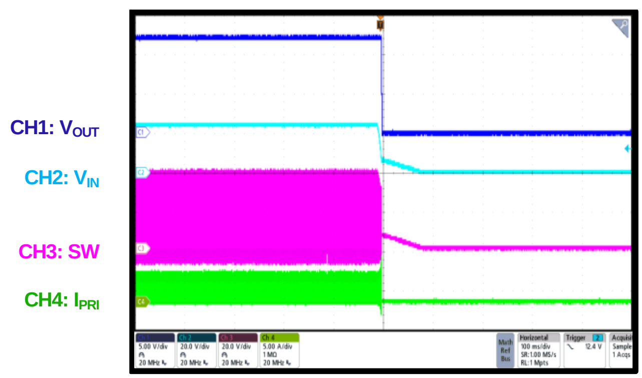
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 1.67A



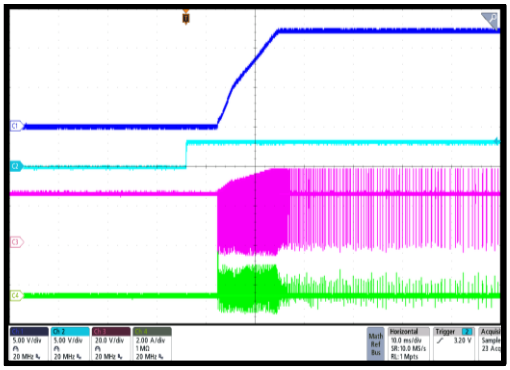
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{EN} = 5V, V_{OUT} = 12V, P_{OUT} = 20W, T_A = 25°C, unless otherwise noted.

Start-Up through EN

I_{OUT} = 0A

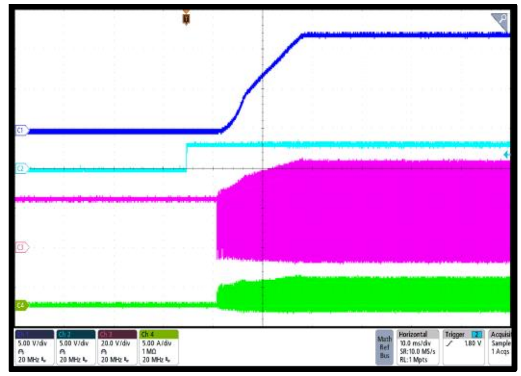
CH1: V_{OUT}
CH2: V_{EN}
CH3: SW
CH4: I_{PRI}



Start-Up through EN

I_{OUT} = 1.67A

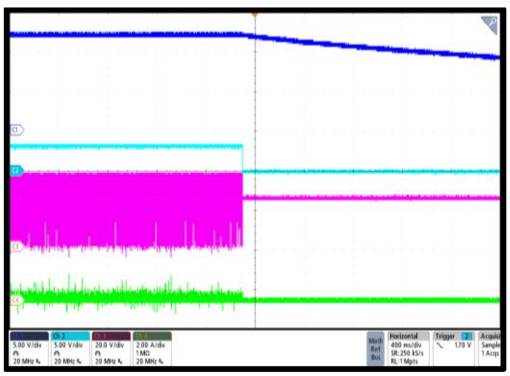
CH1: V_{OUT}
CH2: V_{EN}
CH3: SW
CH4: I_{PRI}



Shutdown through EN

I_{OUT} = 0A

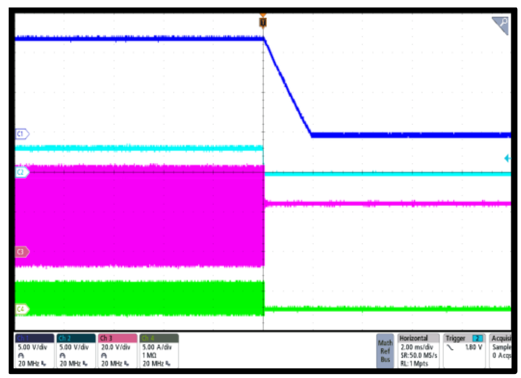
CH1: V_{OUT}
CH2: V_{EN}
CH3: SW
CH4: I_{PRI}



Shutdown through EN

I_{OUT} = 1.67A

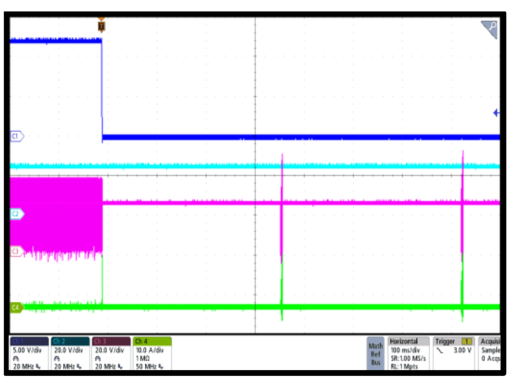
CH1: V_{OUT}
CH2: V_{EN}
CH3: SW
CH4: I_{PRI}



SCP Entry

I_{OUT} = 0A to short

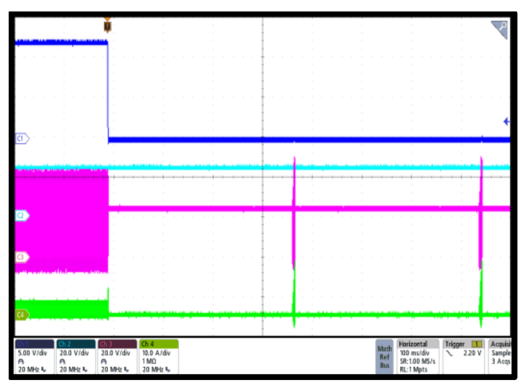
CH1: V_{OUT}
CH2: V_{IN}
CH3: SW
CH4: I_{PRI}



SCP Entry

I_{OUT} = 1.67A to short

CH1: V_{OUT}
CH2: V_{IN}
CH3: SW
CH4: I_{PRI}

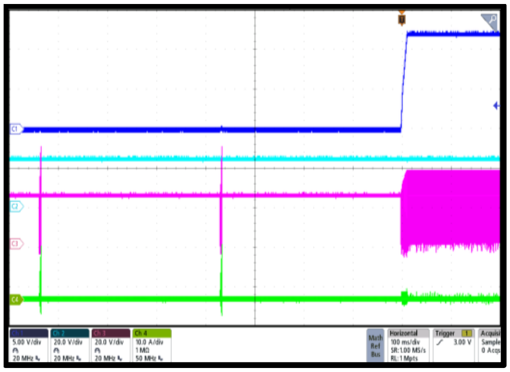


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{EN} = 5V, V_{OUT} = 12V, P_{OUT} = 20W, T_A = 25°C, unless otherwise noted.

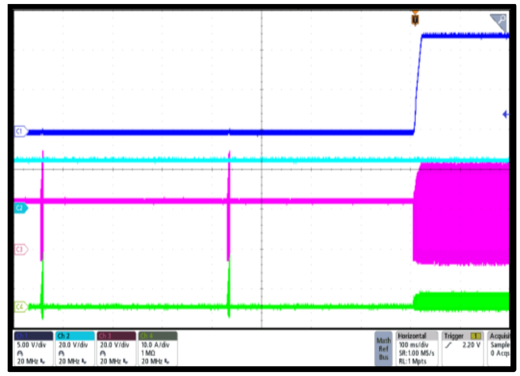
SCP Recovery

I_{OUT} = Short to 0A



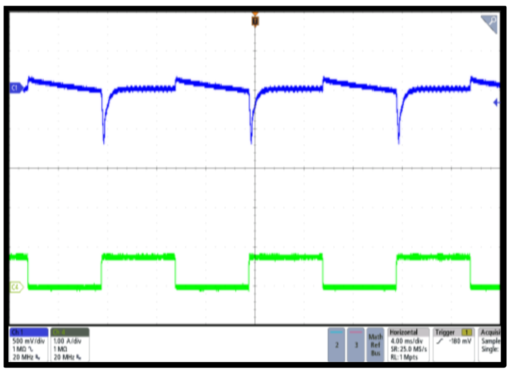
SCP Recovery

I_{OUT} = Short to 1.67A



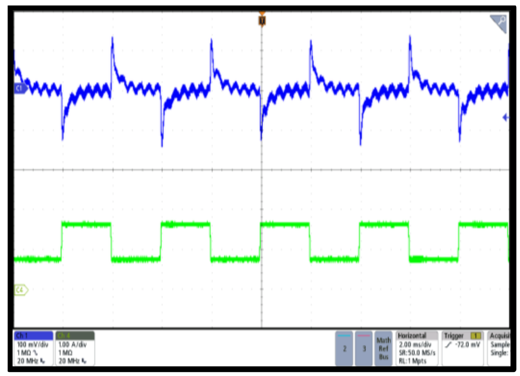
Load Transient

I_{OUT} = 0A to 0.8A, I_{RAMP} = 50mA/µs, $R_{SENSE\text{-}GND}$ = 6.8kΩ



Load Transient

I_{OUT} = 0.8A to 1.67A, I_{RAMP} = 50mA/µs, $R_{SENSE\text{-}GND}$ = 6.8kΩ



FUNCTIONAL BLOCK DIAGRAM

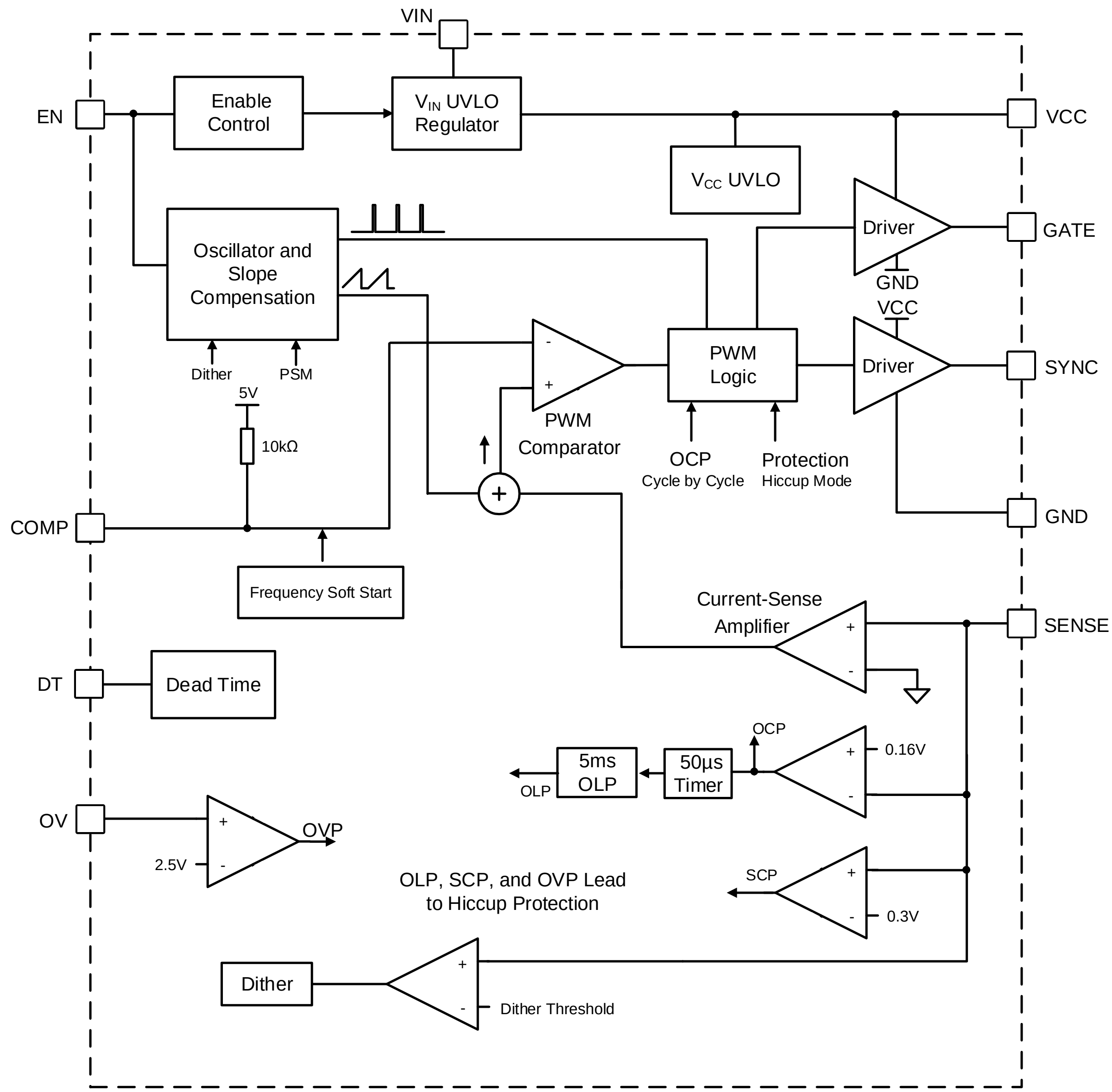


Figure 1: Functional Block Diagram

OPERATION

Start-Up and Power Supply

The MP6005A features an 80V internal start-up circuit. When V_{IN} exceeds 5.5V, the capacitor at VCC is charged through the internal LDO. Generally, V_{CC} is regulated at 8.5V (if V_{IN} is sufficiently high), and the V_{CC} under-voltage lockout (UVLO) threshold is 5.7V. As well as V_{CC} UVLO, the MP6005A has an EN UVLO threshold at 2V. When V_{CC} is charged above its 5.7V UVLO threshold, and the EN pin is high, the MP6005A begins working.

VCC can be powered from the transformer auxiliary winding to save IC power loss after the MP6005A starts switching. The auxiliary power must exceed V_{CC} regulation to override the internal LDO. There is one internal reverse blocking circuit, which means that V_{CC} can exceed V_{IN} if V_{CC} has biased power. V_{CC} should stay below 16V due to its voltage rating.

If V_{IN} is below 8.5V and V_{CC} cannot be regulated to 8.5V, the internal, high-voltage VCC LDO has a 1.5V voltage drop. This means that the MP6005A can work when its input is as low as 8V.

Enable Control

The EN pin enables and disables the MP6005A. When the EN voltage exceeds 1V, the MP6005A starts up some of the internal circuits (micro-power mode). If the EN voltage exceeds the turn-on threshold (2V), the MP6005A enables all functions and starts the GATE/SYNC driver signal. The GATE/SYNC signal can be disabled when the EN voltage drops to about 1.8V, but micro-power mode is disabled only after the EN voltage falls below 0.4V. After shutdown, the MP6005A sinks a maximum 1µA of current from the input power.

The EN pin can configure the V_{IN} start-up voltage through a resistor divider. The maximum recommended voltage on the EN pin is 6.5V. If the resistor divider voltage on EN rises above 6.5V, the resistor divider should be carefully considered to limit the current on the EN pin. One internal Zener diode on EN clamps the EN voltage when the resistor divider voltage exceeds 6.5V. This ensures that the clamped current flowing into EN is below 0.4mA with an external pull-up resistor.

Pulse-Width Modulation (PWM) Operation

The MP6005A can be set to flyback and forward topology. In flyback topology, the external N-channel MOSFET turns on at the beginning of each cycle and forces the current in the transformer to increase. The current through the MOSFET can be sensed. When the sum of the SENSE current and slope compensation signal rise above the voltage set by the COMP pin, the external MOSFET turns off. The transformer current then transmits energy from the primary-side winding to the secondary-side winding, and charges the output capacitor through the Schottky diode.

The transformer's primary-side current is controlled by the COMP voltage (V_{COMP}). V_{COMP} is then controlled by the output feedback voltage through an external TL431 regulator and the optocoupler. Therefore, the output voltage controls the transformer current to satisfy the load. In forward topology, the energy is transferred from the primary-side to secondary-side winding while the primary-side N-channel MOSFET is on. The primary-side peak current is also controlled by V_{COMP}.

Voltage Control

The output voltage (V_{OUT}) feedback signal from the optocoupler is amplified by secondary circuitry, then directly fed back the signal to COMP pin.

Under light-load conditions, the MP6005A maintains a fixed frequency. The peak current can drop when the COMP voltage decreases. This current drop can trigger the power-save mode (PSM) threshold.

Dead Time Setting

The DT pin can configure the dead time between the GATE and SYNC pins. Table 1 lists the available configurations. The resistor on the DT pin must be below 33kΩ.

After the MP6005A is enabled, there is a 500µs period before the device starts switching. The dead time and dither settings can be detected by the MP6005A during this period.

Table 1: Dead Time Configurations

DT-to-GND Resistor (kΩ) (1%)			Dead Time (ns)
Min	Typ	Max	
0	0	3.3	100
7.32	7.5	8.2	150
16	16.9	18.7	200
32.4	32.4	33	300

The DT pin detection current lasts for about 200µs. Generally, it is sufficient to connect one resistor from DT to GND. In noisy environments, a capacitor can be placed between DT and GND to provide filtering. It is recommended for this capacitor to be below 100pF so that the DT pin voltage can rise to a steady state before the MP6005A detects the DT pin voltage. Do not float the DT pin.

Frequency Dithering

The MP6005A integrates a frequency dithering circuit to minimize EMI emissions. During steady state, the frequency is fixed internally. A frequency dithering circuit can be added to the configured frequency with 1.5kHz modulation. Frequency dithering can be configured to ±12.5kHz, ±25kHz, or ±37.5kHz by connecting a resistor from the SENSE pin to GND (see Table 2).

Table 2: Dithering Configurations

SENSE-to-GND Resistor (kΩ) (1%)			Dither Range (kHz)
Min	Typ	Max	
0	0	1.3	0
3	3.3	3.6	±12.5
6.2	6.8	7.5	±25
12.7	12.7	13	±37.5

The SENSE pin detection current lasts for about 200µs after start-up. Generally, it is sufficient to connect one resistor to the SENSE pin. In noisy environments, a capacitor can be placed between SENSE and GND to provide filtering.

Current Sense and Over-Current Protection (OCP)

The MP6005A is a peak current mode flyback/forward controller. The current through the external MOSFET can be sensed through a current-sense resistor that is connected in series with the MOSFET's source. The sensed voltage on the SENSE pin is then amplified and fed to the high-speed current comparator for current mode control. The current comparator takes this sensed voltage (plus slope compensation) as one of its inputs, then compares this value with V_{COMP}. When the amplified current signal exceeds V_{COMP}, the comparator outputs low, and the power MOSFET turns off.

If the voltage on the SENSE pin exceeds the current-limit threshold (about 160mV), the MP6005A turns off the GATE output for the cycle. The current is sensed again after the internal oscillator starts the next cycle. The MP6005A limits the MOSFET's current cycle by cycle.

Over-Voltage Protection (OVP)

The MP6005A provides over-voltage protection (OVP). If the voltage on the OV pin exceeds 2.5V, the MP6005A shuts off the gate driving signal and enters hiccup mode immediately. The MP6005A restarts after 340ms and resumes normal operation if the fault is removed. Connect the OV pin to GND if OVP is not required.

To avoid mistriggering due to the oscillation of the leakage inductance and the parasitic capacitance, there is an OVP blanking time.

Overload Protection (OLP)

The MP6005A limits the peak current cycle by cycle during over-current (OC) conditions. If the load continues increasing after triggering OCP, the output voltage drops, and the peak current triggers OCP every cycle.

The MP6005A sets the overload detection by continuously monitoring the SENSE pin voltage. Once internal soft start finishes, overload protection (OLP) is enabled. If an OCP signal is detected and lasts longer than 5ms, the MP6005A turns off the GATE driver. After a 340ms delay, the MP6005A restarts with a new start-up cycle.

During OLP, a 50µs one-shot timer is activated. This timer also remains active for 50µs after one OCP pulse. This means that if there is one OCP pulse in a 50µs period, the MP6005A registers OCP. If the OC condition is removed within 4.95ms, the MP6005A resumes normal operation.

Short-Circuit Protection (SCP)

When the output is shorted to the ground, the part triggers over-current protection (OCP). During OCP, the current is limited cycle by cycle, and overload protection (OLP) may be triggered as a result.

If the peak current cannot be limited by the 160mV SENSE voltage in every cycle due to minimum gate on time, the current may run out of control, and the transformer may saturate. If the monitored SENSE voltage reaches 300mV, the part turns off GATE and immediately runs in hiccup mode with a 340ms off time.

If the short circuit is removed, the output voltage recovers after the next restart cycle with a 340ms delay.

Soft Start

The MP6005A provides soft start by charging an internal capacitor with a current source. During soft start, the SS signal controls COMP and ramps up slowly. The soft-start capacitor is discharged completely in the event of a commanded shutdown, thermal shutdown, or protection condition.

To avoid triggering short-circuit protection (SCP) when the MP6005A starts up with a large output capacitor, the MP6005A includes a frequency soft-start function. The switching frequency is controlled by the COMP voltage (V_{COMP}). The frequency is about 100kHz when V_{COMP} = 1.5V, and it linearly increases to 420kHz when V_{COMP} = 2.5V. Generally, it takes about 20ms for V_{COMP} to ramp up from 1.5V to 3.5V. After soft start finishes, the soft start function is disabled.

Minimum On Time

The transformer parasitic capacitance and gate driver signal induce a current spike on the sense resistor when the power switch turns on. The MP6005A includes a 250ns leading edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current-sense comparator is disabled, and the gate driver cannot switch off.

Gate Driver

The MP6005A integrates one high-current gate driver for the primary-side N-channel MOSFET. The high-current gate driver provides a strong driving capability and benefits MOSFET selection. If Q_G (the external MOFET's total gate charge) is low, then the switching speed should remain low as well. It is recommended to use a series resistance of 5Ω to reduce EMI.

The MP6005A also integrates one SYNC driver pin. The SYNC pin turns the synchronous switch off when SYNC is high, then turns the synchronous switch on when SYNC is low. Figure 2 shows the phase and dead time relationship between GATE and SYNC.

If the MP6005A turns off due to under-voltage lockout (UVLO) or a protection, both the GATE and SYNC pins stay at a low voltage.

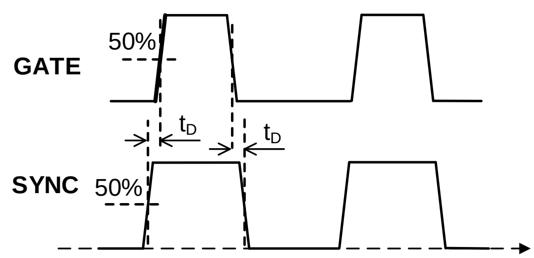


Figure 2: GATE and SYNC Driver

Over-Temperature Protection (OTP)

Thermal shutdown is implemented to prevent the chip from thermal runaway. When the silicon die temperature exceeds its upper threshold, the MP6005A shuts down the whole chip. When the temperature drops below the lower threshold, thermal shutdown is removed, and the chip is enabled again with a new start cycle.

APPLICATION INFORMATION

Output Voltage Setting

The output voltage is set by an external TL431 regulator. If the TL431's reference voltage is 2.5V, and expected output voltage is 12V, then the upper and lower resistor divider ratio should be 3.8. Then TL431 generates an amplified signal that controls the MP6005A's COMP pin through an optocoupler, such as the PC357. COMP controls the current, which regulates V_{OUT} using a feedback signal.

Dead Time Setting

The DT pin can configure the dead time between the GATE and SYNC pins (see Table 1 on page 14).

Enable Control Setting

The EN pin can configure the V_{IN} start-up voltage through a resistor divider (see Figure 3).

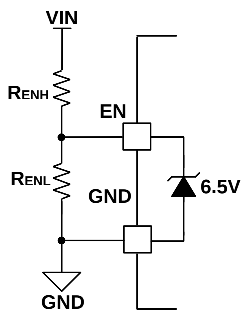


Figure 3: Configuring the UVLO Threshold through EN

The maximum recommended voltage on the EN pin is 6.5V. If the resistor divider voltage on the EN pin exceeds 6.5V, the R_{ENH} resistance should be high enough to limit the current flowing into the EN pin. An internal Zener diode on the EN pin clamps the EN voltage when the divider voltage exceeds 6.5V. Ensure that the Zener diode clamps the current flowing into EN below 0.4mA.

VCC Power Supply Setting

The VCC voltage is regulated by the internal LDO from V_{IN}. Generally, V_{CC} is regulated at 8.5V. It is recommended to place a decoupling capacitor between VCC and GND.

In flyback mode, the VCC capacitor is recommend to be 1µF at minimum. VCC can also be powered from transformer auxiliary winding to save high-voltage LDO power loss (see Figure 4).

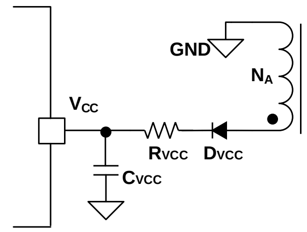


Figure 4: Flyback Mode V_{CC} from N_A Winding

In flyback mode, the auxiliary winding supply voltage (V_{CC}) can be calculated with Equation (1):

$$V_{CC} = \frac{N_A}{N_S} \times (V_{OUT} + V_{DOF}) - V_{DVCCF} \quad (1)$$

Where V_{DVCCF} is the diode (D_{VCC}) voltage drop from auxiliary winding.

In forward mode, the VCC capacitor is recommend to be at minimum 4.7µF. V_{CC} can also be powered from transformer auxiliary winding (see Figure 5).

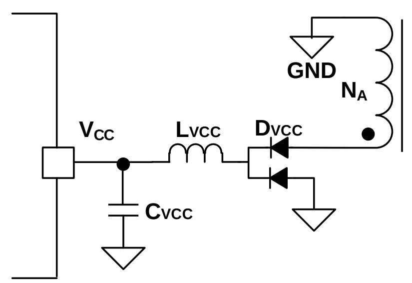


Figure 5: Forward Mode V_{CC} from N_A Winding

In forward mode, the auxiliary winding supply voltage (V_{CC}) can be estimated with Equation (2):

$$V_{CC} = \frac{N_A}{N_S} \times V_{OUT} \quad (2)$$

V_{CC} should be below 16V.

Frequency Dithering Setting

The SENSE pin can set the frequency dithering function. Once enabled, the MP6005A outputs a 100µA current to the SENSE pin to detect the SENSE resistance. Based on the resistance, the MP6005A determines the frequency dithering value (see Table 2 on page 14).

Current-Sense Resistor Setting

The MP6005A is a peak current mode flyback/forward controller. The current through the external MOSFET can be sensed through a current-sense resistor. If the voltage sensed on the SENSE pin exceeds the current-limit threshold voltage (about 160mV), the MP6005A turns off the GATE output for that cycle.

To avoid reaching the current limit, the voltage across the current-sense resistor (R_{SENSE}) should be below 80% of the current limit voltage (about 160mV). R_{SENSE} can be calculated with Equation (3):

$$R_{SENSE} = \frac{0.8 \times 160_{mV}}{I_{PEAK}} \tag{3}$$

Where I_{PEAK} is the primary-side peak current.

Selecting the Power MOSFET

The MP6005A is capable of driving a wide variety of N-channel power MOSFETS. The critical parameters for selecting a MOSFET are the maximum drain-to-source voltage ($V_{DS(MAX)}$), maximum current ($I_{D(MAX)}$), on resistance ($R_{DS(ON)}$), total gate charge (Q_G), and the turn-on threshold (V_{TH}).

In flyback mode, the off-state voltage (V_{MOSFET}) across the MOSFET can be calculated with Equation (4):

$$V_{MOSFET} = V_{IN} + N \times V_{OUT} \tag{4}$$

Where N is the transformer primary winding to output winding ratio.

Consider the voltage spike when the power MOSFET turns off. $V_{DS(MAX)}$ should be greater than 1.5 times V_{MOSFET}.

In forward mode, V_{MOSFET} can be estimated with Equation (5):

$$V_{MOSFET} = \frac{D \times V_{IN}}{1 - D} + V_{IN} \tag{5}$$

Where D is the duty cycle. The maximum duty cycle is typically limited at 70%.

The current through the power MOSFET is at its maximum when the input voltage is at its minimum and the output power is at its maximum. The current rating of the MOSFET should be greater than 1.5 x I_{RMS}.

The on resistance of the MOSFET determines the conduction loss. To reduce conduction loss, the on resistance should be as low as possible.

Q_G is vital for MOSFET selection since it determines the commutation time. A high Q_G leads to high switching loss, while a low Q_G may cause fast turn-on/off speeds. The turn-on/off speeds determine the spike and kick.

Consider the turn-on threshold voltage (V_{TH}). GATE is powered by VCC, so V_{TH} must be below V_{CC}.

Selecting the Transformer for Flyback Mode

In flyback mode, a transformer determines the duty cycle, peak current, efficiency, MOSFET, and output diode rating. A good transformer should consider the winding ratio, primary-side inductance, saturation current, leakage inductance, current rating, and core selection.

The transformer winding ratio determines the duty cycle (D). Calculate D with Equation (6):

$$D = \frac{N \times V_{OUT}}{N \times V_{OUT} + V_{IN}} \tag{6}$$

Where N is the transformer primary winding to output winding ratio. Typically, a duty cycle of about 45% is recommended for most applications.

The primary-side inductance affects the input current ripple ratio factor. A higher inductance results in a physically large transformer and higher costs. A lower inductance results in a high switching peak current and RMS current, which reduces efficiency. Choose a primary-side inductance that makes the current ripple ratio factor about 30% to 50%. Estimate the primary-side inductance with Equation (7):

$$L_P = \frac{V_{IN} \times D^2}{2 \times n \times I_{IN} \times f_{SW}} \tag{7}$$

Where n is the current ripple ratio, I_{IN} is the input current, and L_P is the primary inductance. Calculate L_P based on the minimum input voltage condition.

The transformer should have a high saturation current to support the switching peak current.

Otherwise, the transformer inductance decreases sharply. The SENSE resistor can limit the switching peak current. The energy stored in the leakage inductance cannot couple to the secondary side, which may a high spike when the MOSFET turns off. This reduces efficiency and increases MOSFET stress. Normally, the transformer leakage inductance can be controlled below 2% of the transformer inductance.

The current rating uses the maximum RMS current (I_{RMS}), which allows current to flow through each winding. The current density should be controlled, as an unregulated current can cause a high resistive power loss.

Selecting the RCD Snubber for Flyback Mode

The transformer leakage inductance causes spikes and excessive ringing on the MOSFET drain voltage waveform, and the RCD snubber circuit limits the MOSFET voltage spike (see Figure 6).

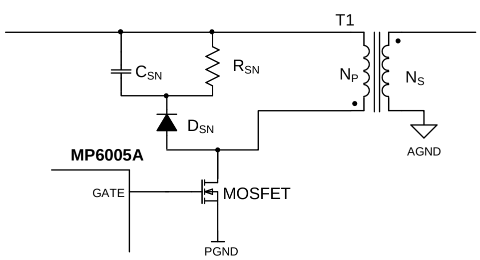


Figure 6: RCD Snubber

The power dissipation (P_{SN}) in the snubber circuit can be estimated with Equation (8):

$$P_{SN} = \frac{1}{2} \times L_K \times I_{PEAK}{}^2 \times f_{SW} \quad (8)$$

Where L_K is the leakage inductance and I_{PEAK} is the peak switching current. Since R_{SN} consumes the leakage inductance power loss, R_{SN} can be calculated with Equation (9):

$$R_{SN} = \frac{V_{SN}{}^2}{P_{SN}} \quad (9)$$

Where V_{SN} is the expected snubber voltage on C_{SN}.

Calculate the voltage ripple (ΔV_{SN}) on the snubber due to the snubber capacitor (C_{SN}) with Equation (10):

$$\Delta V_{SN} = \frac{V_{SN}}{R_{SN} \times C_{SN} \times f_{SW}} \quad (10)$$

A 15% ripple is allowed.

Selecting the Output Diode for Flyback Mode

The flyback output rectifier diode supplies current to the output capacitor when the primary-side MOSFET is off. Use a Schottky diode to reduce losses from the diode forward voltage and recovery time. The diode should be rated for a reverse voltage 1.5 times greater than V_{DIODE}. V_{DIODE} can be calculated with Equation (11):

$$V_{DIODE} = \frac{V_{IN}}{N} + V_{OUT} \quad (11)$$

Where N is the transformer primary winding to output winding ratio.

The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the output winding peak current. It is recommended to use an RC snubber circuit for the output diode.

Selecting the Transformer for Forward Mode

In forward mode, the transformer transfers energy to the output when the power MOSFET turns on. The key parameters for this transformer are the winding ratio, primary winding turns, current rating, and core selection.

The transformer winding ratio determines the duty cycle (D). D can be estimated with Equation (12):

$$D = \frac{V_{OUT} \times N}{V_{IN}} \quad (12)$$

Where N is the transformer primary winding to output winding ratio. A duty cycle of about 45% is recommended for most applications.

When the power MOSFET turns on, the transformer transfers energy to the output, while V_{IN} generates a primary-side inductance current in the transformer. There must be enough primary winding to prevent the transformer from saturating.

The peak exciting current can be calculated with Equation (13):

$$I_{EXC} = \frac{V_{OUT} \times N}{2 \times L_P \times f_{SW}} \quad (13)$$

Where I_{EXC} is the primary-side inductance peak current, and L_P is the primary inductance. Use I_{EXC} to calculate the primary winding. Certain margins are required for extreme conditions, such as load transient and over-current protection (OCP).

The current rating counts on the maximum RMS current, which flows through each winding. The current density should be controlled. An unregulated current density can cause a high resistive power loss.

Selecting the SYNC MOSFET for Forward Mode

The MP6005A supports active-clamp forward mode. The active clamp P-channel MOSFET must have the same maximum voltage as the main switch power MOSFET. The P-channel MOSFET's maximum current should exceed the primary-side inductance peak current and RMS current.

Selecting the Output MOSFET for Forward Mode

The forward mode output uses two diodes to conduct the current. If higher efficiency is required, the diodes can be replaced with MOSFETs (Q_F and Q_R) (see Figure 7).

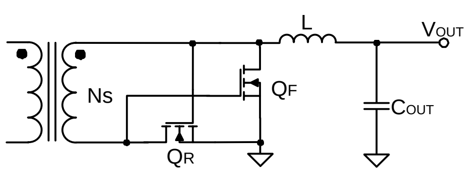


Figure 7: Forward Mode Output MOSFET

The MOSFET voltage rating should exceed its maximum V_{DS} voltage. The Q_R maximum V_{DS} voltage (V_R) can be calculated with Equation (14):

$$V_R = \frac{D \times V_{IN}}{N \times (1 - D)} \quad (14)$$

The Q_F maximum V_{DS} voltage (V_F) can be estimated with Equation (15):

$$V_F = \frac{V_{IN}}{N} \quad (15)$$

Where N is the transformer primary winding to output winding ratio, and D is the primary MOSFET duty cycle. Generally, a margin is required.

The MOSFET current rating should exceed its maximum RMS current and peak current, The Q_R RMS current (I_R) can be estimated with Equation (16):

$$I_R = I_{OUT} \times \sqrt{D} \times \sqrt{1 + \frac{1}{3} \times (\frac{I_{PP}}{I_{OUT}})^2} \quad (16)$$

Where I_{PP} is the inductor's peak to peak current. The Q_F RMS current (I_F) can be calculated with Equation (17):

$$I_F = I_{OUT} \times \sqrt{1 - D} \times \sqrt{1 + \frac{1}{3} \times (\frac{I_{PP}}{I_{OUT}})^2} \quad (17)$$

The Q_R MOSFET's gate driving voltage is equal to V_F, and the Q_F MOSFET's gate driving voltage is equal to V_R. If the driving voltage exceeds the MOSFETs' maximum gate voltage, a clamp circuit is required.

The MOSFET's on resistance determines the conduction loss, while Q_G determines the driver circuit loss. Both the MOSFET's on resistance and Q_G should be low enough to obtain higher efficiency and a lower rising temperature.

Selecting the Output Inductor for Forward Mode

The forward mode output inductor must supply constant current to the output load while the main power MOSFET turns on. A larger-value inductor results in less ripple current and a lower output ripple voltage. However, a larger-value inductor has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% to 50% of the maximum output current. The inductance value (L) can be calculated with Equation (18):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT} \times N}{V_{IN}}) \quad (18)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_{SW} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current.

Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low-ESR capacitor is required to keep the noise near the IC at a minimum. Ceramic capacitors are recommended, but tantalum or low-ESR electrolytic capacitors are sufficient. For ceramic capacitors, the capacitance dominates the input voltage ripple at the switching frequency.

In flyback mode, the input ripple can be estimated with Equation (19):

$$\Delta V_{IN} = I_{IN} \times \frac{V_{IN}}{f_{SW} \times C_{IN} \times (N \times V_{OUT} + V_{IN})} \quad (19)$$

Where ΔV_{IN} is the input voltage ripple, I_{IN} is the input current, and C_{IN} is the input capacitor.

In forward mode, the input voltage ripple can be calculated with Equation (20):

$$\Delta V_{IN} = \frac{I_{IN}}{f_{SW} \times C_{IN}} \times (1 - \frac{V_{OUT} \times N}{V_{IN}}) \quad (20)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. For the best results, use ceramic capacitors or low-ESR capacitors to minimize the output voltage ripple. For ceramic capacitors, the capacitance dominates the output ripple at the switching frequency.

In flyback mode, the output ripple can be estimated with Equation (21):

$$\Delta V_{OUT} = \frac{N \times V_{OUT}}{(V_{IN} + N \times V_{OUT}) \times f_{SW}} \times \frac{I_{OUT}}{C_{OUT}} \quad (21)$$

If the voltage ripple is too high, a π filter is required. Choose the inductor to be between 0.1μH and 0.47μH for a good output voltage ripple and system stability.

In forward mode, the output voltage ripple can be calculated with Equation (22):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times {f_{SW}}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT} \times N}{V_{IN}}) \quad (22)$$

Design Example

Table 3 shows a flyback design example that follows the application guidelines for the specifications below.

Table 3: Flyback Mode Design Example

V_{IN}	9V to 36V
V_{OUT}	12V
I_{OUT}	1.67A

Figure 11 on page 22 shows the detailed application schematic. The Typical Performance Characteristics section on page 8 shows the typical performance and circuit waveforms. For more device applications, refer to related the evaluation board datasheet.

PCB Layout Guidelines

Efficient layout of the high-frequency switching power supply is critical for stable operation. Poor layout may result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, follow the guidelines below.

Flyback Mode

1. Keep the input loop between the input capacitor, transformer, Q1, sense resistor, and GND plane as short as possible for minimal noise and ringing.
2. Keep the output loop between the rectifier diode, output capacitor, and transformer as short as possible.
3. The clamp loop circuit between D2, C4, and the transformer should be as small as possible.
4. The VCC capacitor must be placed close to the VCC pin for decoupling.
5. The COMP feedback trace should be routed far away from noise sources, such as SW.
6. Use a single-point connection between power GND and signal GND.

Figure 8 shows the recommended flyback layout.

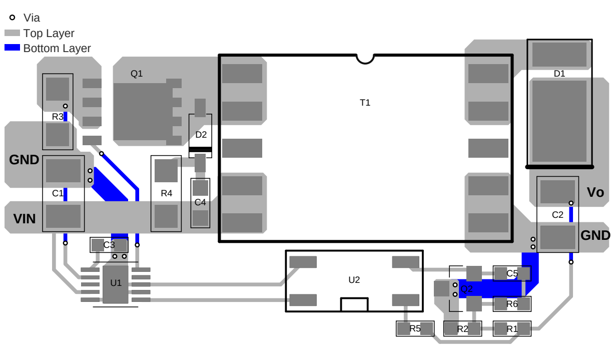


Figure 8: Recommended Flyback PCB Layout

For more details, refer to the related evaluation board datasheet.

Forward Mode

1. Keep the input loop between the input capacitor, transformer, Q1, sense resistor, and GND plane as short as possible for minimal noise and ringing.
2. Keep the active-clamp loop between the input capacitor, transformer, C4, and Q2 as short as possible for minimal noise and ringing.
3. Keep the output high-frequency current loop between the transformers, D1, and D2 as short as possible.
4. The VCC capacitor must be placed close to the VCC pin for decoupling.
5. The COMP feedback trace should be routed away from noise sources, such as SW.
6. Use a single-point connection between power GND and signal GND.

Figure 9 shows the recommended forward layout.

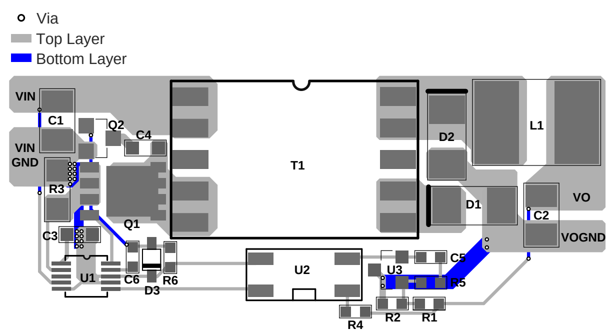


Figure 9: Recommended Forward PCB Layout

Figure 10 shows the schematic for forward mode.

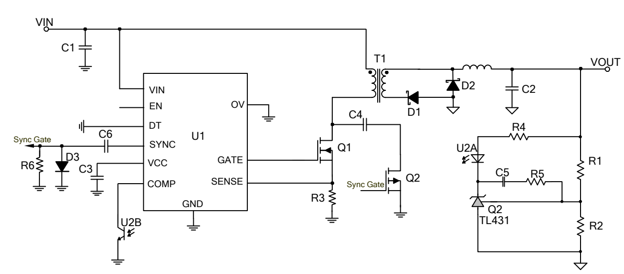


Figure 10: Forward Layout Guide Schematic

For more details, refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUIT

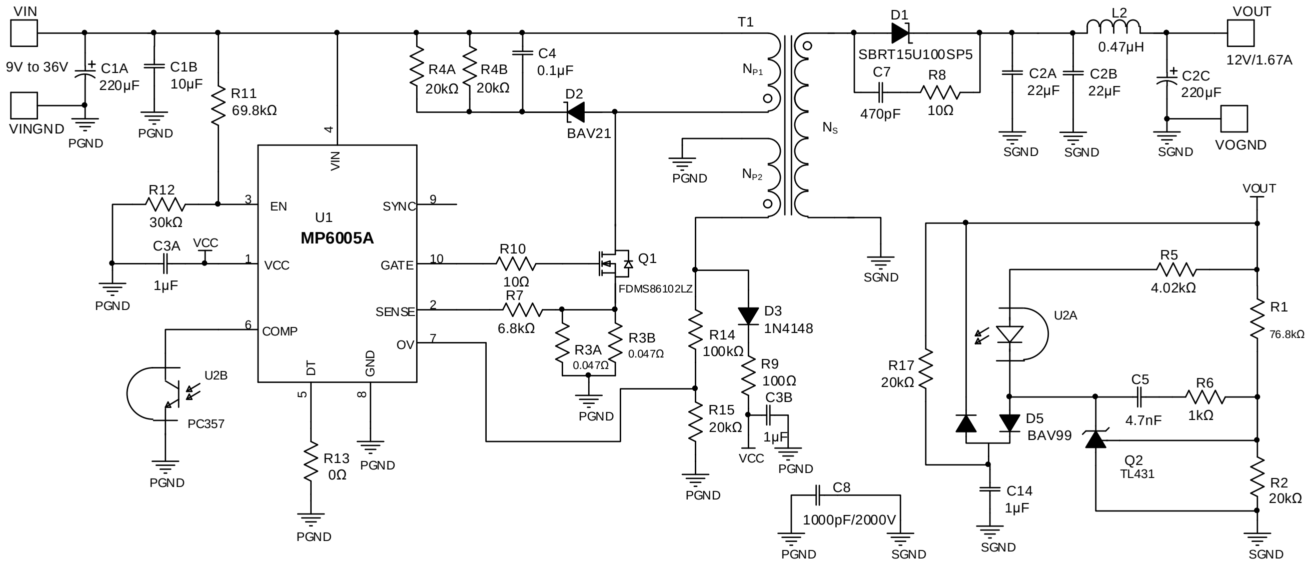
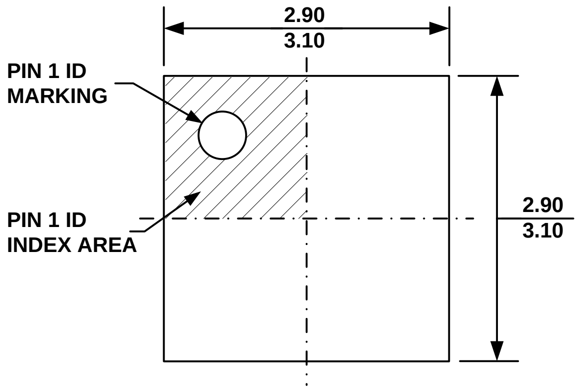


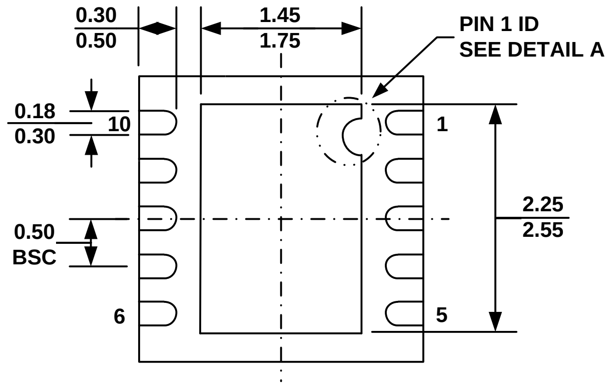
Figure 11: Typical Flyback Application Circuit (V_{IN} = 9V to 36V, V_{OUT} = 12V, I_{OUT} = 1.67A)

PACKAGE INFORMATION

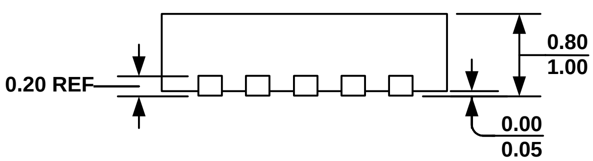
QFN-10 (3mmx3mm)



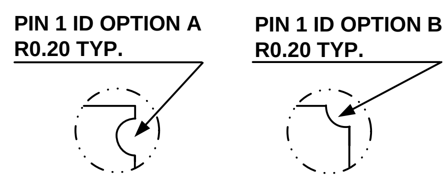
TOP VIEW



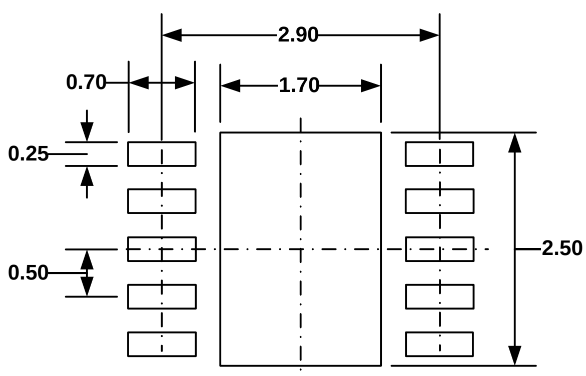
BOTTOM VIEW



SIDE VIEW



DETAIL A

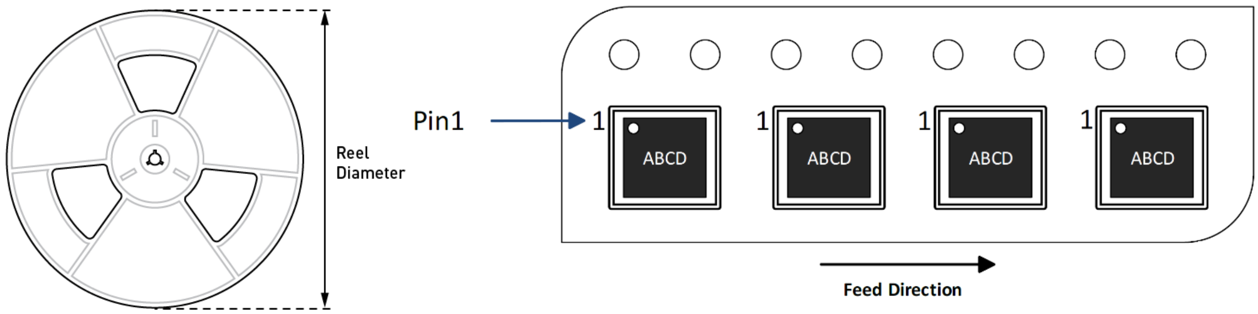


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6005AGQ-Z	QFN-10 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	07/16/2021	Initial Release	-