10A Input, 9V/3A or 12V/2A Output BOOST Converter with True-Shutoff

DESCRIPTION

ETA1188 is a high power, high-efficiency, synchronous boost that can output up to 27W of power. With integrated high power MOSEFTs, it comfortably delivers 9V/3A output from a wide range of input voltage. It also integrates an output short protection MOSEFT on chip to provide over current protection and true-shutoff function. With its tiny package of QFN3x3-20, it sports a small footprint which makes it an ideal all-in-one solution for high power boost applications.

The ETA1188 features a programmable output current limit, configurable by a resistor connected from ISET pin to GND. Output voltage can also be programmed by a resistor divider from VOUT to FB to GND. Furthermore, besides external configuration, ETA1188can also be communicated through an I2C protocol to configure the current limit and output voltage internally, making it suitable for Power Delivery or Quick Charge applications.

The ETA1188 is available in QFN33-20FC package.

FEATURES

- High Power: 9V/3A
- High efficiency: Up to 93% at 9V/3A
- Wide Input Supply Range, 2.7V to 12V
- Wide Output Voltage Range, 3.6V to 12V
- True Shutoff with 20mΩ n-Channel Pass Device
- Low Shutdown Current:2μA
- High Efficiency at Light Load
- Programmable current limit, output voltage by resistor or I²C
- Accurate Output Current with CC Loop Regulation
- Cycle by Cycle Current Limit is up to 12A
- Small footprint: 20-pin 3mm × 3mm Flip Chip QFN Package

APPLICATIONS

- Quick Charge Mobile Power
- Bluetooth Speaker Supply
- Thunderbolt Interface
- Electronic cigarette package.

TYPICAL APPLICATION CIRCUIT

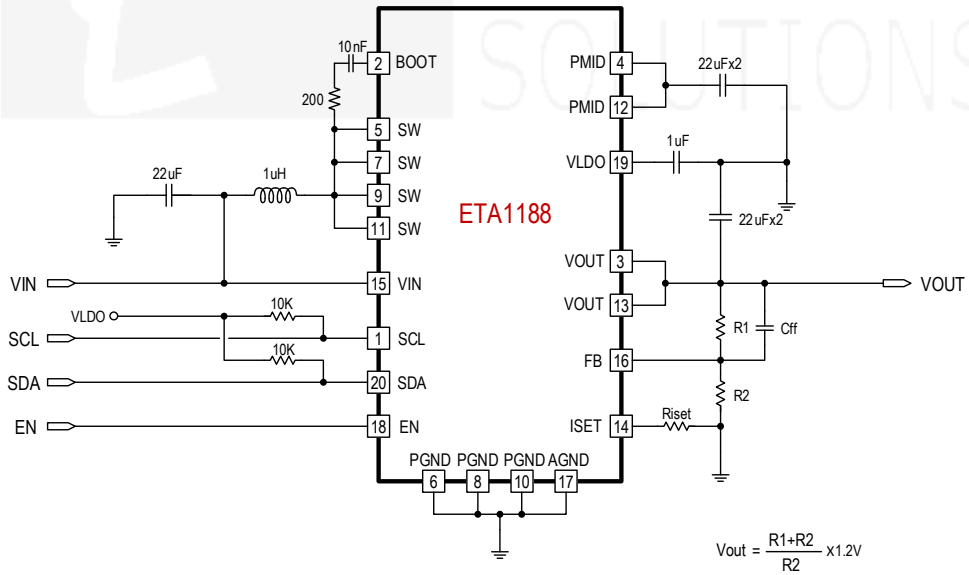
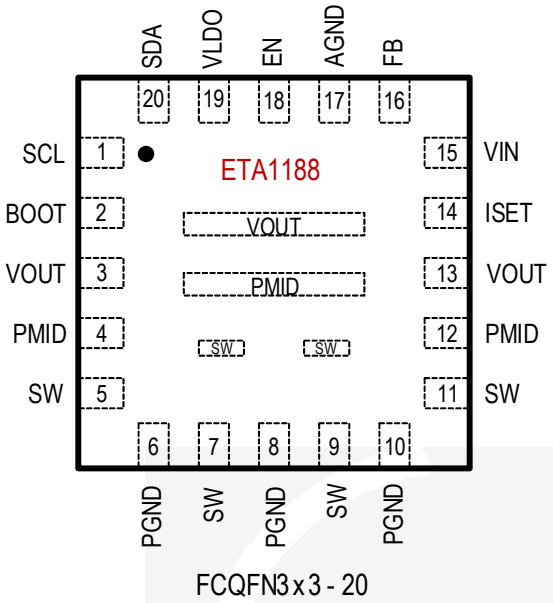


Figure 1: ETA1188 Typical Application Circuit

ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA1188F3W	FCQFN3x3-20	ETA1188 YWW2L	5000

PIN CONFIGURATION



FCQFN3 x 3 - 20

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

IN Voltage to PGND.....–0.3V to 13.2V
OUT, PMID, SW Voltage to PGND.....–0.3V to 16V
BOOT Voltage to SW.....–0.3V to SW+5V
All Other Pin Voltage to PGND.....–0.3V to 6V
SW, IN, OUT to PGND current.....Internally limited
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–55°C to 150°C
Thermal Resistance θ_{JA}
FCQFN3X3-20.....30.....°C/W
Lead Temperature (Soldering, 10sec) .....260°C
ESD HBM (Human Body Mode) 2KV
ESD MM (Machine Mode) 200V

ELECTRICAL CHARACTERISTICS

(V_{IN} =3.3V, V_{OUT}=9V, AGND=PGND, unless otherwise specified. Typical values are at T_A = 25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPLY CONDITIONS						
VIN input voltage range	VIN		2.7		12	V
Input Under-Voltage-Lock-Out	IN_UVLO	IN rising		2.6		V
UVLO hysteresis	IN_UVLO_HYST	IN falling		0.3		V
Input Over-Voltage-Protection	IN_OVP	IN rising		12.5		V
IN_OVP Hysteresis	IN_OVP_HYST	IN falling		1		V
Quiescent Current	IQ	EN=Logic High, No load, No switching		200		µA
Shutdown Supply Current at V_{IN}	ISD	V_{EN}=GND, VIN = 4.2V		2	5	µA
Power Good Deglitch delay	TPG	IN_UVLO < VIN < IN_OVP		1.5		ms
FREQUENCY CONFIGURATION						
Switching Frequency	FREQ			450		kHz
I2C Clock Frequency Range	FI2C		0.05		3.4	MHz

OUTPUT CONFIGURATION						
Feedback Voltage	VFB	V_{OUT} =4.5V to 12.6V	1.176	1.2	1.224	V
FB Leakage Current	IFB			0		nA
ISET Pin Voltage	VISET	VOUT ≥ VOUT_LOWV	0.98	1.0	1.02	V
		VOUT < VOUT_LOWV	0.78	0.8	0.82	V
ISET Output Current ratio	KISET	KISET = IQ1 / IISET		5000		
Output Current Limit	VOUT_ILIM	Adjustable, R_{ISET}=1.6kΩ		3.125		A
Output Current Foldback	VOUT_IFB	Adjustable, R_{ISET}=1.6kΩ		3		A
Switching Cycle-by-Cycle Lowside current limit	IPEAK			12		A
Minimum Inductor Current each cycle	IMIN			750		mA
Inductor Zero Crossing Current Stopping threshold	IQZX			270		mA
PROTECTION						
PMID Over Voltage Protection	PMID_OVP			13.6		V
PMID_OVP Hysteresis	PMID_OVP_HYST			1		
VOUT enter deep condition threshold	VDEEP_ENTER	VOUT falling, VOUT- VIN		250		mV
VOUT exits deep condition threshold	VDEEP_EXIT	VOUT rising over VIN		500		mV
Q1 Swapping sensing threshold	VOUT_HIGH	VOUT rising		2.5		V
VOUT_HIGH Hysteresis	VOUT_HIGH_HYST	VOUT falling		200		mV
FB Over-Voltage-Protection	VFB_OVP	To stop switching		1.38		V
VFB_OVP Hystersis	VFB_OVP_HYST			90		mV
Output Under Voltage Protection	FB_UVP	Track FB pin Voltage		0.60		V
Hiccup Retrying Timer	THCON	Regulator enabled		4.4		ms
Hiccup Disable Timer	THCOFF	Regulator disabled		13.2		ms
Thermal Shutdown	TSD	Rising, Hysteresis=20°C		155		°C

LOGIC PINS, EN, SDA, SCL					
Input Current		2Meg resistor from EN to GND, VEN = 1V.		1	μA
logic high voltage			1.2		V
logic low voltage				0.4	V
POWER FETS					
PMID to OUT Switch On Resistance	RQ1			20	mΩ
Highside Switch On Resistance	RQ2			18	mΩ
Lowside Switch On Resistance	RQ3			14	mΩ
SW Leakage Current	SW_LKG	VOUT = 9V, V_{FB}=1.5V,V_{SW}=0 or 9V, V_{EN}=GND		10	μA
INTERNAL VOUT SETTING					
VOUT ramping slew rate	VOUT_SLEW	SLEW[1:0] = 00		18	mV/μs
		SLEW[1:0] = 01		9	
		SLEW[1:0] = 10		4.5	
		SLEW[1:0] = 11		2.25	
Internal VOUT setting range	VOUT_INT	VOREG_INT[ ] = 1	3.6	12	V
Internal VOUT current limit range	ILIM_INT	IOREG_INT[ ] = 1	500	4000	mA

PIN DESCRIPTION

PIN #	PIN NAME	DESCRIPTION
1	SCL	I²C interface clock. Connect a 10-kΩ pull up resistor to VLDO or external 3.3V rail.
2	BOOT	Bootstrap capacitor connection for the high-side FET gate driver. Connect a 10-nF ceramic capacitor (voltage rating ≥ 10 V) from BOOT pin to SW pin.
3, 13	VOUT	Output pins. Connect a 2x22uF to GND
4, 12	PMID	Midpoint of the Boost output and current limit switch. Connect a 22uF to GND
5, 7, 9, 11	SW	Switching Pin. Connect with an inductor between this pin and input.
6, 8, 10	PGND	Power Ground.
14	ISET	Boost maximum output current setting. Connect a resistor between this pin and analog ground to set the current level.
15	VIN	Input pin. Connect to Battery or input supply. Bypass with a 22uF capacitor from this pin to ground.
16	FB	Feedback pin for setting up the boost output voltage.
17	AGND	Analog Ground pin.
18	EN	Enable pin for the IC.
19	VLDO	LDO Regulator Output. Bypass with 1uF capacitor from this pin to ground.
20	SDA	I²C interface data. Connect a 10-kΩ pull up resistor to VLDO or external 3.3V rail.

FUNCTIONAL BLOCK DIAGRAM

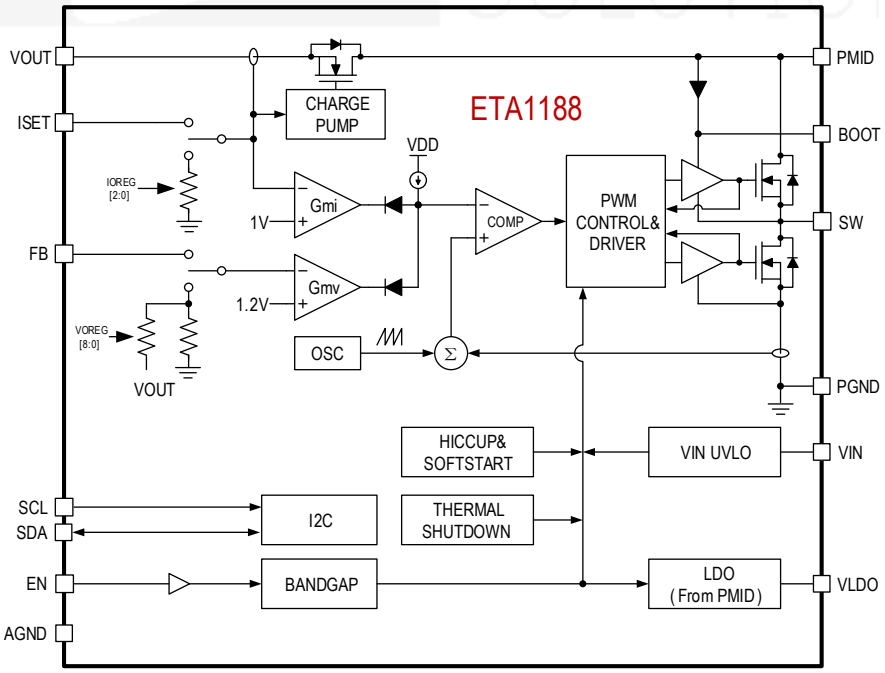
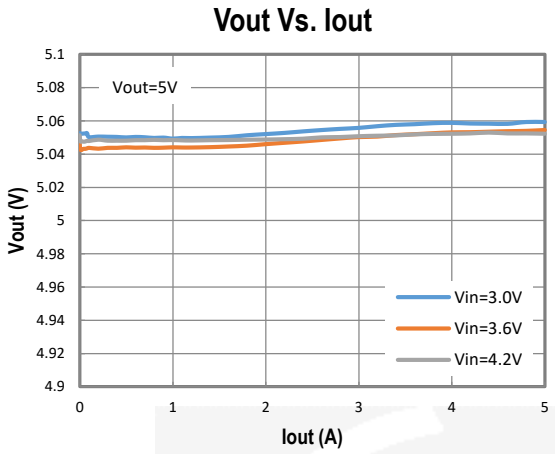
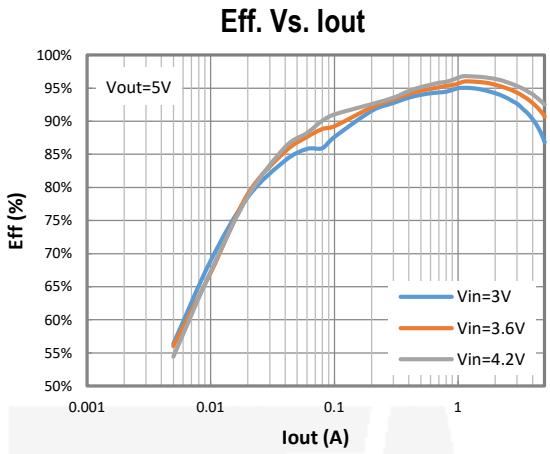
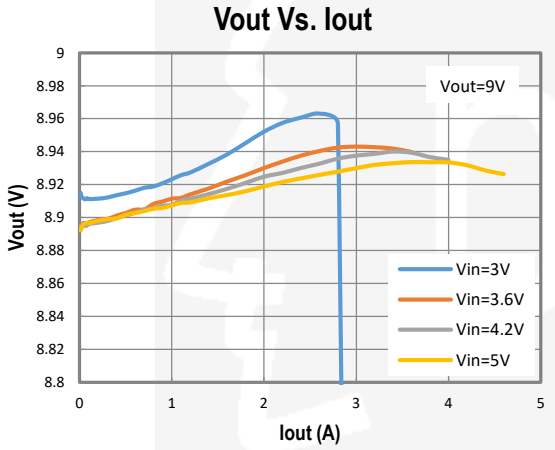


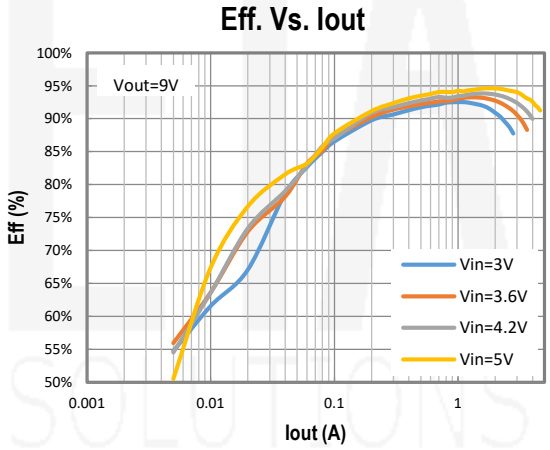
Figure 2: ETA1188 Function Block Diagram

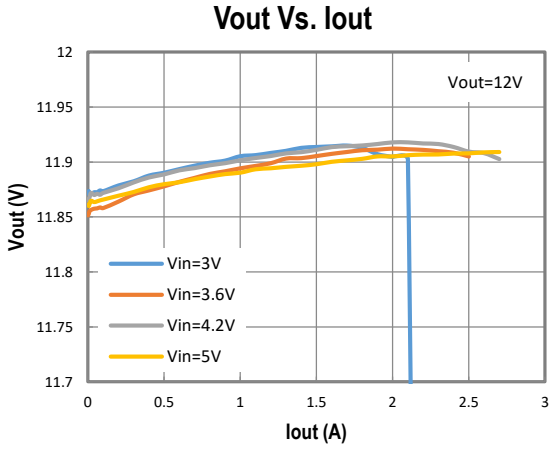
TYPICAL PERFORMANCE CHARATERISTICS

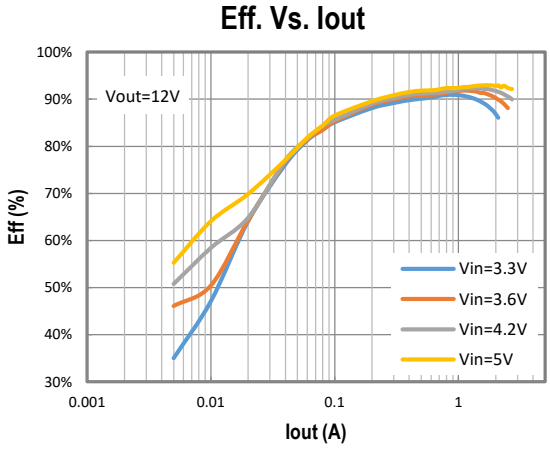






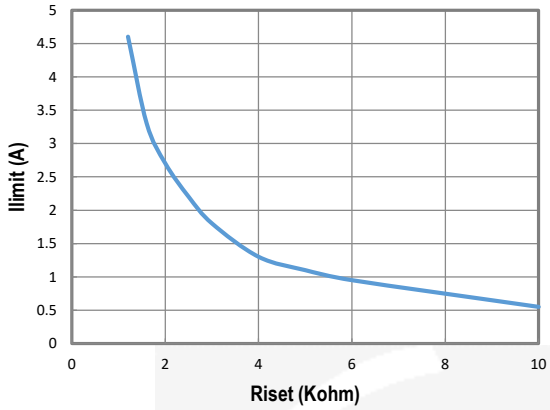




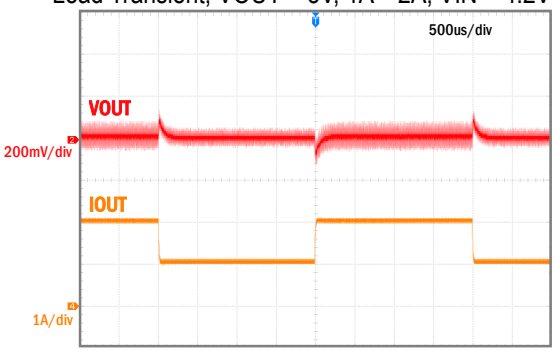


TYPICAL PERFORMANCE CHARATERISTICS (cont')

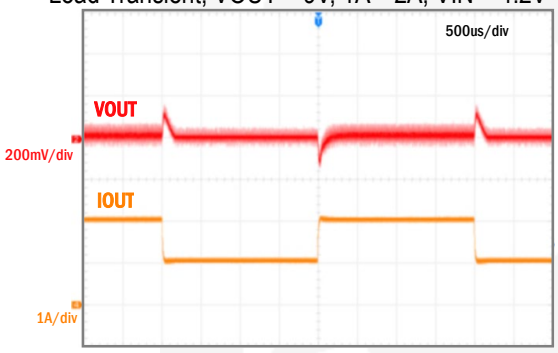
Iout Limit Vs. Riset



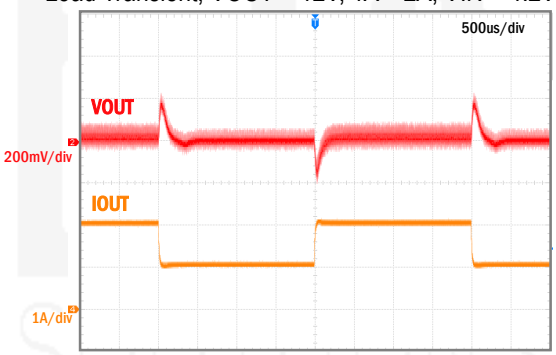
Load Transient, VOUT = 5V, 1A – 2A, VIN = 4.2V



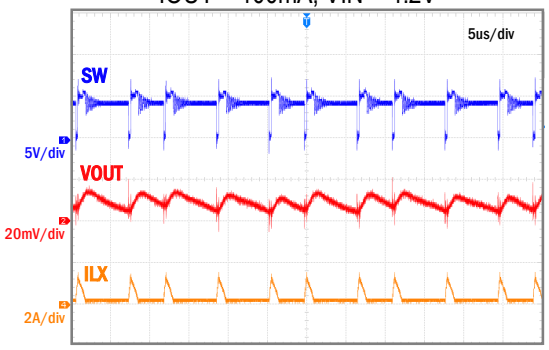
Load Transient, VOUT = 9V, 1A – 2A, VIN = 4.2V



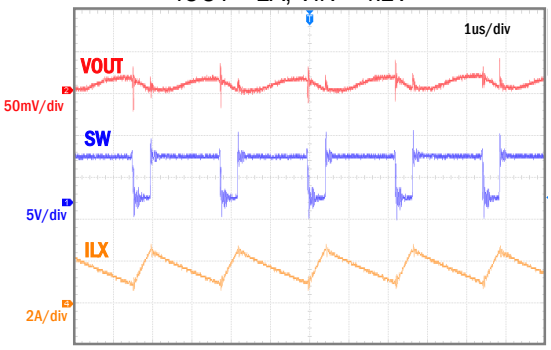
Load Transient, VOUT = 12V, 1A – 2A, VIN = 4.2V



Switching in DCM, VOUT = 5V,
IOUT = 100mA, VIN = 4.2V

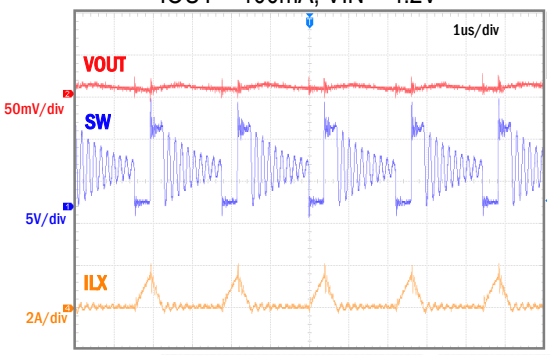


Switching in CCM, VOUT = 5V,
IOUT = 2A, VIN = 4.2V

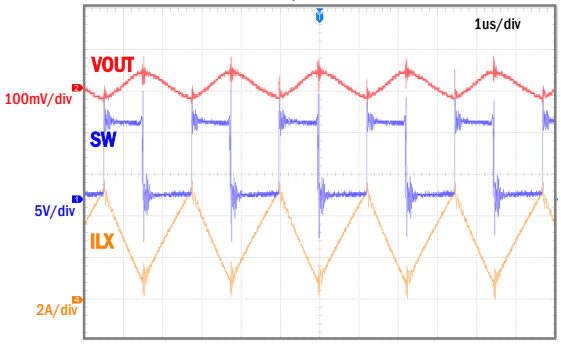


TYPICAL PERFORMANCE CHARATERISTICS (cont')

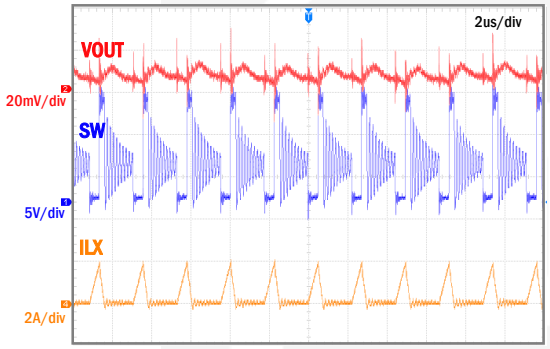
Switching in DCM, VOUT = 9V,
IOUT = 100mA, VIN = 4.2V



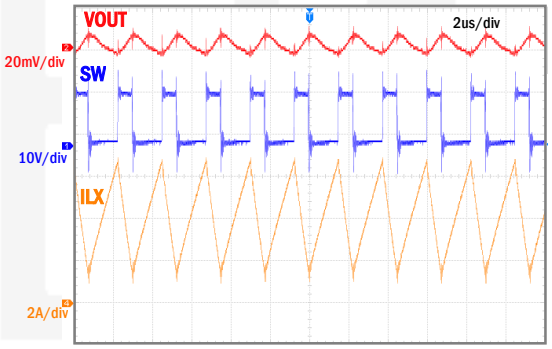
Switching in CCM, VOUT = 9V,
IOUT = 2A, VIN = 4.2V



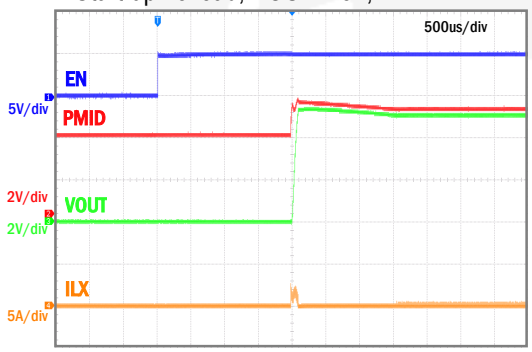
Switching in DCM, VOUT = 12V,
IOUT = 100mA, VIN = 4.2V



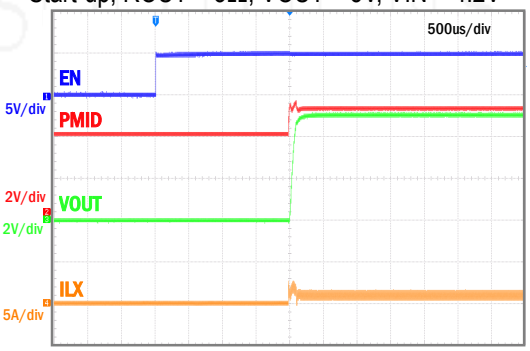
Switching in CCM, VOUT = 12V,
IOUT = 100mA, VIN = 4.2V



Start-up no load, VOUT = 5V, VIN = 4.2V

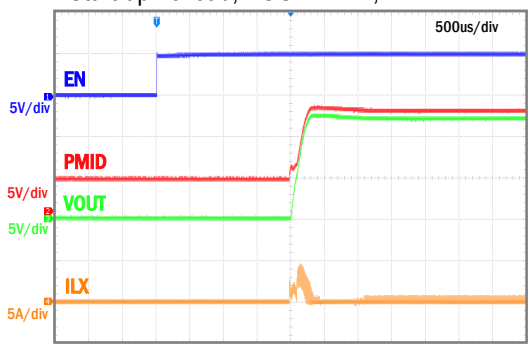


Start-up, ROUT = 3Ω, VOUT = 5V, VIN = 4.2V

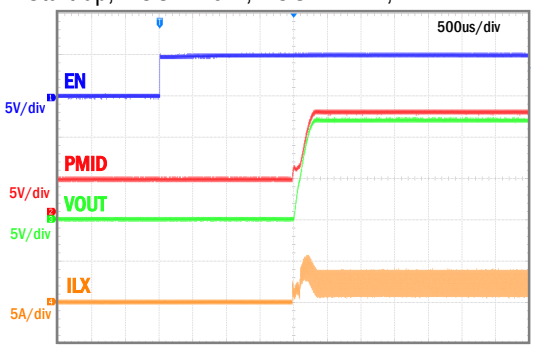


TYPICAL PERFOMANCE CHARATERISTICS (cont')

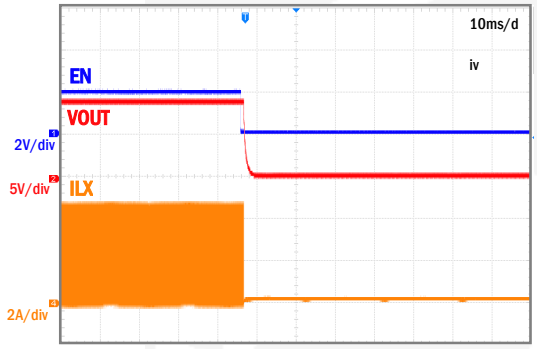
Start-up no load, VOUT = 12V, VIN = 4.2V



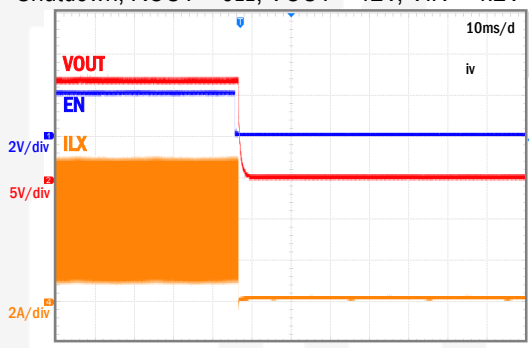
Start-up, ROUT = 8Ω, VOUT = 12V, VIN = 4.2V



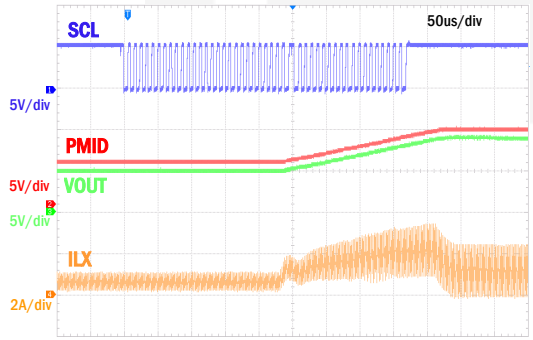
Shutdown, ROUT = 9Ω, VOUT = 9V, VIN = 4.2V



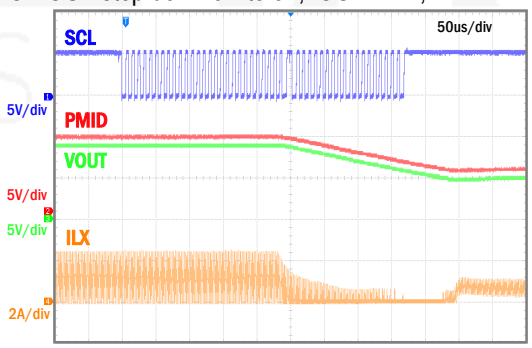
Shutdown, ROUT = 9Ω, VOUT = 12V, VIN = 4.2V



I²C VOUT step up 5V to 9V, IOUT = 1A, VIN = 4.2V



I²C VOUT step down 9V to 5V, IOUT = 1A, VIN = 4.2V



FUNCTION DESCRIPTION

START-UP

ETA1188 is enabled when all following conditions occur:

- EN pin is asserted logic high
- VIN voltage is above VIN_UVLO
- VIN voltage is below VIN_OVP

Once enabling conditions are provided, a start-up is allowed to operate without VOUT_UVP and VOUT_OCP protections in 4ms before a HICCUP protection is enabled to protect part from output short.

Q1 will be enabled same time with BOOST function. Q1 is controlled to operate differently in two modes, depending on the magnitude of the output VOUT versus the input VIN.

- VOUT is lower than VIN: Q1 operates with its current limit to limit VOUT output current at about 80% of full VOUT current limit which is set by ISET resistor. In this mode, PMID is regulated to VIN+1. BOOST will stop switching if PMID voltage is above PMID_OVP level.
- VOUT is greater than VIN: Q1 FET gate will be driver to its maximum voltage. BOOST will sense the current through Q1 and control the limit. Q1 FET will be disabled if FB voltage is above VFB_OVP level.

OUTPUT VOLTAGE REGULATION

An external feedback net is used to set the regulation level of the BOOST. FB pin is input of the error amplifier will be regulated at 1.2V.

Voltage regulation loop is compensated internally.

BOOST PFM/PWM OPERATION

ETA1188 Use IMIN to determine PFM. Inductor current is required to be greater than IMIN each cycle. In the condition output current is small, load is below IMIN energy, it will bring VOUT a little bit higher than regulation, ETA1188 will skip switching until VOUT fall below regulation level.

NEGATIVE INDUCTOR CURRENT PROTECTION

Beside PFM operation to improve efficiency when output current is low, ETA1188 also detects negative inductor current in discontinuous mode, then turn off high side FET Q2 judiciously. Finally, efficiency is improved on whole discontinuous mode.

OUTPUT CURRENT LIMIT AND SWITCHING CURRENT PROTECTION

ETA1188 BOOST regulator is integrated constant output current regulation that provides very accurate output current. Though, at low output condition output current limit is controlled by Q1 to avoid “boost current run away” condition. Anyway, switching inductor peak current is always limited at 12A (typically).

Output current is determined by following rule:

VOUT CONDITION		Q1 BEHAVIOUT	BOOST CC REGULATION	ISET REGULATION VOLATGE
V_{OUT}< V_{IN}	V_{OUT}< 2.5V			
NO	NO	Full Open	Activated	1.0V
YES	NO	Current Regulation	Inactivated	0.8V
ANY	YES	Current Regulation	Inactivated	0.5V

Output current level I_{BSTOUT} is set by ISET pin resistor. Current is sensed to ISET pin is 1/5000 of Q1 current, then I_{BSTOUT} is given by following equation:

$$I_{BSTOUT} = 5000 \times \frac{V_{ISET}}{R_{ISET}} (A)$$

BOOST OUTPUT OVER VOLTAGE PROTECTION

At some conditions that PMID could hit PMID_OVP threshold, boost will stop switching immediately and operate again when PMID goes back to normal. In this condition, Q1 is still fully turned on.

Besides PMID over voltage protection, ETA1188 integrates FB over voltage protection that when FB voltage hits VFB_OVP, boost will stop switching immediately and operate again when FB goes back to normal. This feature to protect output connected device when VIN is higher than regulation level.

BOOST HICCUP OPERATION

During operation if one of FB_UVP or VOUT_OCP occurs, ETA1188 starts HICCUP mode that both Q1 and boost are disabled in 12ms then retried in 4ms. It will exit HICCUP mode when fault conditions are removed in 4ms retrying.

THERMAL SHUTDOWN

ETA1188 is shutdown when junction temperature gets higher than 155˚C. And it will be back to normal operation when cooler than 120˚C.

APPLICATION INFORMATION

VOUT OUTPUT VOLTAGE CONFIGURATION

FB pin voltage is regulated to 1.2V, so feedback resistors are given by following equation:

$$V_{OUT} = 1.2 \times \frac{R_1 + R_2}{R_2} (V)$$

For example, if R_2 = 55kΩ, R_1 is given by below table:

VOUT(V)	R_1 (kΩ)	VOUT(V)	R_1 (kΩ)
5.06	180	9.13	370
5.91	220	10.41	430
6.99	270	11.27	470
8.27	330	12.13	510

OUTPUT CURRENT LIMIT CONFIGURATION

$$I_{BSTOUT} = 5000 \times \frac{V_{ISET}}{R_{ISET}} (A)$$

INTERNAL SETTING BY I²C

Beside the external configuration for VOUT and ILIM, ETA1188 provide an I²C protocol to set VOUT and ILIM internally. Once VOREG_INT[ ] is set to 1 via I²C, there is internal feedback net start run to set VOUT from 3.6V to setting level.

ETA1188 is configured as a slave at I²C address D6xH. Resister map is shown in below table.

BIT	NAME	RESET	RD/WR	FUNCTION
		23	REG00: ADDRESS 00xH: INTERNAL CONFIGURATION REGISTER	
7	VOREG[8]	0	RD/WR	Internal VOUT Configuration bit: 5120mV
6	VOREG[7]	0	RD/WR	Internal VOUT Configuration bit: 2560mV
5	VOREG[6]	1	RD/WR	Internal VOUT Configuration bit: 1280mV
4	VOREG[5]	0	RD/WR	Internal VOUT Configuration bit: 640mV
3	VOREG[4]	0	RD/WR	Internal VOUT Configuration bit: 320mV
2	VOREG[3]	0	RD/WR	Internal VOUT Configuration bit: 160mV
1	VOREG[2]	1	RD/WR	Internal VOUT Configuration bit: 80mV
0	VOREG[1]	1	RD/WR	Internal VOUT Configuration bit: 40mV
		00	REG01: ADDRESS 01xH: INTERNAL CONFIGURATION / CONTROL REGISTER	
7	VOREG[0]	0	RD/WR	Internal VOUT Configuration bit: 20mV
6	VOREG_INT	0	RD/WR	Enable internal VOREG setting: => 0: Use FB pin to configure VOUT regulation. => 1: Use VOREG[8:0] to configure VOUT regulation.
5	IOREG_INT	0	RD/WR	Enable internal IOREG setting: => 0: Use ISET pin to configure VOUT current limit. => 1: Use IOREG[:] to configure VOUT current limit.
4	IOREG[3]	0	RD/WR	Internal Current Limit Configuration bit: 500mA
3	IOREG[2]	0	RD/WR	Internal Current Limit Configuration bit: 1000mA
2	IOREG[1]	0	RD/WR	Internal Current Limit Configuration bit: 2000mA
1	SLEW<1>	0	RD/WR	VOUT Slew Rate setting => 00: 18mV/μs => 01: 9mV/μs => 10: 4.5mV/μs => 11: 2.25mV/μs
0	SLEW<0>	0	RD/WR	

RECOMMENDATION of INTERNAL VOUT CONFIGURATION

ETA1188 allows to configure VOUT via I²C following setting in Register Map. It is able to configure VOUT from 3.6V to 12V. But ETA1188 always start to regulate with external FB until I²C command is sent. This requires to application using I²C to set external FB at 5V default to avoid over voltage supply to output connected devices.

Internal configuration also burns more supply current from VIN in no load condition, so thus to avoid waste dissipation from VIN in application, it is strong recommended to disable internal configuration when load disconnected or even in no load condition.

PCB RECOMMENDATION

Please always put PMID capacitor closet to the PMID pins and PGND pins, with wires directly connected to the PMID and PGND pins. DONOT connect the negative terminal of PMID capacitor to the ground plane, while the PGND pins are also connected to the ground pin. As such PMID capacitor serves as the input capacitor of switching charger, and if the capacitor is connected to the PGND pins thru ground plane, 2 serial vias (capacitor to ground plane and ground plane to PGND pins) are introduced, which means a serial parasitic inductor is placed between the input capacitor and the real input pins. And thus, the decoupling function of such input capacitor is compromised, a lot of switching noise may no longer be filtered by the input capacitor and leads to instability of the switching charger. Please also draw wide enough metal for VIN, VOUT and GND because current through each wire will be huge. Otherwise, it will affect to load regulation or input supply dropping. And just next to the PMID capacitor, VOUT capacitors must be placed, should not be far from PMID capacitors.

Following illustration shows the correct way to place the PMID, and VOUT capacitor.

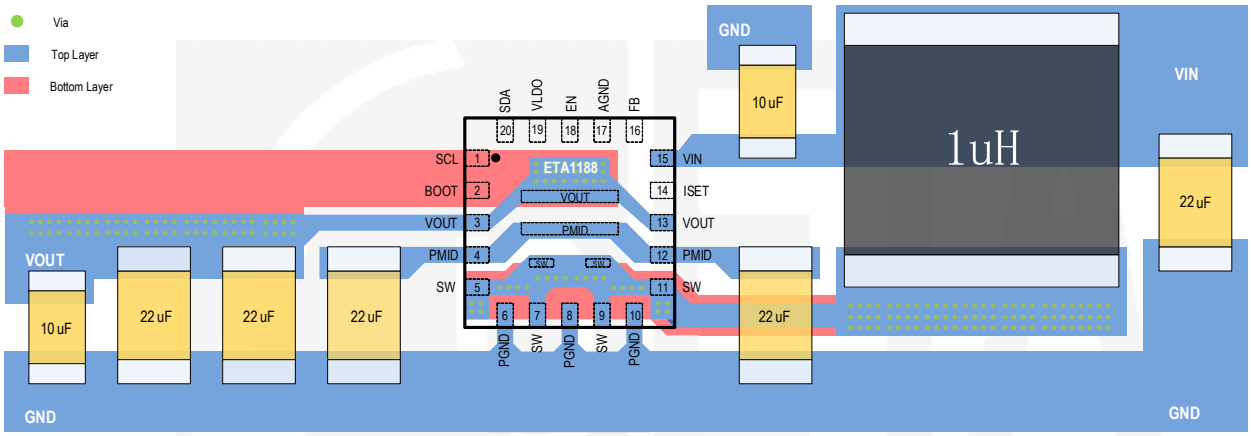
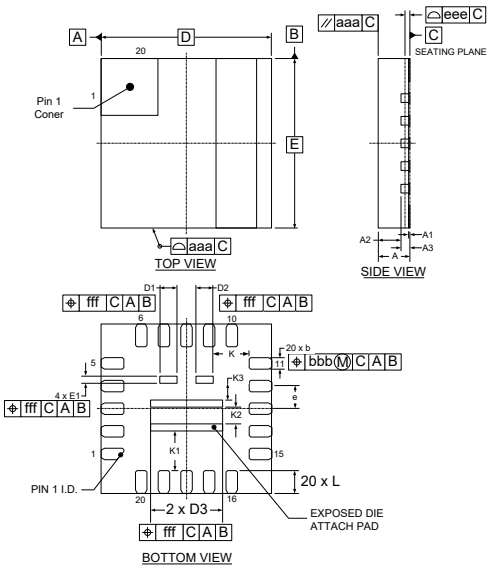


Figure 3: ETA1188 PCB Recommendation

PACKAGE OUTLINE

FCQFN3x3-20



		SYMBOL	MIN	TYP	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3	0.152 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	3 BSC		
	Y	E	3 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	D1	0.2	0.3	0.4
		D2	0.2	0.3	0.4
		D3	1.17	1.27	1.37
	Y	E1	0.02	0.12	0.22
LEAD LENGTH		L1	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K	0.63 REF		
		K1	0.71 REF		
EXPOSED PAD TO EXPOSED PAD EDGE		K2	0.3 REF		
		K3	0.3 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.1		