



**P-Ch 150V Fast Switching MOSFETs**

**Description**

The HSU25P15 uses advanced trench MOSFET technology to provide excellent  $R_{DS(ON)}$  and gate charge for use in a wide variety of other applications.

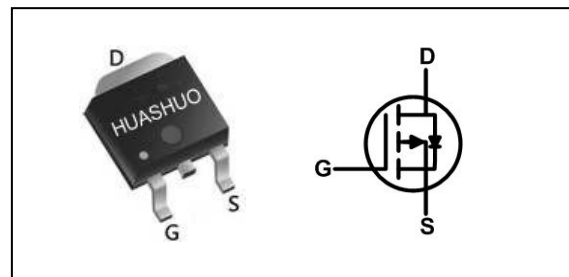
The HSU25P15 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

**Product Summary**

$V_{DS}$	-150	V
$R_{DS(ON),max}$	150	m $\Omega$
$I_D$	-23	A

**TO-252 Pin Configuration**



**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-150	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-23	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-15	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-85	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	220	mJ
$I_{AS}$	Avalanche Current	24	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	100	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	1.25	$^\circ C/W$



**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-150	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V , I <sub>D</sub> =-20A	---	130	150	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-2.0	-2.8	-4.0	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-120V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C	---	---	-1	uA
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> = ± 20V , V <sub>DS</sub> =0V	---	---	± 100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =-10V , I <sub>D</sub> =-20A	---	13	---	S
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-75V , V <sub>GS</sub> =-10V , I <sub>D</sub> =-10A	---	56	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	11	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	8.5	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-75V , V <sub>GS</sub> =-10V , R <sub>G</sub> =6Ω , I <sub>D</sub> =-10A	---	33	---	ns
T <sub>r</sub>	Rise Time		---	19	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	149	---	
T <sub>f</sub>	Fall Time		---	50	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-75V , V <sub>GS</sub> =0V , f=1MHz	---	3600	---	pF
C <sub>oss</sub>	Output Capacitance		---	455	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	186	---	

**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	---	---	-23	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25°C	---	---	-1.3	V

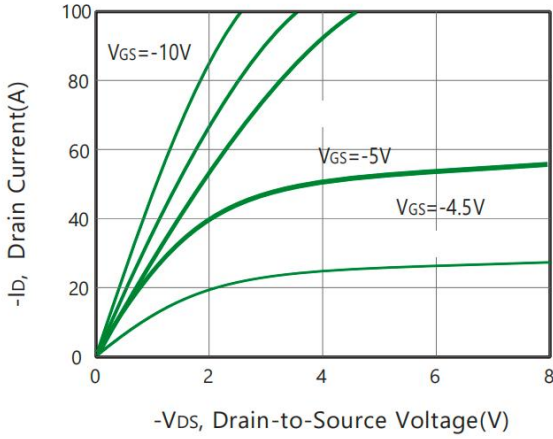
**Note :**

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=-75V,V<sub>GS</sub>=-10V,L=0.5mH,I<sub>AS</sub>=-24A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

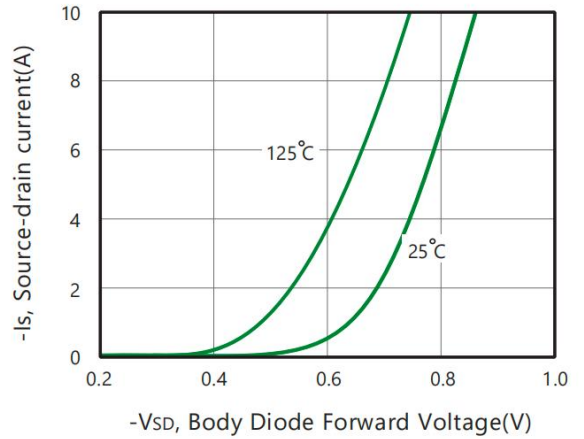


**Typical Characteristics**

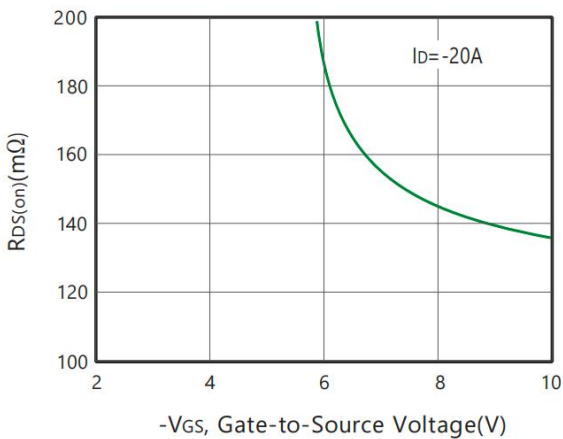
**Figure 1. Output Characteristics**



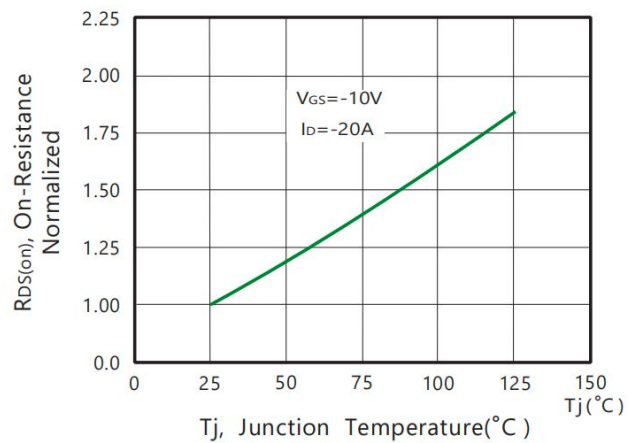
**Figure 2. Body Diode Forward Voltage Variation with Source Current**



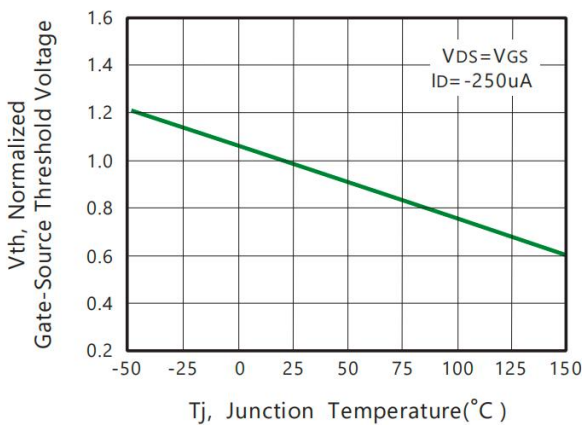
**Figure 3. On-Resistance vs. Gate-Source Voltage**



**Figure 4. On-Resistance Variation with Drain Current and Temperature**



**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Gate Charge**

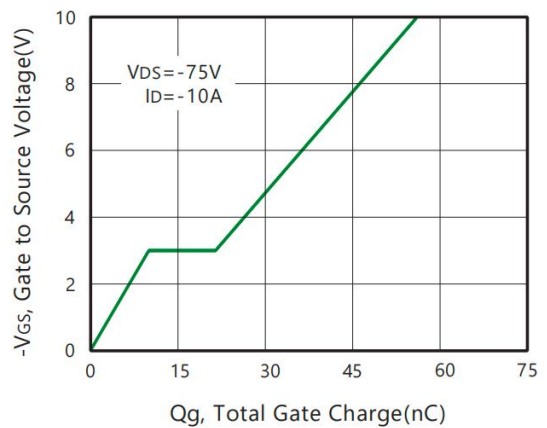




Figure 7. Capacitance

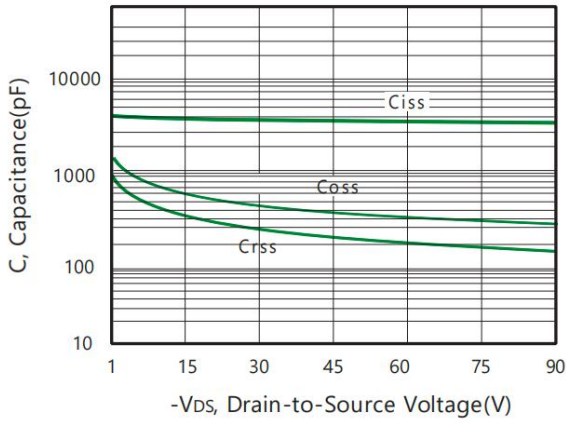


Figure 8. Maximum Safe Operating Area

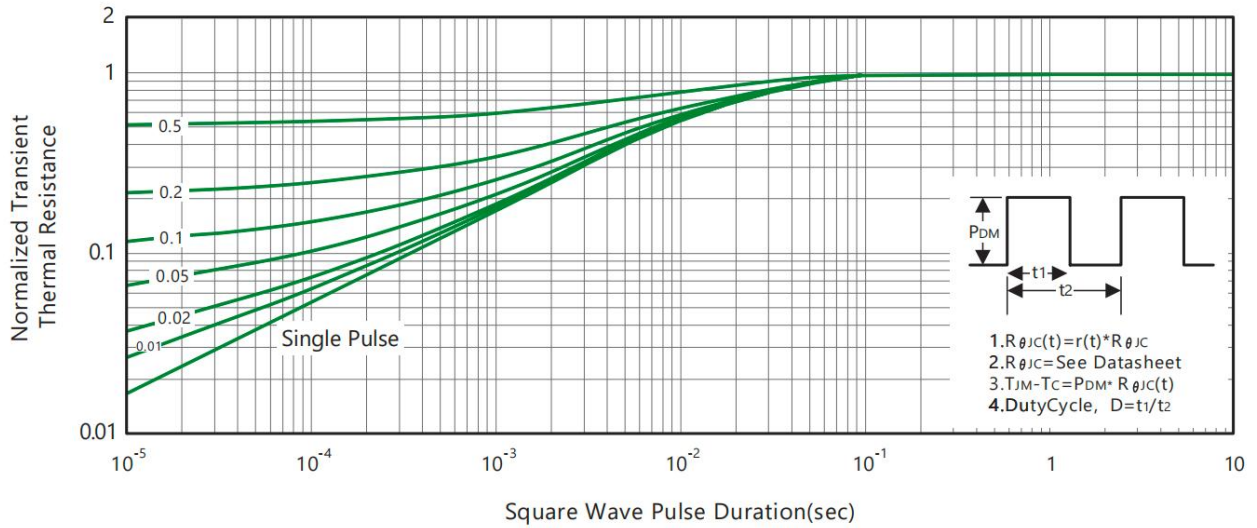
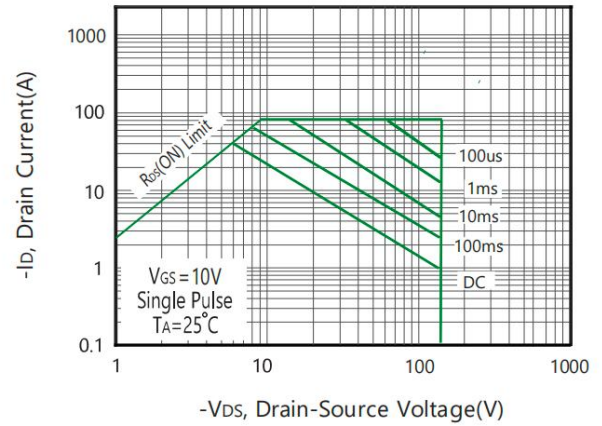
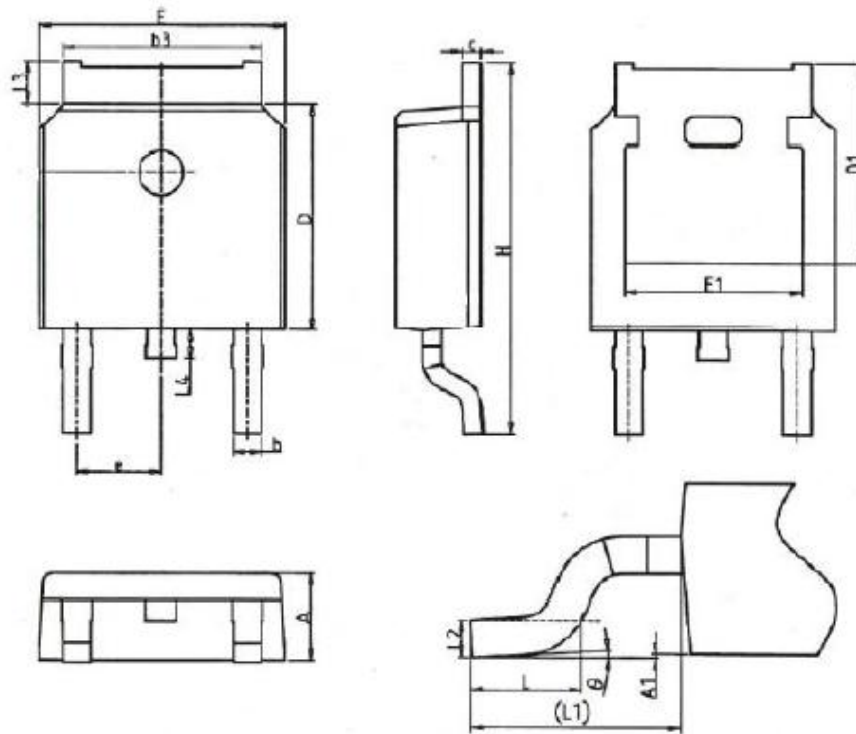


Figure 9. Normalized Thermal Transient Impedance Curve



**TO252-2L Package Outline**



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.40	0.086	0.095
A1	-	0.2	-	0.008
b	0.68	0.9	0.026	0.036
b3	4.95	5.46	0.194	0.215
c	0.43	0.89	0.017	0.035
D	5.97	6.22	0.235	0.245
D1	5.300REF		0.209REF	
E	6.35	6.73	0.250	0.265
E1	4.32	--	0.170	-
e	2.286BSC		0.09BSC	
H	9.4	10.5	0.370	0.413
L	1.38	1.78	0.054	0.070
L1	2.90REF		0.114REF	
L2	0.51BSC		0.020BSC	
L3	0.88	1.28	0.034	0.050
L4	0.5	1	0.019	0.039
θ	0°	8°	0°	8°