

## N-Channel Logic Level Power Field-Effect Transistor

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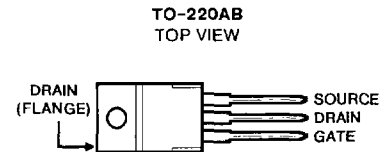
### Features

- 15A, 80V
- $R_{DS(ON)}$ : 0.14 $\Omega$
- Design Optimized for 5 Volt Gate Drive
- Can be Driven Directly from Q-MOS, N-MOS, TTL Circuits
- SOA is Power-Dissipation Limited
- +175°C Rated Junction Temperature
- Logic Level Gate
- High Input Impedance

### Description

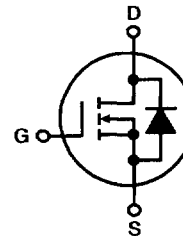
The RFP15N08L is an n-channel enhancement mode silicon gate power field effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control from logic circuit supply voltages.

### Package



### Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



### Absolute Maximum Ratings ( $T_C = +25^\circ\text{C}$ ), Unless Otherwise Specified

	RFP15N08L	UNITS
Drain-Source Voltage .....	80	V
Drain-Gate Voltage .....	80	V
Gate-Source Voltage .....	$\pm 10$	V
Drain Current, RMS Continuous .....	15	A
Pulsed .....	40	A
Power Dissipation Total @ $T_C = +25^\circ\text{C}$ .....	72	W
Power Dissipation Derating $T_C = +25^\circ\text{C}$ .....	0.48	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range .....	-55 to +175	$^\circ\text{C}$

## Specifications RFP15N08L

**Electrical Characteristics** At Case Temperature ( $T_C = +25^\circ\text{C}$ ), Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS		UNITS
				MIN	MAX	
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D = 1\text{mA}$	$V_{GS} = 0\text{V}$	80	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$	$I_D = 1\text{mA}$	1	2.5	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 65\text{V}$		-	1	$\mu\text{A}$
		$V_{DS} = 65\text{V}$	at $T_C = +125^\circ\text{C}$	-	50	$\mu\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 10\text{V}$	$V_{DS} = 0\text{V}$	-	100	nA
Drain-Source On Voltage	$V_{DS(ON)}$	$I_D = 7.5\text{A}$	$V_{GS} = 5\text{V}$	-	1.05	V
		$I_D = 15\text{A}$	$V_{GS} = 5\text{V}$	-	3.0	V
On Resistance	$R_{DS(ON)}$	$I_D = 7.5\text{A}$	$V_{GS} = 5\text{V}$	-	0.14	$\Omega$
Total Gate Charge	$Q_G(\text{TOTAL})$	$V_{GS} = 0-10\text{V}$	$V_{DD} = 64\text{V}$	-	80	nC
Gate Charge at 5V	$Q_G(5)$	$V_{GS} = 0-5\text{V}$	$I_D = 15\text{A}$	-	45	nC
Threshold Gate Charge	$Q_G(\text{TH})$	$V_{GS} = 0-1\text{V}$	$R_L = 4.27\Omega$	-	3	nC
Plateau Voltage	$V_{\text{PLATEAU}}$	$I_D = 15\text{A}$	$V_{DS} = 15\text{V}$	-	4.5	V
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 40\text{V}$	$I_D = 7.5\text{A}$	-	40	ns
Rise Time	$t_r$	$R_G = 6.25\Omega$	$V_{GS} = 5\text{V}$	-	325	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	325	ns
Fall Time	$t_f$			-	325	ns
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	2.083	$^\circ\text{C/W}$

### Source-Drain Diode Ratings and Characteristics

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS		UNITS
				MIN	MAX	
Forward Voltage	$V_{SD}$	$I_{SD} = 7.5\text{A}$		-	1.4	V
Reverse Recovery Time	$T_{RR}$	$I_F = 4\text{A}$ , $dI_F/dt = 100\text{a}/\mu\text{s}$		-	225(typ)	ns