HARRIS

# RFD3N08L
# RFD3N08LSM

## N-Channel Logic Level Power Field Effect Transistors

August 1991

### Features

- 3A, 80V
- $R_{DS(on)} = 0.80\Omega$
- Design Optimized for 5 Volt Gate Drive
- Can be Driven Directly From Q-MOS, N-MOS, or TTL Circuits
- SOA is Power-Dissipation Limited
- 175°C Rated Junction Temperature
- Logic Level Gate
- High Input Impedance

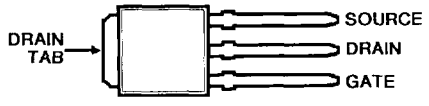
### Description

The RFD3N08L is an n-channel enhancement mode silicon gate power field effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solonoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control from logic circuit supply voltages.

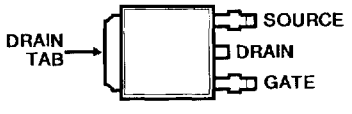
The RFD3N08L is supplied in the JEDEC TO-251 plastic package and the RFD3N08LSM is supplied in the JEDEC TO-252 plastic package.

### Packages

TO-251AA
TOP VIEW

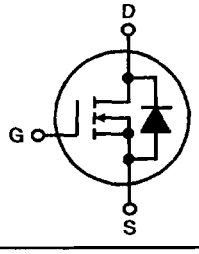



TO-252AA
TOP VIEW




### Terminal Diagram

N-CHANNEL ENHANCEMENT MODE




### Absolute Maximum Ratings ($T_C = +25^oC$), Unless Otherwise Specified

Drain-Source Voltage, $V_{DSS}$ ..... 80V
Drain-Gate Voltage, ($R_{GS} = 1m\Omega$), $V_{DGR}$ ..... 80V
Gate-Source Voltage, $V_{GS}$ ..... ±10V
Drain Current:
  RMS Continuous, $I_D$ ..... 3A
  Pulsed, $I_{DM}$ ..... 7A
Power Dissipation, $P_D$:
  $T_C = +25^oC$ ..... 30W
  Derate Above $T_C = +25^oC$ ..... 0.20W/°C
Operating and Storage Junction Temperature Range, $T_J$, $T_{STG}$ ..... -55 to +175°C

9 PREVIEW PRODUCTS



File Number 2836

**Electrical Characteristics** ($T_C$ = +25°C), Unless Otherwise Specified

| CHARACTERISTICS | SYMBOLS | TEST CONDITIONS | | LIMITS MIN | LIMITS MAX. | UNITS |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = 1mA, $V_{GS}$ = 0V | | 80 | - | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | | 1 | 2.5 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 70V | | - | 1 | μA |
| | | $V_{DS}$ = 70V @ $T_C$ = 125°C | | - | 50 | μA |
| Gate-Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ± 10V, $V_{DS}$ = 0V | | - | 100 | nA |
| Drain-Source on Voltage | $V_{DS(on)}$ | $I_D$ = 1.5A, $V_{GS}$ = 5V | | - | 1.2 | Ω |
| | | $I_D$ = 3A, $V_{GS}$ = 5V | | - | 2.5 | V |
| On Resistance | $R_{DS(on)}$ | $I_D$ = 1.5A, $V_{GS}$ = 5V | | - | 0.8 | Ω |
| Total Gate Charge | $Q_{g(total)}$ | $V_{GS}$ = 0 to 10V | $V_{DD}$ = 48V | - | 8 | nC |
| Gate Charge at 5V | $Q_{g(5)}$ | $V_{GS}$ = 0 to 5V | $I_D$ = 2A | - | 5 | nC |
| Threshold Gate Charge | $Q_{g(th)}$ | $V_{GS}$ = 0 to 1V | $R_L$ = 24Ω | - | 1 | nC |
| Plateau Voltage | $V_{(plateau)}$ | $I_D$ = 3A, $V_{DS}$ = 15V | | - | 4.5 | V |
| Turn-On Delay Time | $t_{D(on)}$ | $V_{DD}$ = 40V, $I_D$ = 1A | | - | 20 | ns |
| Rise Time | $t_R$ | $R_G$ = 6.25V, $V_{GS}$ = 5V | | - | 130 | ns |
| Turn-Off Delay Time | $t_{D(off)}$ | | | - | 40 | ns |
| Fall Time | $t_F$ | | | - | 160 | ns |
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | | | - | 5 | °C/W |

**Source-Drain Diode Ratings and Characteristics**

| CHARACTERISTICS | SYMBOLS | TEST CONDITIONS | LIMITS MIN | LIMITS MAX. | UNITS |
|---|---|---|---|---|---|
| Forward Voltage | $V_{SD}$ | $I_{SD}$ = 1A | - | 1.4 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_f$ = 2A, $di_f/dt$ = 100A/μs | - | 150(typ.) | ns |