

February 1998

### Features

- 17A, 55V
- *Ultra Low On-Resistance*,  $r_{DS(ON)} = 0.070\Omega$
- Diode Exhibits Both High Speed and Soft Recovery
- *Temperature Compensating PSPICE Model*
- *Thermal Impedance SPICE Model*
- *Peak Current vs Pulse Width Curve*
- *UIS Rating Curve*
- *Related Literature*
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

### Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75309P3	TO-220AB	75309P
HUF75309D3	TO-251AA	75309D
HUF75309D3S	TO-252AA	75309D

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-252AA variant in tape and reel, e.g., HUF75309D3ST.

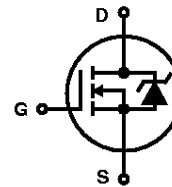
### Description



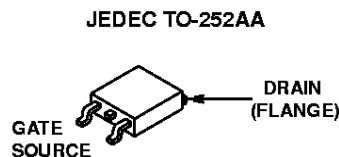
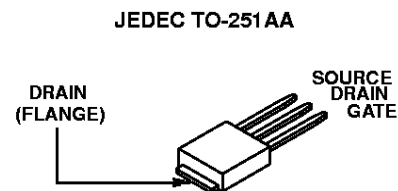
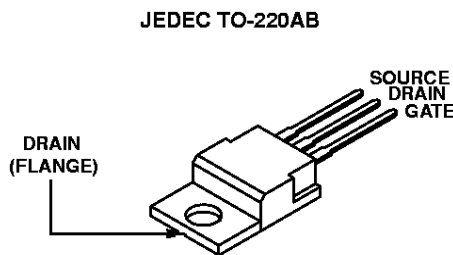
The HUF75309 N-Channel power MOSFET is manufactured using the innovative UltraFET™ process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75309.

### Symbol



### Packaging



## HUF75309P3, HUF75309D3, HUF75309D3S

### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

Drain to Source Voltage (Note 1)	$V_{DSS}$	55	V
Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1)	$V_{DGR}$	55	V
Gate to Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current			
Continuous (Figure 2)	$I_D$	17	A
Pulsed Drain Current	$I_{DM}$	Figure 5	
Pulsed Avalanche Rating	$E_{AS}$	Figures 6, 14, 15	
Power Dissipation	$P_D$	45	W
Derate Above $25^\circ\text{C}$		0.30	W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	$T_L$	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	$T_{pkg}$	260	$^\circ\text{C}$

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

- $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 11)	55	-	-	V	
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ (Figure 10)	2	-	4	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$	
		$V_{DS} = 45\text{V}, V_{GS} = 0\text{V}, T_C = 150^\circ\text{C}$	-	-	250	$\mu\text{A}$	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA	
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 17\text{A}, V_{GS} = 10\text{V}$ (Figure 9)	-	-	0.070	$\Omega$	
Turn-On Time	$t_{ON}$	$V_{DD} = 30\text{V}, I_D \cong 17\text{A}, R_L = 1.76\Omega, V_{GS} = 10\text{V}, R_{GS} = 27\Omega$ (Figures 18,19)	-	-	70	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	7	-	ns	
Rise Time	$t_r$		-	39	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	24	-	ns	
Fall Time	$t_f$		-	30	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	80	ns	
Total Gate Charge	$Q_g(TOT)$	$V_{GS} = 0\text{V}$ to $20\text{V}$	$V_{DD} = 30\text{V}, I_D \cong 17\text{A}, R_L = 1.76\Omega$	-	20	24	nC
Gate Charge at 10V	$Q_g(10)$	$V_{GS} = 0\text{V}$ to $10\text{V}$		-	11	13.5	nC
Threshold Gate Charge	$Q_g(TH)$	$V_{GS} = 0\text{V}$ to $2\text{V}$		$I_g(REF) = 1.0\text{mA}$ (Figures 13, 16, 17)	-	0.68	0.85
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ (Figure 12)	-	350	-	pF	
Output Capacitance	$C_{OSS}$		-	150	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	39	-	pF	
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	3.25	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220	-	-	62	$^\circ\text{C/W}$	
		TO-251, TO252	-	-	100	$^\circ\text{C/W}$	

### Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 17\text{A}$	-	-	1.25	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 17\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	50	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 17\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	70	nC