


**ANALOG
DEVICES**
**Ultrahigh Speed
Track-and-Hold**

ANALOG DEVICES INC

AD9100*
1.1 Scope.

This specification covers the requirements for a high speed track-and-hold amplifier.

1.2 Part Number.

The complete part number is as follows:

Device	Part Number
-1	AD9100S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000; package outline:

(X)	Package	Description
D	D-20	20-Pin Ceramic DIP
E	E-28	28-Pin Ceramic Leadless Chip Carrier

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltages ($\pm V_S$)	$\pm 6\text{ V}$
Analog Input Voltage	$\pm V_S$
Continuous Output Current	70 mA
Junction Temperature	$+175^\circ\text{C}$
Operating Temperature Range (Case)	-55°C to $+125^\circ\text{C}$
Storage Temperature Range (Case)	-65°C to $+150^\circ\text{C}$
Lead Soldering Temperature (10 sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

 Thermal Resistance DIP $\theta_{JA} = 50^\circ\text{C}/\text{W}$; this is valid with device mounted flush to a grounded 2-ounce copper clad board with 16 square inches of surface area and no air flow.

$$\text{LCC } \theta_{JA} = 48^\circ\text{C}/\text{W}$$

*Patent applied for

Table 1.

Test	Symbol	Design Limit ¹	Sub Group 1	Sub Group 2	Sub Group 3	Sub Group 4	Sub Group 5	Sub Group 6	Sub Group 7, 8	Test Condition ²	Units
Gain	A		0.989	0.989	0.989					$\Delta V_{IN} = 2 \text{ V}$	V/V min
Offset Voltage	V_{OS}		± 5	± 5	± 5					$V_{IN} = 0 \text{ V}$	mV
Output Drive	I_{OUT}		± 40	± 40	± 40						mA min
Power Supply Rejection Ratio	PSRR								-48	$\Delta V_S = 0.5 \text{ V p-p}$	dB min
Pedestal Sensitivity to Supply									± 3	$\Delta V_S = 0.5 \text{ V p-p}$	mV/V max
Output Voltage Range	V_{OUT}		± 2	± 2	± 2						V min/max
Analog Input Bias Current	I_B			± 16	± 16						μA
Input Resistance	R_I			350	200						k Ω min
CLOCK/CLOCK Input Bias Current	I_B		5	5	5					$CL/CL = -1.0 \text{ V}$	mA max
CLOCK and CLOCK Input Low Voltage	V_{IL}		-1.5 -1.8	-1.5 -1.8	-1.5 -1.8						V max V min
CLOCK and CLOCK Input High Voltage	V_{IH}		-1.0 -0.8	-1.0 -0.8	-1.0 -0.8						V min V max
Bandwidth (-3 dB)	BW	150								$V_{OUT} \approx 0.4 \text{ V p-p}$	MHz min
Slew Rate	t_{SR}	500								4-Volt Step	V/ μs min
Worst Harmonic (Hold Mode)	HD	-70/-68								$V_{OUT} = 2 \text{ V p-p}$ 12.1 MHz, 30 MSPS +125°C/-55°C	dBFS max
Droop Rate							± 30	± 40		$V_{IN} = 0 \text{ V}$	mV/ μs max
Pedestal Offset	V_{POS}						± 10	± 10		$V_{IN} = 0 \text{ V}$	mV
Settling Time	t_{SETT}	10								To 1 mV	ns max
Acquisition Time	t_{ACQ}	23								2 V Step; to 0.01%	ns max
+ V_S Supply Current	+ I_S			118	118						mA max
- V_S Supply Current	- I_S			132	132						mA max
Power Dissipation	PD			1.25	1.25						Watts max

NOTES

¹Indicates specification which is guaranteed but not tested. Value shown is over full temperature range.

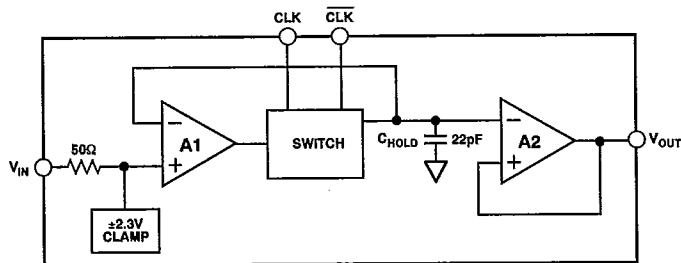
²Unless otherwise specified, $\pm V_S = \pm 5 \text{ V}$; $R_{IN} = 50 \Omega$; $R_{LOAD} = 100 \Omega$.

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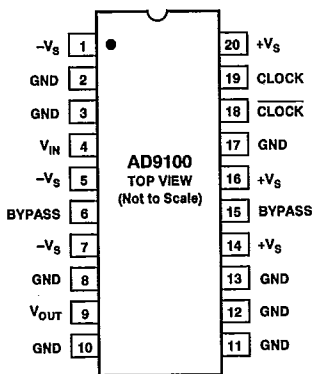
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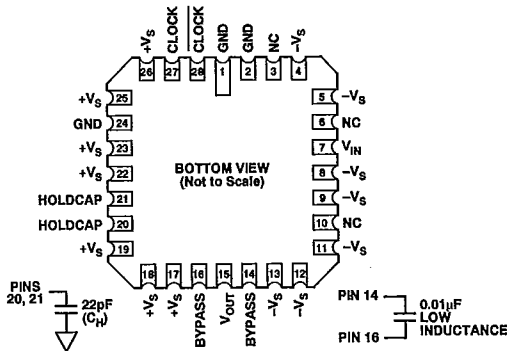
3.2.1 Functional Block Diagram and Terminal Assignments.



AD9100 Block Diagram



AD9100 DIP Pinouts



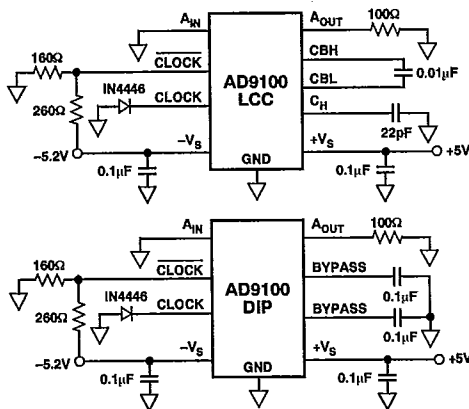
AD9100 LCC Pinouts

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (D-60) for SE version; group (I) for SD version.

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD9100 Burn-In Circuits

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SAMPLE/TRACK-HOLD AMPLIFIERS