National Semiconductor

Comlinear CLC949
Very Low-Power, 12-Bit, 20MSPS Monolithic A/D Convertter

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Very Low-Power, 12-Bit, 20MSPS Monolithic Converter

General Description

The Comlinear CLC949 is a 12-bit analog-to-digital converter subsystem including 12-bit quantizer, sample-and-hold amplifier, and internal reference. The CLC949 has been optimized for low power operation with high dynamic range. The CLC949 has a unique feature which allows the user to adjust internal bias levels in the converter which results in a trade-off between power dissipation and maximum conversion rate. With bias set for 220mW power dissipation the converter operates at 20MSPS. Under these conditions, dynamic performance with a 9.9MHz analog input is typically 68dB SNR and 72dBc SFDR. When bias is set for only 65mW power dissipation the converter maintains excellent performance at 5MSPS. With a 2.4MHz analog input signal the SNR is 70dB and SFDR is 78dBc. This excellent dynamic performance in the frequency domain without high power requirements make the part a strong performer for communications and radar applications. The low input noise of the CLC949, its 0.5LSB differential linearity error specification, fast settling, and low power dissipation also lead to excellent performance in imaging systems. All parts are thoroughly tested to insure that guaranteed specifications are met.

The CLC949 incorporates an input sample-and-hold amplifier followed by a quantizer which uses a pipelined architecture to minimize comparator count and the associated power dissipation penalty. An on-board voltage reference is provided. Analog input signals, conversion clock, and a single supply are all that are required for CLC949 operation.

The CLC949 exhibits very stable performance over the commercial and industrial temperature ranges. Most parameters shift very little as the ambient temperature changes from -40°C to 85°C. An exception to this rule is the dynamic performance of the converter. As the temperature is increased, the distortion increases, especially at higher input frequencies. This can be seen in the plot on page 3. For input frequencies below 7MHz, there is relatively little variation in distortion as the temperature is changed, but at higher input frequencies, it is apparent that the performance degrades as the temperature is increased.

Note that the reason for this degradation is the reduced ability of the CLC949 to handle high slew rates at high temperatures. In applications such as CCD imaging systems, where the slew rate at the A/D sampling instant is very low, this degradation will not be nearly so pronounced.

For applications requiring high temperature operation and very low distortion with high frequency input signals, use of an external sample-and-hold amplifier may enhance performance by reducing the slew rates that the CLC949 sees during its sampling period (just after the falling edge of CLK).

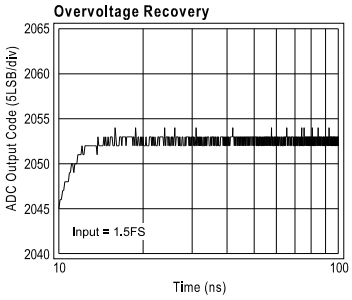
The CLC949 is fabricated in a 0.9µm CMOS technology. The **CLC949ACQ** is specified over the commercial temperature range of **0°C to +70°C** and the **CLC949AJQ** is specified over the industrial range of **-40°C to +85°C**. Both are packaged in a 44-pin Plastic Leaded Chip Carrier (PLCC).

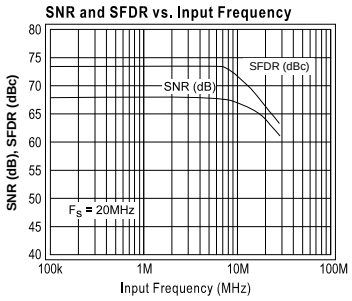
Features

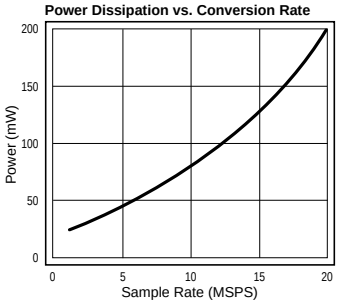
- Very low/programmable power
  - 0.07W @ 5MSPS
  - 0.22W @ 20MSPS
  - 0.40W @ 30MSPS
- Single supply operation (+5V)
- 0.5 LSB differential linearity error
- Wide dynamic range
  - 72dBc spurious-free dynamic range
  - 68dB signal-to-noise ratio
- No missing codes

Applications

- CCD imaging
- IR imaging
- FLIR processing
- Medical imaging
- High definition video
- Instrumentation
- Radar processing
- Digital communications







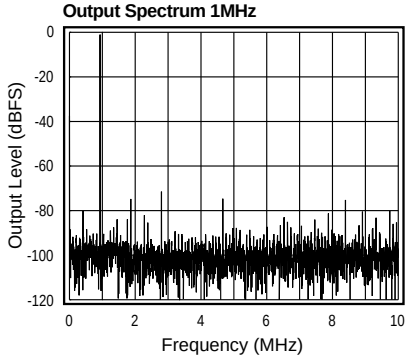
CLC949 Electrical Characteristics (+V_{DD} = +5V, Medium Bias (200μA): unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	SYMBOL
Case Temperature			+25°C	0 to 70°C	-40 to 85°C		
DYNAMIC CHARACTERISTICS							
overvoltage recovery V_{IN} = 1.5FS		15	25	25	25	ns	OR
effective aperture delay		3.0	6.2	6.2	6.2	ns	TA
aperture jitter		7.0	15	15	15	ps(rms)	AJ
slew rate		400				V/μS	SR
settling time		12				ns	ST
NOISE and DISTORTION (20MSPS)							
Signal-to-Noise Ratio (no harmonics)							
4.985MHz;	FS	68	66	66	66	dB	SNR2
9.663MHz;	FS	68	66	66	66	dB	SNR3
Spurious-Free Dynamic Range							
4.985MHz;	FS -1dB	72				dBc	SFDR2
9.663MHz;	FS -1dB	72	63	58	55	dBc	SFDR3
Intermodulation Distortion							
f_1 = 5.58MHz @ FS -7dB; f_2 = 5.70MHz @ FS -7dB		-70				dBc	IMD
3dB bandwidth (full power)		100				MHz	BW
NOISE and DISTORTION (5MSPS, low bias)							
Signal-to-Noise Ratio (no harmonics)							
2.4MHz;	FS	70	68	68	67	dB	SNR1
Spurious-Free Dynamic Range							
2.4MHz;	FS -1dB	78	66	66	64	dBc	SFDR1
NOISE and DISTORTION (25.6MSPS, high bias)							
Signal-to-Noise Ratio (no harmonics)							
9.894MHz;	FS	67	63	63	63	dB	SNR4
Spurious-Free Dynamic Range							
9.894MHz;	FS-1dB	67	59	53	48	dBc	SFDR4
DC ACCURACY and PERFORMANCE							
differential non-linearity	dc; FS	0.5	1.0	1.0	1.0	LSB	DNL
integral non-linearity	dc; FS	1.2	3.5	3.5	3.5	LSB	INL
common mode rejection ratio	dc	60				dB	CMRR
missing codes		0	0	0	0	codes	MC
mid-scale offset		5.0	25	25	25	mV	VIO
temperature coefficient		15				μV/°C	DVIO
gain error		1.0	5.0	5.0	5.0	%FS	GE
power supply rejection							
V_{dda}	dc	55				dB	PSRA
V_{ddd}	dc	50				dB	PSRD
VOLTAGE REFERENCE CHARACTERISTICS							
positive reference voltage (internal)		3.25	3.24-3.26	3.24-3.26	3.24-3.26	V	VREFP
negative reference voltage (internal)		1.25	1.24-1.26	1.24-1.26	1.24-1.26	V	VREFN
differential reference voltage (Vrefp - Vrefn)		2.0	1.98-2.02	1.98-2.02	1.98-2.02	V	VDIFF
ANALOG INPUT PERFORMANCE							
common mode range		2 - 3				V	VCM
differential range		± 2				V	VDM
analog input bias current		±0.1	±1.0	±1.0	±1.0	μA	IBN
analog input capacitance		5.0	10	10	10	pF	CIN
DIGITAL INPUTS							
CMOS input voltage	logic LOW		1	1	1	V	VIL
	logic HIGH		4.0	4.0	4.0	V	VIH
CMOS input current	logic LOW	±0.1	±1.0	±1.0	±1.0	μA	IIL
	logic HIGH	±0.1	±1.0	±1.0	±1.0	μA	IIH
DIGITAL OUTPUTS							
CMOS output voltage	logic LOW	0.25	0.5	0.5	0.5	V	VOL
	logic HIGH	4.8	4.5	4.5	4.5	V	VOH
TIMING							
maximum conversion rate		30	30	30	30	MSPS	CR
minimum conversion rate		10	10	10	10	KSPS	CRM
data hold time		7.0	4.5	4.5	4.5	ns	THLD
pipeline delay		6.5	6.5	6.5	6.5	clocks	
POWER REQUIREMENTS							
supply current (+V_{dd})		44	60	60	60	mA	IDD
power dissipation	20MSPS	220	300	300	300	mW	PDM
power dissipation (low bias)	5MSPS	65				mW	PDL
power dissipation (high bias)	30MSPS	400				mW	PDH

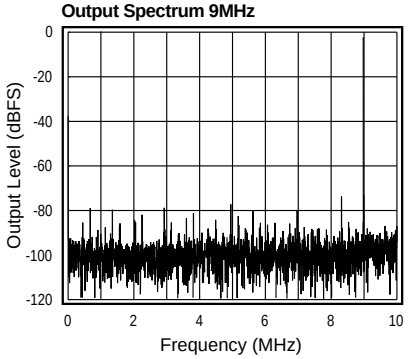
Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

CLC949 Typical Performance Characteristics (+V_{DD} = + 5V, Med Bias, F_S = 20MSPS: unless specified)

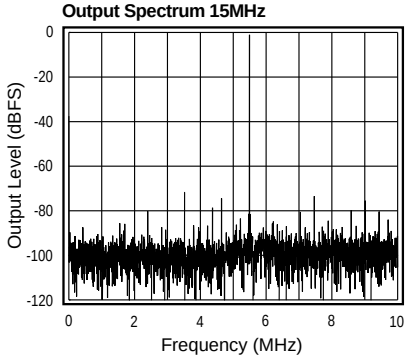
Output Spectrum 1MHz



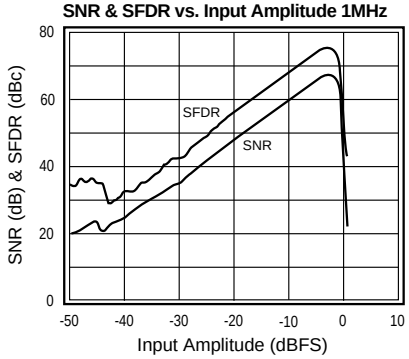
Output Spectrum 9MHz



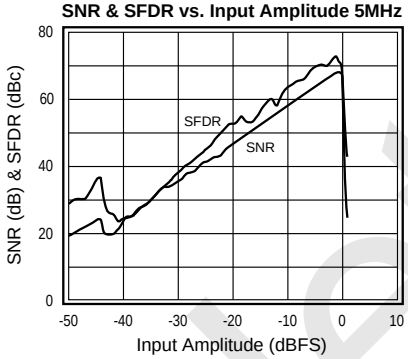
Output Spectrum 15MHz



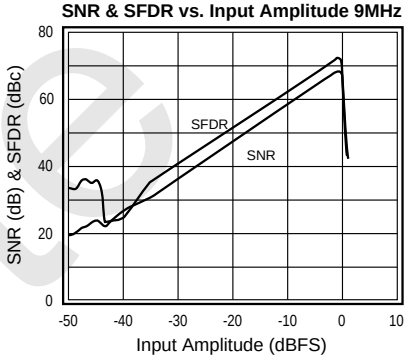
SNR & SFDR vs. Input Amplitude 1MHz



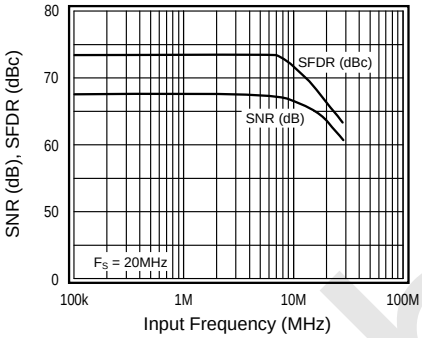
SNR & SFDR vs. Input Amplitude 5MHz



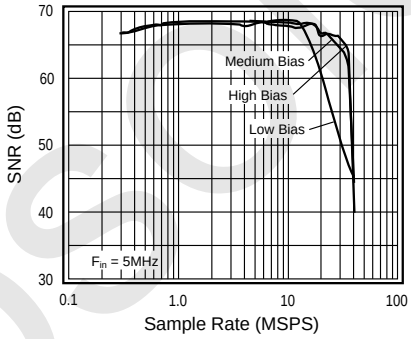
SNR & SFDR vs. Input Amplitude 9MHz



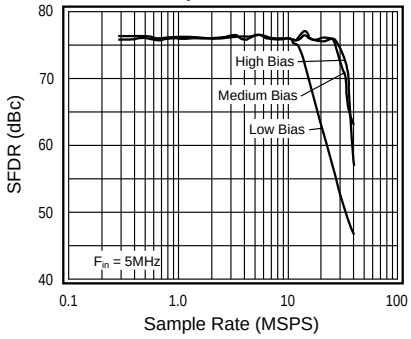
SNR & SFDR vs. Input Frequency



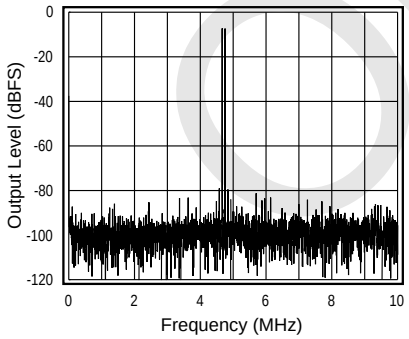
SNR vs. Sample Rate vs. Bias



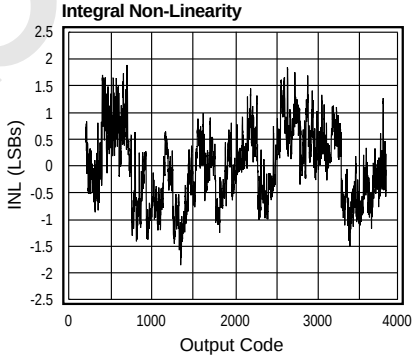
SFDR vs. Sample Rate vs. Bias



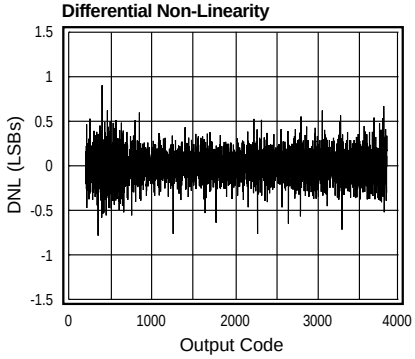
Two Tone Intermodulation Distortion



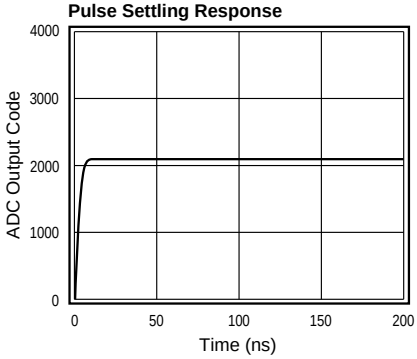
Integral Non-Linearity



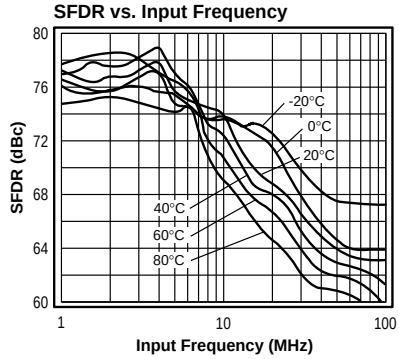
Differential Non-Linearity



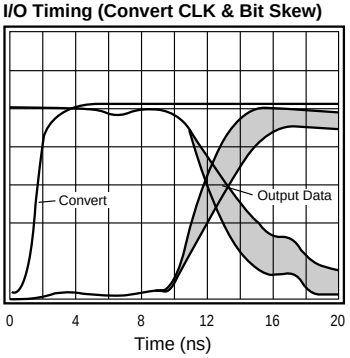
Pulse Settling Response



SFDR vs. Input Frequency



I/O Timing (Convert CLK & Bit Skew)



Recommended Operating Conditions

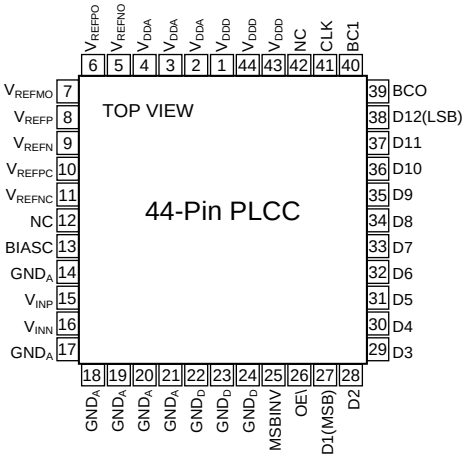
supply voltage (V_{DD})	+5V ±5%
differential voltage between any two GND's	<10mV
analog input voltage range (full scale)	1.25 – 3.25V
digital input voltage range	0 to V_{DD}
operating temperature range	0°C to 70°C
clock pulse-width high (C_{pwh})	> 25ns

Absolute Maximum Ratings*

supply voltage (V_{DD})	-0.5V to +7V
differential voltage between any two GND's	200mV
analog input voltage range	-0.5V to +V_{DD}
digital input voltage range	-0.5V to +V_{DD}
output short circuit duration (one pin to gnd)	infinite
junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10 sec

***NOTE:** Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Pinout & Pin Description and Usage



References (V_{REFN}, V_{REFP}, V_{REFNO}, V_{REFPO}, V_{REFNC}, V_{REFPC}, V_{REFMO})

To use the internal references, connect V_{REFPO} to V_{REFP} and V_{REFNO} to V_{REFN}. The nominal value for V_{REFPO} is 3.25V and for V_{REFNO} is 1.25V. V_{REFPC} and V_{REFNC} are internal reference points which should be bypassed to GND with a 0.1µF capacitor. V_{REFMO} is an output voltage that is equal to the mid point of the reference range and can be used to apply the appropriate offset to the analog inputs. For a more detailed discussion on references, see the paragraph on references in the applications section of this datasheet.

Analog Input (V_{INP}, V_{INN})

The analog input to the CLC949 is a differential signal applied to V_{INP} and V_{INN}. For more detail on driving the inputs, see the paragraphs in the applications section of this datasheet.

Power Supplies and Grounds (V_{DDA}, V_{DDD}, GND_A, GND_D)

The power and ground pins of the CLC949 are split into those that supply the analog portions of the integrated circuit (V_{DDA}, GND_A) and the digital portions of the chip (V_{DDD}, GND_D). If your system uses separate power and ground planes, then performance can be improved by making use of the appropriate pins. In many systems, the power pins will all be tied together and the GND pins will all be tied together. For more detailed discussion, please refer to the paragraph on power and grounds in the applications section of the databook.

Clock (CLK)

The CLK accepts a CMOS clock input. Samples are taken on the falling edges of the CLK and data emerges 6 1/2 clock cycles later, on to the rising edge of the CLK.

Output Data (D1-D12, MSBINV, OE\)

The data emerges from the CLC949 as CMOS level digital data on D1(MSB) through D12(LSB). The outputs can be put into a high impedance state by bringing OE\ high. There is an internal pulldown resistor so that if this input is left open, the output data is enabled. MSBINV will invert the MSB of the output data. With MSBINV in the high state, the output data is two's complement, when low, the output data format is offset binary. An internal pulldown resistor makes the output default to offset binary if MSBINV is left open.

Bias Control (BCO, BC1, BIASC)

The DC bias current of the CLC949 is controlled by three pins: BCO, BC1, and BIASC. BC0 and BC1 are digital CMOS inputs and set the bias current in accordance with the truth table below:

BC0	BC1	Bias Current	PD@10MSPS
0	0	Default: Med Bias (200µA)	200mW
1	0	Analog Mode	Variable
0	1	High Bias (400µA)	350mW
1	1	Low Bias (50µA)	75mW

In the analog mode, the user provides a bias current through the BIASC pin of the CLC949. As the bias current is increased, the power dissipation of the CLC949 is increased and the part becomes capable of increased conversion rates.

NC

No connection - leave these pins open.

CLC949 OPERATION

Application

In a high speed data acquisition system, the overall performance is often determined by the A/D converter and its surrounding circuitry. You should pay special attention to the data converter and its support circuitry if you want to obtain the best possible performance. The information on these pages is intended to help you design the circuitry surrounding the CLC949 in such a way as to achieve superior results. Additional information is available in the form of Comlinear applications notes. Especially useful are AD-01 and AD-02.

Circuit Description

The CLC949 ADC consists of an input Sample-and-Hold Amplifier (SHA) followed by a pipelined quantizer. Internal reference sources and output data latches complete the major functions required of an A/D converter. Digital error correction in the quantizer helps to provide accurate conversions of high speed dynamic signals. The speed of the analog circuitry is determined in part by the internal bias currents applied. The CLC949 allows you to make this important tradeoff between power and performance through settings on two digital control pins and for fine adjustments through the use of an external resistor.

Timing and CLK Generation

The falling edge of the CLK pulse causes the input sample-and-hold amplifier to transition into the hold mode. The sample is taken approximately 3ns after this falling edge. The digitized data is presented to the output latches 6 1/2 clock cycles later and is held until after the next rising edge of CLK. This timing is shown in the timing diagram, Figure 1.

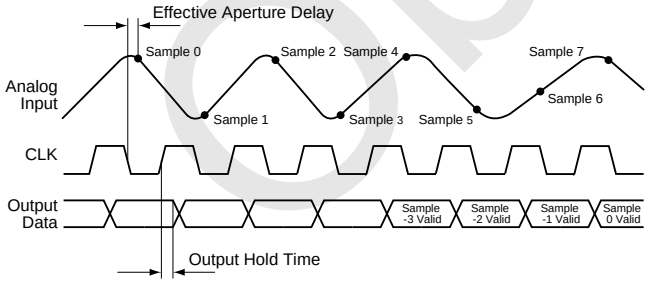


Figure 1: Timing Diagram

The CLC949 is designed to operate with a CMOS clock signal. To obtain the lowest possible noise when digitizing a high frequency input, more care must be taken in the generation of this clock than is usually accorded to CMOS Clocks. To minimize aperture jitter induced errors, the CLK needs to have as low a jitter as possible and as fast an edge rate as possible. To obtain a very low jitter clock from a sinusoidal source, the circuit shown in Figure 2 is recommended.

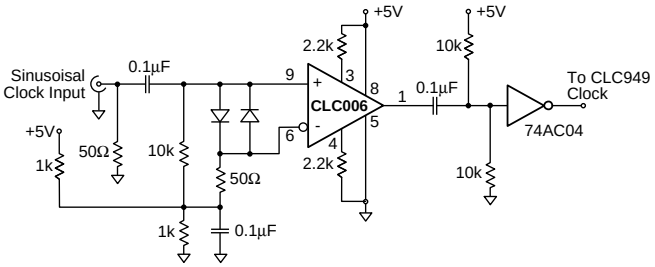


Figure 2: Clock Generation

Here the CLC006 cable driver is used as a comparator to generate a high speed clock. The CLC006 has less than 2ps of jitter and has rise and fall times less than 1ns. The CLC006 output is then buffered by a 74AC04 which maintains fast edge rates and provides CMOS levels for the CLC949. If there is excessive jitter in the CLK, then the digitized signal will exhibit an excessive amount of noise, especially for high frequency inputs. For a more detailed description of this phenomenon, please read the Comlinear Application Note AD-03.

In addition to the circuitry generating the clock, the layout of the clock distribution network can affect the overall performance of the converter. To obtain the best possible performance, a clock driver with very low output impedance and fast edge rates such as the 74AC04, should be placed as close as possible to the CLC949 clock input pin. Additional length in the circuit trace for the clock will cause an increase in the jitter seen by the converter. On the CLC949 evaluation board, the E949PCASM, there is less than 1/16th of an inch between the 74AC04 that is driving the clock input and the input to the CLC949. If the system has several CLC949s, and jitter is liable to generate problems, then use a separate clock driver for each CLC949. Each driver should be placed as close to the converter that it is driving as is practicable.

Driving the Differential Input

The CLC949 has a differential input with a common mode voltage of 2.25V. Since not all applications have a signal preconditioned in this manner there is often a need to do a single-ended-to-differential conversion and to add offset. In systems which do not need to be DC coupled, the best method for doing this is with an RF transformer such as the Minicircuits TMO1-1T. This is an RF transformer with a center tapped secondary which will operate over a frequency range of 50kHz to 200MHz. You can offset the input and split the phases simply by connecting the center tap to the mid scale reference output (V_{REFMO}) as shown in Figure 3.

This set up can be realized on the CLC949 evaluation board by enabling option 1. See E949PCASM data sheet for details. A transformer coupled input will allow the CLC949 to exhibit the best possible distortion performance for high frequency input signals.

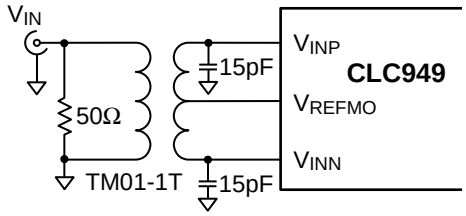


Figure 3: Transformer Coupled Input

Since the transformer response does not extend to DC it is not an effective solution for applications which require DC coupled inputs.

To drive the input of the CLC949, and retain DC information, an amplifier configuration is required. Comlinear suggests the use of the circuit shown in Figure 4. This circuit is used on the E949PCASM.

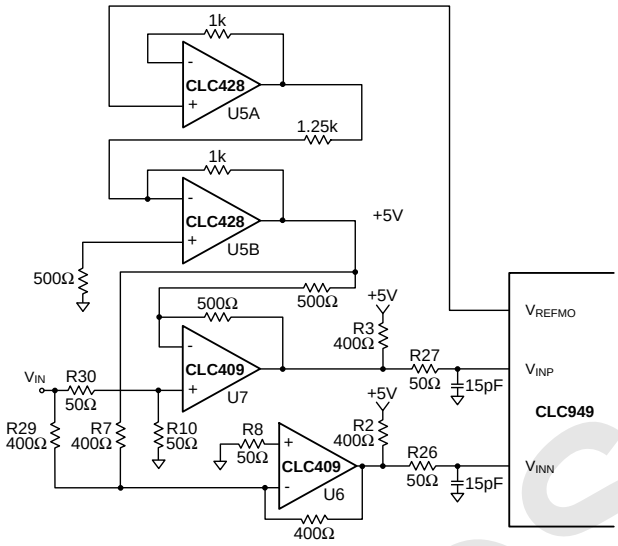


Figure 4: Amplifier Coupled Input

In this circuit U7 buffers the analog input with a gain of +1, and U6 buffers the input with a gain of -1. The circuit has been designed so that U6 and U7 have the same loop gain, thereby offering the best possible match of their AC characteristics. U5 is used to generate the required offset voltages which are summed into the input signal via U6 and U7. The CLC409 was selected for U6 and U7 due to its current feedback topology which allows for very low distortion even at high frequencies, and its excellent phase linearity. Phase match between U6 and U7 is critical for good pulse response. To generate the D.C. offsets, the CLC428 dual Op-amp was selected. The CLC428 is a voltage-feedback op amp with very good DC characteristics, and the large bandwidth makes the output impedance low over a wide range of frequencies, allowing good AC performance.

Regardless of how the input is driven, a small capacitor (15pF) should be added from the V_{INP} and V_{INN} terminals to GND. This will help to reduce the current transients that are generated by the CLC949 inputs during sampling.

Reference Generation

The CLC949 has internally generated reference voltages. To use these references, you must externally connect the reference inputs by shorting V_{REFPO} to V_{REFP} and V_{REFNO} to V_{REFN}. During the conversion cycle, the impedance on these four pins varies dynamically. To maintain stable biases on these pins you must bypass them with 0.1µF to GND. If you want to provide an external reference, then you have to be careful to provide low output impedance drivers to the V_{REFP} and V_{REFN} pins. Bypass capacitors on all reference pins are recommended for best performance.

Bias Control

One of the unique features of the CLC949 is that it allows you to set the internal bias current of the device. When designing an A/D converter a tradeoff is made between the amount of power dissipated and the performance. The CLC949 allows you to make this tradeoff yourself. The bias current is controlled by the pins BC0 and BC1. These two pins are digital input pins from which one of three discrete bias points may be selected (see truth table on page 4 of this datasheet) or an external bias may be provided through the analog bias control pin BIASC. If BC0 and BC1 are left open, they will drift low and provide the default bias condition which results in 220mW of dissipation at 20MHz sampling rate. The actual power dissipated by the device is a function of both the bias condition and the sample rate. The relationship between power and speed is shown for the three discrete bias points in Figure 5.

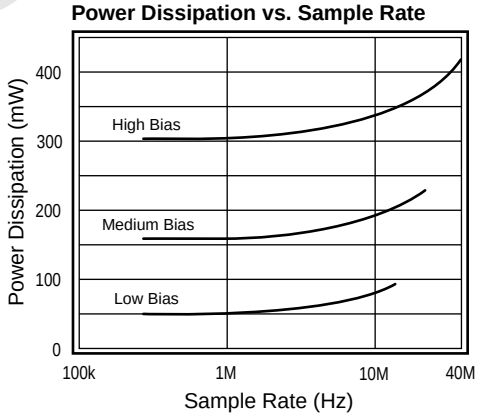


Figure 5: Power Dissipation vs. Sample Rate

As the bias is turned up, the ability of the CLC949 to handle high frequency inputs and the power dissipation of the CLC949 increases. To use the BIASC pin, attach a resistor from the pin to V_{DDA}. The current drawn by this resistor is mirrored in the device to set the internal bias currents. A smaller value resistor will result in higher bias currents and higher performance.Beyond a certain point, additional improvement is not seen, although power continues to increase. For this reason, it is recommended that bias setting resistors of less than 10K not be used. To generate the graph in Figure 6 a CLC949 was set to sample a signal 1dB below full scale

with a frequency of 1/2 the sample rate. The bias current was then turned up until the SNR was better than 65dB and the SFDR exceeded 72dB. The axis on the left shows the power that was dissipated by the device as a function of speed, whereas the other curve uses the axis on the right to show the resistor value required to obtain this bias.

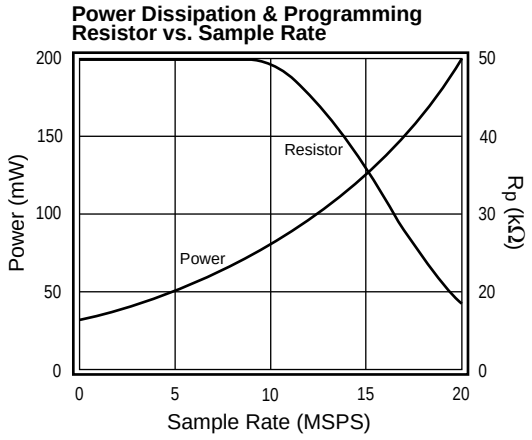


Figure 6: Power Dissipation & Programming Resistor vs. Sample Rate

Dynamic Power Down

In systems where you do not use the A/D converter continually, and low power consumption is a key requirement, the power to the CLC949 can be turned down while it is not being used. This is done through the use of the BIASC pin, and a programming resistor to the power supply. When the potential on this resistor is brought low, the part goes into a sleep mode which saves power. This can be accomplished by connecting the bias setting resistor to a CMOS gate as shown in Figure 7. In sleep mode the CLC949 will draw approximately 8mA, or 40mW on a 5V supply.

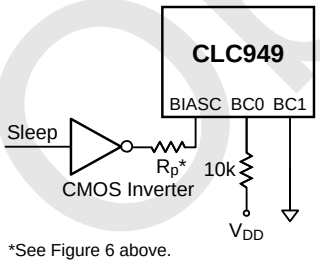


Figure 7: Dynamic Power Savings

PCB Layout

The keys to a successful CLC949 layout are a substantial low-impedance ground plane, short connections in and out of the data converter, and proper power supply decoupling. The use of a socket for the final design is not recommended but if one must be used during debug or prototyping, then Comlinear recommends the McKenzie #PLCC-44P-T-SMT socket which has low parasitic impedances. The traces from the clock source to the CLC949 should be as short as possible, if forced to put the clock driver more than a couple of centimeters away from the CLC949, then add a buffer for the clock right next to the CLC949.

There is an evaluation board available for the CLC949 (E949PCASM) This board can be used to quickly evaluate the performance of the CLC949 data converter. Use of this evaluation board as a model for your PCB layout is recommended. The schematic for this evaluation board is shown in Figure 8 on the following page. The board layout for the E949PCASM is shown in the E949PCASM datasheet.

Power Supplies, Grounding and Bypassing

To obtain the best possible performance from high speed devices, you must pay close attention to power supplies, bypassing and grounding. This applies not only to the A/D converter itself but to the entire system.

The recommended supply decoupling scheme for the CLC949 includes:

- One 0.01 to 0.033µF capacitor between each power pin and GND.
- One 6.8 to 10µF capacitor per board, placed no more than a few inches from the A/D connected between V_{DD} and GND.
- One 0.1µF capacitor from each of the reference inputs (V_{REFP}, V_{REFN}, V_{REFPC}, V_{REFNC}) to GND.
- If the board has supplies that include excessive digital switching noise, then ferrite beads in series with the power feed to the A/D should also be included.
- Proper bypassing of all other integrated circuits on the board, especially digital logic I.C.s.

Package Thermal Resistance

Package	θ_{JC}	θ_{JA}
44-pin PLCC	10°C/W	35°C/W

Ordering Information

Model	Temperature Range	Description
CLC949ACQ	0°C to +70°C	44-pin PLCC
CLC949AJQ	-40°C to +85°C	44-pin PLCC

Power Requirements

	Typ	Units
V_{cc} = +5V, 5MSPS, Low Bias	65	mW
V_{cc} = +5V, 20MSPS, Med Bias	220	mW
V_{cc} = +5V, 30MSPS, High Bias	400	mW

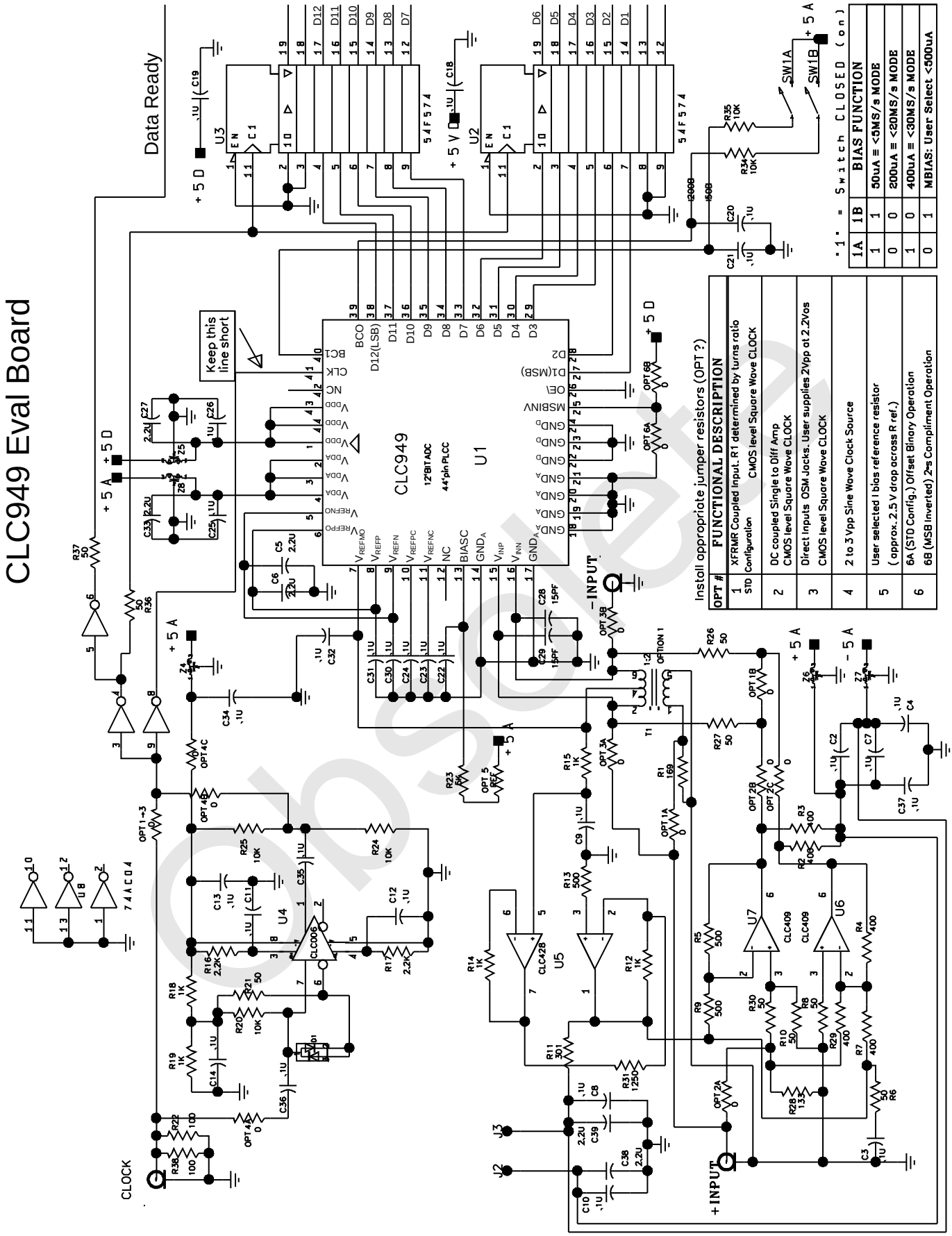


Figure 8: CLC949 Evaluation Board

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
E-mail: europe.support.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Francais Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block
Ocean Centre, 5 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408