1.5V Drive Pch MOSFET + PNP TRANSISTOR

QS8F2

●Structure
Silicon P-channel MOSFET/
PNP TRANSISTOR

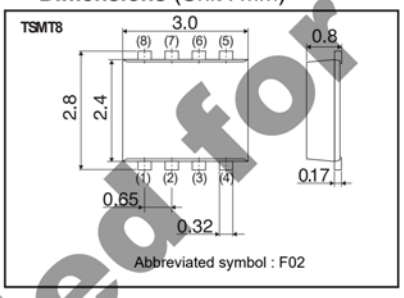
●Features
1) Low on-resistance.
2) High power package(TSMT8).
3) Low voltage drive(1.5V drive).

●Application
Switching

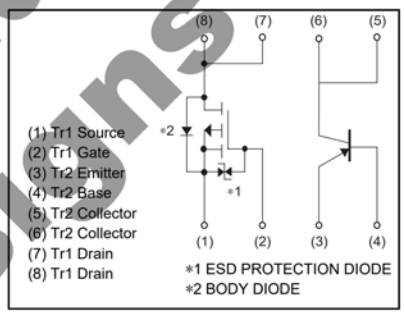
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS8F2		O

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta = 25°C)

<Tr1(Pch MOSFET)>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	−12	V
Gate-source voltage		V_{GSS}	±10	V
Drain current	Continuous	I_D	±2.5	A
	Pulsed	I_{DP}*	±10	A
Source current (Body Diode)	Continuous	I_S	−1	A
	Pulsed	I_{SP}*	−10	A

* Pw≤10μs, Duty cycle≤1%

<Tr2(PNP Tr)>

Parameter		Symbol	Limits	Unit
Collector-Emitter voltage		V_{CEO}	−30	V
Collector-Base voltage		V_{CBO}	−30	V
Emitter-Base voltage		V_{EBO}	−6	V
Collector current	Continuous	I_C	−2	A
	Pulsed	I_{CP}*	−4	A

* Pw=1ms, Pulsed

<MOSFET and Di>

Parameter	Symbol	Limits	Unit
Power dissipation	P_D *	1.5	W / TOTAL
		1.25	W / ELEMENT
Junction temperature	Tj	150	°C
Range of storage temperature	Tstg	−55 to +150	°C

* Mounted on a ceramic board.

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● **Electrical characteristics** (Ta = 25°C)

<Tr1(Pch MOSFET)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	V_{GS}=±10V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	−12	-	-	V	I_D=−1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}		-	−1	μA	V_{DS}=−12V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	−0.3	-	−1.0	V	V_{DS}=−6V, I_D=−1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	-	44	61	mΩ	I_D=−2.5A, V_{GS}=−4.5V
		-	60	84		I_D=−1.2A, V_{GS}=−2.5V
		-	81	121		I_D=−1.2A, V_{GS}=−1.8V
		-	110	220		I_D=−0.5A, V_{GS}=−1.5V
Forward transfer admittance	$\|Y_{fs}\|$*	3.5	-	-	S	V_{DS}=−6V, I_D=−2.5A
Input capacitance	C_{iss}	-	1350	-	pF	V_{DS}=−6V
Output capacitance	C_{oss}	-	130	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	125	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$*	-	9	-	ns	I_D=−1.2A, V_{DD} −6V
Rise time	t_r *	-	35	-	ns	V_{GS}=−4.5V
Turn-off delay time	$t_{d(off)}$*	-	130	-	ns	R_L=5Ω
Fall time	t_f *	-	85	-	ns	R_G=10Ω
Total gate charge	Q_g *	-	13	-	nC	I_D=−2.5A,
Gate-source charge	Q_{gs} *	-	2.5	-	nC	V_{DD} −6V
Gate-drain charge	Q_{gd} *	-	2.0	-	nC	V_{GS}=−4.5V

*Pulsed

●**Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}*	-	-	−1.2	V	I_s=−2.5A, V_{GS}=0V

*Pulsed

<Tr2(PNP Tr)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-Emitter breakdown voltage	BV_{CEO}	−30	-	-	V	I_C=−1mA
Collector-Base breakdown voltage	BV_{CBO}	−30	-	-	V	I_C=−10μA
Emitter-Base breakdown voltage	BV_{EBO}	−6	-	-	V	I_E=−10μA
Collector cut-off current	I_{CBO}	-	-	−100	nA	V_{CB}=−30V
Emitter cut-off current	I_{EBO}	-	-	−100	nA	V_{EB}=−6V
Collector-Emitter saturation voltage	$V_{CE(sat)}$*	-	−180	−370	mV	I_C=−1.5A , I_B=−75mA
DC current gain	h_{FE}	270	-	680	-	V_{CE}=−2V,I_C=−200mA
Transistor frequency	f_T	-	280	-	MHz	V_{CE}=−2V,I_E=200mA, f=100MH z
Collector output capacitance	C_{ob}	-	20	-	pF	V_{CB}=−10V,I_E=0mA, f=1MHz

*Pulsed

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●**Electrical characteristic curves** (Ta=25°C)

〈Tr.1〉

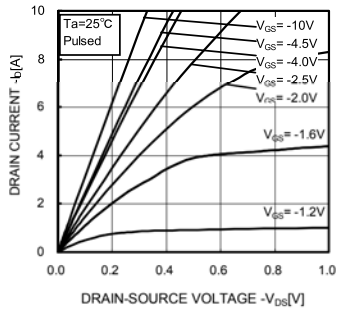

Fig.1 Typical Output Characteristics(Ⅰ)

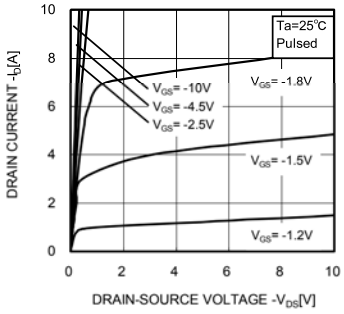

Fig.2 Typical Output Characteristics(Ⅱ)

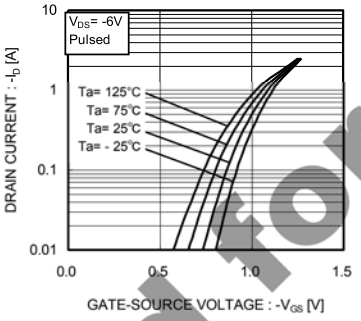

Fig.3 Typical Transfer Characteristics

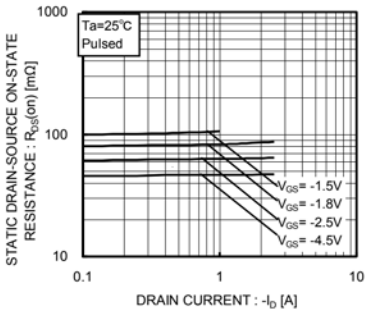

Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(Ⅰ)

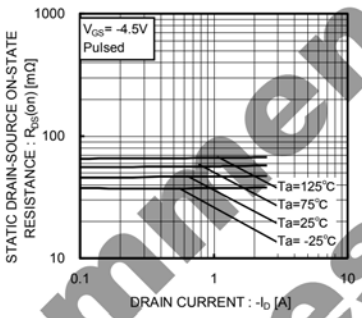

Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(Ⅱ)

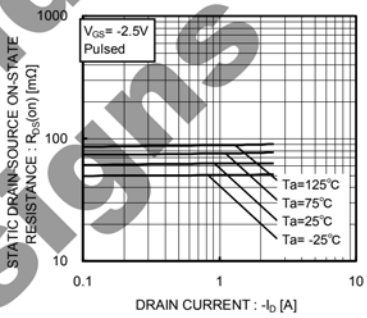

Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

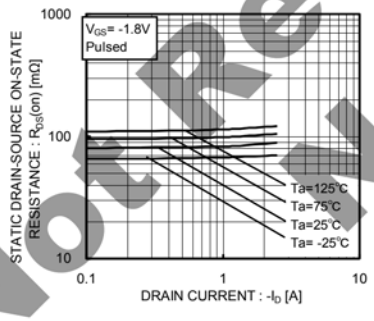

Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

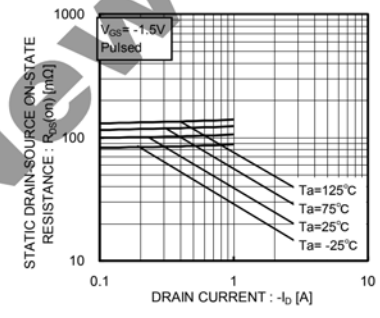

Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

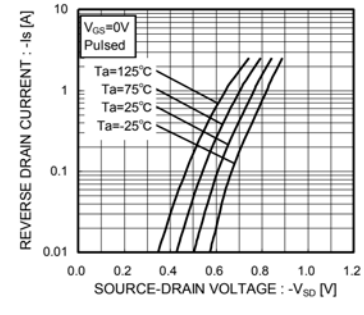

Fig.9 Reverse Drain Current vs. Sourse-Drain Voltage

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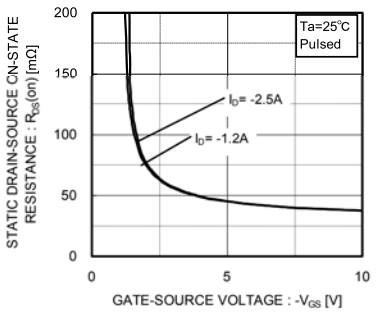


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

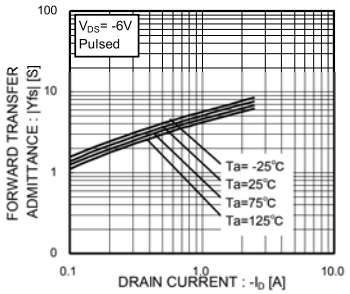


Fig.11 Forward Transfer Admittance vs. Drain Current

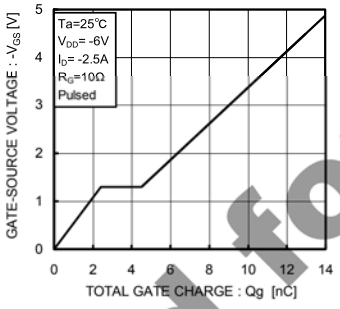


Fig.12 Dynamic Input Characteristics

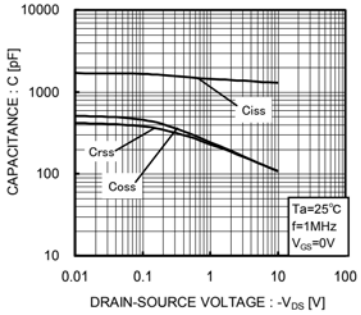


Fig.13 Typical Capacitance vs. Drain-Source Voltage

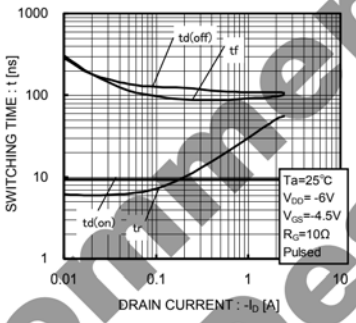
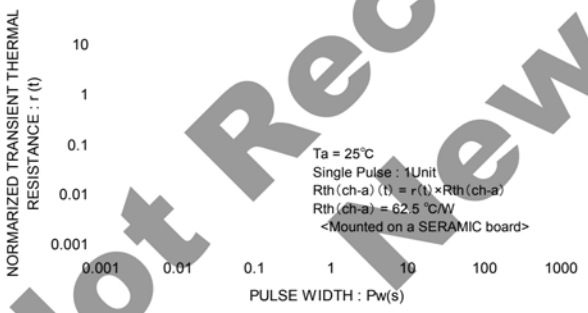


Fig.14 Switching Characteristics



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〈Tr.2〉

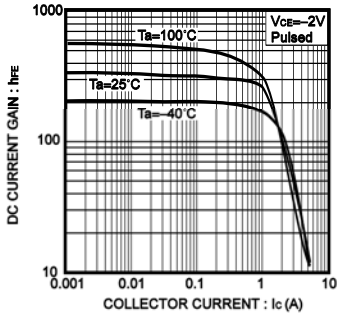

Fig.1 DV current gain vs. collector current

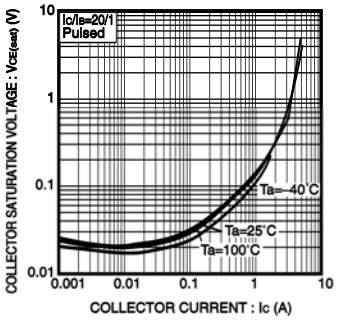

Fig.2 Collector-emitter saturation voltage vs. collector current

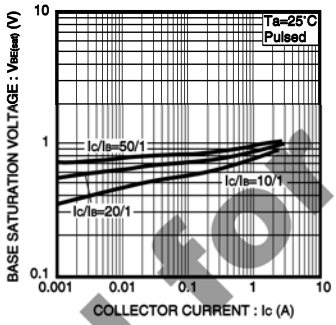

Fig.3 Base-emitter saturation voltage vs. collector current

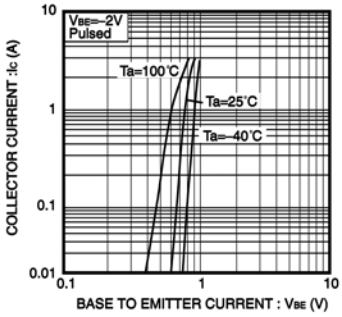

Fig.4 Grounded emitter propagation characteristics

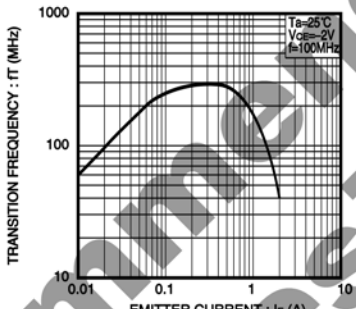

Fig.5 Gain bandwidth product vs. emitter curent

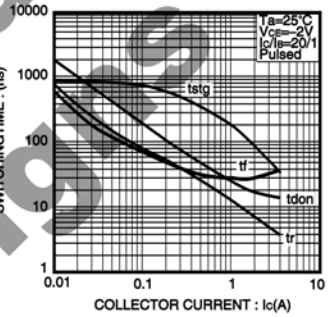

Fig.6 Switching time

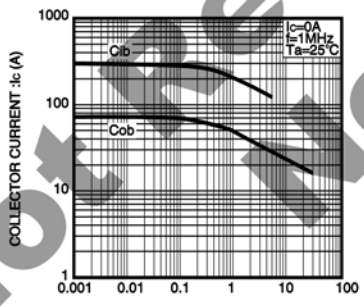

Fig.7 Collector output capacitance vs. collector-base voltage Emitter input capacitance vs. emitter-base voltage

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● **Measurement circuits**

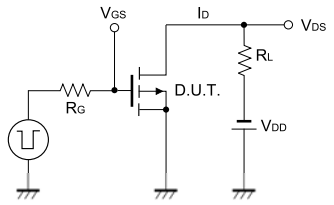

Fig.1-1 Switching Time Measurement Circuit

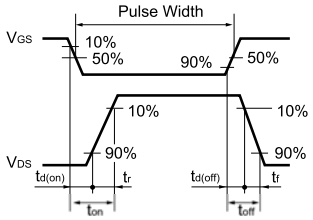

Fig.1-2 Switching Waveforms

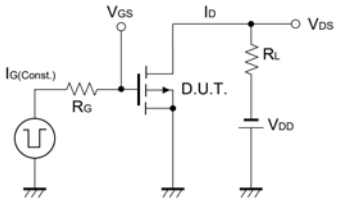

Fig.2-1 Gate Charge Measurement Circuit

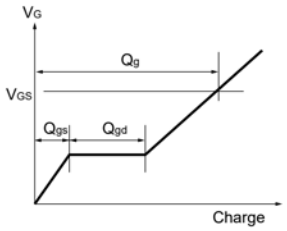

Fig.2-2 Gate Charge Waveform

● **Notice**

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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