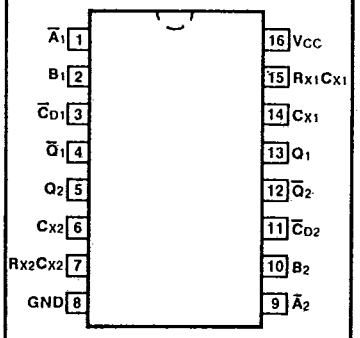
54/74123

DUAL RETRIGGERABLE RESETTABLE MULTIVIBRATOR

CONNECTION DIAGRAM
PINOUT A

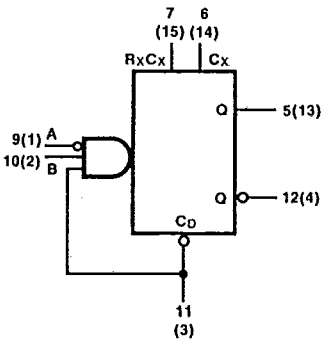


DESCRIPTION — Each half of the '123 features retriggerable capability, complementary dc level triggering and overriding Direct Clear. When a circuit is in the quasi-stable (delay) state, another trigger applied to the inputs (per the Truth Table) will cause the delay period to start again, without disturbing the outputs. By repeating this process, the output pulse period (Q HIGH, $\overline{Q}$ LOW) can be made as long as desired. Alternatively, a delay period can be terminated at any time by a LOW signal on $\overline{C}_D$, which also inhibits triggering. An internal connection from $\overline{C}_D$ to the input gate makes it possible to trigger the circuit by a positive-going signal on $\overline{C}_D$, as shown in the Truth Table. For timing capacitor values greater than 1000 pF, the output pulse width is defined as follows.

$$t_w = 0.28\ R_X C_X\ (1.0 + 0.7/R_X)$$

Where t_w is in ns, R_X is in kΩ and C_X is in pF.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74123PC		9B
Ceramic DIP (D)	A	74123DC	54123DM	6B
Flatpak (F)	A	74123FC	54123FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

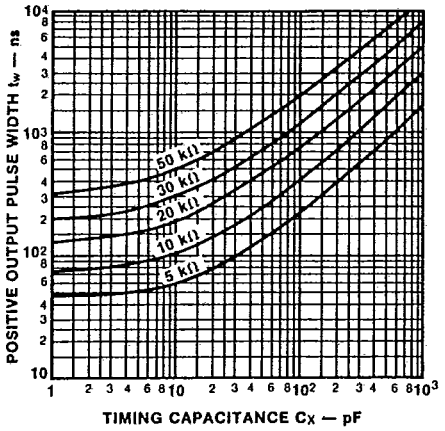
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{A}_1$, $\overline{A}_2$	Trigger Inputs (Active Falling Edge)	1.0/1.0
B_1, B_2	Trigger Inputs (Active Rising Edge)	1.0/1.0
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.0/2.0
Q_1, Q_2	Positive Pulse Output	20/10
$\overline{Q}_1$, $\overline{Q}_2$	Negative Pulse Output	20/10

TRIGGERING TRUTH TABLE

INPUTS			RESPONSE
A	B	$\overline{C}_D$	
X	X	L	No Trigger
↘	L	X	No Trigger
↘	H	H	Trigger
H	↗	X	No Trigger
L	↗	H	Trigger
L	H	↗	Trigger

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

PULSE WIDTH vs R_X AND C_X



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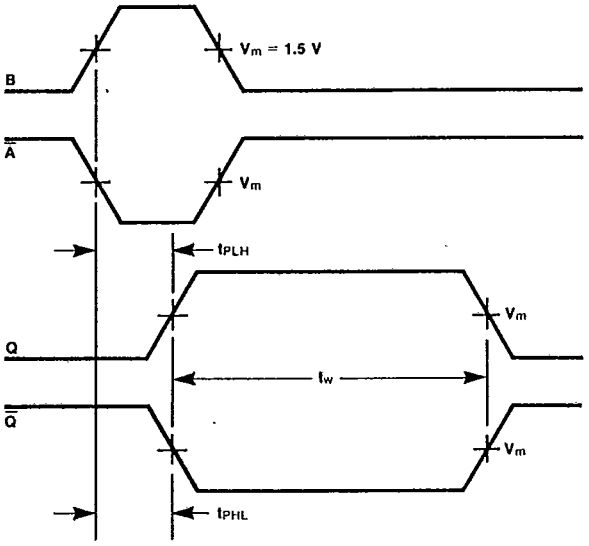

Fig. a.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	-10	-40	mA	V_{CC} = Max
I_{CC}	Power Supply Current		66	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 C_L = 15 pF R_L = 400 Ω Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay B to Q		28	ns	C_X = 0 pF, R_X = 5 kΩ Fig. 3-1, Fig. a
t_{PLH}	Propagation Delay $\overline{A}$ to Q		33	ns	
t_{PHL}	Propagation Delay B to $\overline{Q}$		36	ns	
t_{PHL}	Propagation Delay $\overline{A}$ to $\overline{Q}$		40	ns	
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ to $\overline{Q}$		40	ns	C_X = 0 pF, R_X = 5 kΩ Figs. 3-1, 3-10
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ to Q		27	ns	
$t_{w(min)}$	Pulse Width with Zero Timing Capacitor		65	ns	C_X = 0 pF, R_X = 5 kΩ Fig. 3-1, Fig. a
t_w	Pulse Width with External Timing Components	2.76	3.37	μs	C_X = 1000 pF, R_X = 10 kΩ Fig. 3-1, Fig. a

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
t_w	Trigger Pulse Width		40		ns	Over Operating Temperature Range
R_X	External Timing Resistor	XC	5.0	50	kΩ	
		XM	5.0	25		
C_X	External Timing Capacitor		No Restrictions		pF	