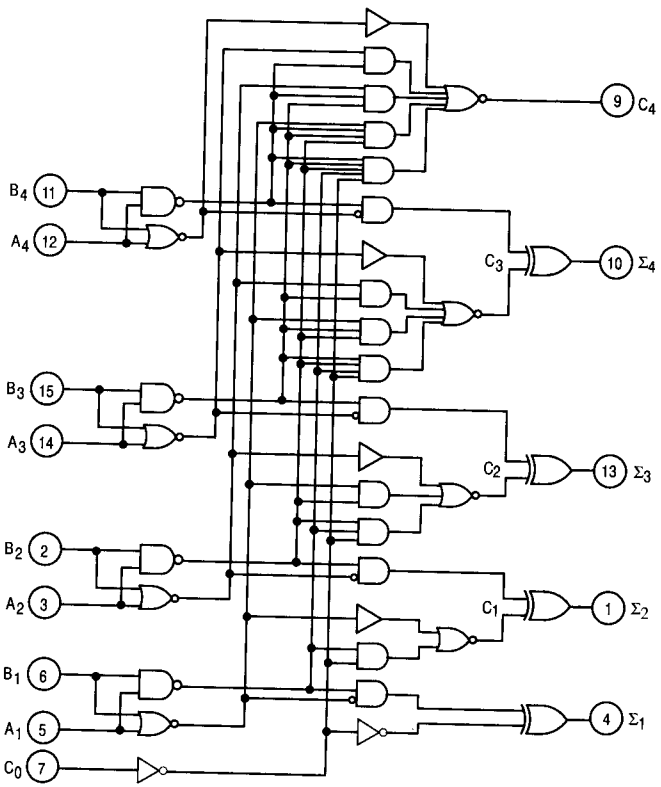
MOTOROLA

4-Bit Full Adder With Fast Carry

ELECTRICALLY TESTED PER:
MIL-M-38510/31202

The 54LS283 is a high-speed 4-Bit Binary full adder with internal carry lookahead. It accepts two 4-bit binary words (A_1–A_4, B_1–B_4) and a Carry input (C_0). It generates the binary Sum output ($\Sigma_1 - \Sigma_4$) and the Carry output (C_4) from the most significant bit. The 'LS283 will operate with either active-HIGH or active-LOW operands (positive or negative logic).

LOGIC DIAGRAM



Military 54LS283

AVAILABLE AS:

1) JAN: JM38510/31202BXA
2) SMD: 7604301
3) 883: 54LS283/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
Σ_2	1	1	2	V_{CC}
B_2	2	2	3	V_{CC}
A_2	3	3	4	V_{CC}
Σ_1	4	4	5	V_{CC}
A_1	5	5	7	V_{CC}
B_1	6	6	8	V_{CC}
C_0	7	7	9	V_{CC}
GND	8	8	10	GND
C_4	9	9	12	V_{CC}
Σ_4	10	10	13	V_{CC}
B_4	11	11	14	V_{CC}
A_4	12	12	15	V_{CC}
Σ_3	13	13	17	V_{CC}
A_3	14	14	18	V_{CC}
B_3	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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FUNCTIONAL DESCRIPTION

The 'LS283 adds two 4-bit binary words (A plus B) plus the incoming carry C_0. The binary sum appears on the Sum ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_4) outputs.

$C_0+(A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4)=\Sigma_1+2\Sigma_2 + 4\,\Sigma_3 + 8\,\Sigma_4 + 16\,C_4$ Where: (+) = plus

Due to the symmetry of the binary add function the 'LS283 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

FUNCTION TABLE

$C_{(n-1)}$	A_n	B_n	Σ_n	C_n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C_1-C_3 are generated internally
C_0 is an external input
C_4 is an output generated internally

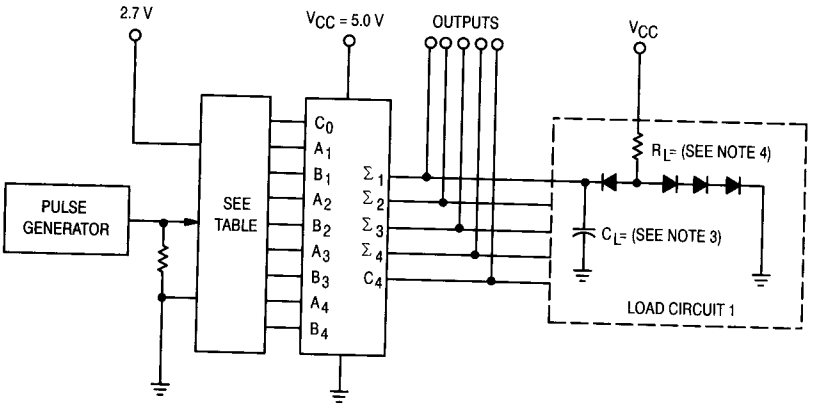
Pin Name		Loading (Note a)	
		HIGH	LOW
A_1-A_4	A Operand Inputs	1.0 U.L.	0.5 U.L.
B_1-B_4	B Operand Inputs	1.0 U.L.	0.5 U.L.
C_0	Carry Output	0.5 U.L.	0.25 U.L.
Σ_1-Σ_4	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C_4	Carry Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. One TTL Unit Load (U.L.) = 40 µA HIGH/ 1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

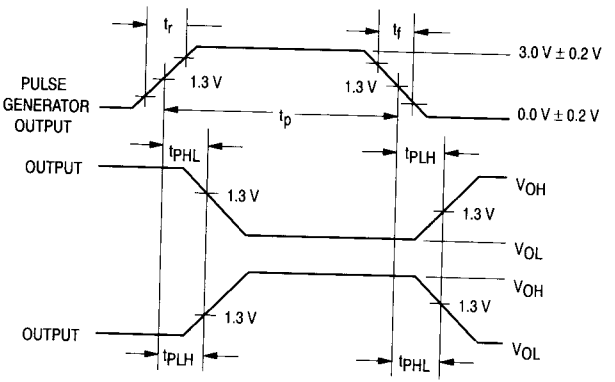
	C_0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active High	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active Low	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Interchanging inputs of equal weight does not effect the operation, thus C_0, A_1, B_1, can be arbitrarily assigned to pins 7, 5 or 3.
(10 + 9 = 19)
(carry + 5 + 6 = 12)

AC TEST CIRCUIT



SWITCHING WAVEFORMS



NOTES:

1. The pulse generator has the following characteristics: PRR ≤ 1.0 MHz, t_r ≤ 15 ns, t_f ≤ 6.0 ns, t_p = 200 ns and Z_{OUT} ≈ 50 Ω.
2. C_L = 50 pF ± 10%, including scope probe, wiring capacitance without package in test fixture.
3. All diodes are 1N3064 or equivalent.
4. R_L = 2.0 kΩ ± 5.0%.
5. Terminal conditions (pins not designated may be high ≥ 2.0 V, or low ≤ 0.7 V, or open).

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA, V_{IH} = 2.0 V (all inputs).
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V (all inputs).
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
$I_{IH(C0)}$	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
$I_{IHH(C0)}$	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IH}	Logical "1" Input Current		40		40		40	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other input = GND.
I_{IHH}	Logical "1" Input Current		200		200		200	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other input = GND.
I_{OS}	Output Short Circuit Current	− 15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), V_{OUT} = GND.
I_{IL}	Logical "0" Input Current	− 0.3	− 0.76	− 0.3	− 0.76	− 0.3	− 0.76	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other input = 5.5 V.
$I_{IL(C0)}$	Logical "0" Input Current	− 0.15	− 0.38	− 0.15	− 0.38	− 0.15	− 0.38	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs are open.
I_{CCL}	Power Supply Current Off		39		39		39	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs).
I_{CCZ}	Power Supply Current Off		34		34		34	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (A inputs only), other inputs = GND
I_{CCH}	Power Supply Current Off		34		34		34	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay C_0 to Any Σ Output	5.0 —	35 24	5.0 —	40 35	5.0 —	40 35	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH1} t_{PLH1}	Propagation Delay C_0 to Any Σ Output	5.0 —	30 24	5.0 —	39 34	5.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL2} t_{PHL2}	Propagation Delay C_0 to Any Σ Output	5.0 —	35 24	5.0 —	40 35	5.0 —	40 35	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH2} t_{PLH2}	Propagation Delay C_0 to Any Σ Output	5.0 —	30 24	5.0 —	39 34	5.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL3} t_{PHL3}	Propagation Delay C_0 to Any Σ Output	5.0 —	35 24	5.0 —	40 35	5.0 —	40 35	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH3} t_{PLH3}	Propagation Delay C_0 to Any Σ Output	5.0 —	30 24	5.0 —	39 34	5.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL4} t_{PHL4}	Propagation Delay C_0 to Any Σ Output	5.0 —	35 24	5.0 —	40 35	5.0 —	40 35	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH4} t_{PLH4}	Propagation Delay C_0 to Any Σ Output	5.0 —	30 24	5.0 —	39 34	5.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL5}	Propagation Delay /Data-Output C_0 to C_4	5.0	28	5.0	35	5.0	35	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH5}	Propagation Delay /Data-Output C_0 to C_4	5.0	25	5.0	32	5.0	32	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PHL6}	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH6}	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PHL7}	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH7}	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PHL8}	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH8}	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PHL9}	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH9}	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.

NOTE:
1. The limit specified for C_L = 15 pF is guaranteed but not tested.