



## DATASHEET

# 2G bits DDR3L SDRAM

**D1216ECMDXGJD(I)-U (128M words x 16 bits)**

**D1216ECMDXGME(I)-U (128M words x 16 bits)**

### Specifications

- Density: 2G bits
- Organization
  - 16M words x 16 bits x 8 banks
- Package
  - 96-ball FBGA
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply: 1.35V (Typ)
  - VDD, VDDQ = 1.283V to 1.45V
  - Backward compatible for VDD, VDDQ=1.5V ± 0.075V
- Data rate
  - 2133Mbps/1866Mbps/1600Mbps/1333Mbps (max.)
- 2KB page size
  - Row address: A0 to A13
  - Column address: A0 to A9
- Eight internal banks for concurrent operation
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- Burst type (BT):
  - Sequential (8, 4 with BC)
  - Interleave (8, 4 with BC)
- Programmable /CAS (Read) Latency (CL)
- Programmable /CAS Write Latency (CWL)
- Precharge: auto precharge option for each burst access
- Driver strength: RZQ/7, RZQ/6 (RZQ = 240Ω)
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  - Average refresh period
  - 7.8μs at 0°C ≤ Temperature ≤ +85°C
  - 3.9μs at +85°C ≤ Temperature ≤ +105°C
- Operating Case temperature range
  - 0°C to +95°C (Commercial Temperature)
  - -40°C to +95°C (Industrial Temperature)

### Features

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- Automatic self refresh (ASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
  - Normal/extended
- Programmable Output driver impedance control

## Revision History

Revision No.	History	Release date	Remark
1.0	Initial release	Feb 2019	
1.1	Second release	Mar 2019	Add Data rate 2133 and I-temp
1.2	Third release	Sept 2019	Add P/N and A-temp
1.3	Fourth release	Nov 2019	Revise file name
1.4	Fifth release	Nov 2019	Add P/N
1.5	Sixth release	Dec 2019	Add P/N
1.6	Seventh release	Sept 2022	Remove x8 and automotive P/N
1.7	Eighth Release	June 2023	Added Kingston Contact Info

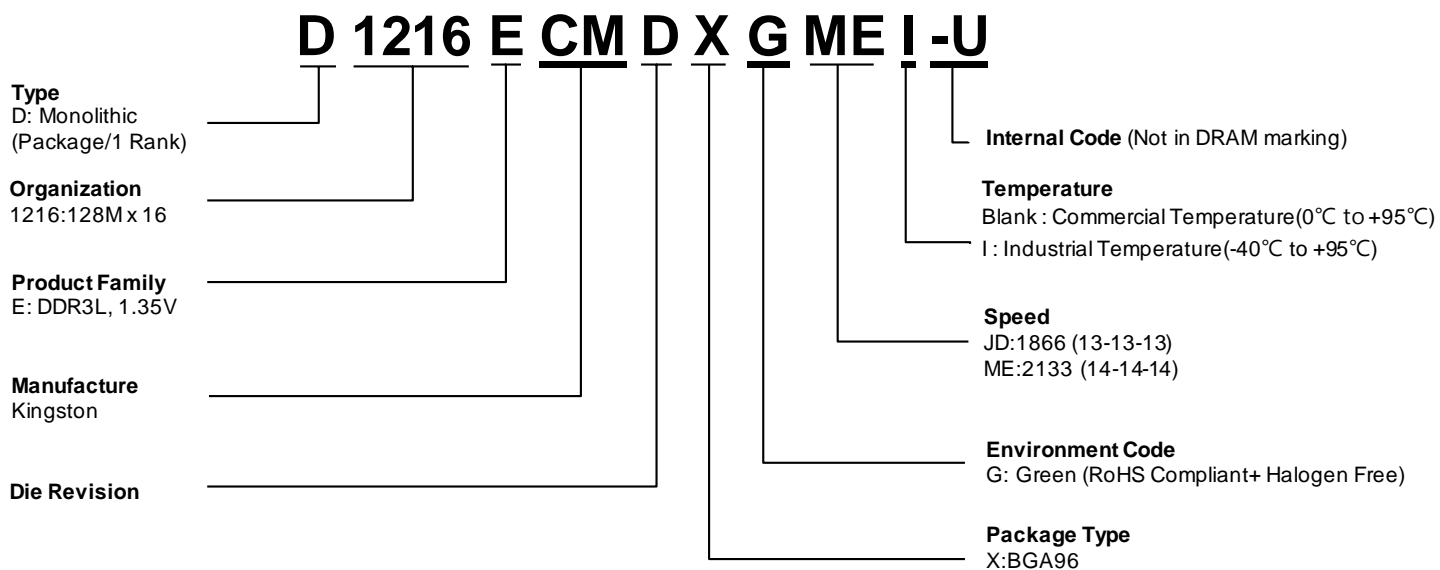
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## Ordering Information

Part Number	Die revision	Organization (words x bits)	Internal Banks	JEDEC speed bin (CL-tRCD-tRP)	Package
D1216ECMDXGJD-U D1216ECMDXGJDI-U	D	128M x 16	8	DDR3L-1866 (13-13-13)	96-ball FBGA
D1216ECMDXGME-U D1216ECMDXGMEI-U	D	128M x 16	8	DDR3L-2133 (14-14-14)	96-ball FBGA

### Part Number

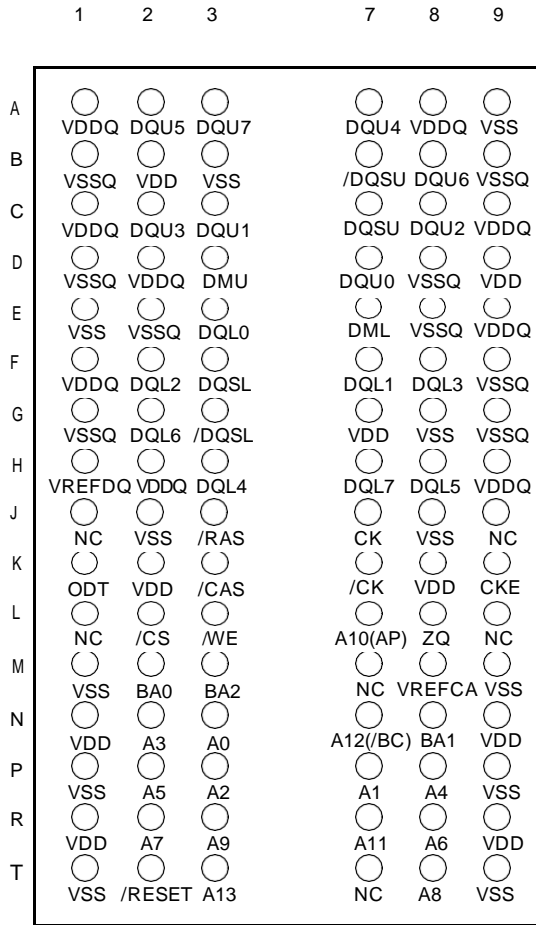


# Pin Configurations

## Pin Configurations ( x16 configuration)

/xxx indicates active low signal

96-ball FBGA



(Top view)

Pin	Function
A0 to A13 <sup>2</sup>	Address inputs A10(AP) : Auto precharge A12(BC) : Burst chop
BA0 to BA2 <sup>2</sup>	Bank select
DQU0 to DQU7 DQL0 to DQL7	Data input/output
DQSU, /DQSU DQSL, /DQSL	Differential data strobe
/CS <sup>2</sup>	Chip select
/RAS, /CAS, /WE <sup>2</sup>	Command input
CKE <sup>2</sup>	Clock enable
CK, /CK	Differential clock input
DMU, DML	Write data mask
ODT <sup>2</sup>	ODT control

Pin name	Function
/RESET <sup>2</sup>	Active low asynchronous reset
VDD	Supply voltage for internal circuit
VSS	Ground for internal circuit
VDDQ	Supply voltage for DQ circuit
VSSQ	Ground for DQ circuit
VREFDQ	Reference voltage for DQ
VREFCA	Reference voltage for CA
ZQ	Reference pin for ZQ calibration
NC <sup>1</sup>	No connection

Notes : 1. Not internally connected with die.

2. Input only pins (address, command, CKE, ODT and /RESET) do not supply termination.

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## 1. Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.

### 1.1 Absolute Maximum Ratings

**Table 1: Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	-0.4 to +1.80	V	1, 3
Power supply voltage for output	VDDQ	-0.4 to +1.80	V	1, 3
Input voltage	VIN	-0.4 to +1.80	V	1
Output voltage	VOUT	-0.4 to +1.80	V	1
Reference voltage	VREFCA	0.49 to $0.51 \times VDD$	V	3
Reference voltage for DQ	VREFDQ	0.49 to $0.51 \times VDDQ$	V	3
Storage temperature	Tstg	-55 to +100	°C	
Power dissipation	PD	1.0	W	1
Short circuit output current	IOUT	50	mA	1

- Notes: 1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be no greater than  $0.6 \times VDDQ$ . When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

**Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

### 1.2 Operating Temperature Condition

**Table 2: Operating Temperature Condition**

Parameter	Rating	Unit	Notes
Commercial temperature	0 to +95	°C	1, 2, 3
Industrial temperature	-40 to +95	°C	1, 2, 3

- Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM temperature must be maintained between 0°C to +85°C for commercial temperature, -40°C to +85°C for industrial temperature under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C to +95°C for commercial/industrial operating temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
- a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9µs. (This double refresh requirement may not apply for some devices.)
  - b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

### 1.3 Recommended DC Operating Conditions

**Table 3-a: Recommended DC Operating Conditions, DDR3L Operation.**

Parameter	Symbol	min	typ	max	Unit	Notes
Supply voltage	VDD	1.283	1.35	1.45	V	1, 2, 3
Supply voltage for DQ	VDDQ	1.283	1.35	1.45	V	1, 2, 3

- Notes: 1. Under all conditions VDDQ must be less than or equal to VDD.  
 2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.  
 3. Commercial Temperature 0°C to +95°C, Industrial Temperature -40°C to +95° and Automotive Temperature -40°C to +105°C.

**Table 3-b: Recommended DC Operating Conditions, DDR3 Operation.**

Parameter	Symbol	min	typ	max	Unit	Notes
Supply voltage	VDD	1.425	1.5	1.575	V	1, 2, 3
Supply voltage for DQ	VDDQ	1.425	1.5	1.575	V	1, 2, 3

- Notes: 1. Under all conditions VDDQ must be less than or equal to VDD.  
 2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.  
 3. Commercial Temperature 0°C to +95°C, Industrial Temperature -40°C to +95° and Automotive Temperature -40°C to +105°C.



## 1.4 IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined.

The figure Measurement Setup and Test Load for IDD and IDDQ Measurements shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Note:IDDQ values cannot be directly used to calculate I/O power of the DDR3 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in correlation from simulated channel I/O power to actual channel I/O power supported by IDDQ measurement.

For IDD and IDDQ measurements, the following definitions apply:

- L and 0:  $V_{IN} \leq V_{IL(AC)max}$
- H and 1:  $V_{IN} \geq V_{IH(AC)min}$
- MID-LEVEL: defined as inputs are  $V_{REF} = V_{DDQ} / 2$
- FLOATING: don't care or floating around  $V_{REF}$ .
- Timings used for IDD and IDDQ measurement-loop patterns are provided in Timings used for IDD and IDDQ Measurement-Loop Patterns table.
- Basic IDD and IDDQ measurement conditions are described in Basic IDD and IDDQ Measurement Conditions table.

Note:The IDD and IDDQ measurement-loop patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.

- Detailed IDD and IDDQ measurement-loop patterns are described in IDD0 Measurement-Loop Pattern table through IDD7 Measurement-Loop Pattern table.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting.  
RON =  $RZQ/7$  (34 $\Omega$  in MR1);  
Qoff = 0B (Output Buffer enabled in MR1);  
RTT\_Nom =  $RZQ/6$  (40 $\Omega$  in MR1);  
RTT\_WR =  $RZQ/2$  (120 $\Omega$  in MR2);  
TDQS Feature disabled in MR1
- Define D = {/CS, /RAS, /CAS, /WE} : = {H, L, L, L}
- Define /D = {/CS, /RAS, /CAS, /WE} : = {H, H, H, H}

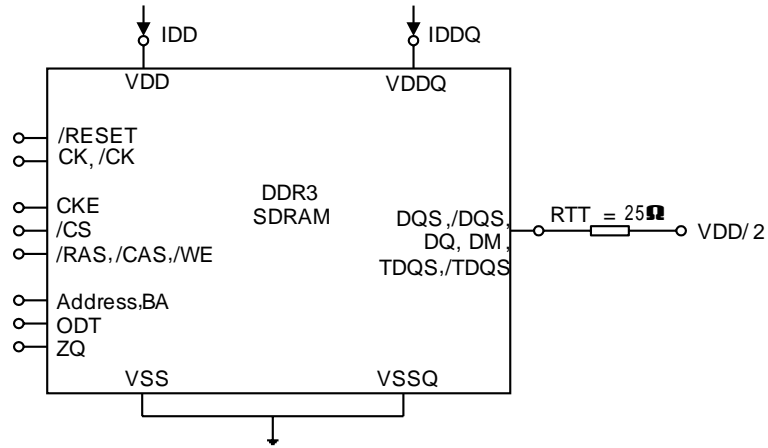


Figure 1: Measurement Setup and Test Load for IDD and IDDQ Measurements

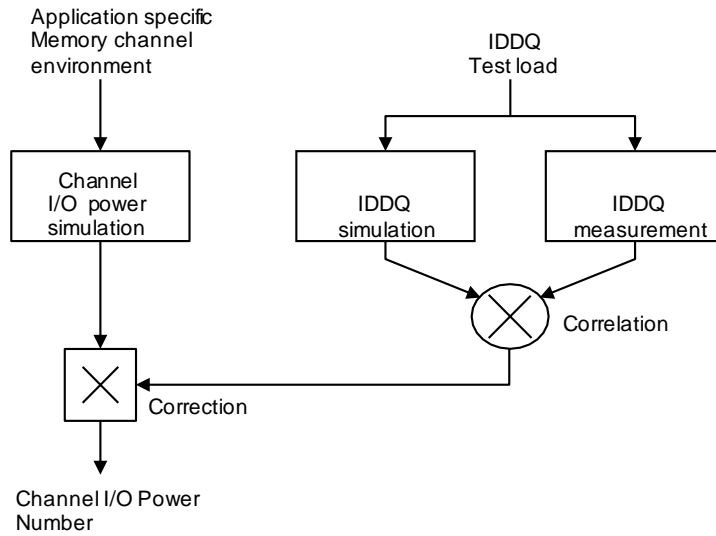


Figure 2: Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement

### 1.4.1 Timings Used for IDD and IDDQ Measurement-Loop Patterns

**Table 4 : Timings Used for IDD and IDDQ Measurement-Loop Patterns**

Parameter	DDR3L-1333	DDR3L-1600	DDR3L-1866	DDR3L-2133	Unit
	9-9-9	11-11-11	13-13-13	14-14-14	
CL	9	11	13	14	nCK
tCK(min)	1.5	1.25	1.071	0.938	ns
nRCD(min)	9	11	13	14	nCK
nRC(min)	33	39	45	50	nCK
nRAS(min)	24	28	32	36	nCK
nRP(min)	9	11	13	14	nCK
nFAW	30	32	33	27	nCK
nRRD	5	6	6	6	nCK
nRFC	174	208	243	279	nCK

### 1.4.2 Basic IDD and IDDQ Measurement Conditions

**Table 5: Basic IDD and IDDQ Measurement Conditions**

Parameter	Symbol	Description
Operating one bank active precharge current	IDD0	CKE: H; External clock: on; tCK, nRC, nRAS, CL: see <a href="#">Table 4</a> ; BL: 8*1; AL: 0; /CS: H between ACT and PRE; Command, address, bank address inputs: partially toggling according to <a href="#">Table 6</a> ; Data I/O: MID-LEVEL; DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see <a href="#">Table 6</a> ); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; Pattern details: see <a href="#">Table 6</a>
Operating one bank active-read-precharge current	IDD1	CKE: H; External clock: On; tCK, nRC, nRAS, nRCD, CL: see <a href="#">Table 4</a> ; BL: 8*1, *6; AL: 0; /CS: H between ACT, RD and PRE; Command, address, bank address inputs, data I/O: partially toggling according to <a href="#">Table 7</a> ; DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see <a href="#">Table 7</a> ); Output buffer and RTT: enabled in MR*2; ODT Signal: stable at 0; Pattern details: see <a href="#">Table 7</a>
Precharge standby current	IDD2N	CKE: H; External clock: on; tCK, CL: see <a href="#">Table 4</a> BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to <a href="#">Table 8</a> ; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in mode registers*2; ODT signal: stable at 0; pattern details: see <a href="#">Table 8</a>
Precharge standby ODT current	IDD2NT	CKE: H; External clock: on; tCK, CL: see <a href="#">Table 4</a> ; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to <a href="#">Table 9</a> ; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: toggling according to <a href="#">Table 9</a> ; pattern details: see <a href="#">Table 9</a>
Precharge standby ODT IDDQ current	IDDQ2NT	Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
Precharge power-down current slow exit	IDD2P0	CKE: L; External clock: on; tCK, CL: see <a href="#">Table 4</a> ; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: EMR*2; ODT signal: stable at 0; precharge power down mode: slow exit*3
Precharge power-down current fast exit	IDD2P1	CKE: L; External clock: on; tCK, CL: see <a href="#">Table 4</a> ; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; precharge power down mode: fast exit*3
Precharge quiet standby current	IDD2Q	CKE: H; External clock: On; tCK, CL: see <a href="#">Table 4</a> ; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Active standby current	IDD3N	CKE: H; External clock: on; tCK, CL: see <a href="#">Table 4</a> ; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to <a href="#">Table 8</a> ; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see <a href="#">Table 8</a>
Active power-down current	IDD3P	CKE: L; External clock: on; tCK, CL: see <a href="#">Table 4</a> ; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Operating burst read current	IDD4R	CKE: H; External clock: on; tCK, CL: see <a href="#">Table 4</a> ; BL: 8*1, *6; AL: 0; /CS: H between RD; Command, address, bank address Inputs: partially toggling according to <a href="#">Table 11</a> ; data I/O: seamless read data burst with different data between one burst and the next one according to <a href="#">Table 11</a> ; DM: stable at 0; bank activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see <a href="#">Table 11</a> ); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see <a href="#">Table 11</a>

**Table 5: Basic IDD and IDDQ Measurement Conditions (cont'd)**

Parameter	Symbol	Description
Operating burst write current	IDD4W	CKE: H; External clock: on; tCK, CL: see <a href="#">Table 4</a> ; BL: 8*1; AL: 0; /CS: H between WR; command, address, bank address inputs: partially toggling according to <a href="#">Table 12</a> ; data I/O: seamless write data burst with different data between one burst and the next one according to IDD4W Measurement-Loop Pattern table; DM: stable at 0; bank activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see <a href="#">Table 12</a> ); Output buffer and RTT: enabled in MR*2; ODT signal: stable at H; pattern details: see <a href="#">Table 12</a>
Burst refresh current	IDD5B	CKE: H; External clock: on; tCK, CL, nRFC: see <a href="#">Table 4</a> ; BL: 8*1; AL: 0; /CS: H between REF; Command, address, bank address Inputs: partially toggling according to <a href="#">Table 13</a> ; data I/O: MID-LEVEL; DM: stable at 0; bank activity: REF command every nRFC (Table 12); output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see <a href="#">Table 13</a>
Self-refresh current normal temperature range	IDD6	Commercial temperature : 0 to 85°C and Industrial temperature -40 to 85°C; ASR: disabled*4; SRT: Normal*5; CKE: L; External clock: off; CK and /CK: L; CL: see <a href="#">Table 4</a> ; BL: 8*1; AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Self-refresh operation; output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Self-refresh current extended temperature range	IDD6ET	Commercial temperature : 0 to 95°C and Industrial temperature -40 to 95°C; ASR: Disabled*4; SRT: Extended*5; CKE: L; External clock: off; CK and /CK: L; CL: <a href="#">Table 4</a> ; BL: 8*1; AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Extended temperature self-refresh operation; output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Operating bank interleave read current	IDD7	CKE: H; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see <a href="#">Table 4</a> ; BL: 8*1, *6; AL: CL-1; /CS: H between ACT and RDA; Command, address, bank address Inputs: partially toggling according to <a href="#">Table 15</a> ; data I/O: read data bursts with different data between one burst and the next one according to <a href="#">Table 15</a> ; DM: stable at 0; bank activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see <a href="#">Table 15</a> ; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see <a href="#">Table 15</a>
RESET low current	IDD8	/RESET: low; External clock: off; CK and /CK: low; CKE: FLOATING; /CS, command, address, bank address, Data IO: FLOATING; ODT signal: FLOATING RESET low current reading is valid once power is stable and /RESET has been low for at least 1ms.

- Notes: 1. Burst Length: BL8 fixed by MRS: MR0 bits [1,0] = [0,0].  
 2. MR: Mode Register  
 Output buffer enable: set MR1 bit A12 = 1 and MR1 bits [5, 1] = [0,1];  
 RTT\_Nom enable: set MR1 bits [9, 6, 2] = [0, 1, 1]; RTT\_WR enable: set MR2 bits [10, 9] = [1,0].  
 3. Precharge power down mode: set MR0 bit A12=0 for Slow Exit or MR0 bit A12 = 1 for fast exit.  
 4. Auto self-refresh (ASR): set MR2 bit A6 = 0 to disable or 1 to enable feature.  
 5. Self-refresh temperature range (SRT): set MR0 bit A7= 0 for normal or 1 for extended temperature range.  
 6. Read burst type: nibble sequential, set MR0 bit A3 = 0

**Table 13: IDD0 Measurement-Loop**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA* <sup>3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data* <sup>2</sup>			
Toggling Static H		0	0	ACT	0	0	1	1	0	0	0	0	0	0	0				
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0			
			3, 4	/D, /D	1	1	1	1	0	0	0	0	0	0	0	0			
			...	Repeat pattern 1...4 until nRAS - 1, truncate if necessary															
			nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	0	0		
			...	Repeat pattern 1...4 until nRC - 1, truncate if necessary															
			1 x nRC + 0	ACT	0	0	1	1	0	0	0	0	0	0	0	F	0		
			1 x nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	F	0		
			1 x nRC + 3, 4	/D, /D	1	1	1	1	0	0	0	0	0	0	0	F	0		
			...	Repeat pattern nRC + 1,...,4 until 1*nRC + nRAS - 1, truncate if necessary															
			1 x nRC + nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	F	0		
			...	Repeat nRC + 1,...,4 until 2 x nRC - 1, truncate if necessary															
			1	2 x nRC	Repeat Sub-Loop 0, use BA= 1 instead														
			2	4 x nRC	Repeat Sub-Loop 0, use BA= 2 instead														
			3	6 x nRC	Repeat Sub-Loop 0, use BA= 3 instead														
			4	8 x nRC	Repeat Sub-Loop 0, use BA= 4 instead														
			5	10 x nRC	Repeat Sub-Loop 0, use BA= 5 instead														
6	12 x nRC	Repeat Sub-Loop 0, use BA= 6 instead																	
7	14 x nRC	Repeat Sub-Loop 0, use BA= 7 instead																	

- Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING.  
 2. DQ signals are FLOATING.  
 3. BA: BA0 to BA2.  
 4. Am: m means Most Significant Bit (MSB) of Row address.

**Table 14: IDD1 Measurement-Loop**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA <sup>3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data <sup>2</sup>			
Toggling Static H		0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	—			
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	—		
			3, 4	/D, /D	1	1	1	1	1	0	0	0	0	0	0	0	—		
			...	Repeat pattern 1...4 until nRCD - 1, truncate if necessary															
			nRCD	RD	0	1	0	1	0	0	0	0	0	0	0	0	0	00000000	
			...	Repeat pattern 1...4 until nRAS - 1, truncate if necessary															
			nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	0	0	—	
			...	Repeat pattern 1...4 until nRC - 1, truncate if necessary															
			1 x nRC + 0	ACT	0	0	1	1	0	0	0	0	0	0	0	F	0	—	
			1 x nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	F	0	—	
			1 x nRC + 3, 4	/D, /D	1	1	1	1	0	0	0	0	0	0	0	F	0	—	
			...	Repeat pattern nRC + 1, ..., 4 until nRC + nRCD - 1, truncate if necessary															
			1 x nRC + nRCD	RD	0	1	0	1	0	0	0	0	0	0	0	F	0	00110011	
			...	Repeat pattern nRC + 1, ..., 4 until nRC + nRAS - 1, truncate if necessary															
			1 x nRC + nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	F	0	—	
			...	Repeat pattern nRC + 1, ..., 4 until 2 x nRC - 1, truncate if necessary															
			1	2 x nRC	Repeat Sub-Loop 0, use BA= 1 instead														
			2	4 x nRC	Repeat Sub-Loop 0, use BA= 2 instead														
			3	6 x nRC	Repeat Sub-Loop 0, use BA= 3 instead														
			4	8 x nRC	Repeat Sub-Loop 0, use BA= 4 instead														
			5	10 x nRC	Repeat Sub-Loop 0, use BA= 5 instead														
6	12 x nRC	Repeat Sub-Loop 0, use BA= 6 instead																	
7	14 x nRC	Repeat Sub-Loop 0, use BA= 7 instead																	

- Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.  
 2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.  
 3. BA: BA0 to BA2.  
 4. Am: m means Most Significant Bit (MSB) of Row address.

**Table 8: IDD2N and IDD3N Measurement-Loop Pattern**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA <sup>*3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data <sup>*2</sup>	
Toggling Static H	0	0		D	1	0	0	0	0	0	0	0	0	0	0	0	
		1		D	1	0	0	0	0	0	0	0	0	0	0	0	
		2		/D	1	1	1	1	0	0	0	0	0	0	F	0	
		3		/D	1	1	1	1	0	0	0	0	0	0	F	0	
	1	4 to 7	Repeat Sub-Loop 0, use BA= 1 instead														
	2	8 to 11	Repeat Sub-Loop 0, use BA= 2 instead														
	3	12 to 15	Repeat Sub-Loop 0, use BA= 3 instead														
	4	16 to 19	Repeat Sub-Loop 0, use BA= 4 instead														
	5	20 to 23	Repeat Sub-Loop 0, use BA= 5 instead														
	6	24 to 27	Repeat Sub-Loop 0, use BA= 6 instead														
7	28 to 31	Repeat Sub-Loop 0, use BA= 7 instead															

- Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING.  
 2. DQ signals are FLOATING.  
 3. BA: BA0 to BA2.  
 4. Am: m means Most Significant Bit (MSB) of Row address.

**Table 9: IDD2NT and IDDQ2NT Measurement-Loop Pattern**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA <sup>*3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data <sup>*2</sup>	
Toggling Static H	0	0		D	1	0	0	0	0	0	0	0	0	0	0	0	
		1		D	1	0	0	0	0	0	0	0	0	0	0	0	
		2		/D	1	1	1	1	0	0	0	0	0	0	F	0	
		3		/D	1	1	1	1	0	0	0	0	0	0	F	0	
	1	4 to 7	Repeat Sub-Loop 0, but ODT = 0 and BA= 1														
	2	8 to 11	Repeat Sub-Loop 0, but ODT = 1 and BA= 2														
	3	12 to 15	Repeat Sub-Loop 0, but ODT = 1 and BA= 3														
	4	16 to 19	Repeat Sub-Loop 0, but ODT = 0 and BA= 4														
	5	20 to 23	Repeat Sub-Loop 0, but ODT = 0 and BA= 5														
	6	24 to 27	Repeat Sub-Loop 0, but ODT = 1 and BA= 6														
7	28 to 31	Repeat Sub-Loop 0, but ODT = 1 and BA= 7															

- Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING.  
 2. DQ signals are FLOATING.  
 3. BA: BA0 to BA2.  
 4. Am: m means Most Significant Bit (MSB) of Row address.



Table 10: IDD2P0, IDD2P1, IDD2Q and IDD3P Measurement-Loop Pattern

External Clock	Name	CK	CKE	RC	RAS	RCD	RRD	CL	AL	CSB	Comm and	A0-Am	BA	DM	ODT	DQ, DQS	Burst length	Active banks	Idle banks	Data
Toggling	IDD2P0 Precharge Power-Down Current (Slow Exit)	CK (MIN) IDD	0	N/A	N/A	N/A	N/A	N/A	N/A	1	0	0	0	0	Acted, off	Acted	8	None	All	Midlevel
	IDD2P1 Precharge Power-Down Current (Fast Exit)	CK (MIN) IDD	0	N/A	N/A	N/A	N/A	N/A	N/A	1	0	0	0	0	Acted, off	Acted	8	None	All	Midlevel
	IDD2Q Precharge Quiet Standby Current	CK (MIN) IDD	1	N/A	N/A	N/A	N/A	N/A	N/A	1	0	0	0	0	Acted, off	Acted	8	None	All	Midlevel
	IDD3P Active Power-Down Current	CK (MIN) IDD	0	N/A	N/A	N/A	N/A	N/A	N/A	1	0	0	0	0	Acted, off	Acted	8	All	None	Midlevel

- Notes: 1. MR0[12] defines DLL on/off behavior during precharge power-down only; DLL on (fast exit, MR0[12] = 1) and DLL off (slow exit, MR0[12] = 0).
2. "Acted, off" means the MR bits are enabled, but the signal is LOW.

**Table 11: IDD4R and Measurement-Loop Pattern**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA <sup>*3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data <sup>*2</sup>	
Toggling Static H	0	0	RD	0	1	0	1	0	0	0	0	0	0	0	0	00000000	
		1	D	1	0	0	0	0	0	0	0	0	0	0	0	—	
		2,3	/D, /D	1	1	1	1	0	0	0	0	0	0	0	0	—	
		4	RD	0	1	0	1	0	0	0	0	0	0	F	0	00110011	
		5	D	1	0	0	0	0	0	0	0	0	0	F	0	—	
		6,7	/D, /D	1	1	1	1	0	0	0	0	0	0	F	0	—	
		1	8 to 15	Repeat Sub-Loop 0, but BA= 7													
		2	16 to 23	Repeat Sub-Loop 0, but BA= 6													
	3	24 to 31	Repeat Sub-Loop 0, but BA= 5														
	4	32 to 39	Repeat Sub-Loop 0, but BA= 4														
	5	40 to 47	Repeat Sub-Loop 0, but BA= 3														
	6	48 to 55	Repeat Sub-Loop 0, but BA= 2														
	7	56 to 63	Repeat Sub-Loop 0, but BA= 1														

- Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.  
 2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.  
 3. BA: BA0 to BA2.  
 4. Am: m means Most Significant Bit (MSB) of Row address.

**Table 12: IDD4W Measurement-Loop Pattern**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA <sup>*3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data <sup>*2</sup>		
Toggling Static H	0	0	0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000		
		1	1	D	1	0	0	0	1	0	0	0	0	0	0	0	—	
		23	/D, /D	1	1	1	1	1	1	0	0	0	0	0	0	0	—	
		4	RD	0	1	0	0	0	1	0	0	0	0	F	0	00110011		
		5	D	1	0	0	0	0	1	0	0	0	0	F	0	—		
		6,7	/D, /D	1	1	1	1	1	1	0	0	0	0	F	0	—		
		1	8 to 15	Repeat Sub-Loop 0, but BA= 1														
		2	16 to 23	Repeat Sub-Loop 0, but BA= 2														
	3	24 to 31	Repeat Sub-Loop 0, but BA= 3															
	4	32 to 39	Repeat Sub-Loop 0, but BA= 4															
	5	40 to 47	Repeat Sub-Loop 0, but BA= 5															
	6	48 to 55	Repeat Sub-Loop 0, but BA= 6															
	7	56 to 63	Repeat Sub-Loop 0, but BA= 7															

- Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.  
 2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.  
 3. BA: BA0 to BA2.  
 4. Am: m means Most Significant Bit (MSB) of Row address.

**Table 13: IDD5B Measurement-Loop Pattern**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA <sup>*3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data <sup>*2</sup>		
Toggling Static H		0	0	REF	0	0	0	1	0	0	0	0	0	0	0	—		
			1,2	D	1	0	0	0	0	0	0	0	0	0	0	0	—	
		1	3,4	/D, /D	1	1	1	1	1	0	0	0	0	0	F	0	—	
			5 to 8	Repeat cycles 1...4, but BA= 1														
			9 to 12	Repeat cycles 1...4, but BA= 2														
			13 to 16	Repeat cycles 1...4, but BA= 3														
			17 to 20	Repeat cycles 1...4, but BA= 4														
			21 to 24	Repeat cycles 1...4, but BA= 5														
			25 to 28	Repeat cycles 1...4, but BA= 6														
			29 to 32	Repeat cycles 1...4, but BA= 7														
		2	33 to nRFC - 1	Repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary														

- Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING.  
 2. DQ signals are FLOATING.  
 3. BA: BA0 to BA2.  
 4. Am: m means Most Significant Bit (MSB) of Row address

Table 14: IDD6, IDD6ET and IDD8 Measurement-Loop Pattern

External Clock	Name	CK	CKE	RC	RAS	RCD	RRD	CL	AL/CS	Command	A0-Am	BA	SRT	ASR	ODT	DQ, DQS	Burst length	Active banks	Idle banks	Data
Off, CK and /CK = Low	IDD6: Self Refresh Current Normal Temperature Range 0°C to +85°C	N/A	0	N/A						Midlevel			Disabled (normal)	Disabled	Acted, Midlevel	Acted	N/A	None	All	Midlevel
	IDD6: Self Refresh Current Extended Temperature Range Commercial-Temp: 0°C to +95°C, Industrial-Temp: -40°C to +95°C	N/A	0	N/A						Midlevel			Enabled (extended)	Disabled	Acted, Midlevel	Acted	N/A	None	All	Midlevel
Midlevel	IDD8: Reset	N/A	Midlevel	N/A						Midlevel			N/A	N/A	Midlevel	Midlevel	N/A	None	All	Midlevel

- Notes: 1. "Acted, midlevel" means the MR command is enabled, but the signal is midlevel.  
 2. During a cold boot RESET (initialization), current reading is valid after power is stable and RESET has been LOW for 1 ms;  
 During a warm boot RESET (while operating), current reading is valid after RESET has been LOW for 200ns + tRFC.

**Table 15: IDD7 Measurement-Loop Pattern**

CK, /CK	CKE	Sub-Loop	Cycle number	Command	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2			
Toggling Static H		0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	—			
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	0	00000000		
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	—		
			...	Repeat above D Command until nRRD – 1															
			nRRD	ACT	0	0	1	1	0	1	0	0	0	0	F	0	—		
			nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	1	0	F	0	00110011	
			nRRD + 2	D	1	0	0	0	0	0	1	0	0	0	F	0	—		
			...	Repeat above D Command until 2 x nRRD – 1															
			2	2 x RRD	Repeat Sub-Loop 0, but BA= 2														
			3	3 x RRD	Repeat Sub-Loop 1, but BA= 3														
			4	4 x nRRD	D	1	0	0	0	0	0	3	0	0	0	F	0	—	
			Assert and repeat above D Command until nFAW – 1, if necessary																
			5	nFAW	Repeat Sub-Loop 0, but BA= 4														
			6	nFAW + nRRD	Repeat Sub-Loop 1, but BA= 5														
			7	nFAW + 2 x nRRD	Repeat Sub-Loop 0, but BA= 6														
			8	nFAW + 3 x nRRD	Repeat Sub-Loop 1, but BA= 7														
			9	nFAW + 4 x nRRD	D	1	0	0	0	0	0	7	0	0	0	F	0	—	
			Assert and repeat above D Command until 2 x nFAW – 1, if necessary																
			10	2 x nFAW + 0	ACT	0	0	1	1	0	0	0	0	0	0	F	0	—	
				2 x nFAW + 1	RDA	0	1	0	1	0	0	0	0	1	0	F	0	00110011	
2 x nFAW + 2	D	1		0	0	0	0	0	0	0	0	0	F	0	—				
Repeat above D Command until 2 x nFAW + nRRD – 1																			
11	2 x nFAW + nRRD	ACT	0	0	1	1	0	1	0	0	0	0	0	0	—				
	2 x nFAW + nRRD + 1	RDA	0	1	0	1	0	0	1	0	1	0	0	0	00000000				
	2 x nFAW + nRRD + 2	D	1	0	0	0	0	0	1	0	0	0	0	0	—				
Repeat above D Command until 2 x nFAW + 2 x nRRD – 1																			
12	2 x nFAW + 2 x nRRD	Repeat Sub-Loop 10, but BA= 2																	
13	2 x nFAW + 3 x nRRD	Repeat Sub-Loop 11, but BA= 3																	
14	2 x nFAW + 4 x nRRD	D	1	0	0	0	0	0	3	0	0	0	0	0	—				
Assert and repeat above D Command until 3 x nFAW – 1, if necessary																			
15	3 x nFAW	Repeat Sub-Loop 10, but BA= 4																	
16	3 x nFAW + nRRD	Repeat Sub-Loop 11, but BA= 5																	
17	3 x nFAW + 2 + nRRD	Repeat Sub-Loop 10, but BA= 6																	
18	3 x nFAW + 3 + nRRD	Repeat Sub-Loop 11, but BA= 7																	
19	3 x nFAW + 4 + nRRD	D	1	0	0	0	0	0	7	0	0	0	0	0	—				
Assert and repeat above D Command until 4 x nFAW – 1, if necessary																			

- Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.  
 2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.  
 3. BA: BA0 to BA2.  
 4. Am: m means Most Significant Bit (MSB) of Row address

## 2. Electrical Specifications

### 2.1 DC Characteristics

Table 16: DC Characteristics 1 (VDD, VDDQ = 1.283V to 1.45V)

Parameter	Symbol	Data rate (Mbps)	x8(max)	x16(max)	unit	Notes
Operating current (ACT-PRE)	IDD0	1333	43	46	mA	
		1866	45	47		
		1866	47	49		
		2133	49	51		
Operating current (ACT-RD-PRE)	IDD1	1333	57	65	mA	
		1866	59	67		
		1866	62	70		
		2133	65	73		
Precharge power-down standby current	IDD2P0	1333	7	11	mA	SlowPD Exit
		1866	7	11		
		1866	7	11		
		2133	7	11		
	IDD2P1	1333	10	14	mA	FastPD Exit
		1866	12	14		
		1866	14	14		
		2133	16	14		
Precharge standby current	IDD2N	1333	20	22	mA	
		1866	22	22		
		1866	24	22		
		2133	26	22		
Precharge standby ODT current	IDD2NT	1333	24	34	mA	
		1866	26	35		
		1866	28	37		
		2133	30	39		
Precharge quiet standby current	IDD2Q	1333	20	21	mA	
		1866	22	21		
		1866	24	21		
		2133	26	21		
Active power-down current (Always fast exit)	IDD3P	1333	22	21	mA	
		1866	24	21		
		1866	26	21		
		2133	28	21		
Active standby current	IDD3N	1333	26	34	mA	
		1866	28	35		
		1866	30	37		
		2133	32	39		
Operating current (Burst read operating)	IDD4R	1333	133	110	mA	
		1866	143	130		
		1866	153	150		
		2133	163	170		
Operating current (Burst write operating)	IDD4W	1333	133	122	mA	
		1866	143	141		
		1866	153	159		
		2133	163	176		
Burst refresh current	IDD5B	1333	226	151	mA	
		1866	233	152		
		1866	240	153		
		2133	247	154		
All bank interleave read current	IDD7	1333	168	174	mA	
		1866	178	197		
		1866	188	221		
		2133	198	246		
RESET low current	IDD8	1333		10	mA	
		1600	IDD2P+2	10		
		1866		10		
		2133		10		

**Table 17: Self-Refresh Current (VDD, VDDQ = 1.283V to 1.45V)**

<b>Parameter</b>	<b>Symbol</b>	<b>x8(max)</b>	<b>x16(max)</b>	<b>unit</b>	<b>Notes</b>
Self-refresh current normal temperature range	IDD6	10	11	mA	Max
Self-refresh current extended temperature range	IDD6ET	14	12	mA	Max@95°C

## 2.2 Pin Capacitance

**Table 18: Pin Capacitance [DDR3L-1333 to 2133] (Operating Temperature = 25°C, VDD, VDDQ = 1.283V to 1.45V)**

Parameter	Symbol	DDR3L-1333		DDR3L-1600		DDR3L-1866		DDR3L-2133		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Input/output	CIO	1.4	2.4	1.4	2.3	1.4	2.2	1.4	2.1	pF	1,2
Input capacitance, CK and /CK	CCK	0.8	1.4	0.8	1.4	0.8	1.3	0.8	1.3	pF	2
Input capacitance delta, CK and /CK	CDCK	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3
Input/output capacitance delta, DQS and /DQS	CDDQS	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,4
Input capacitance, (control, address, command, input-only pins)	CI	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	pF	2,5
Input capacitance delta, (All control input-only pins)	CDI_CTRL	-0.4	0.2	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,6,7
Input capacitance delta, (All address/command input-only pins)	CDI_ADD_CMD	-0.4	0.4	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2,8,9
Input/output capacitance delta, DQ,DM, DQS, /DQS, TDQS, /TDQS	CDIO	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,10
Input/output capacitance of ZQ pin	CZQ	-	3	-	3	-	3	-	3	pF	2,11

- Notes: 1. Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.  
2. VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, /RESET and ODT as necessary). VDD = VDDQ = 1.5V, VBIAS=VDD/2 and on-die termination off.  
3. Absolute value of CCK-C/CK.  
4. Absolute value of CIO(DQS)-CIO(/DQS).  
5. CI applies to ODT, /CS, CKE, A0-A14, BA0-BA2, /RAS, /CAS and /WE.  
6. CDI\_CTRL applies to ODT, /CS and CKE.  
7. CDI\_CTRL = CI(CTRL) – 0.5 × (CI(CLK)+CI(/CLK)).  
8. CDI\_ADD\_CMD applies to A0-A15, BA0-BA2, /RAS, /CAS and /WE.  
9. CDI\_ADD\_CMD = CI(ADD\_CMD) – 0.5 × (CI(CLK)+CI(/CLK)).  
10. CDIO=CIO(DQ,DM) – 0.5 × (CIO(DQS)+CIO(/DQS)).  
11. Maximum external load capacitance on ZQ pin: 5pF.



## 2.3 Standard SpeedBins

Table 19: DDR3L-1333 Speed Bins

Speed Bin		DDR3L-1333			
CL-tRCD-tRP		9-9-9			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		13.5 (13.125)	20	ns	10
tRCD		13.5 (13.125)	—	ns	10
tRP		13.5 (13.125)	—	ns	10
tRC		49.5 (49.125)	—	ns	10
tRAS		36	9 x tREFI	ns	5
tCK(avg)@CL=5	CWL=5	3.0	3.3	ns	1, 2, 3, 4, 5, 9
	CWL=6, 7,	Reserved	Reserved	ns	4
tCK(avg)@CL=6	CWL=5	2.5	3.3	ns	1, 2, 3, 5
	CWL=6	Reserved	Reserved	ns	1, 2, 3, 4, 5
	CWL=7,	Reserved	Reserved	ns	4
tCK(avg)@CL=7	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	< 2.5	ns	1, 2, 3, 4, 5
	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 5
tCK(avg)@CL=8	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	<2.5	ns	1, 2, 3, 5
	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 5
tCK(avg)@CL=9	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	<1.875	ns	1, 2, 3, 4, 5
tCK(avg)@CL=10	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	<1.875	ns	1, 2, 3, 5
Supported CL settings		5, 6, (7), 8, (9), 10,		nCK	
Supported CWL settings		5, 6, 7,		nCK	

**Table 20: DDR3L-1600 Speed Bins**

Speed Bin		DDR3L-1600			
CL-tRCD-tRP		11-11-11			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		13.75 (13.125)	20	ns	11
tRCD		13.75 (13.125)	—	ns	11
tRP		13.75 (13.125)	—	ns	11
tRC		48.75 (48.125)	—	ns	11
tRAS		35	9 x tREFI	ns	9
tCK(avg)@CL=5	CWL=5	3.0	3.3	ns	1, 2, 3, 4, 6, 9
	CWL=6, 7, 8	Reserved	Reserved	ns	4
tCK(avg)@CL=6	CWL=5	2.5	3.3	ns	1, 2, 3, 6
	CWL=6	Reserved	Reserved	ns	1, 2, 3, 4, 6
	CWL=7, 8	Reserved	Reserved	ns	4
tCK(avg)@CL=7	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	< 2.5	ns	1, 2, 3, 4, 6
	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 6
	CWL=8	Reserved	Reserved	ns	4
tCK(avg)@CL=8	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	<2.5	ns	1, 2, 3, 6
	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 6
tCK(avg)@CL=9	CWL=8	Reserved	Reserved	ns	1, 2, 3, 4
	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	<1.875	ns	1, 2, 3, 4, 6
tCK(avg)@CL=10	CWL=8	Reserved	Reserved	ns	1, 2, 3, 4
	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	<1.875	ns	1, 2, 3, 6
tCK(avg)@CL=11	CWL=8	Reserved	Reserved	ns	1, 2, 3, 4
	CWL=5, 6, 7	Reserved	Reserved	ns	4
	CWL=8	1.25	<1.5	ns	1, 2, 3
Supported CL settings		5, 6, (7), 8, (9), 10, 11		nCK	
Supported CWL settings		5, 6, 7, 8		nCK	

**Table 26: DDR3L-1866 Speed Bins**

<b>Speed Bin</b>		<b>DDR3L-1866</b>			
<b>CL-tRCD-tRP</b>		<b>13-13-13</b>			
<b>Symbol</b>	<b>/CAS write latency</b>	<b>min</b>	<b>max</b>	<b>Unit</b>	<b>Notes</b>
tAA		13.91 (13.125)	20	ns	
tRCD		13.91 (13.125)	—	ns	
tRP		13.91 (13.125)	—	ns	
tRC		47.91 (47.125)	—	ns	
tRAS		34	9 x tREFI	ns	
tCK(avg)@CL=5	CWL=5	Reserved	Reserved	ns	1, 2, 3, 4, 7
	CWL=6, 7, 8, 9	Reserved	Reserved	ns	4,
tCK(avg)@CL=6	CWL=5	2.5	3.3	ns	1, 2, 3, 7
	CWL=6	Reserved	Reserved	ns	1, 2, 3, 4, 7
	CWL=7, 8, 9	Reserved	Reserved	ns	4
tCK(avg)@CL=7	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	< 2.5	ns	1, 2, 3, 4, 7
	CWL=7, 8, 9	Reserved	Reserved	ns	4
tCK(avg)@CL=8	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	< 2.5	ns	1, 2, 3, 7
	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 7
	CWL=8,9	Reserved	Reserved	ns	4
tCK(avg)@CL=9	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	< 1.875	ns	1, 2, 3, 4, 7
	CWL=8	Reserved	Reserved	ns	4
	CWL=9	Reserved	Reserved	ns	1, 2, 3, 4, 7
tCK(avg)@CL=10	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	< 1.875	ns	1, 2, 3, 7
	CWL=8	Reserved	Reserved	ns	1, 2, 3, 4, 7
tCK(avg)@CL=11	CWL=5, 6, 7	Reserved	Reserved	ns	4
	CWL=8	1.25	< 1.5	ns	1, 2, 3, 4, 7
	CWL=9	Reserved	Reserved	ns	1, 2, 3, 4
tCK(avg)@CL=12	CWL=5, 6, 7, 8	Reserved	Reserved	ns	4
	CWL=9	Reserved	Reserved	ns	1, 2, 3, 4
tCK(avg)@CL=13	CWL=5, 6, 7, 8	Reserved	Reserved	ns	4
	CWL=9	1.07	< 1.25	ns	1, 2, 3
Supported CL settings		6, 8, 10, 13, (7), (9), (11)		nCK	
Supported CWL settings		5, 6, 7, 8, 9		nCK	

**Table 27: DDR3L-2133 Speed Bins**

Speed Bin		DDR3L-2133			
CL-tRCD-tRP		14-14-14			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		13.09	20	ns	
tRCD		13.09	—	ns	
tRP		13.09	—	ns	
tRC		46.09	—	ns	
tRAS		33.0	9 x tREFI	ns	
tCK(avg)@CL=5	CWL=6,7,8,9,10	Reserved	Reserved	ns	1,2,3,4,8
	CWL=5	2.5	3.3	ns	1,2,3,8
tCK(avg)@CL=6	CWL=6	Reserved	Reserved	ns	1,2,3,4,8
	CWL=7,8,9,10	Reserved	Reserved	ns	4
tCK(avg)@CL=7	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	< 2.5	ns	1,2,3,8
	CWL=7	Reserved	Reserved	ns	1,2,3,4,8
	CWL=8,9,10	Reserved	Reserved	ns	4
tCK(avg)@CL=8	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	< 2.5	ns	1,2,3,8
	CWL=7	Reserved	Reserved	ns	1,2,3,4,8
tCK(avg)@CL=8	CWL=8,9,10	Reserved	Reserved	ns	4
	CWL=5,6	Reserved	Reserved	ns	4
	CWL=7	1.5	< 1.875	ns	1,2,3,8
tCK(avg)@CL=9	CWL=8	Reserved	Reserved	ns	1,2,3,4,8
	CWL=9,10	Reserved	Reserved	ns	4
	CWL=5,6	Reserved	Reserved	ns	4
tCK(avg)@CL=10	CWL=7	1.5	< 1.875	ns	1,2,3,8
	CWL=8,9	Reserved	Reserved	ns	1,2,3,4,8
	CWL=10	Reserved	Reserved	ns	4
tCK(avg)@CL=11	CWL=5,6,7	Reserved	Reserved	ns	4
	CWL=8	1.25	< 1.5	ns	1,2,3,8
	CWL=9	Reserved	Reserved	ns	1,2,3,4,8
tCK(avg)@CL=11	CWL=10	Reserved	Reserved	ns	1,2,3,4,8
	CWL=5,6,7,8	Reserved	Reserved	ns	4
	CWL=9	Reserved	Reserved	ns	1,2,3,4,8
tCK(avg)@CL=12	CWL=10	Reserved	Reserved	ns	1,2,3,4
	CWL=5,6,7,8	Reserved	Reserved	ns	4
	CWL=9	1.07	< 1.25	ns	1,2,3,8
tCK(avg)@CL=13	CWL=10	Reserved	Reserved	ns	1,2,3,4
	CWL=5,6,7,8,9	Reserved	Reserved	ns	4
tCK(avg)@CL=14	CWL=10	0.938	< 1.07	ns	1,2,3,5
Supported CL settings		5,6,7,8,9,10,11,12,13,14		nCK	
Supported CWL settings		5,6,7,8,9,10		nCK	

**Electrical Characteristics & AC Timing for DDR3L-1600 to DDR3L-2133 (Cont'd)**  
**Standard Speed Bins (Cont'd)**

- NOTE 1.** The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
- NOTE 2.** tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, 1.25, 1.07, or 0.938 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
- NOTE 3.** tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.5 ns or 1.25 ns or 1.07 ns or 0.938 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
- NOTE 4.** 'Reserved' settings are not allowed. User must program a different value.
- NOTE 5.** Any DDR3L-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- NOTE 6.** Any DDR3L-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- NOTE 7.** Any DDR3L-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- NOTE 8.** Any DDR3L-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- NOTE 9.** For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.
- NOTE 10.** tREFI depends on operating commercial temperature and industrial temperature.
- NOTE 11.** For devices supporting optional down binning to CL=11 and CL=9, tAA/tRCD/tRPmin must be 13.125ns. SPD setting must be programmed to match.

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### 3. Package Drawing

#### 3.1 96-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm

## NOTES FOR CMOS DEVICES

### ⦿ PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

### ⦿ HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

### ⦿ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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[Usage environment]

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Example:

- 1) Usage in liquids, including water, oils, chemicals and organic solvents.
- 2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
- 3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>x</sub>.
- 4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
- 5) Usage in places where dew forms.
- 6) Usage in environments with mechanical vibration, impact, or stress.
- 7) Usage near heating elements, igniters, or flammable items.

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