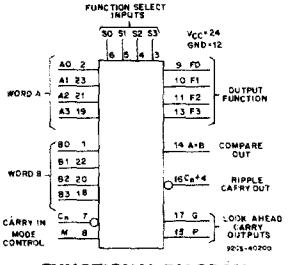
# CD54/74HC181
# CD54/74HCT181

File Number **1829**

## High-Speed CMOS Logic




**FUNCTIONAL DIAGRAM**
**ACTIVE-HIGH DATA**

# 4-Bit Arithmetic Logic Unit

**Type Features:**

- *Full look-ahead carry for speed operations on long words*
- *Generates 16 logic functions of two Boolean variables*
- *Generates 16 arithmetic functions of two 4-bit binary words*
- *A = B comparator output available (open drain)*
- *Ripple-carry input and output available*
- *Available in both narrow- and wide-body plastic packages*

The RCA CD54/74HC181 and CD54/74HCT181 are low-power four-bit parallel arithmetic logic units (ALU) capable of providing 16 binary arithmetic operations on two four-bit words and 16 logical functions of two Boolean variables. The mode control input M selects logical (M=High) or arithmetic (M=Low) operation. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR, and exclusive-OR and -NOR in the logic mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. The HC/HCT181 operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs, by using the appropriate truth table.

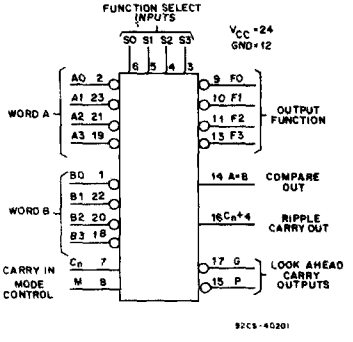
The HC/HCT181 contains logic for full look-ahead carry operation for fast-carry generation using the carry-generate and carry-propagate outputs G and P for the four bits of the HC/HCT181. Use of the HC/HCT182 look-ahead carry generator in conjunction with multiple HC/HCT181s permits high-speed arithmetic operations on long words. A ripple-carry output $C_{n+4}$ is available for use in systems where speed is not of primary importance.

Also included in these devices is a comparator output A = B, which assumes a high level whenever the two four-bit input words A and B are equal and the device is in the subtract mode. A=B is an open-drain output that can be wire-AND connected to give a comparison for more than 4 bits. In addition, relative magnitude information may be derived from the carry-in input $C_n$ and ripple carry-out output $C_{n+4}$ by placing the unit in the subtract mode and externally decoding using the information in the Magnitude Comparison table.

The CD54HC181 and CD54HCT181 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC181 and CD74HCT181 are supplied in 24-lead dual-in-line, narrow-body plastic packages (EN suffix), in 24-lead dual-in-line, wide-body plastic packages (E suffix), and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

**Family Features:**

- *Fanout (over temperature range):*
  *Standard outputs - 10 LSTTL loads*
  *Bus driver outputs - 15 LSTTL loads*
- *Wide operating temperature range:*
  *CD74HC/HCT: −40 to +85°C*
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  *2 to 6 V operation*
  *High noise immunity:*
  *$N_{IL}$=30%, $N_{IH}$=30% of $V_{CC}$; @ $V_{CC}$=5 V*
- *CD54HCT/CD74HCT types:*
  *4.5 to 5.5 V operation*
  *Direct LSTTL input logic compatibility*
  *$V_{IL}$=0.8 V max., $V_{IH}$=2 V min.*
  *CMOS input compatibility*
  *$I_I \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*




**FUNCTIONAL DIAGRAM**
**ACTIVE-LOW DATA**

# CD54/74HC181
# CD54/74HCT181

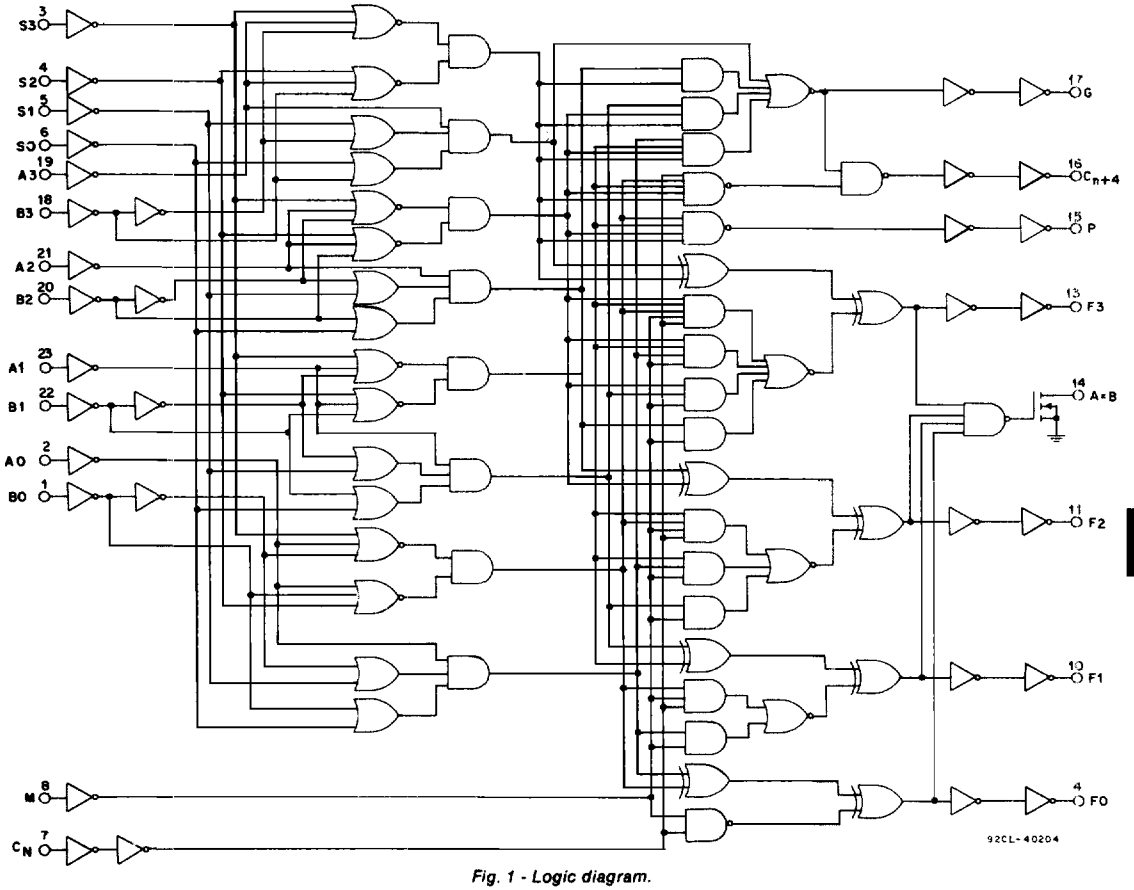



*Fig. 1 - Logic diagram.*

## FUNCTION TABLES

| Function Select | | | | Inputs/Outputs Active High | | |
|---|---|---|---|---|---|---|
| | | | | Logic Function | Arithmetic Function M = L | |
| S3 | S2 | S1 | S0 | M = H | $C_n$=H (no carry) | $C_n$=L (with carry) |
| L | L | L | L | $\overline{A}$ | A | A plus 1 |
| L | L | L | H | $\overline{A+B}$ | A + B | (A + B) plus 1 |
| L | L | H | L | $\overline{A}B$ | A + $\overline{B}$ | (A + $\overline{B}$) plus 1 |
| L | L | H | H | Logic 0 | minus 1 (2's compl.) | Zero |
| L | H | L | L | $\overline{AB}$ | A plus A$\overline{B}$ | A plus A$\overline{B}$ plus 1 |
| L | H | L | H | $\overline{B}$ | (A + B) plus A$\overline{B}$ | (A+B)plus A$\overline{B}$ plus 1 |
| L | H | H | L | A ⊕ B | A minus B minus 1 | A minus B |
| L | H | H | H | A$\overline{B}$ | A$\overline{B}$ minus 1 | A$\overline{B}$ |
| H | L | L | L | $\overline{A}$ + B | A plus AB | A plus AB plus 1 |
| H | L | L | H | $\overline{A \oplus B}$ | A plus B | A plus B plus 1 |
| H | L | H | L | B | (A + $\overline{B}$) plus AB | (A+$\overline{B}$)plus AB plus 1 |
| H | L | H | H | AB | AB minus 1 | AB |
| H | H | L | L | Logic 1 | A plus A* | A plus A plus 1 |
| H | H | L | H | A + $\overline{B}$ | (A + B) plus A | (A+B) plus A plus 1 |
| H | H | H | L | A + B | (A + $\overline{B}$) plus A | (A+$\overline{B}$) plus A plus 1 |
| H | H | H | H | A | A minus 1 | A |

| Function Select | | | | Inputs/Outputs Active Low | | |
|---|---|---|---|---|---|---|
| | | | | Logic Function | Arithmetic Function M = L | |
| S3 | S2 | S1 | S0 | M = H | $C_n$=L (no carry) | $C_n$=H (with carry) |
| L | L | L | L | $\overline{A}$ | A minus 1 | A |
| L | L | L | H | $\overline{AB}$ | AB minus 1 | AB |
| L | L | H | L | $\overline{A}$ + B | A$\overline{B}$ minus 1 | A$\overline{B}$ |
| L | L | H | H | Logic 1 | minus 1 (2's compl.) | Zero |
| L | H | L | L | $\overline{A+B}$ | A plus (A + $\overline{B}$) | A plus (A+$\overline{B}$) plus 1 |
| L | H | L | H | $\overline{B}$ | AB plus (A + B) | AB plus (A+$\overline{B}$) plus 1 |
| L | H | H | L | A ⊕ B | A minus B minus 1 | A minus B |
| L | H | H | H | A + $\overline{B}$ | A + $\overline{B}$ | (A + $\overline{B}$) plus 1 |
| H | L | L | L | $\overline{A}$B | A plus (A + B) | A plus (A+B) plus 1 |
| H | L | L | H | A ⊕ B | A plus B | A plus B plus 1 |
| H | L | H | L | B | A$\overline{B}$ plus (A + B) | A$\overline{B}$ plus (A+B) plus 1 |
| H | L | H | H | A + B | A + B | (A + B) plus 1 |
| H | H | L | L | Logic 0 | A plus A* | A plus A plus 1 |
| H | H | L | H | A$\overline{B}$ | AB plus A | AB plus A plus 1 |
| H | H | H | L | AB | A$\overline{B}$ plus A | A$\overline{B}$ plus A plus 1 |
| H | H | H | H | A | A | A plus 1 |

H = High Level  L = Low Level

* Each bit is shifted to the next more significant position.

# CD54/74HC181
# CD54/74HCT181

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_o$) (FOR $-0.5$ V $< V_o <$ $V_{CC}$ +0.5 V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT ($I_{CC}$) ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = −40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = −55 to +100° C (PACKAGE TYPE F,H) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F,H) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = −40 to +70° C (PACKAGE TYPE M) ..... 400 mW
For $T_A$ = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F,H ..... −55 to +125° C
PACKAGE TYPE E,M ..... −40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... −65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
*Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)*
with solder contacting lead tips only ..... +300° C

**RECOMMENDED OPERATING CONDITIONS**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

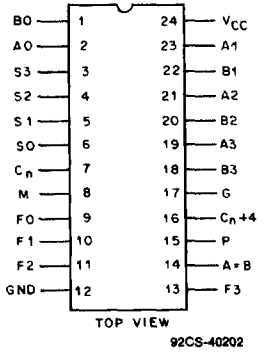
| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$=Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | |
| DC Input or Output Voltage, $V_I$, $V_O$ | 0 | $V_{CC}$ | V |
| Operating Temperature, $T_A$: | | | |
| CD74 Types | −40 | +85 | °C |
| CD54 Types | −55 | +125 | |
| Input Rise and Fall Times, $t_r$,$t_f$: | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | |
| at 6 V | 0 | 400 | |

*Unless otherwise specified, all voltages are referenced to Ground.

**MAGNITUDE COMPARISON TABLE**

| Active - High Data | | | | Active - Low Data | | |
|---|---|---|---|---|---|---|
| Input $C_n$ | Output $C_{n+4}$ | Magnitude | | Input $C_n$ | Output $C_{n+4}$ | Magnitude |
| 1 | 1 | A ≤ B | | 0 | 0 | A ≤ B |
| 0 | 1 | A < B | | 1 | 0 | A < B |
| 1 | 0 | A > B | | 0 | 1 | A > B |
| 0 | 0 | A ≥ B | | 1 | 1 | A ≥ B |

1 = High Level
0 = Low Level




**TERMINAL ASSIGNMENT**

# CD54/74HC181
# CD54/74HCT181

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CD74HC181/CD54HC181 | | | | | | | | | | CD74HCT181/CD54HCT181 | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC TYPES | | | 74HC TYPES | | 54HC TYPES | | TEST CONDITIONS | | 74HCT/54HCT TYPES | | | 74HCT TYPES | | 54HCT TYPES | | |
| | $V_I$ V | $I_O$ mA | $V_{CC}$ V | +25°C | | | -40/ +85°C | | -55/ +125°C | | $V_I$ V | $V_{CC}$ V | +25°C | | | -40/ +85°C | | -55/ +125°C | | |
| | | | | Min | Typ | Max | Min | Max | Min | Max | | | Min | Typ | Max | Min | Max | Min | Max | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 to 5.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.5 | — | 0.5 | — | 0.5 | — | 4.5 to 5.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 1.35 | — | 1.35 | — | 1.35 | | | | | | | | | | |
| | | | 6 | — | — | 1.8 | — | 1.8 | — | 1.8 | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | -0.02 | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | | | | | | | | |
| TTL Loads | $V_{IL}$ or $V_{IH}$ | -4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | -5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | | | | | | | | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | 0.02 | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | |
| TTL Loads | $V_{IL}$ or $V_{IH}$ | 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | | | | | | | | |
| Input Leakage Current $I_I$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | Any Voltage Between $V_{CC}$ & Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | 0 | 6 | — | — | 8 | — | 80 | — | 160 | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | μA |
| Additional Quiescent Device Current per input pin: 1 unit load $\Delta I_{CC}$* | | | | | | | | | | | $V_{CC}$ -2.1 | 4.5 to 5.5 | — | 100 | 360 | — | 450 | — | 490 | μA |

*For dual-supply systems theoretical worst case ($V_I$ = 2.4 V, $V_{CC}$ = 5.5 V) specification is 1.8 mA.

### HCT Input Loading Table

| Input | Unit Loads* |
|---|---|
| S0-S3 | 1 |
| All A and B (Data) | 0.75 |
| M, $C_n$ | 0.5 |

*Unit Load is $\Delta I_{CC}$ limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

# CD54/74HC181
# CD54/74HCT181

**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $T_A$=25° C, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | | $C_L$ (pF) | TYPICAL VALUES | | UNITS |
|---|---|---|---|---|---|
| | | | HC | HCT | |
| | Propagation Delay: $t_{PLH}$, $t_{PHL}$ | | | | |
| SUM Mode | $A_n$ or $B_n$ to $C_{n+4}$ | 15 | 19 | 22 | ns |
| | $A_n$ or $B_n$ to G | 15 | 18 | 23 | |
| | $A_n$ or $B_n$ to P | 15 | 14 | 17 | |
| | $A_n$ or $B_n$ to $F_n$ | 15 | 19 | 24 | |
| DIFFERENCE Mode | $A_n$ or $B_n$ to $C_{n+4}$ | 15 | 20 | 23 | |
| | $A_n$ or $B_n$ to G | 15 | 18 | 23 | |
| | $A_n$ or $B_n$ to P | 15 | 14 | 17 | |
| | $A_n$ or $B_n$ to $F_n$ | 15 | 20 | 24 | |
| | $A_n$ or $B_n$ to A = B | 15 | 21 | 25 | |
| LOGIC Mode | $A_n$ or $B_n$ to $F_n$ | 15 | 19 | 23 | |
| SUM and | $C_n$ to $C_{n+4}$ | 15 | 13 | 18 | |
| DIFFERENCE Mode | $C_n$ to $F_n$ | 15 | 17 | 20 | |
| Power Dissipation Capacitance* | $C_{PD}$ | — | 120 | 140 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where $f_i$ = input frequency

$f_o$ = output frequency

$C_L$ = output load capacitance

$V_{CC}$ = supply voltage.

**AC Test Setup Reference (Active-Low Data)**

| Test Delay Times | AC Paths | | DC Data Inputs | | Mode* |
|---|---|---|---|---|---|
| | Inputs | Outputs | To Gnd | To $V_{CC}$ | |
| $SUM_{IN}$ to $SUM_{OUT}$ | $\overline{BO}$ | Any $\overline{F}$ | $\overline{B1}$, $\overline{B2}$, $\overline{B3}$, M, $C_n$ | All $\overline{A}$'s | ADD |
| $SUM_{IN}$ to $\overline{P}$ | $\overline{AO}$ | $\overline{P}$ | $\overline{A1}$, $\overline{A2}$, $\overline{A3}$, M, $C_n$ | All $\overline{B}$'s | ADD |
| $SUM_{IN}$ to $\overline{G}$ | $\overline{BO}$ | $\overline{G}$ | All $\overline{A}$'s, M, $C_n$ | $\overline{B1}$, $\overline{B2}$, $\overline{B3}$ | ADD |
| $SUM_{IN}$ to $C_{n+4}$ | $\overline{BO}$ | $C_{n+4}$ | All $\overline{A}$'s, M, $C_n$ | $\overline{B1}$, $\overline{B2}$, $\overline{B3}$ | ADD |
| $C_n$ to $SUM_{OUT}$ | $C_n$ | Any $\overline{F}$ | All $\overline{A}$'s, M | All $\overline{B}$'s | ADD |
| $C_n$ to $C_{n+4}$ | $C_n$ | $C_{n+4}$ | All $\overline{A}$'s, M | All $\overline{B}$'s | ADD |
| $SUM_{IN}$ to A = B | $\overline{BO}$ | A = B | All A's, B1, B2, B3, M | $C_n$ | SUBTRACT |
| $SUM_{IN}$ to $SUM_{OUT}$ (Logic Mode) | All $\overline{B}$'s | Any $\overline{F}$ | All $\overline{A}$'s, $C_n$ | M | EXCLUSIVE-OR |

*ADD Mode: S0, S3 = $V_{CC}$; S1, S2 = Gnd.
SUBTRACT Mode: S0, S3 = Gnd; S1, S2 = $V_{CC}$.

# CD54/74HC181
# CD54/74HCT181

**SWITCHING CHARACTERISTICS ($C_L$ = 50 pF, Input $t_r$,$t_f$ = 6 ns)**

| CHARACTERISTIC | | $V_{CC}$ (V) | LIMITS | | | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 25°C | | | | -40°C to +85°C | | | | -55°C to +125°C | | | | |
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay, | $t_{PLH}$ | 2 | — | 225 | — | — | — | 280 | — | — | — | 345 | — | — | |
| SUM Mode | $t_{PHL}$ | 4.5 | — | 45 | — | 53 | — | 56 | — | 66 | — | 69 | — | 80 | |
| $A_n$ or $B_n$ to $C_{n+4}$ | | 6 | — | 38 | — | — | — | 48 | — | — | — | 59 | — | — | |
| | | 2 | — | 210 | — | — | — | 265 | — | — | — | 315 | — | — | |
| $A_n$ or $B_n$ to G | | 4.5 | — | 42 | — | 54 | — | 53 | — | 53 | — | 63 | — | 63 | |
| | | 6 | — | 36 | — | — | — | 45 | — | — | — | 54 | — | — | |
| | | 2 | — | 170 | — | — | — | 215 | — | — | — | 255 | — | — | |
| $A_n$ or $B_n$ to P | | 4.5 | — | 34 | — | 41 | — | 43 | — | 51 | — | 51 | — | 62 | |
| | | 6 | — | 29 | — | — | — | 37 | — | — | — | 43 | — | — | |
| | | 2 | — | 230 | — | — | — | 290 | — | — | — | 345 | — | — | |
| $A_n$ or $B_n$ to $F_n$ | | 4.5 | — | 46 | — | 58 | — | 58 | — | 58 | — | 69 | — | 69 | |
| | | 6 | — | 39 | — | — | — | 49 | — | — | — | 59 | — | — | |
| Propagation Delay, | $t_{PHL}$ | 2 | — | 235 | — | — | — | 285 | — | — | — | 355 | — | — | |
| DIFFERENCE Mode | $t_{PLH}$ | 4.5 | — | 47 | — | 55 | — | 59 | — | 69 | — | 71 | — | 83 | |
| $A_n$ or $B_n$ to $C_{n+4}$ | | 6 | — | 40 | — | — | — | 50 | — | — | — | 60 | — | — | |
| | | 2 | — | 215 | — | — | — | 270 | — | — | — | 325 | — | — | |
| $A_n$ or $B_n$ to G | | 4.5 | — | 43 | — | 54 | — | 54 | — | 54 | — | 65 | — | 65 | |
| | | 6 | — | 37 | — | — | — | 46 | — | — | — | 55 | — | — | |
| | | 2 | — | 170 | — | — | — | 215 | — | — | — | 255 | — | — | |
| $A_n$ or $B_n$ to P | | 4.5 | — | 34 | — | 40 | — | 43 | — | 50 | — | 51 | — | 60 | ns |
| | | 6 | — | 29 | — | — | — | 37 | — | — | — | 43 | — | — | |
| | | 2 | — | 235 | — | — | — | 295 | — | — | — | 355 | — | — | |
| $A_n$ or $B_n$ to $F_n$ | | 4.5 | — | 47 | — | 57 | — | 59 | — | 71 | — | 71 | — | 86 | |
| | | 6 | — | 40 | — | — | — | 50 | — | — | — | 60 | — | — | |
| | | 2 | — | 245 | — | — | — | 305 | — | — | — | 370 | — | — | |
| $A_n$ or $B_n$ to A=B | | 4.5 | — | 49 | — | 60 | — | 61 | — | 75 | — | 74 | — | 90 | |
| | | 6 | — | 42 | — | — | — | 52 | — | — | — | 63 | — | — | |
| Propagation Delay, | $t_{PHL}$ | 2 | — | 230 | — | — | — | 290 | — | — | — | 345 | — | — | |
| LOGIC Mode | $t_{PLH}$ | 4.5 | — | 46 | — | 54 | — | 58 | — | 68 | — | 69 | — | 81 | |
| $A_n$ or $B_n$ to $F_n$ | | 6 | — | 39 | — | — | — | 49 | — | — | — | 59 | — | — | |
| Propagation Delay, | $t_{PHL}$ | 2 | — | 165 | — | — | — | 205 | — | — | — | 250 | — | — | |
| SUM & DIFF. Modes | $t_{PLH}$ | 4.5 | — | 33 | — | 42 | — | 41 | — | 53 | — | 50 | — | 63 | |
| $C_n$ to $C_{n+4}$ | | 6 | — | 28 | — | — | — | 35 | — | — | — | 43 | — | — | |
| | | 2 | — | 200 | — | — | — | 250 | — | — | — | 300 | — | — | |
| $C_n$ to $F_n$ | | 4.5 | — | 40 | — | 48 | — | 50 | — | 56 | — | 60 | — | 68 | |
| | | 6 | — | 34 | — | — | — | 43 | — | — | — | 51 | — | — | |
| Output Transition | $t_{THL}$ | 2 | — | 75 | — | — | — | 95 | — | — | — | 110 | — | — | |
| Time | $t_{TLH}$ | 4.5 | — | 15 | — | 15 | — | 19 | — | 19 | — | 22 | — | 22 | |
| | | 6 | — | 13 | — | — | — | 16 | — | — | — | 19 | — | — | |
| Input Capacitance | $C_I$ | — | — | 10 | — | 10 | — | 10 | — | 10 | — | 10 | — | 10 | pF |