CD54/74HC182
CD54/74HCT182

HARRIS SEMICONDUCTOR

NOT RECOMMENDED FOR NEW DESIGNS

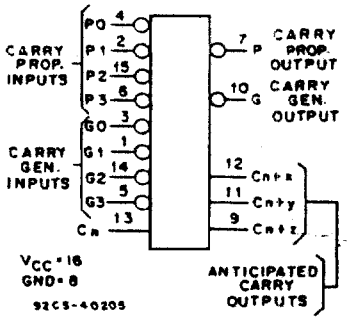
December 1997

High-Speed CMOS Logic

Look-Ahead Carry Generator

Type Features:

- *Provides carry look-ahead across a group of four ALU s*
- *Multi-level look-ahead for high-speed arithmetic operation over long word length*



FUNCTIONAL DIAGRAM

The Harris CD54/74HC182 and CD54/74HCT182 carry look-ahead generatos are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL).

The CD54/74HC/HCT182 accept up to four pairs of active LOW carry propagate ($\overline{P_0}$, $\overline{P_1}$, $\overline{P_2}$, $\overline{P_3}$) and carry generate ($\overline{G_0}$, $\overline{G_1}$, $\overline{G_2}$, $\overline{G_3}$) signals and an active HIGH carry input(C_n). The devices provide anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The HC/HCT182 also has active LOW carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs which may be used for further levels of look ahead.

The logic equations provided at the outputs are:

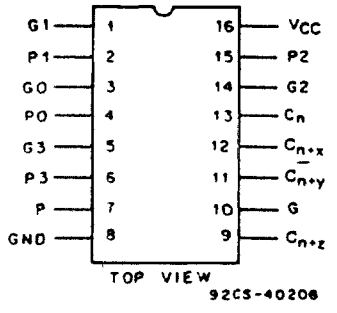
$$C_{n+x} = P_0C_n + G_0$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

The CD54/74HC/HCT182 can also be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

The CD54HC182 and CD54HCT182 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC182 and CD74HCT182 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  -55 to +125°C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL input logic compatibility
  V_{IL} = 0.8 V max., V_{IH} = 2 V Min.
  CMOS input compatiblity
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

File Number **1830.1**

CD54/74HC182
CD54/74HCT182

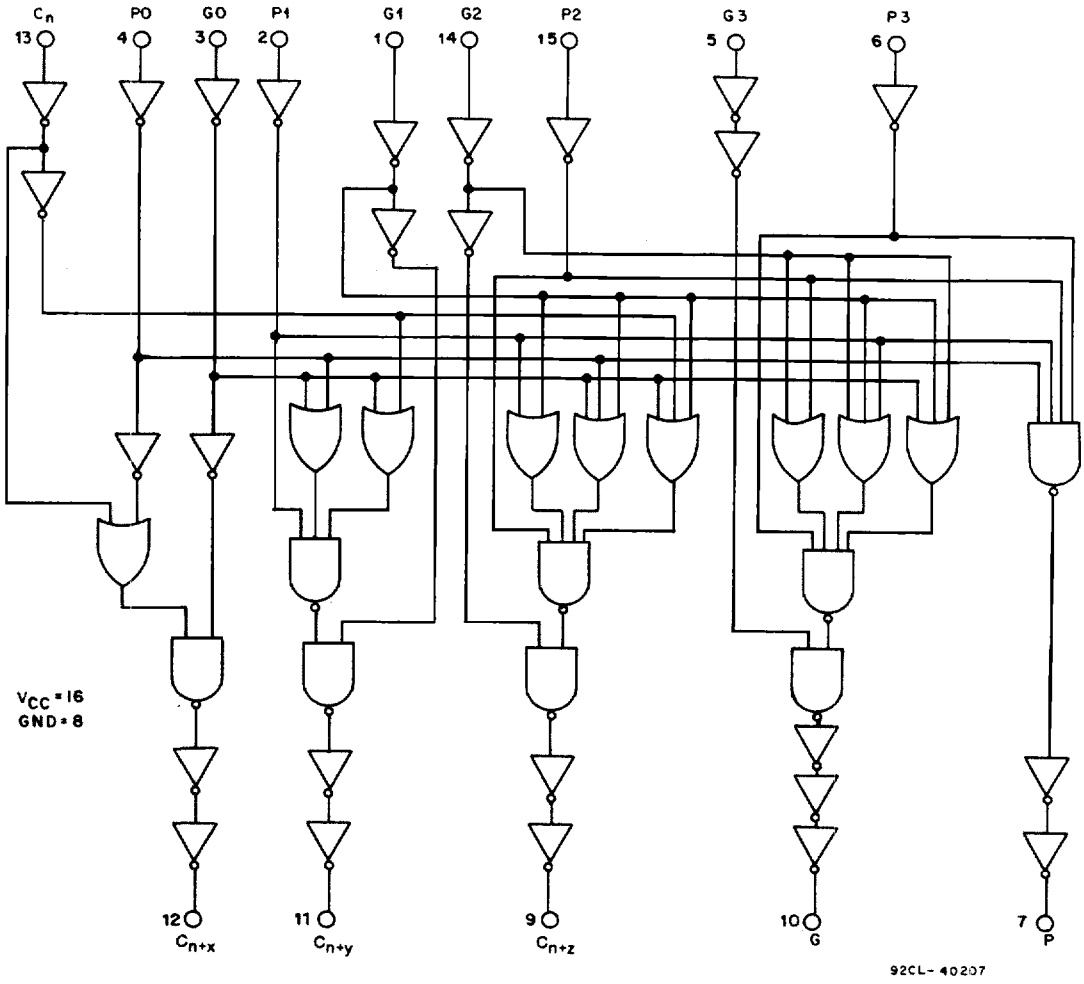


Fig. 1 - Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E, F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E, F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Lineary at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

CD54/74HC182
CD54/74HCT182

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	G_0	P_0	G_1	P_1	G_2	P_2	G_3	P_3	C_{n+x}	C_{n+y}	C_{n+z}	G	P
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	H	H	H	H					L		
X	X	H	H	X	H	X					L		
X	H	X	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	L	L	L					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	L	X	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH voltage level L = LOW voltage level X = don't care

CD54/74HC182
CD54/74HCT182

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC182/CD54HC182										CD74HCT182/CD54HCT182								UNITS
	TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)							TEST CONDITIONS		AMBIENT TEMPERATURE (T_A)						
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C	
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—									
			6	4.2	—	—	4.2	—	4.2	—									
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35									
			6	—	—	1.8	—	1.8	—	1.8									
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—									
			6	5.9	—	—	5.9	—	5.9	—									
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—									
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1									
			6	—	—	0.1	—	0.1	—	0.1									
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4									
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
P_0, P_1, P_2, G_0, G_1	1.5
P_3, G_2, C_n	1.25
G_3	0.3

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC182
CD54/74HCT182

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay Time:					
P_n to P	t_{PHL}, t_{PLH}	15	9	11	ns
C_n to any output	t_{PHL}, t_{PLH}	15	12	17	
P_n to any output	t_{PHL}, t_{PLH}	15	12	13	
G_n to any output	t_{PHL}, t_{PLH}	15	11	13	
Power Dissipation Capacitance *	C_{PD}	—	66	72	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i = input frequency

f_o = output frequency

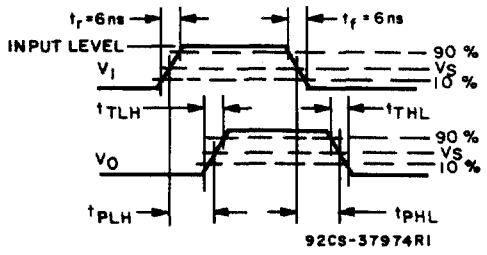
C_L = output load capacitance

V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITIONS V_{CC} V	AMBIENT TEMPERATURE (T_A)												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		HC		HCT		HC		HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, P_n to P	t_{PLH}	2	—	120	—	—	—	150	—	—	—	180	—	—	ns
	t_{PHL}	4.5	—	24	—	28	—	30	—	35	—	36	—	42	
		6	—	20	—	—	—	26	—	—	—	31	—	—	
C_n to any output	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PHL}	4.5	—	30	—	40	—	38	—	50	—	45	—	60	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
P_n to any output	t_{PLH}	2	—	145	—	—	—	180	—	—	—	220	—	—	
	t_{PHL}	4.5	—	29	—	33	—	36	—	41	—	36	—	50	
		6	—	25	—	—	—	31	—	—	—	31	—	—	
G_n to any output	t_{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	
	t_{PHL}	4.5	—	27	—	32	—	34	—	40	—	41	—	48	
		6	—	23	—	—	—	29	—	—	—	35	—	—	
Transition Time	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC182
CD54/74HCT182



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times and propagation delay times.