

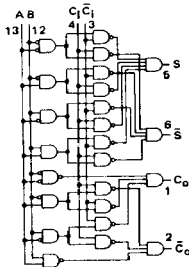
FULL ADDERS

MECL II MC1000/1200 series

MC1019
MC1219

Provides the SUM, $\overline{\text{SUM}}$, CARRY, and $\overline{\text{CARRY}}$ functions while requiring only AUGEND (A) and ADDEND (B) inputs with CARRY IN and CARRY IN.

POSITIVE LOGIC



$$S = ABC_1 + \overline{A}BC_1 + A\overline{B}C_1 + \overline{A}\overline{B}C_1$$

$$\overline{S} = \overline{A}BC_1 + ABC_1 + A\overline{B}C_1 + \overline{A}\overline{B}C_1$$

$$C_0 = ABC_1 + \overline{A}BC_1 + A\overline{B}C_1 + \overline{A}\overline{B}C_1$$

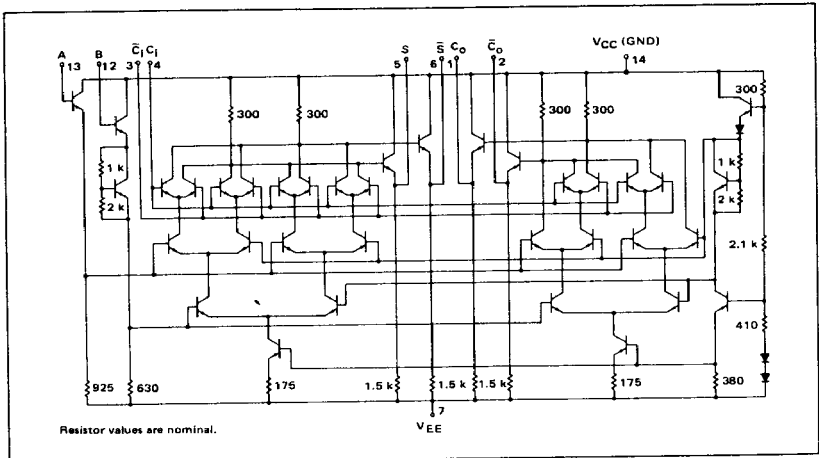
$$\overline{C_0} = \overline{A}BC_1 + \overline{A}\overline{B}C_1 + A\overline{B}C_1 + \overline{A}\overline{B}C_1$$

DC Input Loading Factor: A, B = 1
C₁, C₁[̄] = 2
DC Output Loading Factor = 25
Power Dissipation = 145 mW typical

TRUTH TABLE

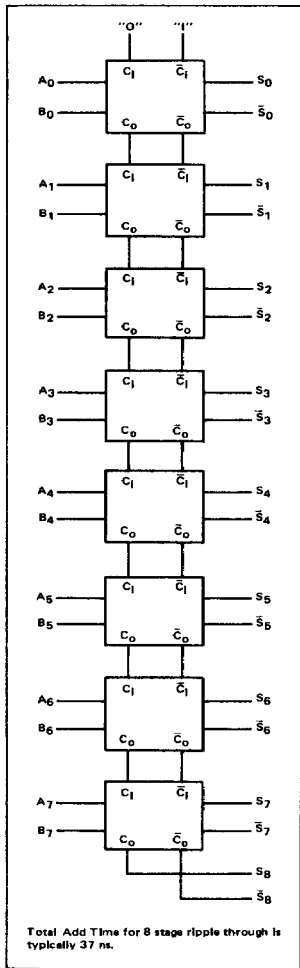
INPUT LOGIC LEVEL				OUTPUT LOGIC LEVEL			
A	B	C ₁	C ₁ [̄]	S	\overline{S}	C ₀	C ₀ [̄]
0	0	0	1	0	1	0	1
0	0	1	0	1	0	0	1
0	1	0	1	1	0	0	1
0	1	1	0	0	1	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	1	0
1	1	0	1	0	1	1	0
1	1	1	0	1	0	1	0

CIRCUIT SCHEMATIC



Resistor values are nominal.

FIGURE 1 - 8 BIT
RIPPLE-THROUGH ADDER

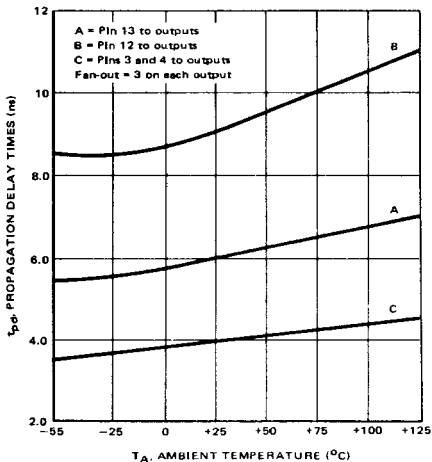


APPLICATIONS INFORMATION

The MC1019/MC1219 full adder exhibits an average propagation delay time of 5.0 ns per stage in a system employing ripple Carry. This device permits practical ripple-through adders as shown in Figure 1, as well as ripple-through multipliers.

The schematic of the full adder illustrates the techniques employed to obtain the necessary logic equations. A compensated current source drives a transistor "tree" with three levels of branching. The B input is translated negative two levels, to switch current between either the left or right branch of the tree. The A input is translated negative one level to switch current at the second level of branching. The Carry inputs switch current through the third level of branching. Depending upon the eight possible combinations of inputs, one specific branch in the Sum generating tree will be carrying current. Thus the proper output state is determined. The Carry generating tree operates in the same manner. This series gating technique results in the best speed-power product obtainable with bipolar technology. Typical propagation delay times from the inputs to outputs are shown in Figure 2.

FIGURE 2 - TYPICAL PROPAGATION DELAY TIMES



172

MC1019, MC1219 (continued)

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1219 Test Limits						Unit	MC1019 Test Limits						Unit	
			-55°C		+25°C		+125°C			0°C		+25°C		+75°C			
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I_{EG}	7	-	-	-	35	-	-	mAdc	-	-	-	35	-	-	mAdc	
Input Current	$2 I_{in}$	3	-	-	-	200	-	-	μ Adc	-	-	-	200	-	-	μ Adc	
	$2 I_{in}$	4	-	-	-	200	-	-	μ Adc	-	-	-	200	-	-	μ Adc	
	$1.5 I_{in}$	12	-	-	-	150	-	-	μ Adc	-	-	-	150	-	-	μ Adc	
	$1.5 I_{in}$	13	-	-	-	150	-	-	μ Adc	-	-	-	150	-	-	μ Adc	
Input Leakage Current	I_{IR}	12	-	-	-	0.2	-	1.0	μ Adc	-	-	-	0.2	-	1.0	μ Adc	
		13	-	-	-	0.2	-	1.0	μ Adc	-	-	-	0.2	-	1.0	μ Adc	
		3	-	-	-	1.0	-	5.0	μ Adc	-	-	-	1.0	-	5.0	μ Adc	
		4	-	-	-	1.0	-	5.0	μ Adc	-	-	-	1.0	-	5.0	μ Adc	
"SUM" Logic "1" Output Voltage [†]	V_{OH}^{1*}	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	
"SUM" Logic "0" Output Voltage	V_{OL}^0	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	
"CARRY" Logic "1" Output Voltage [†]	V_{OH}^{1*}	1	-0.890	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	
"CARRY" Logic "0" Output Voltage	V_{OL}^0	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	
Switching Times (Fan-out = 3) Addend Input Propagation Delay	t_{12-5+}	5	Typ	8.0	13.0	8.0	13.0	8.0	13.0	ns	8.0	13.0	8.0	13.0	8.0	13.0	ns
			Max	5.0	7.0	11.5	12.0	10.0	16.0	12.0	12.0	9.0	14.0	14.0	14.0	14.0	14.0
			Typ	8.0	12.0	9.0	12.0	11.0	17.0	12.0	12.0	12.0	14.5	14.5	14.5	14.5	14.5
			Max	1.0	9.0	14.5	9.0	14.5	10.0	15.0	9.0	14.5	9.0	14.5	14.5	14.5	14.5
	Rise Time	5	Typ	8.0	13.0	9.0	14.0	9.0	14.0	9.0	14.0	14.0	14.0	14.0	14.0	14.0	14.0
			Max	5.0	8.0	11.5	12.0	10.0	16.0	12.0	12.0	9.0	14.0	14.0	14.0	14.0	14.0
			Typ	5.0	8.0	8.5	5.0	8.5	8.0	12.0	5.0	8.5	5.0	8.5	7.0	10.0	10.0
			Max	1.0	8.0	8.0	8.0	7.0	11.5	8.0	8.5	8.0	8.5	6.0	9.5	9.5	9.5
	Fall Time	1	Typ	8.0	13.0	9.0	14.0	9.0	14.0	9.0	14.0	14.0	14.0	14.0	14.0	14.0	14.0
			Max	5.0	8.0	11.5	12.0	10.0	16.0	12.0	12.0	9.0	14.0	14.0	14.0	14.0	14.0
			Typ	5.0	8.0	8.5	5.0	8.5	8.0	12.0	5.0	8.5	5.0	8.5	7.0	10.0	10.0
			Max	1.0	8.0	8.0	8.0	7.0	11.5	8.0	8.5	8.0	8.5	6.0	9.5	9.5	9.5
Augend Input Propagation Delay	5	Typ	8.0	8.5	6.0	8.5	7.0	10.5	ns	8.0	8.5	6.0	8.5	6.0	9.5	ns	
		Max	5.0	5.0	5.0	5.0	5.0	11.0	5.0	8.5	5.0	8.5	5.0	9.0	9.0	9.0	
		Typ	6.0	6.0	6.0	6.0	6.0	11.0	6.0	9.0	6.0	9.0	6.0	9.5	9.5	9.5	
		Max	5.0	5.0	5.0	5.0	5.0	11.0	5.0	8.5	5.0	8.5	5.0	9.5	9.5	9.5	
Carry Input Propagation Delay	5	Typ	3.0	5.0	3.0	5.0	3.0	5.0	ns	3.0	5.0	3.0	5.0	3.0	5.0	ns	
		Max	4.0	7.5	4.0	7.5	4.0	10.0	4.0	7.5	4.0	7.5	5.0	8.0	8.0	8.0	
		Typ	5.0	8.0	5.0	8.0	5.0	10.5	5.0	8.5	5.0	8.5	5.0	8.0	8.0	8.0	
		Max	5.0	8.0	5.0	8.5	7.0	11.0	5.0	8.5	5.0	8.5	5.0	8.5	6.0	9.5	9.5

[†] V_{OH} limits apply from no load (0 mA) to full load (-3.5 mA)

* V_{OH} and V_{OL} limits apply only if not more than one input (pin 3, 4, 12 or 13) is at a Threshold Voltage

(V_{IL} max or V_{IH} min). Conduct tests with one input at a Threshold Voltage and apply appropriate V_{OL} max or V_{OH} min voltages to all other inputs.

@ Test Temperature
 MC1219 -55°C
 +25°C
 +125°C
 MC1019 0°C
 +25°C
 +75°C

TEST VOLTAGE/CURRENT VALUES							
V _{dc} ±1.0%							
V _{K min} to V _{K max}	V _{OL max}	V _{IH min} to V _{IH max}	V _{OH min}	V _{IH max}	V _{EE}	I _L	mAdc
-5.2 to -1.405	-1.580	-1.165 to -0.825	-0.990	-	5.2	-2.5	-
-5.2 to -1.225	-1.500	-1.025 to -0.700	-0.850	-0.700	5.2	-2.5	-
-5.2 to -1.205	-1.380	-0.875 to -0.530	-0.700	-	5.2	-2.5	-
-5.2 to -1.350	-1.525	-1.070 to -0.740	-0.875	-	-5.2	-2.5	-
-5.2 to -1.325	-1.500	-1.025 to -0.700	-0.850	-0.700	-5.2	-2.5	-
-5.2 to -1.280	-1.435	-0.950 to -0.615	-0.775	-	-5.2	-2.5	-

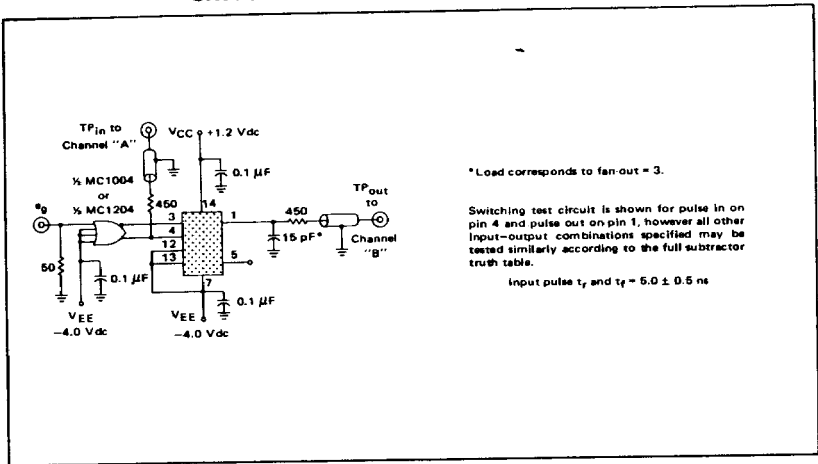
TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:				V _{CC} (Gnd)		
			V _{K min} to V _{K max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}			
Power Supply Drain Current	I _E	7	3	4	-	7, 12, 13	14		
Input Current	2 I _{1 in}	3	4, 13	-	3, 12	7	14		
	2 I _{1 in}	4	3, 12	-	4, 13	-	-		
	1.5 I _{1 in}	12	3, 13	-	4, 12	-	-		
	1.5 I _{1 in}	13	3, 12	-	4, 13	-	-		
Input Leakage Current	I _R	12	4	3	-	7, 12, 13	14		
		13	4	3	-	7, 12, 13	-		
		3	-	4	-	3, 7, 12, 13	-		
		4	-	3	-	4, 7, 12, 13	-		
"SUM" Logic "1" Output Voltage	V _{OH} ¹	5	3, 12, 13 [*] 4, 13 [*] 4, 12 [*] 3 [*]	4 [*] 3, 12 3, 13 [*] 4, 12, 13 [*]	-	7	5, 14		
"SUM" Logic "0" Output Voltage	V _{OL} [*]	5	4, 12, 13 [*] 3, 13 [*] 3, 12 [*] 4 [*]	3 [*] 4, 12 [*] 3, 13 [*] 3, 12, 13 [*]	-	7	-, 14		
"CARRY" Logic "1" Output Voltage	V _{OH} ^{1*}	1	3, 13 [*] 3, 12 [*] 4 [*] 3 [*]	4, 12 [*] 4, 13 [*] 3, 12, 13 [*] 4, 12, 13 [*]	-	7	1, 14		
"CARRY" Logic "0" Output Voltage	V _{OL} [*]	1	4, 12, 13 [*] 3, 12, 13 [*] 4, 13 [*] 4, 12 [*]	3 [*] 4 [*] 3, 12 [*] 3, 13 [*]	-	7	-, 14		
Switching Times (Fan-out = 3)	Addend Input Propagation Delay	t ₁₂₋₅₊	5	12	5	-	7	14	
									t ₁₂₋₅₋
		t ₁₂₋₁₊	1	1	-	-			
							t ₁₂₋₁₋	1	1
		Rise Time	t ₅₊	5	5	-			
							Fall Time	t ₁₊	1
		t ₅₋	5	5	-	-			
							t ₁₋	1	1
		Augend Input Propagation Delay	t ₁₃₋₅₊	5	13	5			
							t ₁₃₋₅₋	5	-
			Rise Time	t ₅₊	5	5			
							Fall Time	t ₅₋	5
		Carry Input Propagation Delay	t ₄₋₅₊	5	4	5			
							Rise Time	t ₄₋₅₋	5
Fall Time	t ₅₋	5	4	5	-	-			

174

MC1019, MC1219 (continued)

SWITCHING TIME TEST CIRCUIT @ 25°C



SWITCHING TIME WAVEFORMS

